TDA19998HL

Smart HDMI 1.4a (4 : 1) switch with auto-adaptive equalizer

Rev. 3 — 4 August 2010 Product data sheet

1. General description

The High-Definition Multimedia Interface (HDMI) switch enables connection of multiple DVI/HDMI inputs to a receiver with at least one input. The TDA19998HL is a switch with four HDMI 1.4a compliant DVI/HDMI inputs and one DVI/HDMI output. Each HDMI input has its own dedicated embedded EDID memory. A fifth DDC-bus input is available for VGA or second HDMI input of SoC. The built-in auto-adaptive equalizer improves signal quality, allowing the use of cable lengths up to 30 m.

The TDA19998HL supports Deep Color mode in 10-bit and 12-bit per channel up to 1920 × 1080p at 50/60 Hz. The TDA19998HL supports DVI/HDMI streams with or without High-bandwidth Digital Content Protection (HDCP 1.4) and all Data Island packets.

The TDA19998HL settings are controllable via the I^2C-bus.

The TDA19998HL, pin compatible with TDA19997, is embedding the "F^3 technology" from NXP, allowing no delay in switching from one HDMI port to any other HDMI port while keeping HDMI output stream encrypted.

2. Features and benefits

- Complies with the HDMI 1.4a, DVI 1.0, EIA/CEA-861D and HDCP 1.4 standards
- Four independent DVI/HDMI inputs, up to 2.25 gigasamples per second
- Pin compatible with TDA9996/TDA9995/TDA19997/TDA19995
- "F^3 technology" for fast switching HDMI port
- Robust auto-adaptive equalizer
  - up to 20 m AWG26 at 2.25 Gbit/s
  - up to 30 m AWG24 at 1.5 Gbit/s
- Integrated 50 Ω single-ended termination resistors
- +5 V signal detection for each HDMI input
- Supports color depth processing at 24-bit, 30-bit or 36-bit per pixel
- Supports 3D video formats with all structures and all timings up to 2.25 GHz
- Supports all Data Island packets
- Activity detection on each input, manages output activity and power consumption
- Extended mode: re-generate output TMDS waveform removing jitter and skew
- Frequency measurement allowing direct reading of format/resolution
- Automatic mode for main features:
  - Automatic Hot Plug Detect (HPD) generation and termination resistors management

- Automatic HPD generation with programmable duration
- Automatic EDID load

- Display Data Channel (DDC) bus:
  - 5 V tolerant, DDC-bus inputs with bit rates up to 400 kbit/s
  - One DDC-bus output with the same latency as the HDMI stream pipeline delay
  - DDC-bus master switch functionality avoids bus corruption
  - DDC-bus level-shifting buffer with digital lock-up protection
  - A fifth DDC-bus input available for VGA or second HDMI input of SoC
- I^2C-bus controllable at bit rates up to 400 kbit/s
- Non-volatile memory for switch management (Hot Plug Detect, Power-down)
- Embedded Extended Display Identification Data (EDID) memory:
  - 5 embedded EDID memory supplied by +5 V from HDMI source
  - 253-byte shared and 3-byte of dedicated EDID memory per HDMI input
  - Non-volatile memory for programming default EDID content
  - Supports sources without +5 V
  - An extra 128-byte blocks for DVI or PC formats
  - EDID update by I^2C-bus, example for AVR applications
- Fail-safe output in Idle mode
- Mute pin preventing from pop noise/image noise
- ATC/Rx compliant for 36-bit Deep Color 1080p 60 Hz
- ATC/Tx eye diagram compliant for 36-bit Deep color 1080p 60 Hz
- Programmable slave address
- Ready for HDMI Ethernet Audio return Channel (HEAC)
- 3.3 V and 1.8 V power supplies
- Additional ESD protection pin for CEC line
- ESD protection:
  - HBM: class 2
  - MM: class B
  - FCDM: class IV
  - IEC 61000-4-2 class 3 for HDMI inputs
- Power-down mode with dedicated pin
- CMOS process
- Lead (Pb) free LQFP100 14 × 14 × 1 mm package, pitch 0.5 mm

3. Applications

- 3D-TV
- HDTV (plasma, Rear projection TV and LCD TV)
- YCbCr or RGB Hi-Speed video digitizer
- Projector
- Home theater
- AVR
- Switch box

4. Quick reference data

Table 1. Quick reference data

In accordance with the Absolute Maximum Rating System (IEC 60134). $V_{DDH(3V3)}$ = 3.13 V to 3.47 V; $V_{DDDC(3V3)}$ = 3.0 V to 3.6 V; $V_{DDH(1V8)}$ = 1.65 V to 1.95 V; $V_{DDDC(1V8)}$ = 1.65 V to 1.95 V; T_{amb} = 0 °C to +70 °C; typical values measured at $V_{DDH(3V3)}$ and $V_{DDDC(3V3)}$ = 3.3 V; $V_{DDH(1V8)}$ and $V_{DDDC(1V8)}$ = 1.8 V and T_{amb} = 25 °C; f_{max} = 2.25 GHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HDMI input pins: RXx_D0+, RXx_D0–, RXx_D1+, RXx_D1–, RXx_D2+, RXx_D2–, RXx_C+, RXx_C–, RXx_HPD, RXx_5V, RXy_DDC_DAT, RXy_DDC_CLK, CEC[1][2]						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 class 3 (contact discharge)	7	-	-	kV
HDMI pins: OUT_D0+, OUT_D0–, OUT_D1+, OUT_D1–, OUT_D2+, OUT_D2–, RXx_D0+, RXx_D0–, RXx_D1+, RXx_D1–, RXx_D2+, RXx_D2–[1]						
f_{max}	maximum frequency		2.25	-	-	GHz
Supplies						
$V_{DDH(3V3)}$	HDMI supply voltage (3.3 V)		3.13	3.3	3.47	V
$V_{DDH(1V8)}$	HDMI supply voltage (1.8 V)		1.65	1.8	1.95	V
$V_{DDS(3V3)}$	supervisor supply voltage (3.3 V)		3.0	3.3	3.6	V
$V_{DDDC(1V8)}$	core digital supply voltage (1.8 V)		1.65	1.8	1.95	V

[1] x = A, B, C, D.

[2] y = A, B, C, D, E.

5. Ordering information

Table 2. Ordering information

Type number	Maximum data rate per channel	Package		
		Name	Description	Version
TDA19998HL	2.25 gigasamples per second	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

6. Block diagram

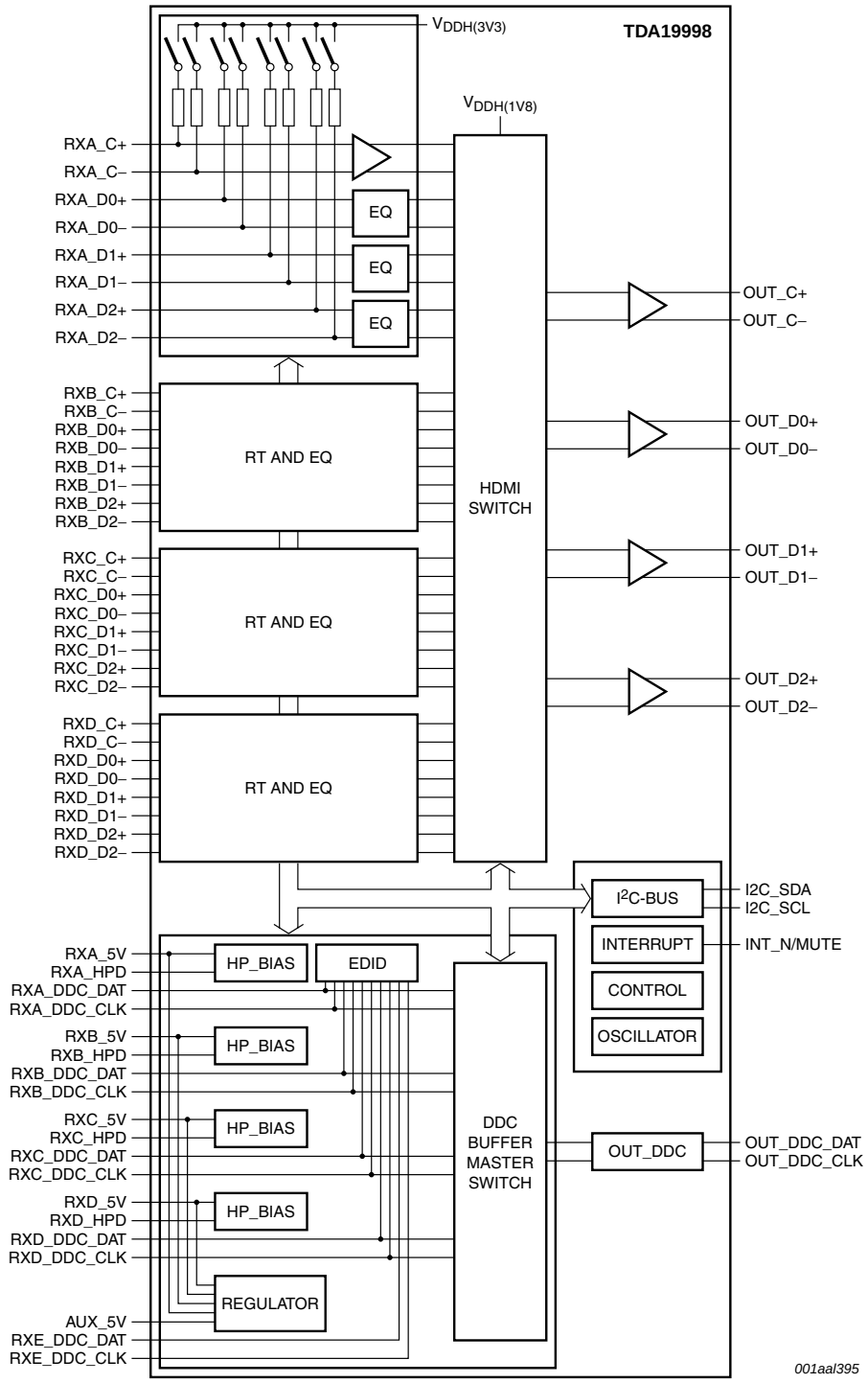


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

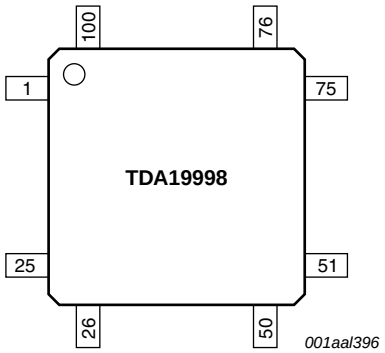


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
V_{SS}	1	G	ground
OUT_C+	2	O	HDMI output positive clock channel
OUT_C−	3	O	HDMI output negative clock channel
$V_{DDO(3V3)}$	4	P	output supply voltage; 3.3 V
OUT_DDC_CLK	5	O	DDC-bus clock output; open-drain; 5 V tolerant
OUT_DDC_DAT	6	I/O	DDC-bus data input/output; open-drain; 5 V tolerant
V_{SS}	7	G	ground
$V_{DDDC(1V8)}$	8	P	digital core supply voltage; 1.8 V
RXA_HPD	9	O	HDMI output A Hot Plug Detect; 5 V tolerant
RXA_5V	10	I	input A HDMI +5 V
RXA_DDC_DAT	11	I/O	HDMI input/output A DDC-bus serial data; open-drain; 5 V tolerant
RXA_DDC_CLK	12	I	HDMI input A DDC-bus serial clock; open-drain; 5 V tolerant
RXA_C−	13	I	HDMI input A negative clock channel
RXA_C+	14	I	HDMI input A positive clock channel
$V_{DDH(3V3)}$	15	P	HDMI input A supply voltage; 3.3 V
RXA_D0−	16	I	HDMI input A negative data channel 0
RXA_D0+	17	I	HDMI input A positive data channel 0
V_{SS}	18	G	ground
RXA_D1−	19	I	HDMI input A negative data channel 1
RXA_D1+	20	I	HDMI input A positive data channel 1
$V_{DDH(3V3)}$	21	P	HDMI input A supply voltage; 3.3 V
RXA_D2−	22	I	HDMI input A negative data channel 2

Table 3. Pin description *...continued*

Symbol	Pin	Type[1]	Description
RXA_D2+	23	I	HDMI input A positive data channel 2
$V_{DDH(1V8)}$	24	P	HDMI core supply voltage; 1.8 V
AUX_5V	25	I	auxiliary input; 5 V
V_{SS}	26	G	ground
TEST1	27	I	reserved for test (connect to ground)
RXB_HPD	28	O	HDMI output B Hot Plug Detect; 5 V tolerant
RXB_5V	29	I	input B HDMI +5 V
RXB_DDC_DAT	30	I/O	HDMI input/output B DDC-bus serial data; open-drain; 5 V tolerant
RXB_DDC_CLK	31	I	HDMI input B DDC-bus serial clock; open-drain; 5 V tolerant
RXB_C−	32	I	HDMI input B negative clock channel
RXB_C+	33	I	HDMI input B positive clock channel
$V_{DDH(3V3)}$	34	P	HDMI input B supply voltage; 3.3 V
RXB_D0−	35	I	HDMI input B negative data channel 0
RXB_D0+	36	I	HDMI input B positive data channel 0
V_{SS}	37	G	ground
RXB_D1−	38	I	HDMI input B negative data channel 1
RXB_D1+	39	I	HDMI input B positive data channel 1
$V_{DDH(3V3)}$	40	P	HDMI input B supply voltage; 3.3 V
RXB_D2−	41	I	HDMI input B negative data channel 2
RXB_D2+	42	I	HDMI input B positive data channel 2
V_{SS}	43	G	ground
CDEC_DDC	44	P	internal supply voltage regulator decoupling capacitor; 1.8 V
$V_{DDDC(1V8)}$	45	P	digital core supply voltage; 1.8 V
$V_{DDDC(3V3)}$	46	P	digital core supply voltage; 3.3 V
TEST2	47	I	reserved for test (connect to ground)
PD	48	I	power-down control input; active HIGH
I2C_SDA	49	O	I^2C-bus output serial data
I2C_SCL	50	I	I^2C-bus serial clock
RXE_DDC_CLK	51	I	Additional input DDC-bus serial clock; open-drain; 5 V tolerant
RXE_DDC_DAT	52	I/O	Additional input/output DDC-bus serial data; open-drain; 5 V tolerant
INT_N/MUTE	53	O	interrupt request for I^2C-bus mode or 5 V detection MUTE output pin
CDEC_STBY	54	P	internal supply voltage regulator decoupling capacitor; 1.8 V
$V_{DDS(3V3)}$	55	P	supervisor supply voltage; 3.3 V
V_{SS}	56	G	ground
CEC	57	I	8 kV System level ESD protection
RXC_HPD	58	I	HDMI input C Hot Plug Detect; 5 V tolerant
RXC_5V	59	I	input C HDMI +5 V
RXC_DDC_DAT	60	I/O	HDMI input/output C DDC-bus serial data; open-drain; 5 V tolerant

Table 3. Pin description *...continued*

Symbol	Pin	Type[1]	Description
RXC_DDC_CLK	61	I	HDMI input C DDC-bus serial clock; open-drain; 5 V tolerant
RXC_C−	62	I	HDMI input C negative clock channel
RXC_C+	63	I	HDMI input C positive clock channel
$V_{DDH(3V3)}$	64	P	HDMI input C supply voltage; 3.3 V
RXC_D0−	65	I	HDMI input C negative data channel 0
RXC_D0+	66	I	HDMI input C positive data channel 0
V_{SS}	67	G	ground
RXC_D1−	68	I	HDMI input C negative data channel 1
RXC_D1+	69	I	HDMI input C positive data channel 1
$V_{DDH(3V3)}$	70	P	HDMI input C supply voltage; 3.3 V
RXC_D2−	71	I	HDMI input C negative data channel 2
RXC_D2+	72	I	HDMI input C positive data channel 2
V_{SS}	73	G	ground
R12K	74	I	termination resistor control
$V_{DDH(1V8)}$	75	P	HDMI core supply voltage; 1.8 V
RXD_HPD	76	O	HDMI output D Hot Plug Detect; 5 V tolerant
RXD_5V	77	I	input D HDMI +5 V
RXD_DDC_DAT	78	I/O	HDMI input/output D DDC-bus serial data; open-drain; 5 V tolerant
RXD_DDC_CLK	79	I	HDMI input D DDC-bus serial clock; open-drain; 5 V tolerant
RXD_C−	80	I	HDMI input D negative clock channel
RXD_C+	81	I	HDMI input D positive clock channel
$V_{DDH(3V3)}$	82	P	HDMI input D supply voltage; 3.3 V
RXD_D0−	83	I	HDMI input D negative data channel 0
RXD_D0+	84	I	HDMI input D positive data channel 0
V_{SS}	85	G	ground
RXD_D1−	86	I	HDMI input D negative data channel 1
RXD_D1+	87	I	HDMI input D positive data channel 1
$V_{DDH(3V3)}$	88	P	HDMI input D supply voltage; 3.3 V
RXD_D2−	89	I	HDMI input D negative data channel 2
RXD_D2+	90	I	HDMI input D positive data channel 2
$V_{DDDC(1V8)}$	91	P	digital core supply voltage; 1.8 V
V_{SS}	92	G	ground
OUT_D2+	93	O	HDMI output positive data channel 2
OUT_D2−	94	O	HDMI output negative data channel 2
$V_{DDO(1V8)}$	95	P	output supply voltage; 1.8 V
OUT_D1+	96	O	HDMI output positive data channel 1
OUT_D1−	97	O	HDMI output negative data channel 1
V_{SS}	98	G	ground
OUT_D0+	99	O	HDMI output positive data channel 0
OUT_D0−	100	O	HDMI output negative data channel 0

[1] P = power supply; G = ground; I = input and O = output; I/O = input/output.

8. Functional description

The TDA19998HL is a DVI/HDMI switch comprising four DVI/HDMI inputs and one output optimized for Hi-Speed TMDS data. All inputs meet HDMI compliance tests and include a built-in auto-adaptive input equalizer. The TDA19998HL includes an activity detection module and Hot Plug Detect management.

In addition, the TDA19998HL stores the Extended Display Identification Data (EDID) for each input in the built-in EDID memory. Full DDC-bus functionality is provided by the TDA19998HL, including level-shifting.

8.1 HDMI input

The TDA19998HL supports bit rate inputs up to 2.25 Gbit/s enabling high frame rate formats such as 1080p60, 1080i120 and 720p120 in 36-bit Deep Color mode or 720p60 and 1080p24 in 3D video format.

The termination resistor control (R12K) needs an external resistor of 12 k$\Omega \pm 1$ %.

The termination resistor can be disconnected from the 3.3 V supply to remove the common-mode voltage via the I^2C-bus and/or when RXx_HPD is LOW.

8.2 F^3 technology

This F^3 technology is implemented in order to take full benefit of the HDCP specification by detecting the HDCP state A0 of the source and decides if reset is necessary or not when input selection is changed (from one HDMI port to any other HDMI input port).

8.3 Equalizer

The input equalizer is fully auto-adaptive, needing no external control. Signals from short cables with very low TMDS clock frequencies (20 MHz) to long cables (up to 20 m) at high TMDS clock frequencies (225 MHz) are easily managed by the TDA19998HL's equalizer.

8.4 Activity detection

When activity is detected, the output is automatically activated. If no input activity is detected, the output is disabled to avoid false detections by the HDMI receiver. The power consumption is reduced accordingly. The detection range is fixed by I^2C-bus. An interrupt output can be used to indicate any activity change.

The TMDS frequency can be read by I^2C-bus, however, the precision of the value depends on internal oscillator accuracy.

8.5 Embedded EDID memory

The size of the EDID memory is 253-byte shared and 3-byte dedicated for each input. The memory can be accessed by each input at the same time.

EDID content programming is performed using the non-volatile memory. The EDID memory can be powered by +5 V from the source or directly from the PCB using the dedicated AUX_5V pin. In Power-down mode, the EDID memory remains active and it is

possible to modify its content. Access from pins RXx_DDC_DAT and RXx_DDC_CLK is independent of other supplies. Consequently, the source has access to the EDID memory when TDA19998HL is not powered.

Content can be modified using the I^2C-bus. However, data modified using the I^2C-bus must be powered by the 1.8 V supply from pin CDEC_DDC or the AUX_5V auxiliary supply pin.

EDID memory accesses are only acknowledged when EDID-only mode is enabled.

Remark: Embedded non-volatile memory content shall be programmed with all termination resistors disconnected to ensure proper programming.

8.6 Display Data Channel (DDC)

The DDC-bus is 5 V tolerant and supports all direct connections from the HDMI source. The TDA19998HL provides level-shifting and buffering for both OUT_DDC_DAT and OUT_DDC_CLK pins. It allows level-shifting from 5 V on the source side to 3.3 V on the receiver side.

To prevent a lock-up condition, a specific digital protection is implemented on the DDC-bus.

Pins RXx_DDC_DAT, RXx_DDC_CLK, OUT_DDC_DAT and OUT_DDC_CLK are compatible with the I^2C-bus specification in Fast-mode (400 kHz):

- Pins RXx_DDC_DAT and RXx_DDC_CLK at V_{DD} = 4.5 V to 5.5 V
- Pins OUT_DDC_DAT and OUT_DDC_CLK at V_{DD} = 3.0 V to 3.6 V

When the TDA19998HL is not 1.8 V core supplied, pins OUT_DDC_DAT and OUT_DDC_CLK are high-impedance. In addition, pins RXx_DDC_DAT and RXx_DDC_CLK are high-impedance when the device is not 5 V supplied.

TDA19998HL acts as a DDC-bus master switch to prevent bus corruption. When the input selection changes, the upstream DDC-bus communication (using RXx_DDC_DAT and RXx_DDC_CLK) is disconnected and a stop bit is sent on the downstream DDC-bus communication (using OUT_DDC_DAT and OUT_DDC_CLK). The DDC-bus is then connected on the next upstream DDC during a free bus period to avoid bus corruption.

8.7 HDMI features

TDA19998HL does not decode Data Island or Deep Color information, it forwards these packets including Null Packets and Vendor Specific InfoFrames (for example 3D data information).

8.8 +5 V signal detection

+5 V signal detection from source is used for activity control through I^2C-bus by setting a bit and an interrupt.

8.9 AUX_5V pin

This pin can be used to supply the built-in EDID memory and DDC-bus enabling access to EDID memory using the DDC-bus without a +5 V signal from any of the input sources. When pin AUX_5V is powered, the TDA19998HL provides support for HDMI cabled sources without a +5 V signal. In addition, the AUX_5V supply ensures EDID data stored in active memory is not lost when a +5 V signal is not available from the input sources. Input signal detection (+5 V) is also available when AUX_5V pin is powered.

AUX_5V is necessary when using the fifth DDC-bus input (RXE_DDC_DAT, RXE_DDC_CLK).

8.10 HDMI output

The TDA19998HL HDMI output port is only activated when data is detected on the selected input.

HDMI output can be switched OFF (high-impedance) using an I^2C-bus bit or using pin PD.

In Idle mode, HDMI output is either fixed at a constant value (fail-safe protection) or high-impedance. Configuration is performed using an I^2C-bus bit. When output is fixed at a constant value, it creates a voltage difference in the differential pairs and stabilizes the receiver differential amplifier. This mode ensure better noise protection between TDA19998HL switch and receiver.

8.11 Enabling HEAC module with TDA19998

The Hot Plug Detect output of each HDMI port is biased to 4 V to support an external HEAC module.

8.12 Power management

The following five power modes are available:

- Operating mode: the device is fully functional
- Power-off mode: no supplies are available
- EDID-only mode: only +5 V from the source available
- Power-down mode: all supplies are available and pin PD is HIGH.
- Idle mode: all supplies are available and there is no HDMI input. As a power saving feature, Idle mode is automatically selected when there is no activity on the inputs. When activity is detected, Operating mode wake-up is automatically selected

Table 4. Power management

Functions	Mode			
	EDID-only	Power-down	Idle	Operating
+5 V signal detection	n/a	on	on	on
RXx_HPD (if 5 V)[1][2]	[3]	[4]	[4]	[4]
RXx_DDC_DAT; RXx_DDC_CLK (if 5 V)[2][5]	on	[4]	[4]	[4]
EDID DDC read (if 5 V)[2]	[3]	[4]	[4]	[4]
EDID I^2C-bus write (If 5 V)[2]	off	on	on	on
OUT_DDC_DAT; OUT_DDC_CLK	off	off	[4]	[4]

Table 4. Power management *…continued*

Functions	Mode			
	EDID-only	Power-down	Idle	Operating
INT_N/MUTE management	off	on	on	on
Termination resistors	off	off	[4]	[4]
Activity detection	off	off	[4]	[4]
Equalizer (when active)	off	off	[4]	[4]
TMDS buffer extended mode	off	off	[3]	[3]
TMDS output (if active)	off	off	[4]	[4]
Configuration register read/write	off	on	on	on
Configuration nonvolatile memory download	off	on	on	on
Configuration nonvolatile memory write	off	off	on	on

[1] x = A, B, C or D.

[2] When 5 V is indicated, a +5 V input signal is available on at least one HDMI input and/or pin AUX_5V is powered.

[3] Nonvolatile memory.

[4] Bit state dependent.

[5] x = A, B, C, D or E.

8.13 Power supplies

The termination supply voltage must be 3.3 V ± 5 % with a termination resistance of 50 Ω ± 10 % as defined in the *HDMI 1.4a specification*.

A dedicated 3.3 V ± 10 % supply (powering interrupt pin INT_N/MUTE) is kept for compatibility with TDA9996. This pin shall be connected to the rest of 3.3 V supply line.

The 1.8 V supply must also be ±10 %.

A double Power-On Reset (POR) is implemented to manage different delays between both supply ramp-ups. POR is managed internally without a reset pin. All 1.8 V power supply pins (V_{DDDC}, V_{DDH}, V_{DDO}) could be connected together (i.e. these pins must be shorted out).

+5 V from the HDMI connector and AUX_5V pin are used to supply the EDID memory and the corresponding DDC-bus slave module. To maintain the EDID (volatile memory part) contents modified by I²C-bus, it is necessary to have +5 V (from HDMI connector or AUX_5V pin) constantly available.

8.14 I²C-bus

The TDA19998HL allows software programming of its internal registers using the I²C-bus. The I²C-bus is a separate bus to the DDC-bus, ensuring that I²C-bus programming of the TDA19998HL's registers does not influence DDC-bus operation. The TDA19998HL supports I²C-bus Fast-mode (400 kHz).

8.14.1 I²C-bus protocol

To access registers, the TDA19998HL uses the I²C-bus. The TDA19998HL acts as an I²C-bus slave device. Pin I2C_SCL is used as the input pin. Both Fast-mode (400 kHz) and Standard-mode (100 kHz) are supported by the TDA19998HL. The slave I²C-bus address is shown in Table 5.

The I²C-bus slave address is 1100 A2 A1 A0 R/W. Address bit values are stored in the non-volatile configuration memory and enable selection of the slave address. The default slave address value is 1100 000x.

The I²C-bus slave address is identical to TDA9996.

Table 5. Default slave address

Device type	Bit							
	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
TDA19998HL	1	1	0	0	A2	A1	A0	1/0

I²C-bus access is explained in Figure 3. The I²C-bus master writes the TDA19998HL address and the subaddress to access the specific register, then it writes the data.

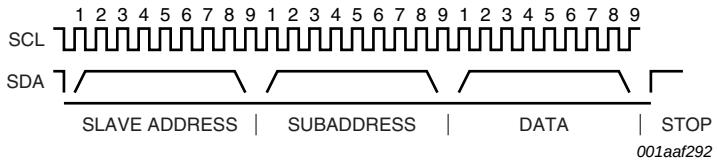


Fig 3. I²C-bus access

8.14.2 Memory page management

The I²C-bus memory is split into several pages, selected using the common register CURPAGE_ADR. It is only necessary to write in this register once to change the current page. Multiple read or write operations in the same page must start by writing to register CURPAGE_ADR once.

- Page 00h: general control
- Page 20h: EDID block0
- Page 21h: EDID block1 and control
- Page 22h: alternative EDID block0
- Page 30h: configuration

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDx(3V3)}$	supply voltage on all 3.3 V pins		–0.5	+4.6	V
$V_{DDx(1V8)}$	supply voltage on all 1.8 V pins		–0.5	+2.5	V
ΔV_{DD}	supply voltage difference		–0.5	+0.5	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		0	+70	°C
T_j	junction temperature		-	+125	°C
HDMI input pins: RXx_D0+, RXx_D0–, RXx_D1+, RXx_D1–, RXx_D2+, RXx_D2–, RXx_C+, RXx_C–, RXx_HPD, RXx_5V, RXy_DDC_DAT, RXy_DDC_CLK, CEC[1][2]					
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 class 3 (contact discharge)	7	-	kV
HDMI output pins: OUT_D0+, OUT_D0–, OUT_D1+, OUT_D1–, OUT_D2+, OUT_D2–, OUT_C+, OUT_C–, OUT_DDC_BAT, OUT_DDC_CLK					
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 class 2 (contact discharge)	5	-	kV
All pins					
V_{ESD}	electrostatic discharge voltage	EIA/JESD22-A114-F (human body model) class 2	–2500	+2500	V
		EIA/JESD22-A115-A (machine model) class B	–200	+200	V
		EIA/JESD22-C101-D (FCDM) class IV	1500	-	V

[1] x = A, B, C, D.

[2] y = A, B, C, D, E.

10. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	49.5	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		18.9	K/W

11. Characteristics

Table 8. Characteristics

$V_{DDH(3V3)}$ = 3.13 V to 3.47 V; $V_{DDDC(3V3)}$ = 3.0 V to 3.6 V; $V_{DDH(1V8)}$ = 1.65 V to 1.95 V; $V_{DDDC(1V8)}$ = 1.65 V to 1.95 V; T_{amb} = 0 °C to +70 °C; typical values measured at $V_{DDH(3V3)}$ and $V_{DDDC(3V3)}$ = 3.3 V; $V_{DDH(1V8)}$ and $V_{DDDC(1V8)}$ = 1.8 V and T_{amb} = 25 °C; f_{max} = 2.25 GHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
$V_{DDH(3V3)}$	HDMI supply voltage (3.3 V)		3.13	3.3	3.47	V
$V_{DDH(1V8)}$	HDMI supply voltage (1.8 V)		1.65	1.8	1.95	V

Table 8. Characteristics *...continued*

$V_{DDH(3V3)}$ = 3.13 V to 3.47 V; $V_{DDDC(3V3)}$ = 3.0 V to 3.6 V; $V_{DDH(1V8)}$ = 1.65 V to 1.95 V; $V_{DDDC(1V8)}$ = 1.65 V to 1.95 V; T_{amb} = 0 °C to +70 °C; typical values measured at $V_{DDH(3V3)}$ and $V_{DDDC(3V3)}$ = 3.3 V; $V_{DDH(1V8)}$ and $V_{DDDC(1V8)}$ = 1.8 V and T_{amb} = 25 °C; f_{max} = 2.25 GHz; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DDS(3V3)}$	supervisor supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDDC(3V3)}$	core digital supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDDC(1V8)}$	core digital supply voltage (1.8 V)			1.65	1.8	1.95	V
$V_{DDO(3V3)}$	output supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDO(1V8)}$	output supply voltage (1.8 V)			1.65	1.8	1.95	V
$I_{DDH(3V3)}$	HDMI supply current (3.3 V)		[1][2]	-	22	29	mA
$I_{DDH(1V8)}$	HDMI supply current (1.8 V)			-	13	16	mA
$I_{DDS(3V3)}$	supervisor supply current (3.3 V)			-	2	3	mA
$I_{DDDC(3V3)}$	core digital supply current (3.3 V)			-	6	8	mA
$I_{DDDC(1V8)}$	core digital supply current (1.8 V)	Pin 8		-	51	70	mA
		Pin 45		-	77	90	mA
		Pin 91		-	92	105	mA
$I_{DDO(3V3)}$	output supply current (3.3 V)			-	23	28	mA
$I_{DDO(1V8)}$	output supply current (1.8 V)			-	15	18	mA
I_{AUX_5V}	current on pin AUX_5V			-	3	5	mA
$T_{j(max)}$	maximum junction temperature	$R_{th(j-a)}$ = 49.5 K/W		-	-	124	°C
P_{cons}	Power consumption	0 = Power-down; no 5 V					
		3.3 V		-	-	0	mW
		1.8 V		-	-	0	mW
		1 = EDID read only; using +5 V (20 mW) from source for EDID					
		3.3 V		-	-	0	mW
		1.8 V		-	-	0	mW
		2 = Idle mode; EDID + I^2C-bus + HDMI, no HDMI activity on selected input, 20 mW from source					
		3.3 V	[3]	-	-	28	mW
		1.8 V		-	-	15	mW
		3 = Operating mode; all ON, with HDMI activity on selected input					
		3.3 V	[3]	-	-	241	mW
		1.8 V		-	-	583	mW
		total power consumption in Operating mode	[3]	-	-	824	mW

Table 8. Characteristics *...continued*

$V_{DDH(3V3)}$ = 3.13 V to 3.47 V; $V_{DDDC(3V3)}$ = 3.0 V to 3.6 V; $V_{DDH(1V8)}$ = 1.65 V to 1.95 V; $V_{DDDC(1V8)}$ = 1.65 V to 1.95 V; T_{amb} = 0 °C to +70 °C; typical values measured at $V_{DDH(3V3)}$ and $V_{DDDC(3V3)}$ = 3.3 V; $V_{DDH(1V8)}$ and $V_{DDDC(1V8)}$ = 1.8 V and T_{amb} = 25 °C; f_{max} = 2.25 GHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HDMI inputs: pins RXx_C+, RXx_C−, RXx_D0+, RXx_D0−, RXx_D1+, RXx_D1−, RXx_D2+, RXx_D2−[4]						
$V_{i(dif)}$	differential input voltage	R12K = 12 kΩ ± 1 %	150	-	1200	mV
$V_{I(cm)}$	common-mode input voltage		2.735	-	3.475	V
HDMI output pins: OUT_D0+, OUT_D0−, OUT_D1+, OUT_D1−, OUT_D2+, OUT_D2−, OUT_C+, OUT_C−						
$V_{o(p-p)}$	peak-to-peak output voltage	with test load and operating conditions as described in the *HDMI 1.4a specification*	400	525	600	mV
V_{OH}	HIGH-level output voltage		3.125	3.3	3.475	V
V_{OL}	LOW-level output voltage		2.535	2.8	3.065	V
HDMI pins: OUT_C+, OUT_C−, RXx_C+, RXx_C−[4]						
$f_{clk(max)}$	maximum clock frequency		225	-	-	MHz
HDMI pins: OUT_D0+, OUT_D0−, OUT_D1+, OUT_D1−, OUT_D2+, OUT_D2−, RXx_D0+, RXx_D0−, RXx_D1+, RXx_D1−, RXx_D2+, RXx_D2−[4]						
f_{max}	maximum frequency		2.25	-	-	GHz
Digital inputs[5]: pin PD						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
Digital inputs[5]: pin RXx_HPD[4]						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
C_i	input capacitance		-	-	2.8	pF
Digital outputs: pin INT_N/MUTE						
V_{OH}	HIGH-level output voltage	C_L = 10 pF; I_{OH} = 2 mA	2.4	-	-	V
V_{OL}	LOW-level output voltage	C_L = 10 pF; I_{OL} = 2 mA	-	-	0.4	V
I^2C-bus: pins I2C_SCL and I2C_SDA (Fast-mode)[5]						
f_{SCL}	SCL clock frequency		-	-	400	kHz
C_b	capacitive load for each bus line		-	-	400	pF
C_i	input capacitance		-	-	10	pF
DDC I^2C-bus: pins RXx_DDC_DAT and RXx_DDC_CLK[5][6]						
f_{SCL}	SCL clock frequency	Standard-mode	-	-	100	kHz
		Fast-mode	-	-	400	kHz
C_i	input capacitance		-	-	10	pF
DDC I^2C-bus[5]: master bus; pins OUT_DDC_DAT and OUT_DDC_CLK						
f_{SCL}	SCL clock frequency	Standard-mode	-	-	100	kHz
		Fast-mode	-	-	400	kHz
MTP endurance						
$N_{endu(W)}$	write endurance	number of cycles at $T_{j(max)}$	1000	-	-	

[1] Typical values: add 40 mA by connected link for regulator dimensioning.

[2] Maximum values: add 48 mA by connected link for regulator dimensioning.

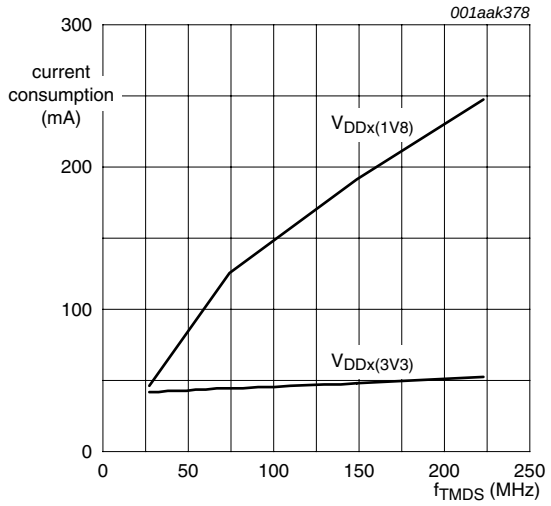
[3] Maximum values: add 167 mW by connected link for regulator dimensioning (12 mA × 3.47 V = 167 mW).

[4] x = A, B, C, D.

[5] 5 V tolerant.

[6] x = A, B, C, D, E.

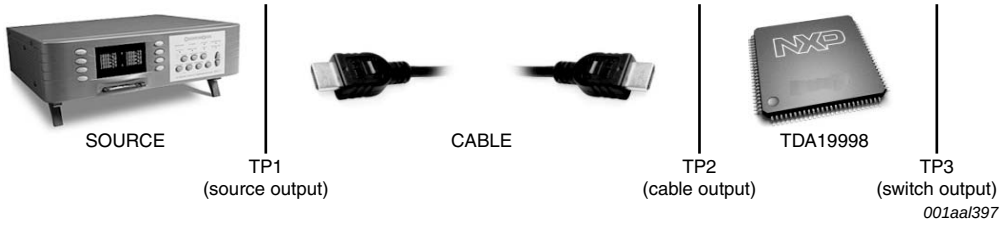
12. Typical operating characteristics



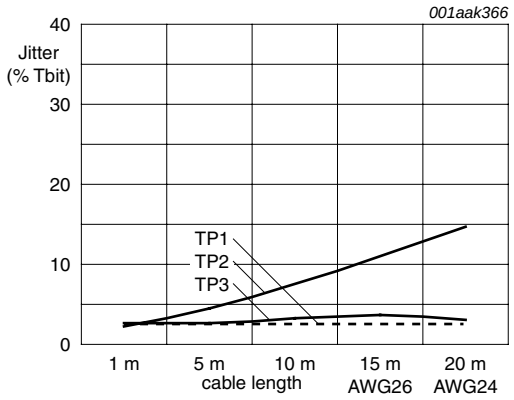
(1) $V_{DDx(1V8)}$ = sum of current from all $V_{DD(1V8)}$ supply pins.

(2) $V_{DDx(3V3)}$ = sum of current from all $V_{DD(3V3)}$ supply pins, excluding current from HDMI source.

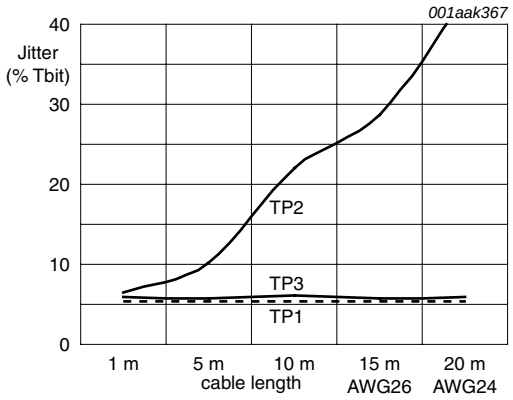
Fig 4. Typical current consumption



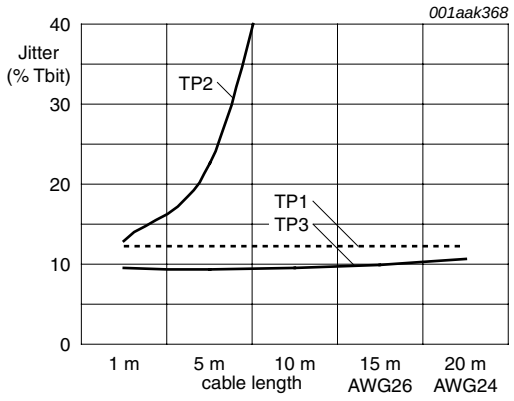
a. Jitter measurement test bench



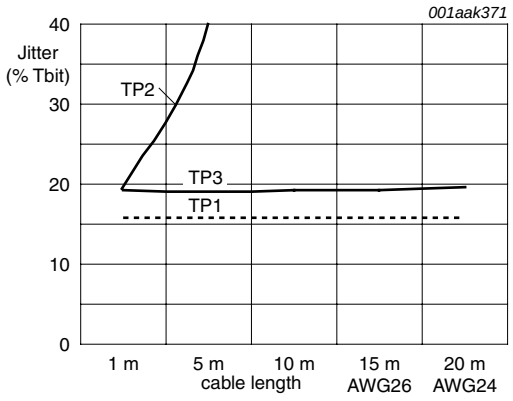
b. Typical jitter measurement in 480p60 24-bit deep color video format



c. Typical jitter measurement in 720p60 24-bit deep color video format

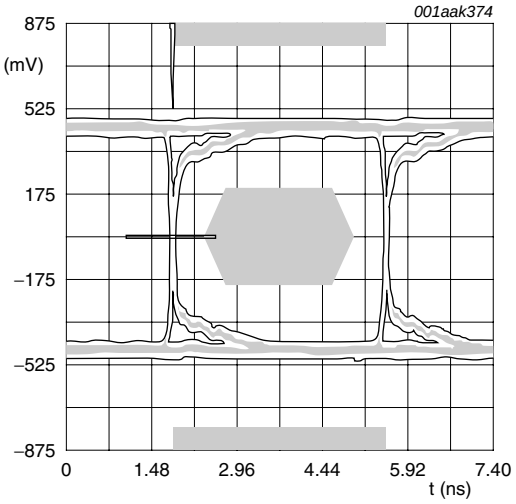


d. Typical jitter measurement in 1080p60 24-bit deep color video format

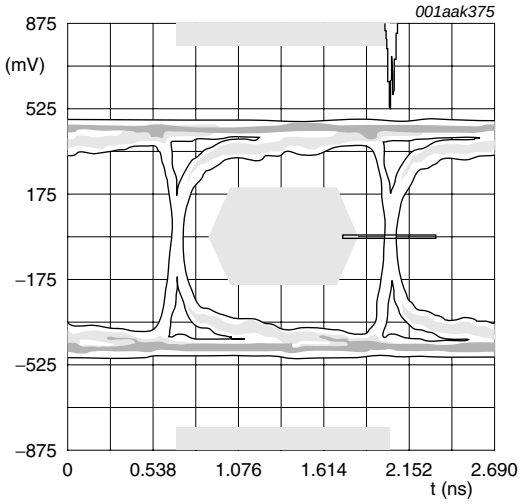


e. Typical jitter measurement in 1080p60 36-bit deep color video format

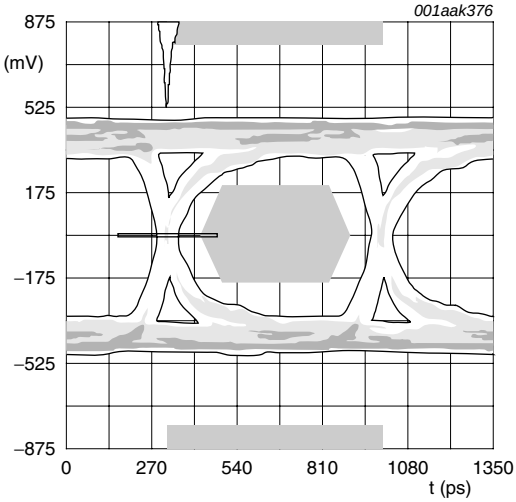
Fig 5. Typical jitter measurement



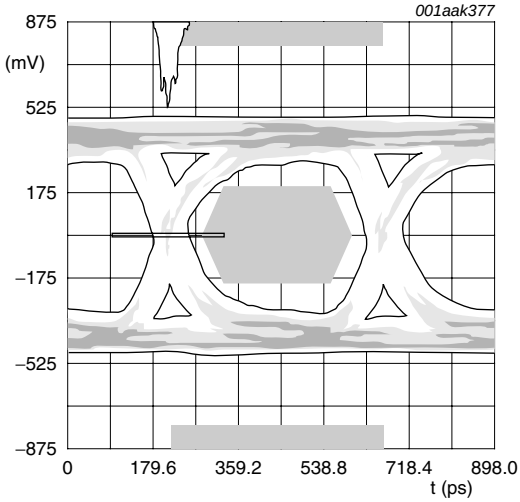
a. Typical eye diagram in 480p60 24-bit deep color video format



b. Typical eye diagram in 720p60 24-bit deep color video format



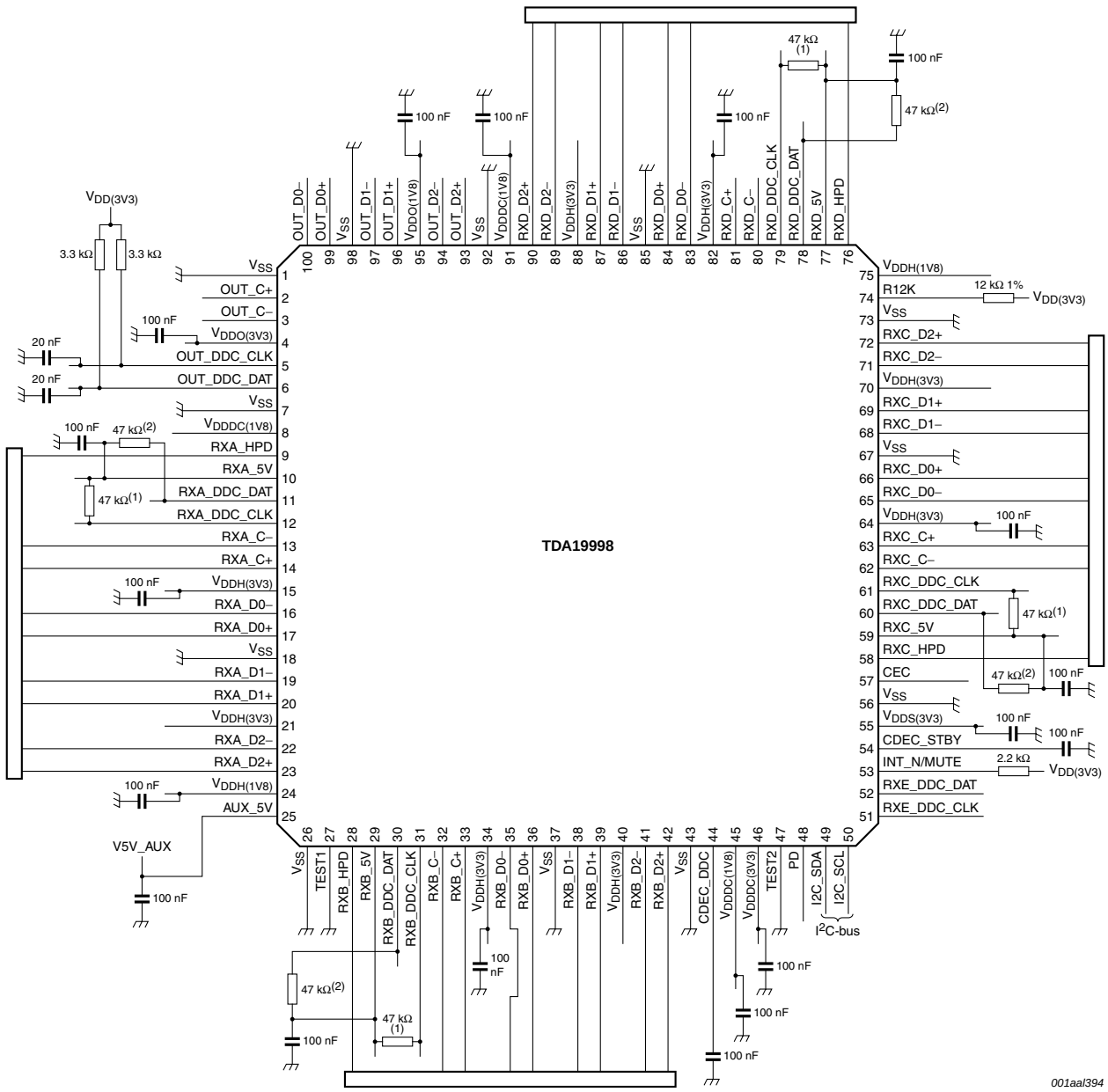
c. Typical eye diagram in 1080p60 24-bit deep color video format



d. Typical eye diagram in 1080p60 36-bit deep color video format

Fig 6. Typical eye diagram measurement with Tx compliancy mask

13. Application information



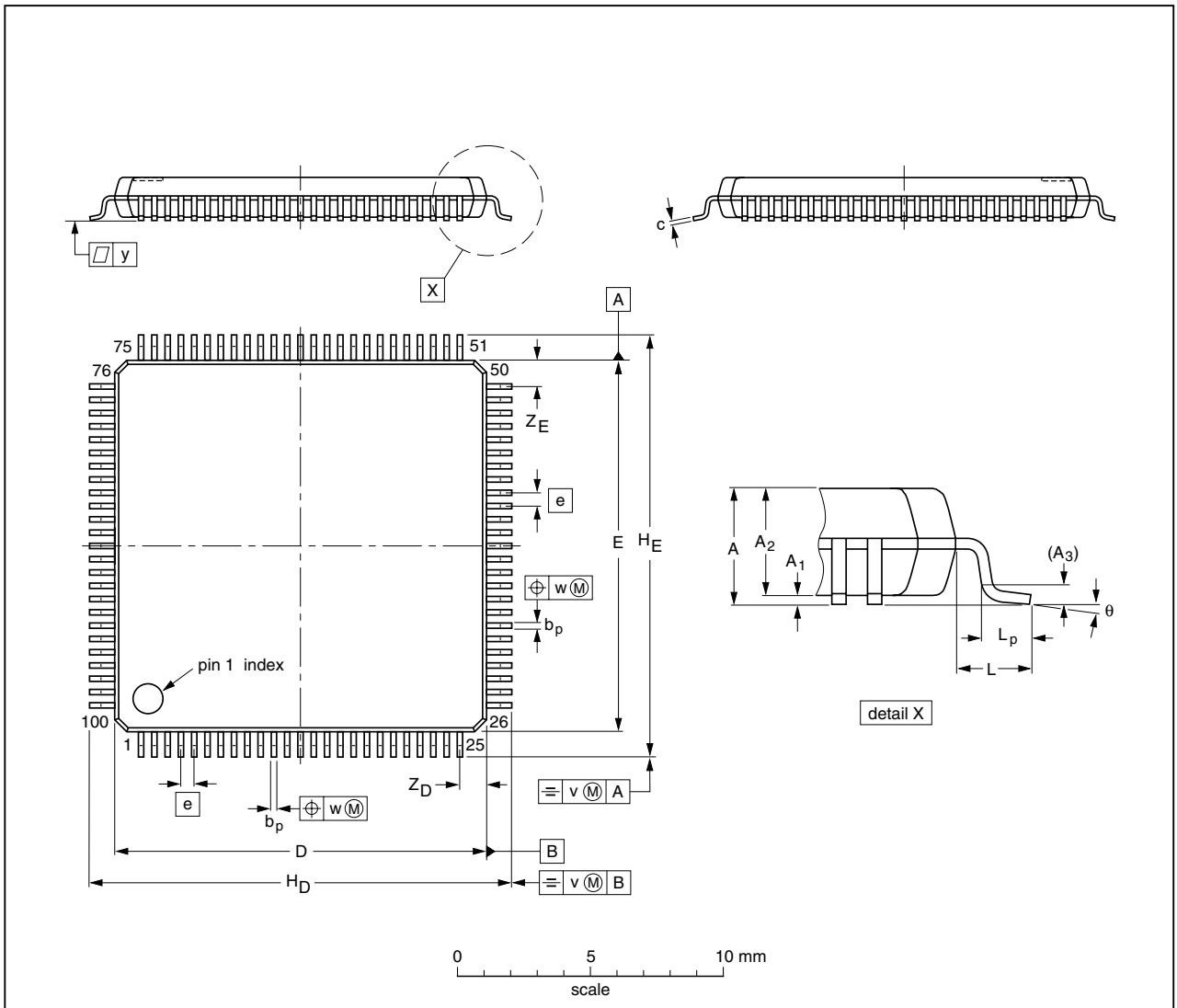
(1) Mandatory.

(2) Recommended.

Fig 7. Application diagram

14. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 8. Package outline SOT407-1 (LQFP100)

15. Abbreviations

Table 9. Abbreviations

Acronym	Description
ATC	Authorized Test Center
AVR	Audio/Video Receiver
AWG	American Wire Gauge
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide-Semiconductor
DDC	Display Data Channel
DVI	Digital Video Input
EDID	Extended Display Identification Data
ESD	ElectroStatic Discharge
EQ	EQualizer
FCDM	Field Charged Device Model
HBM	Human Body Model
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition TeleVision
HEAC	HDMI Ethernet Audio return Channel
HPD	Hot Plug Detect
I^2C	Inter-Integrated Circuit
LCD	liquid crystal display
MM	Machine Model
MTP	Multi-Time Programmable
POR	Power-On Reset
RGB	Red/Green/Blue
RT	Resistor Termination
SoC	System On a Chip
TMDS	Transition Minimized Differential Signaling
VGA	Video Graphic Array
YCbCr	Y = Luminance, Cb = Chroma blue, Cr = Chroma red

16. References

[1] **HDMI 1.4a —** High-Definition Multimedia Interface; Specification Version 1.4a; 4 March 2010.

[2] **CEA-861D —** A DTV profile for Uncompressed High-Speed Digital Interfaces; CEA-861rDv18; 5 August 2006.

[3] **IEC-60958 —** Digital audio interface - Part 1: General; Second edition; March 2004. Digital audio interface - Part 3: Consumer applications; Second edition; January 2003.

[4] **IEC-61937 —** Digital audio interface - Interface for non-linear PCM encode audio bit stream applying IEC-60958 - Part 1: General; First edition; May 2003.

[5] **HDCP 1.4 —** High-bandwidth Digital Content Protection; Revision 1.4; 8 July 2009.

[6] **E-DDC 1.1 —** VESA Enhanced Display Data Channel Standard; Version 1.1; 24 March 2004.

[7] **DVI 1.0 —** DVI Digital Video Interface; Revision 1.0; 2 April 1999.

17. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA19998HL v.3	20100804	Product data sheet	-	TDA19998HL v.2
Modifications:	• Figure 7: updated to fit with I^2C specification, on pins 5 and 6 changed pull-up resistors to 3.3 kΩ and added 20 nF loading capacitors			
TDA19998HL v.2	20100601	Product data sheet	-	TDA19998HL v.1
TDA19998HL v.1	20100330	Objective data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Tables

21. Figures

22. Contents

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Date of release: 4 August 2010
Document identifier: TDA19998HL