

# SN54ALS86, SN54AS86A, SN74ALS86, SN74AS86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SDAS006B – APRIL 1982 – REVISED DECEMBER 1994

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean functions  $Y = A \oplus B$  or  $Y = \overline{A}B + A\overline{B}$  in positive logic.

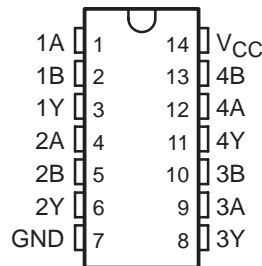
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN54ALS86 and SN54AS86A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS86 and SN74AS86A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

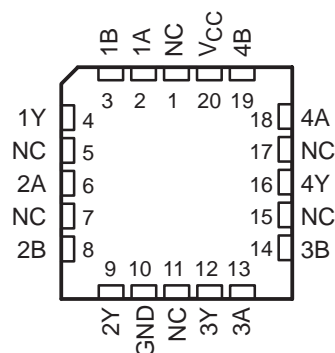
FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

SN54ALS86, SN54AS86A . . . J PACKAGE  
SN74ALS86, SN74AS86A . . . D OR N PACKAGE  
(TOP VIEW)

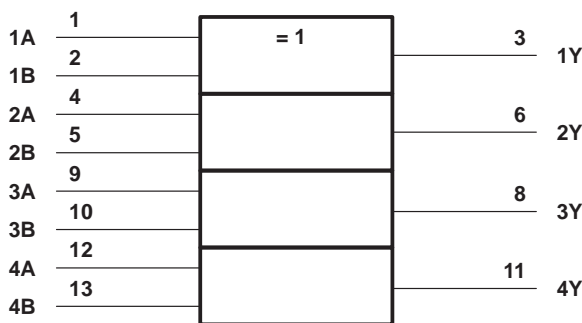


SN54ALS86, SN54AS86A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## logic symbol†



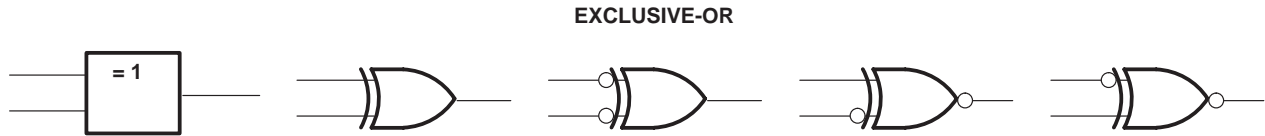
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

# SN54ALS86, SN54AS86A, SN74ALS86, SN74AS86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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## exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



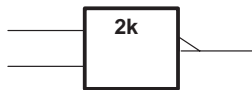
These are five equivalent exclusive-OR symbols valid for an 'ALS86 or 'AS86A gate in positive logic. Negation may be shown at any two ports.

### LOGIC-IDENTITY ELEMENT



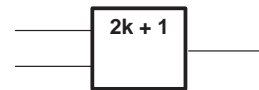
The output is active (low) if all inputs are at the same logic level (i.e.,  $A = B$ ).

### EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

### ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

# SN54ALS86, SN54AS86A, SN74ALS86, SN74AS86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SDAS006B – APRIL 1982 – REVISED DECEMBER 1994

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54ALS86	-55°C to 125°C
SN74ALS86	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54ALS86			SN74ALS86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			-0.4			-0.4	mA
$I_{OL}$	Low-level output current			4			8	mA
$T_A$	Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS86			SN74ALS86			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5 V$ , $I_I = -18 mA$			-1.5			-1.5	V
$V_{OH}$	$V_{CC} = 4.5 V$ to $5.5 V$ , $I_{OH} = -0.4 mA$	$V_{CC} - 2$			$V_{CC} - 2$			V
$V_{OL}$	$V_{CC} = 4.5 V$	$I_{OL} = 4 mA$		0.25	0.4	$I_{OL} = 4 mA$		V
		$I_{OL} = 8 mA$				0.35	0.5	
$I_I$	$V_{CC} = 5.5 V$ , $V_I = 7 V$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5 V$ , $V_I = 2.7 V$			20			20	μA
$I_{IL}$	$V_{CC} = 5.5 V$ , $V_I = 0.4 V$			-0.1			-0.1	mA
$I_{O§}$	$V_{CC} = 5.5 V$ , $V_O = 2.25 V$	-20		-112	-30		-112	mA
$I_{CC}$	$V_{CC} = 5.5 V$ , All inputs at 4.5 V		3.9	5.9		3.9	5.9	mA

‡ All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25°C$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 V$ to $5.5 V$ , $C_L = 50 pF$ , $R_L = 500 \Omega$ , $T_A = MIN$ to $MAX$ ¶				UNIT
			SN54ALS86		SN74ALS86		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B (other input low)	Y	3	22	3	17	ns
$t_{PHL}$			2	14	2	12	
$t_{PLH}$	A or B (other input high)	Y	3	22	3	17	ns
$t_{PHL}$			2	12	2	10	

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



# SN54ALS86, SN54AS86A, SN74ALS86, SN74AS86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SDAS006B – APRIL 1982 – REVISED DECEMBER 1994

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54AS86A	-55°C to 125°C
SN74AS86A	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

	SN54AS86A			SN74AS86A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$I_{OH}$ High-level output current			-2			-2	mA
$I_{OL}$ Low-level output current			20			20	mA
$T_A$ Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS86A			SN74AS86A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -2\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 20\text{ mA}$	0.35	0.5		0.35	0.5		V
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$		0.1			0.1		mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$		20			20		μA
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$		-0.5			-0.5		mA
$I_{OS}§$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-30	-112		-30	-112		mA
$I_{CCH}$	$V_{CC} = 5.5\text{ V}$ , $V_{I(A)} = 4.5\text{ V}$ , $V_{I(B)} = 0$		11	18		11	18	mA
$I_{CCL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 4.5\text{ V}$		20	38		20	38	mA

‡ All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

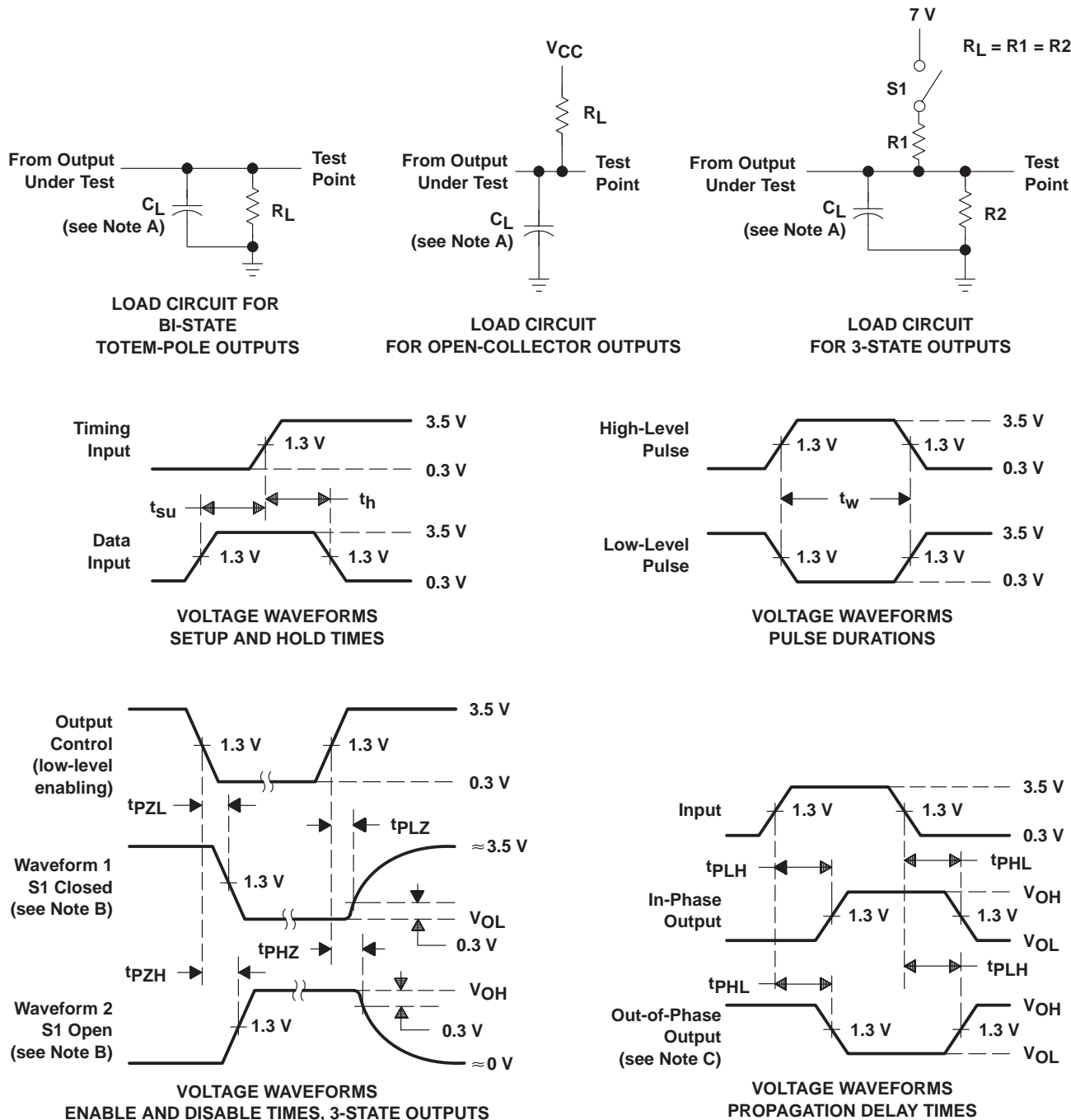
## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 500\ \Omega$ , $T_A = \text{MIN to MAX}¶$				UNIT
			SN54AS86A		SN74AS86A		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B (other input low)	Y	2	8.5	2	7.5	ns
$t_{PHL}$			2	8	2	6.5	
$t_{PLH}$	A or B (other input high)	Y	1	8	1	6.5	ns
$t_{PHL}$			1	9	1	7	

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



PARAMETER MEASUREMENT INFORMATION  
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8862101CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8862101CA SNJ54ALS86J	<a href="#">Samples</a>
5962-8862101DA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8862101DA SNJ54ALS86W	<a href="#">Samples</a>
SN54ALS86J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54ALS86J	<a href="#">Samples</a>
SN74ALS86D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS86	<a href="#">Samples</a>
SN74ALS86DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS86	<a href="#">Samples</a>
SN74ALS86DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS86	<a href="#">Samples</a>
SN74ALS86N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS86N	<a href="#">Samples</a>
SN74ALS86NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS86N	<a href="#">Samples</a>
SN74ALS86NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS86	<a href="#">Samples</a>
SN74AS86AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS86A	<a href="#">Samples</a>
SN74AS86ADG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS86A	<a href="#">Samples</a>
SN74AS86AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74AS86AN	<a href="#">Samples</a>
SNJ54ALS86J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8862101CA SNJ54ALS86J	<a href="#">Samples</a>
SNJ54ALS86W	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8862101DA SNJ54ALS86W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ALS86, SN74ALS86 :**

● Catalog : [SN74ALS86](#)

● Military : [SN54ALS86](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

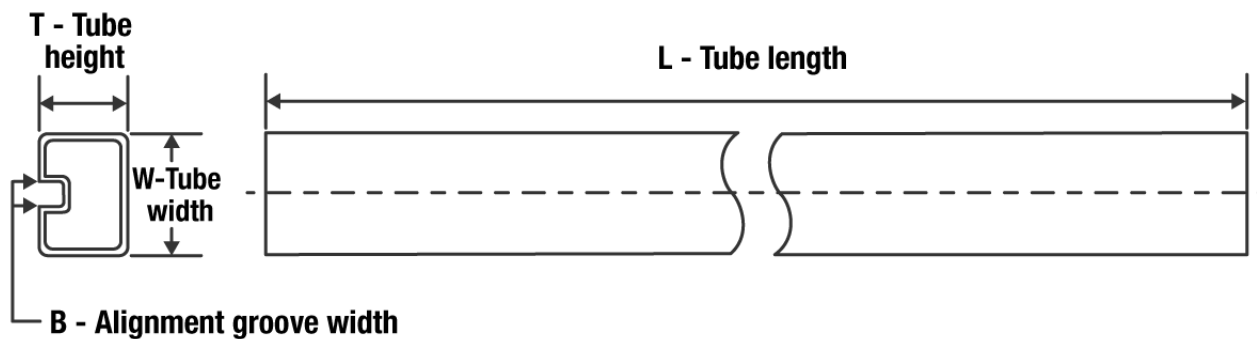
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS86DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ALS86NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS86DR	SOIC	D	14	2500	853.0	449.0	35.0
SN74ALS86NSR	SO	NS	14	2000	853.0	449.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS86D	D	SOIC	14	50	506.6	8	3940	4.32
SN74ALS86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS86NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS86NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74AS86AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74AS86ADG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74AS86AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74AS86AN	N	PDIP	14	25	506	13.97	11230	4.32

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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