SLG46200

GreenPAK™ Programmable Mixed Signal Array

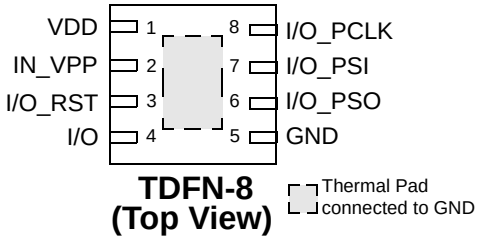
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macro Cells
- 3.3V Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- Pb-Free TDFN-8 2mm x 2mm Package

Applications

- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

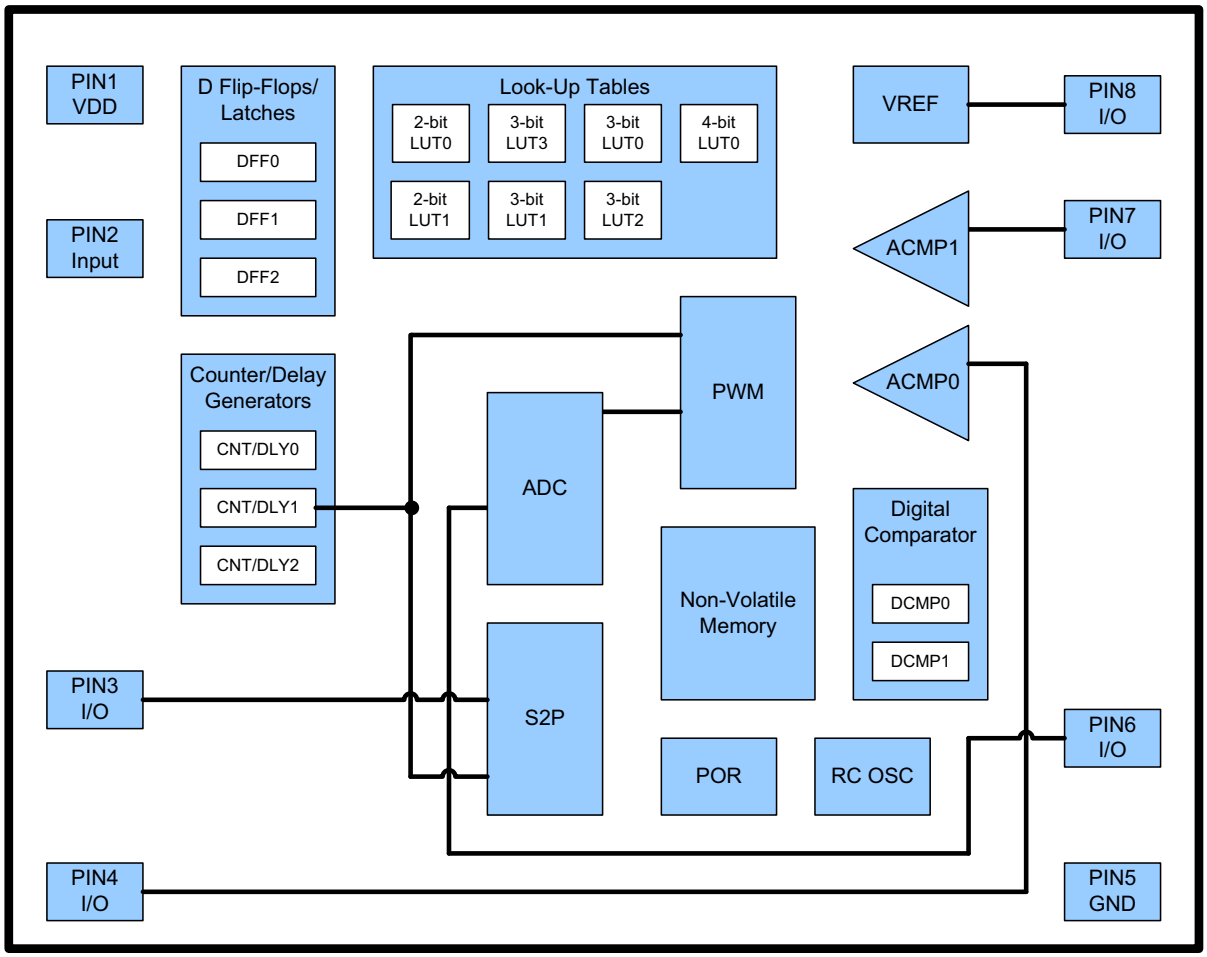
Pin Configuration



TDFN-8 (Top View)

Thermal Pad connected to GND

Block Diagram



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1.0 Overview

The SLG46200 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure interconnect logic, I/O Pins and macro cells of the SLG46200. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macro cells in the device include the following:

- Pulse Width Modulator (PWM)
- 8-Bit Successive Approximation Register Analog to Digital Converter (SAR ADC)
- Serial to Parallel Converter (S2P)
- Power-On Reset Device (POR)
- Voltage Reference (V_{REF})
- RC Oscillator (RC OSC)
- 3 Counter/Delay Generators (CNT/DLY)
- 3 D Flip-Flop/Latches (DFF)
- 2 Digital Comparators (DCMP)
- 2 Analog Comparators (ACMP)
- 7 Combinatorial Lookup Tables (LUT)
- Configurable I/O Pins (Open Drain, Push-Pull, Schmitt Trigger Input, Low Voltage Digital Input and Analog I/O)

The specific functions that can be designed using the SLG46200 include:

- Power-On-Reset Generators
- Signal Delay Elements
- One-Shot Detection
- Voltage Level Detectors
- Voltage Level-Shift Circuits
- Battery Charge Controller
- LED Lighting Control
- Fan Controller
- Optical Encoder
- Level Shifters
- Hall Effect Driver
- Signal De-Glitches
- and many other functions

The PWM and ADC macro cells also support more complex control circuits such fan speed controllers, stepper motor controllers and interface to a wide variety of sensor devices. Traditionally these devices were designed from combinations of low complexity logic and discrete devices requiring costly board space while having complex testing strategies. Silego's SLG46200 allows the functionality of these circuits to be fully tested before being mounted onto a PCB – greatly simplifying the system design and testing procedures.

2.0 Pin Description

2.1 Functional Pin Description

Pin #	Pin Name	Function
1	VDD	3.3V Supply
2	IN_VPP	I
3	I/O_RST	I/O
4	I/O	I/O
5	GND	GND
6	I/O_PSO	I/O
7	I/O_PSI	I/O
8	I/O_PCLK	I/O
Exposed Bottom Pad	GND	GND

2.2 Programming Pin Description

Pin #	Pin Name	Programming Description
1	VDD	3.3V Power
2	IN_VPP	Program Power Voltage
3	I/O_RST	Program Reset
4	I/O	N/A
5	GND	GND
6	I/O_PSO	Program Serial Data Out
7	I/O_PSI	Program Serial Data In
8	I/O_PCLK	Program Clock In

3.0 User Programmability

The SLG46200 is a user programmable device with One-Time-Programmable (OTP) memory elements that are able to construct combinatorial logic elements. Three of the I/O Pins provide a connection for the bit patterns into the OTP on board memory. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpp file) is forwarded to Silego to integrate into a production process.

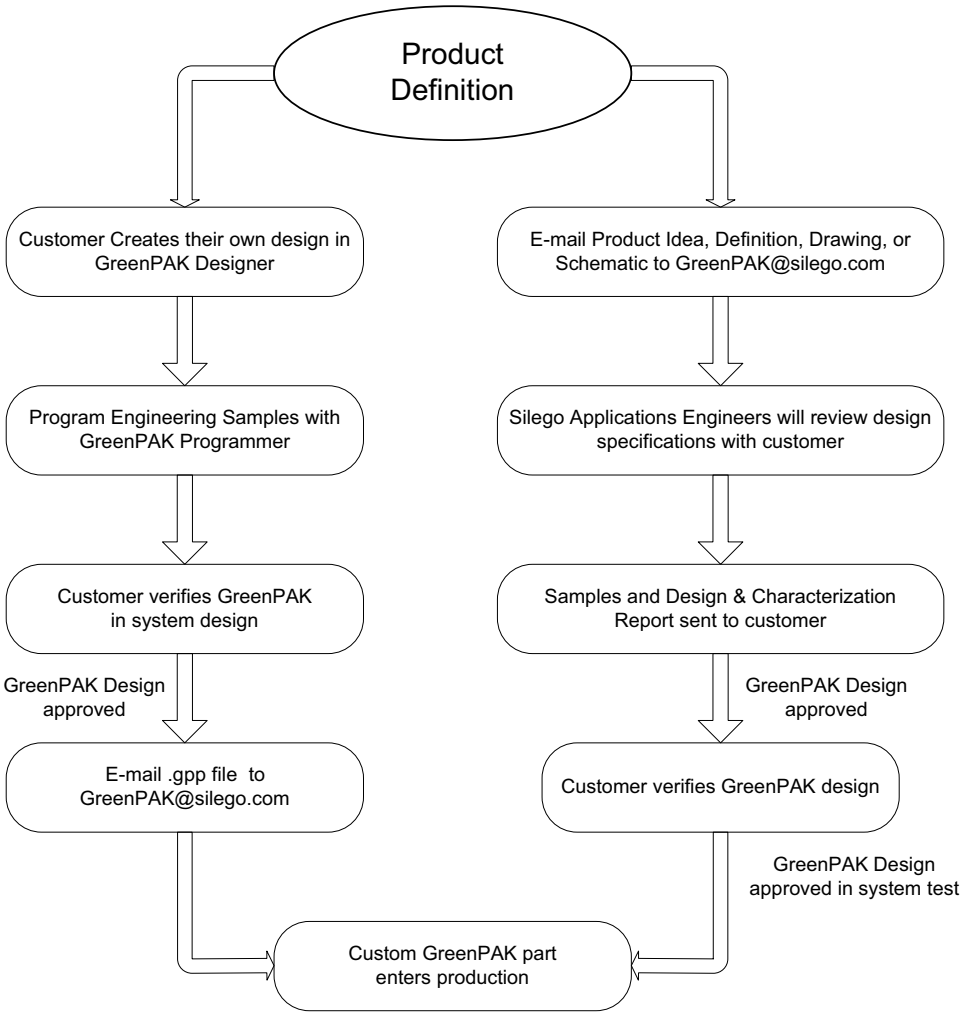


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46200V	TDFN-8
SLG46200VTR	TDFN-8 - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	4.6	V
Voltage at Input Pin	-0.3	4.6	V
Current at Input Pin	-1.0	1.0	mA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Human Body Model	2000	--	V
ESD Machine Model	200	--	V

5.2 Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
V_O	Output Voltage	Voltage range applied to any output in the high-impedance	0	--	V_{DD}	V
V_{PP}	Programming Voltage	Chip programming	--	6.5	--	V
		Chip reading	--	5.0	--	V
V_{AIR}	Analog Input Voltage Range		0	--	2.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.6	--	--	V
		Logic Input with Schmitt Trigger	2.1	--	--	V
		LOW-Level Logic Input	1.0	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.95	V
		Logic Input with Schmitt Trigger	--	--	0.90	V
		LOW-Level Logic Input	--	--	0.50	V
V_{IHYS}	Input Hysteresis	Digital Input with Buffered Schmitt Trigger	--	±250	--	mV
I_{IH}	HIGH-Level Input Leakage Current	Logic Input Pins; V_{IN}=3.3V	-100	--	100	nA
I_{IL}	LOW-Level Input Leakage Current	Logic Input Pins; V_{IN}=0V	-100	--	100	nA
V_{OH}	HIGH-Level Output Voltage	CMOS Push-Pull, Logic Level Outputs	2.4	--	3.3	V
V_{OL}	LOW-Level Output Voltage	CMOS Push-Pull, Open Drain Logic Level Outputs	0	--	0.4	V
I_{OH}	HIGH-Level Output Current	Push-Pull Double Current	--	16	--	mA
		Push Pull	--	8	--	mA
I_{OL}	LOW-Level Output Current	1X Open Drain	--	20	--	mA
		2X Open Drain	--	40	--	mA
		Push-Pull Double Current	--	-16	--	mA
		Push Pull	--	-8	--	mA
T_{SU}	Startup Time	After VDD reaches 2.5V	--	7[1]	--	ms
T_{PD}	Propagation Delay	Single LUT Cell from Output to Input Pin	--	25	--	ns

1. If startup time lower than 7 ms is required, please contact Silego regarding a potential custom mixed-signal IC with a reduced startup time for your design.

5.3 Logic Cell Current Measurements

V_{DD} = 3.3V, T_A = 25°C (unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{VREF}	V_{REF} Current	V_{REF}	--	15.0	--	µA
		V_{REF} + 2 ACMP	--	32.0	--	
		V_{REF} + ADC Single-end mode (0V)	--	48.0	--	
		V_{REF} + ADC Single-end mode (1.75V)	--	75.0	--	
		V_{REF} + ADC Single-end mode (0V) + RC OSC (10MHz)	--	230.0	--	
		V_{REF} + ADC Differential mode (1V) + RC OSC (10MHz)	--	250.0	--	
		V_{REF} + ADC Single-end mode (1.75V) + RC OSC (10MHz)	--	370.0	--	
I_{PWM}	PWM Current	@3.0V	--	13.6	--	µA
		@3.3V	--	15.9	--	
		@3.6V	--	18.0	--	
I_{REG}	Power Regulator Current	@3.0V	--	0.65	--	µA
		@3.3V	--	0.75	--	
		@3.6V	--	0.8	--	
$I_{RC\ OSC}$	RC Oscillator Current	@ 43kHz + V_{REF}	--	19.0	--	µA
		@ 85kHz + V_{REF}	--	21.0	--	
		@ 128kHz + V_{REF}	--	22.5	--	
		@ 160KHz + V_{REF}	--	24.5	--	
		@ 240kHz + V_{REF}	--	27.0	--	
		@ 384kHz + V_{REF}	--	30.5	--	
		@ 440kHz + V_{REF}	--	35.0	--	
		@ 625kHz + V_{REF}	--	39.0	--	
		@ 800kHz + V_{REF}	--	60.0	--	
		@ 870kHz + V_{REF}	--	51.0	--	
		@ 950kHz + V_{REF}	--	51.0	--	
		@ 1290kHz + V_{REF}	--	68.0	--	
		@ 1750kHz + V_{REF}	--	88.0	--	
		@ 2100kHz + V_{REF}	--	86.5	--	
		@ 4800kHz + V_{REF}	--	135.5	--	
		@ 7812kHz + V_{REF}	--	196.0	--	

5.4 Input Pin Current Measurements

V_{DD} = 3.3V, T_A = 25°C (unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{INPUT}	Digital Input	Digital Input (1MHz input frequency) with Schmitt Trigger	--	5.5	--	µA
		Digital Input (1MHz input frequency) without Schmitt Trigger	--	4.0	--	
I_{INPUT}	Low Voltage Digital Input	Digital Input (1MHz input frequency) @ 0.9V	--	7.5	--	µA
		Digital Input (1MHz input frequency) @ 1.2V	--	6.5	--	
		Digital Input (1MHz input frequency) @ 1.5V	--	6.5	--	
		Digital Input (1MHz input frequency) @ 1.8V	--	6.5	--	
I_{INPUT}	Low Voltage Digital Input	Digital Input (100kHz input frequency) @ 0.9V	--	1.0	--	µA
		Digital Input (100kHz input frequency) @ 1.2V	--	0.8	--	
		Digital Input (100kHz input frequency) @ 1.5V	--	0.7	--	
		Digital Input (100kHz input frequency) @ 1.8V	--	0.7	--	
I_{INPUT}	Low Voltage Digital Input	Digital Input (constant voltage) @ 0.0V	--	<1.0	--	µA
		Digital Input (constant voltage) @ 0.9V	--	<1.0	--	

6.0 Summary of Macro Cell Function

6.1 I/O Pins (6 total)

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain
- Push-Pull
- Analog I/O
- 50kΩ/100kΩ/300kΩ pull-up/pull-down resistors

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Delays/Counters (CNT/DLY 3 total)

- 0.5µs to 380ms (4.5s for DLY1) delay time range
- Three 14-bit counters (one Finite State Machine counter)

6.4 Analog to Digital Converter (ADC)

- 8-bit, up to 7.5kHz, Successive Approximation Register ADC
- DNL < ±1LSB, INL < ±2LSB
- V_{IN} Range: 0 ~ 1.7V
- Common Mode Voltage Range: $V_{PP}/2$ ~ $V_{DD}/2$
- 3-bit Programmable Gain Amplifier with gain values of (1, 2, 4, 8,16X in differential mode and 0.5, 1, 2, 4, 8X in single-ended mode)
- SPI output format

6.5 Analog Comparators (ACMP 2 total)

- 50mV Hysteresis

6.6 Pulse Width Modulator (PWM)

- 8-bit
- Clock Frequency 43kHz - 7.8MHz, with dead band control

6.7 Digital Comparators (DCMP 2 total)

- 8-bit
- Clock Frequency 43kHz - 7.8MHz

6.8 Serial-to-Parallel / Parallel-to-Serial Converter (S2P)

- Serial-to-Parallel
- Parallel-to-Serial
- SPI Format

6.9 Combinatorial Logic LUTs (7 total)

- Used to create either standard or custom digital logic functions
- Two 2-bit Lookup Tables
- Four 3-bit Lookup Tables
- One 4-bit Lookup Tables

6.10 Logic Storage Devices (DFFs/LATCHes 3 total)

- D Flip-Flops or Latches

7.0 I/O Pins

The SLG46200 has a total of six multi-function I/O Pins which can be used as either a user defined Input or Output, as well as serve as the interface for the one time Non-Volatile Memory for configuration.

Normal Mode Pin Definition is as follows:

- PIN 2: (input pin only) used for ADC Channel Select, GPI
- PIN 3: Serial Data transfer for either SPI (input & output) or ADC (output), GPIO
- PIN 4: Analog Comparator 0 input, SPI clock input or ADC external clock, GPIO
- PIN 6: ADC IN+, GPIO
- PIN 7: ADC IN- or Analog Comparator 1 input, GPIO
- PIN 8: ADC & ACMP V_{REF} input & output or V_{REF} output, GPIO

Progamming Mode Pin Definition is as follows:

- PIN 2: Voltage for Programming Power
- PIN 3: Program Reset
- PIN 6: Program Serial Data Output
- PIN 7: Program Serial Data Input
- PIN 8: Program Clock Input

Of the six user defined I/O Pins in the SLG46200, five pins (PINs 3, 4, 6, 7 and 8) can be used for either input or output and one pin (PIN 2) is defined as input only.

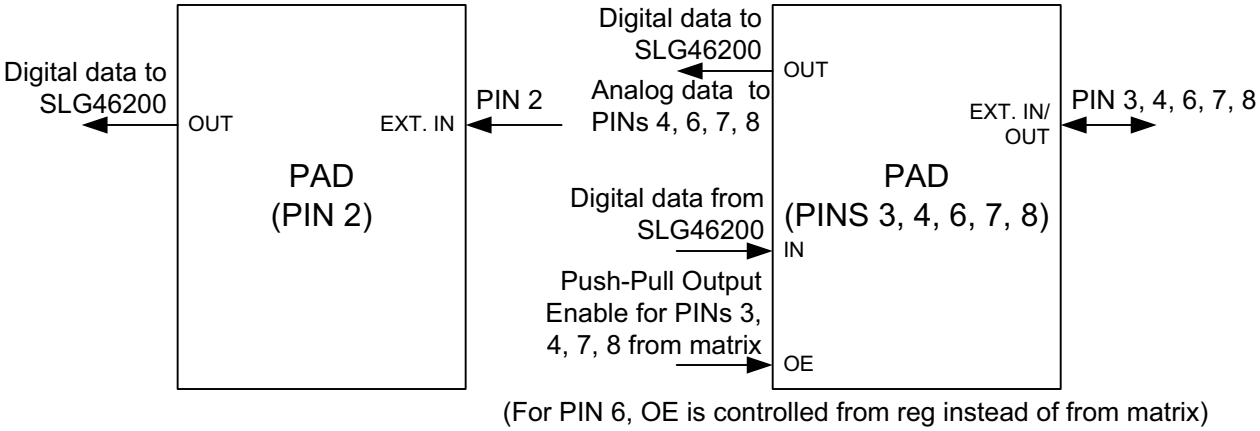


Figure 2. I/O Pads Layout

7.1 Input Modes

Each input pin can be configured as a Digital Input with/without Buffered Schmitt Trigger, Low Voltage Digital In, or Analog In to control the user signals that are inputted into the SLG46200. All digital input pins will either have a logic “1” or “0” value inputted into the SLG46200, based on the configuration of the input pin which is defined by the user.

7.2 Output Modes

PIN 3, PIN4, PIN6, PIN7 and PIN8 can be configured as either an open drain output or push-pull output (with Output Enable). Additionally PIN 8 can be also be configured as an analog output in the SLG46200 device.

The OE functionality for each of the output pins is controlled by the connection matrix except for PIN 6, which is controlled by a register bit, reg<406>.

7.2.1 Open Drain Output

The Open Drain Output setting has a 1X current ratio. The open drain output signal from the SLG46200 design will decide the port's output state (Hi-Z or ground).

If the signal = 1, output will be Hi-Z (high impedance)

If the signal = 0, output will be connected to ground

PINs 4 and 8 have a 2X current sinking option and the current of the output pin will be 40mA.

7.2.2 Push Pull with Output Enable

The Push Pull with Output Enable setting has either a 1X or 2x current ratio and the Output Enable signal will make the output Hi-Z.

PIN 3, PIN 4, PIN 6, PIN 7 and PIN 8 have an Push Pull 2X current sinking option that produces a 16mA current.

7.2.3 Analog Output

Analog output functionality of V_{REF} is only available on PIN 8.

Analog Output = internal signal value

7.3 Creating a Bi-Directional Pin

PIN 3, PIN 4, PIN 7, and PIN 8 can be configured as Bi-Directional Pins with the following steps:

1. Configure the I/O Pins as one of the following:
    a. Digital Input with Schmitt Trigger
    b. Digital Input without Schmitt Trigger
    c. Low voltage Digital Input
2. Use a control signal for the Output Enable on the I/O Pin
3. The I/O Pin will function as Push Pull 1x current by setting the OE signal of the pin to HIGH.

7.4 Pull Up/Down Resistors

All six I/O Pins have the option of a 50kΩ/100kΩ/300kΩ pull up/down resistor with ±20% accuracy. Resistors can be used with any of the input or output pin configurations previously defined.

7.5 I/O Pins Register Settings

7.5.1 PIN 2 Register Settings

Table 1. PIN 2 Register Settings

Signal Name	Register Bit Address	Register Definition
PIN 2 Mode Control	<321:320>	00: Digital in with Schmitt trigger 01: Digital in without Schmitt trigger 10: Low voltage digital in 11: Reserved
PIN 2 Pull Up/Down Resistor Value Selection	<324:323>	00: Floating 01: 50kΩ resistor 10: 100kΩ resistor 11: 300kΩ resistor
PIN 2 Pull Up/Down Resistor	<325>	0: Pull down resistor 1: Pull up resistor

7.5.2 PIN 3 Register Settings

Table 2. PIN 3 Register Settings

Signal Name	Register Bit Address	Register Definition
PIN 3 Mode Control	<328:326>	000: Digital in with Schmitt trigger 001: Digital in without Schmitt trigger 010: Low voltage digital in 011: Reserved 100: Push pull 2x current 101: Open drain 110: Push pull (output tri-state when OE = 0; output enable when OE = 1) 111: Reserved
PIN 3 Pull Up/Down Resistor Value Selection	<330:329>	00: Floating 01: 50kΩ resistor 10: 100kΩ resistor 11: 300kΩ resistor
PIN 3 Pull Up/Down Resistor	<331>	0: Pull down resistor 1: Pull up resistor
PIN 3 Digital Out Source Selection	<373:372>	00: From connection matrix 01: From connection matrix 10: S2P - serial output data (selection made in S2P properties) 11: ADC - serial output data (selection made in ADC properties)

7.5.3 PIN 4 Register Settings

Table 3. PIN 4 Register Settings

Signal Name	Register Bit Address	Register Definition
PIN 4 Mode Control	<334:332>	000: Digital in with Schmitt trigger 001: Digital in without Schmitt trigger 010: Low voltage digital in 011: Analog in 100: Push pull 2x current 101: Open drain 110: Push pull (output tri-state when OE = 0; output enable when OE = 1) 111: Reserved
PIN 4 Pull Up/Down Resistor Value Selection	<300:299>	00: Floating 01: 50kΩ resistor 10: 100kΩ resistor 11: 300kΩ resistor
PIN 4 Pull Up/Down Resistor	<301>	0: Pull down resistor 1: Pull up resistor
PIN 4 Open Drain 2x Enable	<338>	0: Open drain 2x disable 1: Open drain 2x enable
PIN 4 Digital Out Source Selection	<477>	0: From connection matrix 1: ADC output clock (selection made in ADC properties)

7.5.4 PIN 6 Register Settings

Table 4. PIN 6 Register Settings

Signal Name	Register Bit Address	Register Definition
PIN 6 Mode Control	<298:296>	000: Digital in with Schmitt trigger 001: Digital in without Schmitt trigger 010: Low voltage digital in 011: Analog in 100: Push pull 2x current 101: Open drain 110: Push pull (output tri-state when OE = 0; output enable when OE = 1) 111: Reserved
PIN 6 Pull Up/Down Resistor Value Selection	<300:299>	00: Floating 01: 50kΩ resistor 10: 100kΩ resistor 11: 300kΩ resistor
PIN 6 Pull Up/Down Resistor	<301>	0: Pull down resistor 1: Pull up resistor enable
PIN 6 Output Enable Control	<406>	0: OE disable 1: OE enable

7.5.5 PIN 7 Register Settings

Table 5. PIN 7 Register Settings

Signal Name	Register Bit Address	Register Definition
PIN 7 Mode Control	<304:302>	000: Digital in with Schmitt trigger 001: Digital in without Schmitt trigger 010: Low voltage digital in 011: Analog in 100: Push pull 2x current 101: Open drain 110: Push pull (output tri-state when OE = 0; output enable when OE = 1) 111: Reserved
PIN 7 Pull Up/Down Resistor Value Selection	<306:305>	00: Floating 01: 50kΩ resistor 10: 100kΩ resistor 11: 300kΩ resistor
PIN 7 Pull Up/Down Resistor	<307>	0: Pull down resistor 1: Pull up resistor

7.5.6 PIN 8 Register Settings

Table 6. PIN 8 Register Settings

Signal Name	Register Bit Address	Register Definition
PIN 8 Mode Control	<310:308>	000: Digital in with Schmitt trigger 001: Digital in without Schmitt trigger 010: Low voltage digital in 011: Analog IO 100: Push pull 2x current 101: Open drain 110: Push pull (output tri-state when OE = 0; output enable when OE = 1) 111: Reserved
PIN 8 Pull Up/Down Resistor Value Selection	<312:311>	00: Floating 01: 50kΩ resistor 10: 100kΩ resistor 11: 300kΩ resistor
PIN 8 Pull Up/Down Resistor	<313>	0: Pull down resistor 1: Pull up resistor
PIN 8 Open Drain 2x Enable	<314>	0: Open drain 2x disable 1: Open drain 2x enable

8.0 Digital Comparator (DCMP)

The SLG46200 has two 8-bit digital comparator logic cells available that can operate at up to a clock frequency of 7.8MHz. The input power for each the two DCMP logic cells is controlled by two register bits, reg<402> for DCMP0 and reg<406> for DCMP1.

8.1 DCMP Input Modes

Both DCMP logic cells have a positive (IN+) and a negative (IN-) input that are compared within the logic cell. The *ip* signal (connected to the IN+ input) takes the value from a 2:1 mux selection between an 8-bit S2P logic cell output (S2P<7:0> for DCMP0 and S2P<15:8> for DCMP1) and the output from the SLG46200's ADC Output. The *in* signal (connected to the IN- input) takes the value from a 4:1 mux selection between the 8-bit S2P logic cell output (S2P<15:8>) and one of three 8-bit registers which can have a programmed value ranging from 0 to 255.

8.2 DCMP Output Modes

The two 8-bit data inputs from IN+ and IN- are compared within the DCMP logic cells to produce the output and a match signal.

- If *ip* > *in*, the *OUT* is equal to "1", otherwise the *OUT* is equal to "0"
- If *ip* = *in*, the *EQ* signal is equal to "1", otherwise the *EQ* is equal to "0"

Both the output and match signals are triggered by the falling edge of the *CLK4PWM* signal.

8.3 DCMP0 Functional Diagram

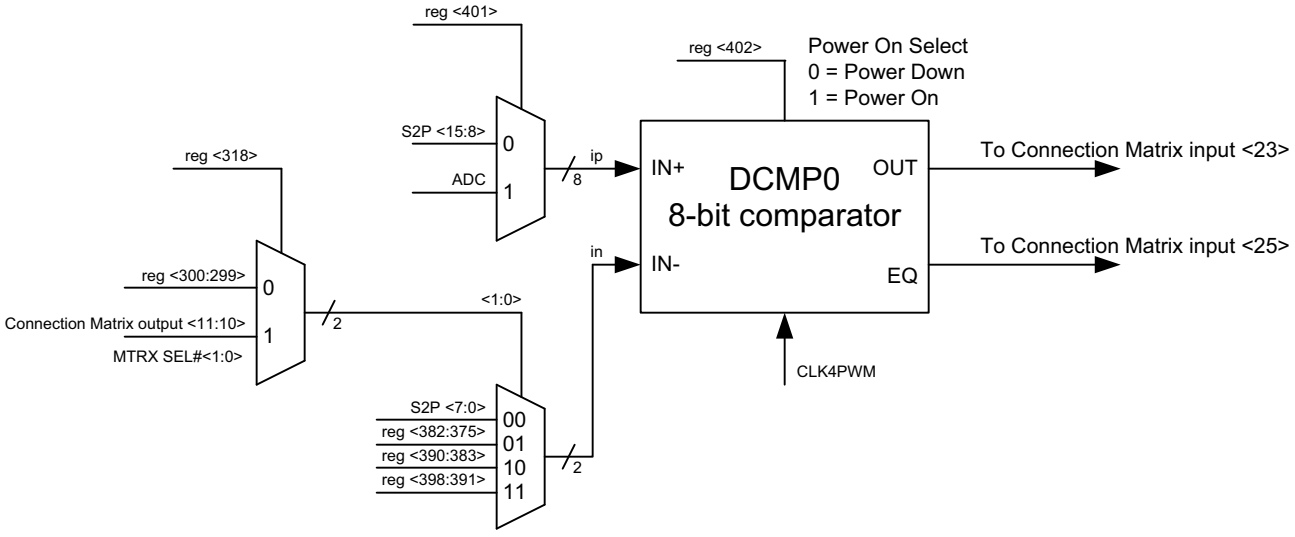


Figure 3. DCMP0 Functional Diagram

8.4 DCMP1 Functional Diagram

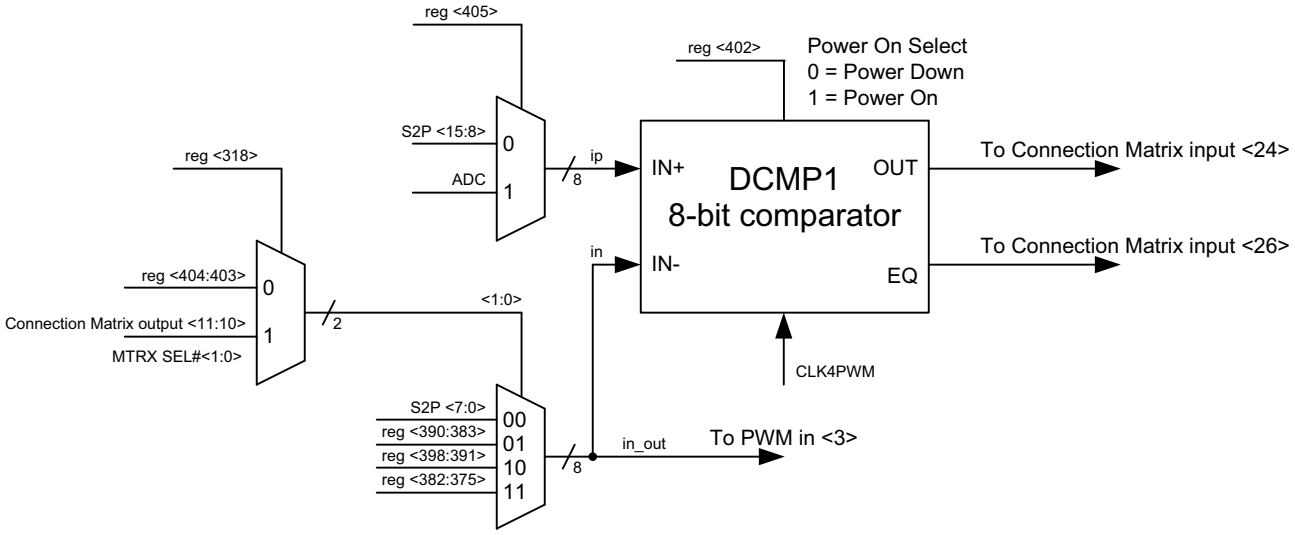


Figure 4. DCMP1 Functional Diagram

8.5 DCMP0 & DCMP1 Register Settings

Table 7. DCMP0 & DCMP1 Register Settings

Signal Function	Register Bit Address	Register Definition
DCMP IN- Selection Control	<318>	0: reg<400:399> for DCMP0, reg<404:403> for DCMP1 1: from Connection Matrix Out <11:10>
DCMP IN- Input Signal	<382:375>	00000000 to 11111111: User defined 8-bit signal input *Register0* for DCMP0 and *Register2* for DCMP1
DCMP IN- Input Signal	<390:383>	00000000 to 11111111: User defined 8-bit signal input *Register1* for DCMP0 and *Register0* for DCMP1
DCMP IN- Input Signal	<398:391>	00000000 to 11111111: User defined 8-bit signal input *Register2* for DCMP0 and *Register1* for DCMP1
DCMP0 IN- Input Selection from reg<318>	<400:399>	00: From S2P<15:8> 01: From reg<382:375> 10: From reg<390:383> 11: From reg<398:391>
DCMP0 IN+ Input Selection	<401>	0: From S2P<7:0> 1: From ADC Output
DCMP0 & DCMP1 Power Down	<402>	0: Power down mode 1: Power on mode
DCMP1 IN- Input Selection from reg<318>	<404:403>	00: From S2P<7:0> 01: From reg<390:383> 10: From reg<398:391> 11: From reg<382:375>
DCMP1 IN+ Input Selection	<405>	0: From S2P<15:8> 1: From ADC Output

9.0 Pulse Width Modulator (PWM)

The SLG46200 contains a 2-input Pulse Width Modulator with an 8-bit resolution and 7.8MHz clocking speed. The PWM has a 4:1 mux for IN1 selection, an 8-bit Comparator, a Mode Select option and a Dead Band Control function.

9.1 PWM Input Modes

IN1 for the PWM is an 8-bit data string that can be selected from one of four sources; the ADC Output, the S2P <15:8>, the Finite State Machine (through the Counter/Delay logic cells) or the source IN- of the DCMP1 logic cell. Reg <408:407> is used as a 2-bit selection input to the 4:1 mux with the previously mentioned 8-bit data strings.

IN2's 8-bit data string is sourced from the Counter/Delay logic cell in the SLG46200 device.

The 8-bit PWM has two control signals; a SET bit and a Power Down signal. Both of these signals come from the SLG46200's Connection Matrix.

- If SET = "1" then PWM IN1 = "255", otherwise PWM normal operation
- If PWR DOWN = "1" then PWM is "off", otherwise PWM is "on"

9.2 PWM Output Mode Selection

The output (OUT+) duty cycle can be set to either 0% to 99.6% or 0.39% to 100%. When both inputs are equal the output signal (EQ) will go high.

9.3 PWM Functional Diagram

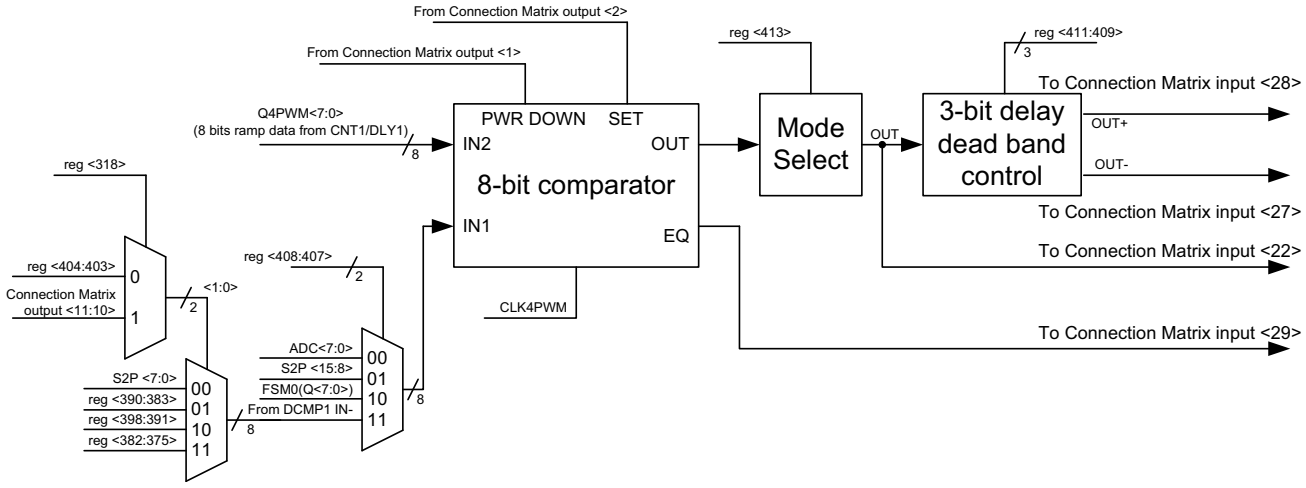


Figure 5. PWM Functional Diagram

9.4 PWM Mode Select

The PWM Mode Select (reg<413>) is used to control the output duty cycle:

When reg<413> = “0”

- PWM output duty cycle ranges from 0% to 99.61% and is determined by: Output Duty Cycle = IN1/256
- (IN1 = 0: output duty cycle = 0/255 = 0%; IN1 = 255: output duty cycle = 255/256 = 99.6%)
- Output signals are triggered by the rising edge of CLK4PWM

When reg<413> = “1”

- PWM output duty cycle ranges from 0.39% to 100% and is determined by Output Duty Cycle = (IN1+1)/256
- (IN1 = 0: output duty cycle = 1/256 = 0.39%; IN1=255: output duty cycle = 256/256 = 100%)
- Output signals are triggered by the falling edge of CLK4PWM

When IN1 = IN2 the EQ = “1”

9.5 PWM Dead Band Control

The dead band interval can be controlled with NVM bits (reg<411:409>). The typical dead band time starts at 8ns and can go to 64ns, increasing by 8ns intervals.

For the Delay dead band control, the dead time control range is;

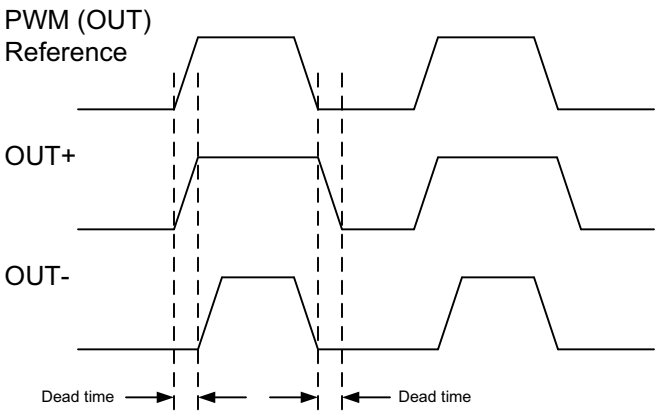
$$T_D = (dead\ time + 1) \times 8ns$$

For the Counter dead band control, the maximum clock frequency is 10MHz;

$$T_C = Clock\ period \times (dead\ time + 1)$$

The total dead band time is the sum of both the Delay and Counter dead band times:

$$T_T = T_D + T_C.$$



9.6 PWM Register Settings

Table 8. PWM Register Settings

Signal Function	Register Bit Address	Register Definition
PWM IN1 Selection Control	<408:407>	00: From ADC Output 01: From S2P <15:8> 00: From CNT2/DLY2/FSM0 <7:0> 00: From DCMP1 Negative Input. See DCMP1 section for details.
PWM Dead Band Selection	<411:409>	000: 8ns 100: 40ns 001: 16ns 101: 48ns 010: 24ns 110: 56ns 011: 32ns 111: 64ns
PWM Output Duty Cycle Control	<413>	0: 0 ~ 99.61% duty cycle 1: 0.39 ~ 100% duty cycle

10.0 Serial to Parallel / Parallel to Serial Converter (S2P)

The Serial to Parallel / Parallel to Serial Converter (S2P) transfers the data between the SLG46200 and the larger system design through either the serial to parallel or parallel to serial interface. It has two 16-bit registers (2 bytes) that are used for data transfer. The clock signal comes from PIN 4 and the nCSB (Enable Control Signal) comes from the Connection Matrix Out.

S2P uses edge detection from the CNT1/DLY1 for capturing its counter data.

10.1 S2P Functional Diagram

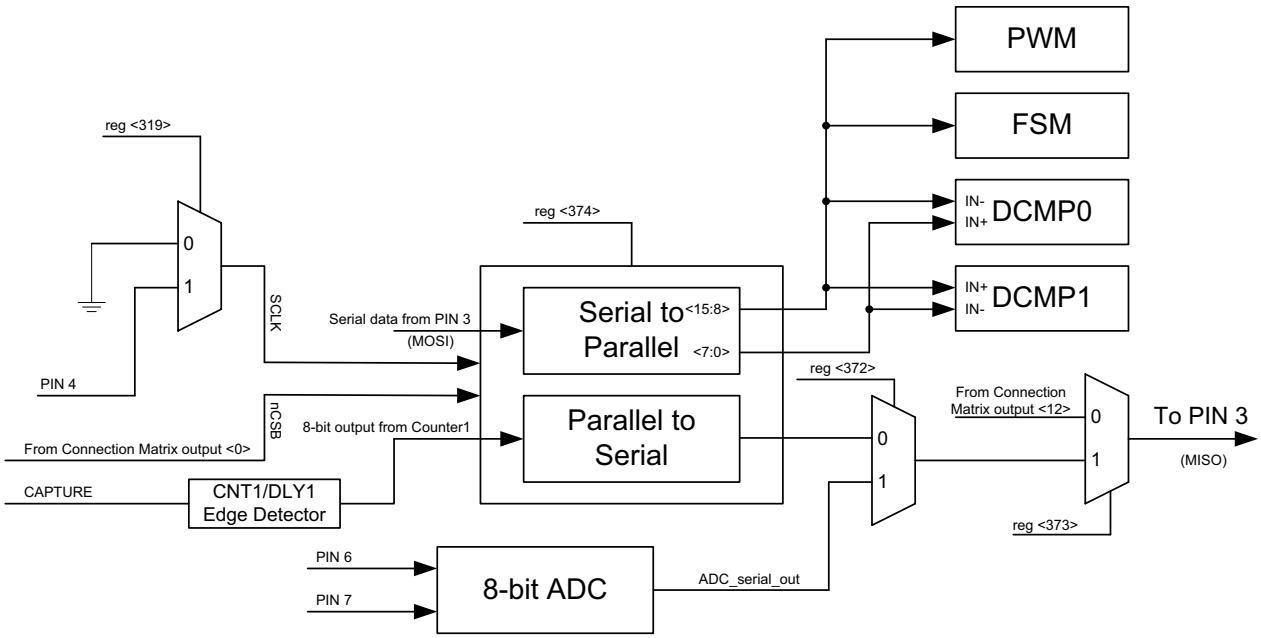


Figure 6. S2P Functional Diagram

10.2 Serial to Parallel Operation

For serial to parallel operation (S2P), the serial data in (SDI) comes from PIN 3 (MOSI) of the SLG46200. The S2P will produce a 16-bit parallel data output (PDO<15:0>) which is used by the PWM, FSM, and the two Digital Comparators (DCMP0 and DCMP1).

The MSB S2P<15:8> can be used by the PWM, FSM, DCMP0, and DCMP1 logic cells, while the LSB S2P<7:0> can be used by the DCMP0 and DCMP1 logic cells.

10.3 Serial to Parallel Timing Diagram

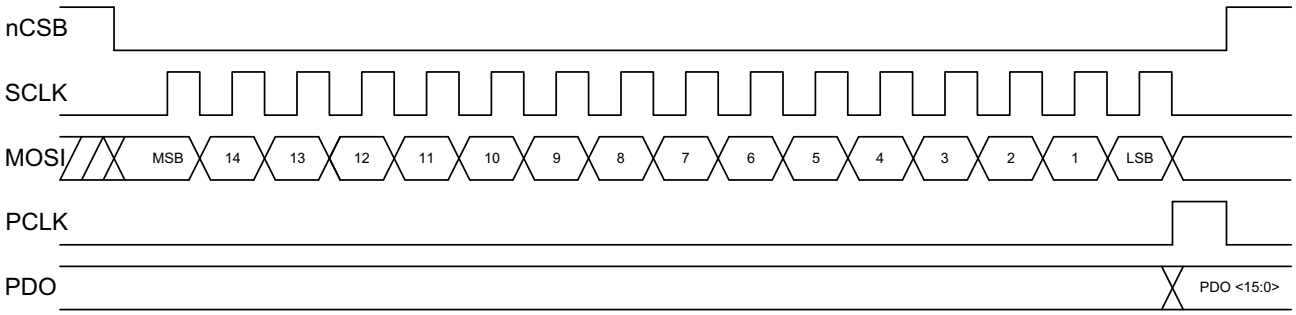


Figure 7. Serial to Parallel Timing Diagram

10.4 Parallel to Serial Operation

For parallel to serial operation (P2S), the 8-bit parallel data in (PAR IN<15:8>) comes in from either the ADC Output or the CNT1 logic cell. PIN 3 is used to output the 8-bit serial data out (MISO) signal.

10.5 Parallel to Serial Timing Diagram

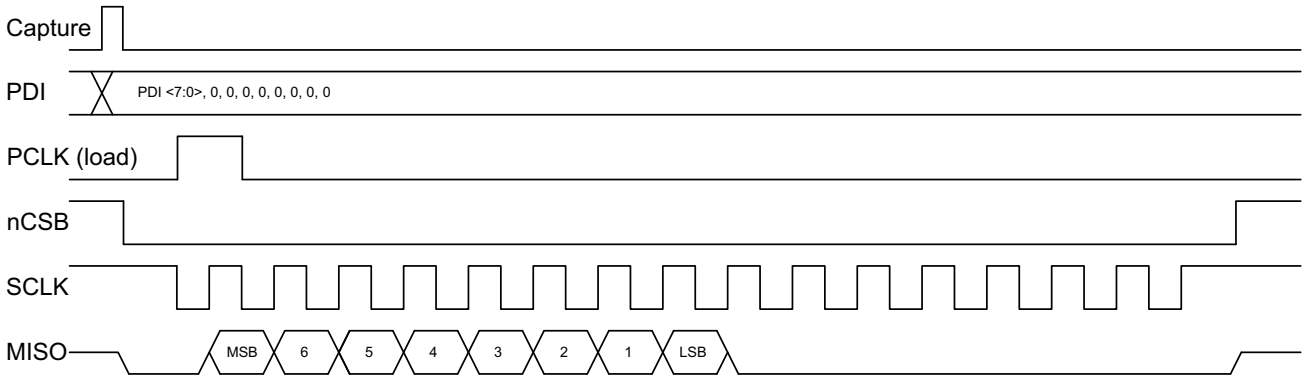


Figure 8. Parallel to Serial Timing Diagram

10.6 S2P Notes

Some functions of the S2P Converter share logic cells within the SLG46200, and as a result only one of these functions can be enabled at a time. The logic cells that are shared are:

- S2P serial in parallel out or S2P parallel in serial out
- S2P parallel in serial out or DLY2 cell

10.7 S2P Register Settings

Table 9. S2P Register Settings

Signal Function	Register Bit Address	Register Definition
S2P Clock Enable	<319>	0: Disable 1: Enable
S2P Output Source selection on PIN 3	<373:372>	10: S2P serial output data 11: ADC serial output data
S2P Mode Selection	<374>	0: Serial input (from PIN 3) / parallel output 1: Parallel input (from CNT1) / serial output

11.0 Analog to Digital Converter (ADC)

The Analog to Digital Converter in the SLG46200 is an 8-bit Successive Approximation Register Analog to Digital Converter (SAR ADC) which operates at a maximum sampling speed of 7.5kHz. User controlled inputs and outputs of the ADC are listed below:

Inputs:

- CH SELECTOR: Single-Ended Mode ADC Selection and Analog Input Mux Control Signal
- IN+: Single-Ended Mode Input and Differential Mode Positive Input
- IN-: Differential Mode Negative Input
- EXT. VREF: ADC External Voltage Reference Input
- EXT. CLK: ADC External Clock Input
- PWR DOWN: ADC Power Down Signal

Outputs:

- PGA: Output of the PGA to ACMP0
- SER DATA: ADC serial output to PIN 3
- PAR DATA: ADC parallel data to either the PWM or DCMP0.
- OUT CLK: ADC Clock Output to PIN 4

11.1 ADC Functional Diagram

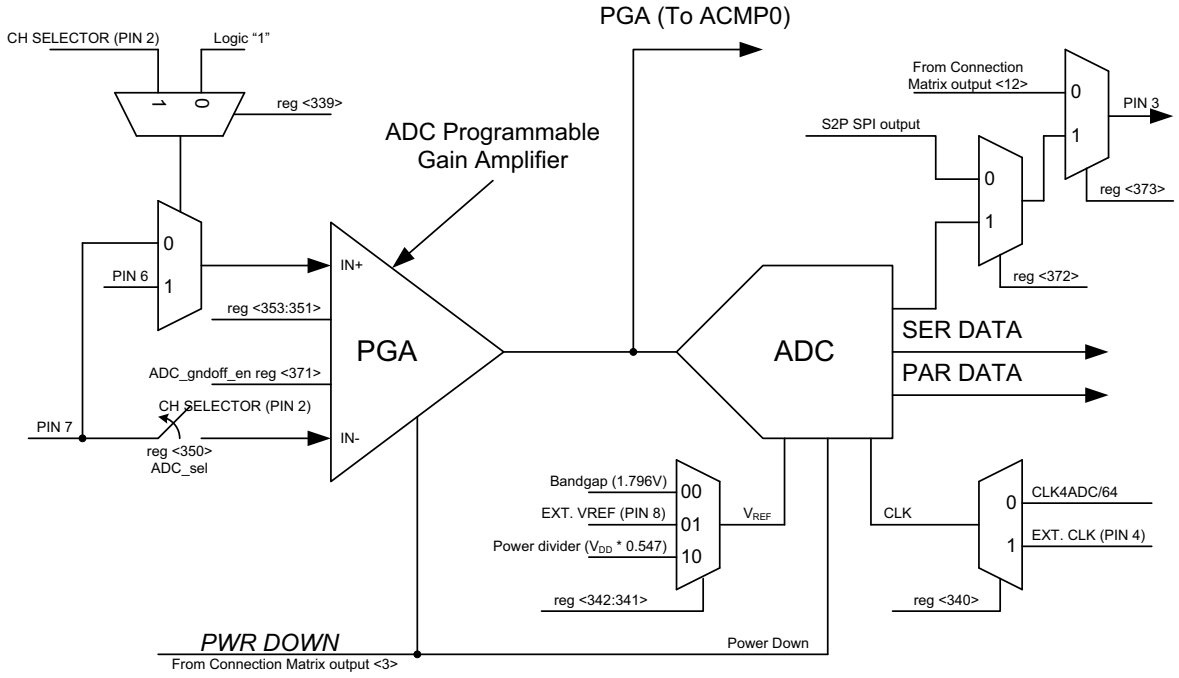


Figure 9. ADC Functional Diagram

11.2 ADC Operation Modes

The ADC has three operating modes:

- Single-Ended ADC operation using IN+ from PIN 6, when *ADC_sel* (reg <350>) is “0”
- Differential ADC operation using IN+ from PIN 6 and IN- from PIN 7, when *ADC_sel* (reg <350>) is “1”
- Pseudo-Differential ADC operation using IN+ from PIN 6 and IN- from PIN 7, when *ADC_sel* (reg <350>) and *ADC_gndoff_en* (reg <371>) bits are both set to “1”

11.3 ADC 3-bit Programmable Gain Amplifier

The front end of the ADC is a PGA with 3 bits for setting gain. The gain settings range from 0.5x to 16x. The PGA buffers the ADC in all cases except with the singled ended gain is 0.5x. Single-ended PGA operation has gain settings of 0.5, 1, 2, 4, and 8x, while Differential operation has gain settings of 1, 2, 4, 8, and 16x. The PGA gain is set by the ADC_gain_control (reg<353:351>). See ADC Register Settings Table.

For Pseudo-Differential mode, the PGA gain can only be 1x.

11.4 ADC 2-Channel Selection

When *ADC_channel_sel* (reg <339>) is set to “1”, the PGA of the ADC will sample either PIN 6 or PIN 7 on the IN+ input, where the selection is controlled by PIN 2.

- When PIN 2 is set to “0”, the ADC will sample PIN 7
- When PIN 2 is set to “1”, the ADC will sample PIN 6

When *ADC_channel_sel* (reg <339>) is set to “0”, the PGA of the ADC will sample PIN 6 on the IN+ input

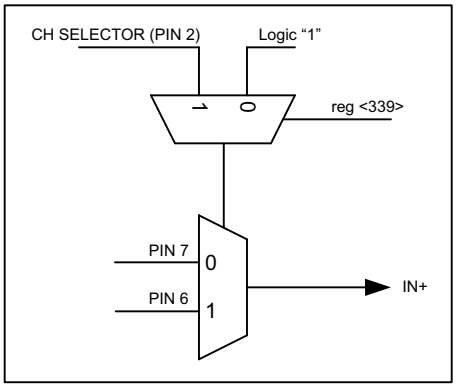


Figure 10. ADC 2-Channel Selection

11.5 ADC Input Voltage Definition

The ADC’s input voltage (V_{IN_ADC}) is calculated based on either the single-ended or differential operation modes the logic cell is set to. In single-ended mode V_{IN_ADC} is the sum of the positive input voltage and the gain of the PGA. While in differential mode the V_{IN_ADC} is the difference between the positive and negative input voltages times the gain of the PGA plus one half of the reference voltage.

$$V_{in\_adc} = \begin{cases} V_{in+} \times G_{pga\_gain} & \text{Single-ended mode} \\ (V_{in+} - V_{in-}) \times G_{pga\_gain} + V_{ref}/2 & \text{Differential mode} \end{cases}$$

Equation 1. ADC Input Voltage equation

11.6 ADC Reference Voltage

The ADC's reference voltage (V_{REF}) is from a 3-input mux that is controlled by the 2-bit *ADC_Vref_sel* signal (reg <342:341>). The three reference voltage inputs are chosen from the following:

- V_{BG} of 1.796V from Internal Source
- External User Defined Voltage Source (PIN 8)
- Power Divider of 0.547 * V_{DD}

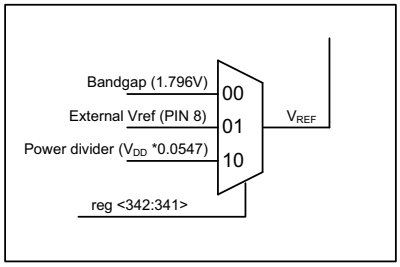


Figure 11. ADC Reference Voltage

Table 10. ADC Reference Voltage.

reg <342:341>	V_{REF}
00	Bandgap (1.796V)
01	External (PIN 8)
10	Power Divider (0.547 * V_{DD})
11	N/A

11.7 ADC Power Down Mode

The ADC's power down is controlled by the connection matrix output 3 where a value of "1" will drive the ADC and the PGA to power down mode.

11.8 ADC Clock Source

The ADC clock source comes from either the internal RC oscilator (CLK4ADC/64) or an external clock from PIN 4. The selection is made from the *ADC_clk_sel* signal via reg <340> where:

- The RC Oscillator is used when the *ADC_clk_select* is "0"
- An external clock from PIN 4 is used when the *ADC_clk_sel* is "1"

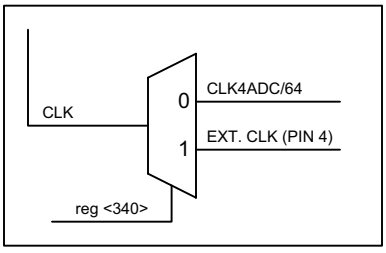


Figure 12. ADC Clock Source

The ADC requires 16 clock cycles to sample the analog voltage and output the sampled data.

When the internal RC Oscillator is used for providing timing to the ADC, a total of 1024 clock cycles are needed since the *CLK4ADC* signal is also divided by 64.

When an external clock is used on PIN5, the ADC will only need 16 clock cycles, as it bypasses the divide by 64 logic.

$$F_{ADC} = \frac{F_{OSC}}{64 \times 16 cycles} = \frac{F_{OSC}}{1024} cycles$$ ADC using Internal RC Oscillator

$$F_{ADC} = \frac{F_{ext\_clk}}{16}$$ ADC using an external clock

Equation 2. ADC Input Voltage equation

11.9 ADC Outputs

The ADC's output can be shifted out through the S2P logic cell. The *SER DATA* produces eight single data bits over eight individual clock cycles when activated. While the *PAR DATA* produces an 8-bit data string over 16 clock cycles.

11.9.1 ADC Serial Output

The 8-bit serial data can be outputted from the SLG46200 device on PIN 3. The individual 8 serial data bits can be read into an external device within the larger system design.

To initialize the *SER DATA* the ADC needs a Power Down signal, which can be configured through the connection matrix. After three ADC clock cycles the ADC will start to output the 8-Bit Serial Data. This PD signal needs to be held for at least 16 ADC clock cycles. The ADC clock is determined by either the SLG46200 clock, the RC Oscillator/64, or an external clock (from PIN 4).

11.9.2 ADC Parallel Output

The 8-bit parallel data can be outputted from the ADC logic cell to either the DCMP/PWM or FSM logic cells within the SLG46200 device.

To initialize the *PAR DATA* the ADC needs a Power Down signal, which can be configured through the connection matrix. After ten ADC clock cycles the ADC will start to output the 8-Bit Parallel Data. This PD signal needs to be held for at least 16 ADC clock cycles. The ADC clock is determined by either the SLG46400 clock, the RC Oscillator/64, or an external clock (from PIN 4).

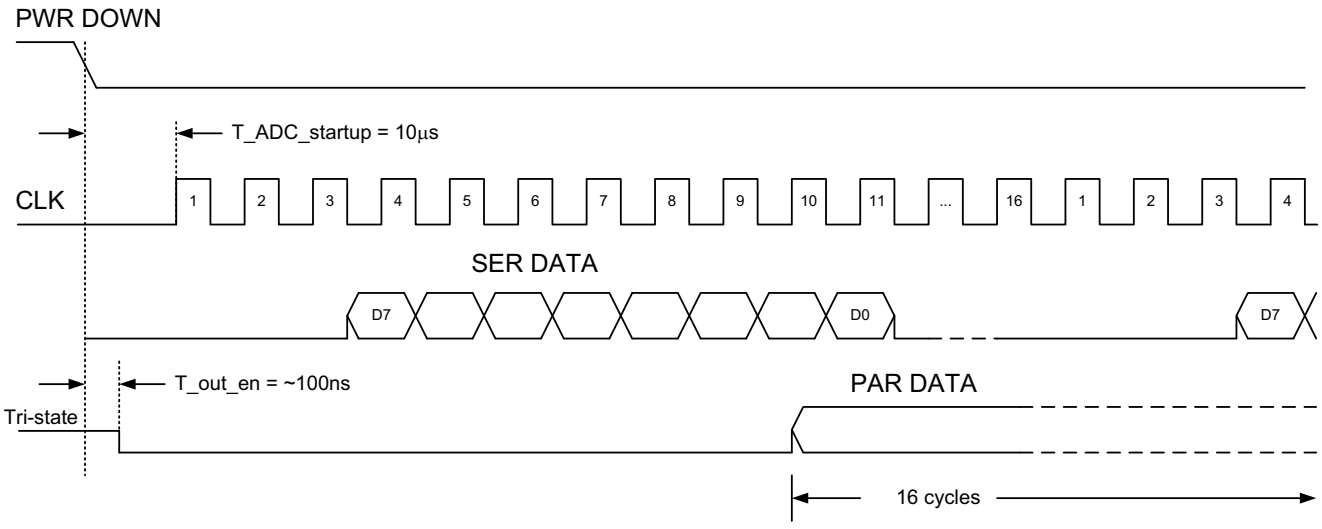


Figure 13. ADC Output Timing (power on signal comes from external signal)

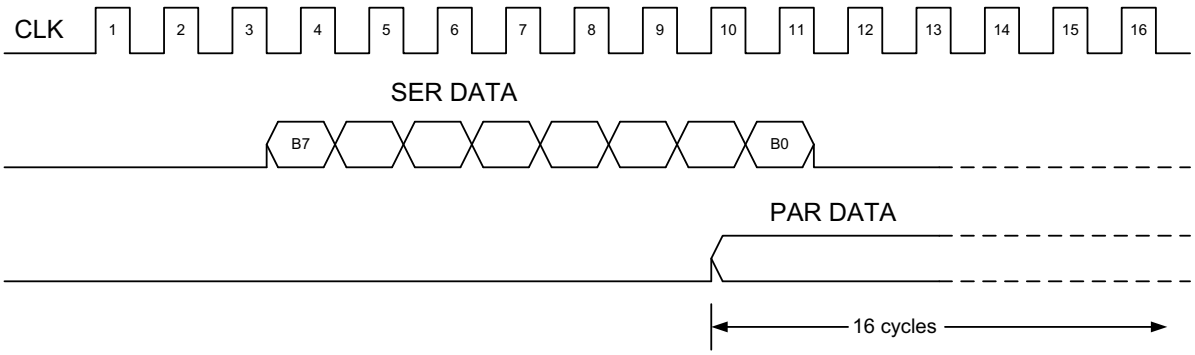


Figure 14. ADC Output Timing (power on signal comes from register)

11.10 ADC Register Settings

Table 11. ADC Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
ADC_mux_en	ADC analog input mux enable	<339>	0: No change 1: Mux enable
ADC_clk_sel	ADC clock selection	<340>	0: Internal oscillator 1: External clock from PIN 4
ADC_Vref_sel	V_{REF} setting	<342:341>	00: Bandgap (1.796V from internal source) 01: External voltage source 10: Power divider (V_{DD}* 0.547)
ADC_sel	ADC mode select	<350>	0: Single-ended operation using PIN 6 1: Differential mode operation using PIN 6 & PIN 7 Note: For Pseudo-Differential mode, reg <351:350> will be set to “11”
ADC_gain_control	ADC PGA gain control	<353:351>	000: Single-ended (0.5X gain) or differential (N/A) 001: Single-ended (1X gain) or differential (1x gain) 010: Single-ended (2X gain) or differential (2X gain) 011: Single-ended (4X gain) or differential (4X gain) 100: Single-ended (8X gain) or differential (8X gain) 101: Single-ended (N/A) or differential (16X gain)
ADC_DAC_Vref	ADC reference DAC feedback select	<362>	0: Normal 1: 0.5x gain (use this setting when V_{REF} is externally selected)
ADC_gndoff_en	ADC pseudo diff input enable under ADC diff mode	<371>	0: N/A 1: Enable
Pin3_dig_out	PIN 3 digital output source selection	<373:372>	00/01: From connection matrix output <12> 10: Serial data from the S2P 11: Serial data from the ADC

12.0 Analog Comparator (ACMP)

There are two Analog Comparator (ACMP) macro cells in the SLG46200. In order for the ACMP cells to be used in a GreenPAK design the power up signals (*PWR UP*) need to be active.

Each of the two ACMP cells have positive and negative input signals that are either created from an internal V_{REF} or provided by way of the external sources.

The two analog comparators (ACMP0 and ACMP1) must have the same power state (on or off). The Power Up input is set to high to turn on the analog comparators, and the comparators are turned off when the Power Up input is low. When the analog comparators are turned off, they both have an output that is logic high. Also note that the ACMP output is unpredictable for 100 µs after power on (except after POR).

12.1 ACMP0 Input Modes

ACMP0's positive input (IN+) can be enabled from PIN 4 or ADC/PGA out by the *ACMP0_PGA_en* signal, reg<357>. The negative input (IN-) of the ACMP0 cell can come from the internal V_{REF} macro cell (which will generate a 50mV to 1.5V signal) or from an external voltage source that is placed on PIN 8. Selection is made using a 4-bit value from NVM, reg<361:358>.

12.2 ACMP0 Functional Diagram

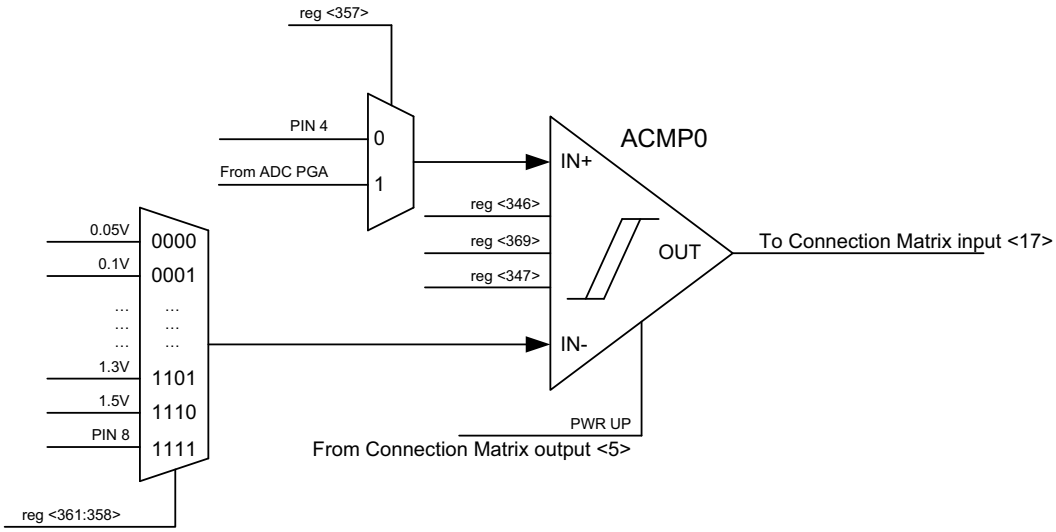


Figure 15. ACMP0 Functional Diagram

12.3 ACMP1 Input Modes

ACMP1's positive input (IN+) comes from PIN 7 with selection gain of 1X or 0.5X (two 50kΩ resistor divider). The *ACMP1_0.5gain_en* signal (reg<345>) is used as a control signal into a mux which has the 1X and 0.5X signals as inputs.

The negative input (IN-) of the ACMP1 cell can come from the internal V_{REF} macro cell (which will generate a 50mV to 1.5V signal) or from an external voltage source that is placed on PIN 8. Selection is made using a 4-bit value from NVM, reg<366:363>.

12.4 ACMP1 Functional Diagram

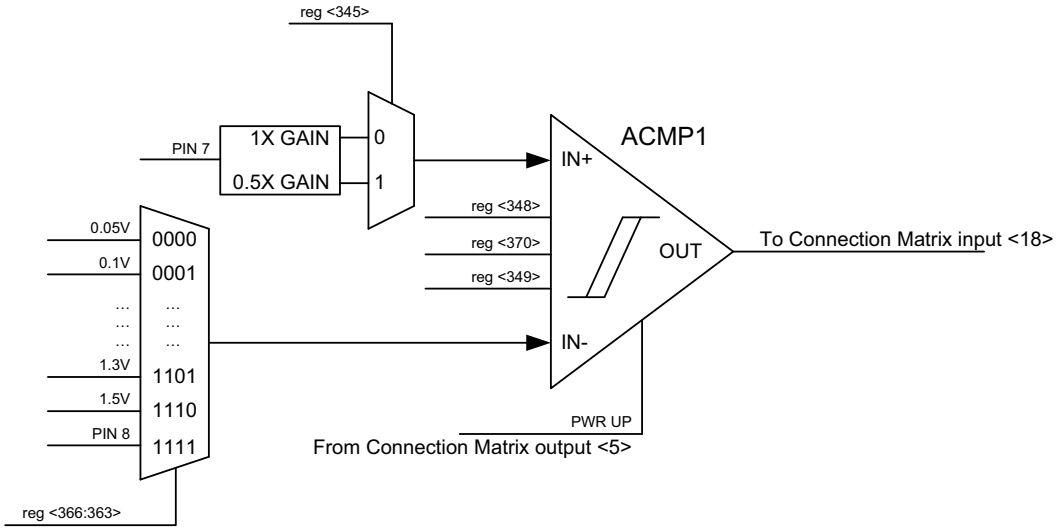


Figure 16. ACMP1 Functional Diagram

12.5 ACMP Output Modes

When IN+ has a greater voltage than IN-, the ACMP's output will be "1". Otherwise, that output will be a "0" signal. The ACMP of the SLG46200 has an offset voltage of +/- 20mV.

12.6 ACMP 1µA Input Current Option

Both ACMP's can source 1µA on their respected outputs. This feature is controlled by the following signals:

ACMP0_l1u_en, reg<346> for ACMP0

ACMP1_l1u_en, reg<348> for ACMP1

When either of these signals are equal to "1" the output will source a 1µA current.

12.7 ACMP Low Bandwidth

Both ACMP's have a low bandwidth enable feature; this is controlled by the following signals:

ACMP0_low_bw, reg<347> for ACMP0

ACMP1_low_bw, reg<349> for ACMP1

When either of these signals are equal to "1" and the input frequency is more than 200kHz, the output retains its last value

12.8 ACMP Frequency Bode Plot

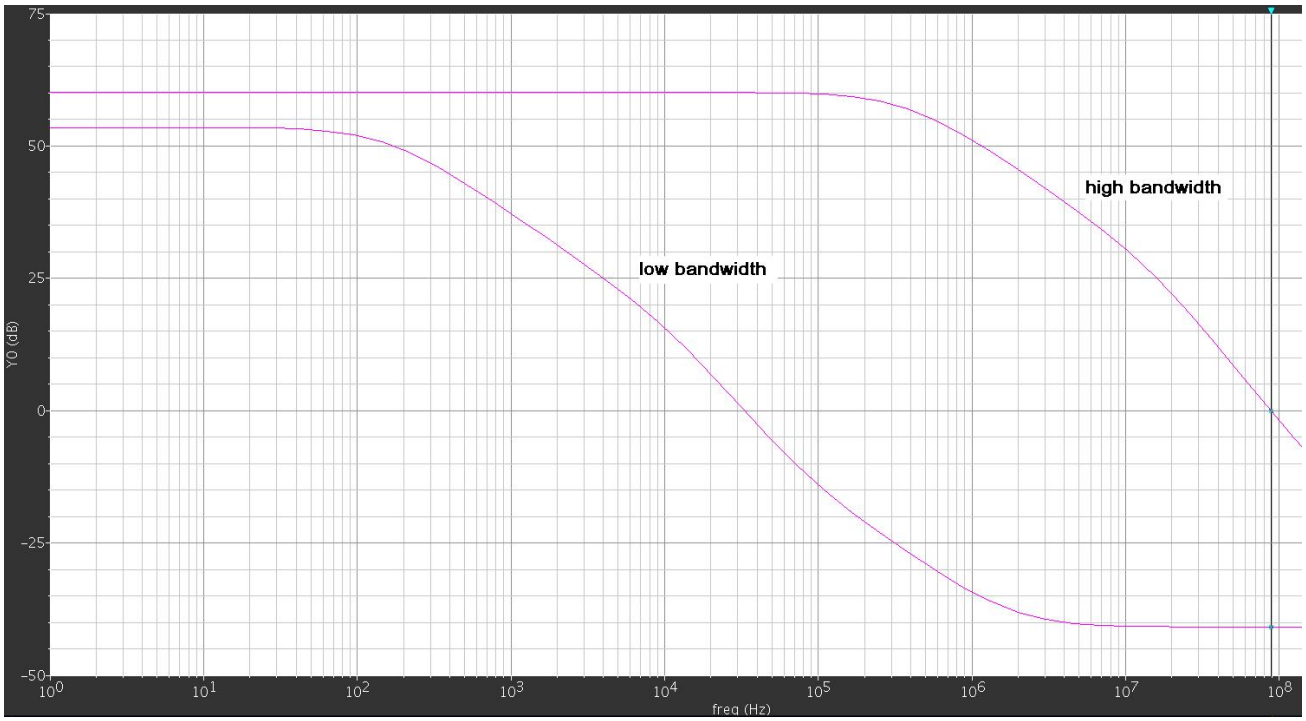


Figure 17. ACMP Bode Plot

12.9 ACMP Hysteresis

Both ACMP's have a 50mV hysteresis feature, where either the addition or subtraction of 25mV to the IN- signal will change the ACMP's output value. The 50mV hysteresis signals are controlled as follows:

ACMP0_hy_en, reg<369> when set to "1" will turn on the hysteresis,

- Output from "0" becomes "1" when IN+ ≥ IN- + 0.025V
- Output from "1" becomes "0" when IN+ ≤ IN- - 0.025V

ACMP1_hy_en, reg<370> when set to "1" will turn on the hysteresis,

- Output from "0" becomes "1" when IN+ ≥ IN- + 0.025V
- Output from "1" becomes "0" when IN+ ≤ IN- - 0.025V

12.10 ACMP0 & ACMP1 Register Settings

12.10.1 ACMP0 Register Settings

Table 12. ACMP0 Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
ACMP0_l1u_en	ACMP0 1µA input current option	<346>	0: Disable 1: Enable
ACMP0_low_bw	ACMP0 low bandwidth enable	<347>	0: Disable 1: Enable
ACMP0_PGA_en	PGA gain to ACMP0 input enable	<357>	0: Disable (IN+ input from PIN 4) 1: Enable (IN+ input from ADC PGA Out)
ACMP0_Vref_sel	ACMP0 IN- voltage select	<361:358>	0000: 50mV 0001: 100mV 0010: 150mV 0011: 200mV 0100: 250mV 0101: 300mV 0110: 400mV 0111: 500mV 1000: 600mV 1001: 700mV 1010: 800mV 1011: 900mV 1100: 1100mV 1101: 1300mV 1110: 1500mV 1111: External (PIN 8)
ACMP0_hy_en	ACMP0 50mV hysteresis enable	<369>	0: Disable 1: Enable

12.10.2 ACMP1 Register Settings

Table 13. ACMP1 Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
ACMP1_0.5gain_en	ACMP1's 0.5 gain enable	<345>	0: Disable (1X gain on PIN 7) 1: Enable (0.5X gain on PIN 7)
ACMP1_l1u_en	ACMP1 1µA input current option	<348>	0: Disable 1: Enable
ACMP1_low_bw	ACMP1 low bandwidth enable	<349>	0: Disable 1: Enable
ACMP1_Vref_sel	ACMP1 IN- voltage select	<366:363>	0000: 50mV 0001: 100mV 0010: 150mV 0011: 200mV 0100: 250mV 0101: 300mV 0110: 400mV 0111: 500mV 1000: 600mV 1001: 700mV 1010: 800mV 1011: 900mV 1100: 1100mV 1101: 1300mV 1110: 1500mV 1111: External (PIN 8)
ACMP1_hy_en	ACMP1 50mV hysteresis enable	<370>	0: Disable 1: Enable

13.0 Voltage Reference Out (V_{REF} Out)

The V_{REF} macro cell supplies an accurate reference voltage for the SLG46200.

13.1 V_{REF} Output

The output of the V_{REF} cell can be connected to PIN 8 as a buffered or non-buffered output. In order to use the V_{REF} cell within the SLG46200, the V_{REF} output enable signal (reg<343>) must be turned on.

When the op amp output buffer is enabled through the *Vrefo_buf_en* signal (reg<367>) the PIN 8 output voltage reference's impedance becomes 1kΩ. With the op amp buffer switched out, the PIN8 output voltage reference's impedance is 100kΩ.

13.2 V_{REF} Sources

The value of V_{REF} can be set to either use $V_{DD}/2$ as a voltage source or by setting the ACMP0 to provide the desired voltage (50mV to 1.5V is selectable). The V_{REF} macro cell uses ACMP0's negative input for the desired reference voltage.

13.3 V_{REF} Functional Diagram

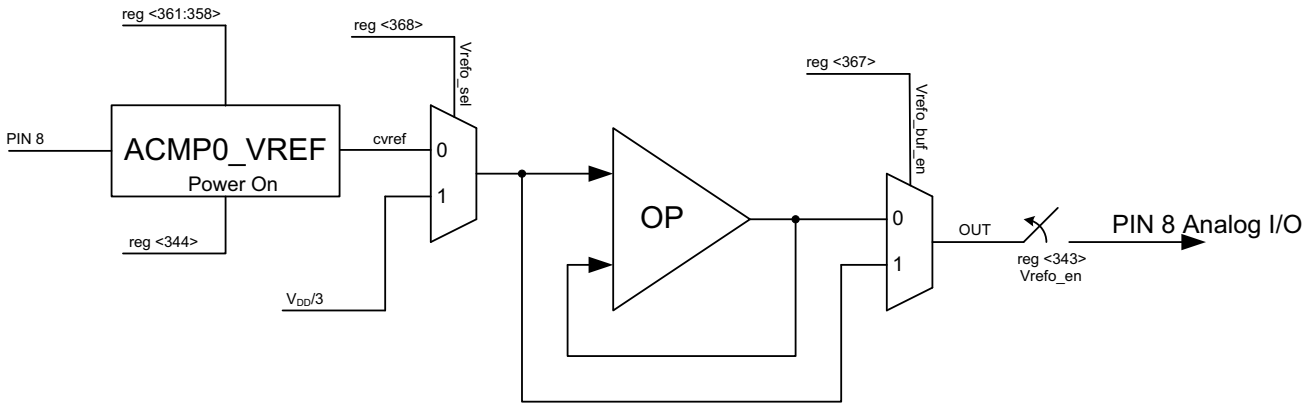


Figure 18. V_{REF} Functional Diagram

13.4 V_{REF} Register Settings

Table 14. V_{REF} Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
Vrefo_en	V_{REF} Output Enable	<343>	0: Disable V_{REF} output 1: Enable V_{REF} output
Vref_on	V_{REF} Power On	<344>	0: ACMP0_Vref off 1: Force V_{REF} output with ACMP0_Vref power on
Vrefo_buf_en	V_{REF} Output Buffer Enable	<367>	0: V_{REF} output through buffer 1: V_{REF}output not through buffer
Vrefo_sel	V_{REF} Output select	<368>	0: ACMP0 IN- reference voltage 1: V_{DD}/2

Refer to reg <361:358> for possible V_{REF}configurations.

14.0 Power On Reset (POR)

The Power On Reset (POR) macro cell will produce a “1” signal as an output when the power supply (V_{DD}) rises to 2.5V or greater. This signal (POR4NVM) requires approximately 3ms of delay before it will go from low to high.

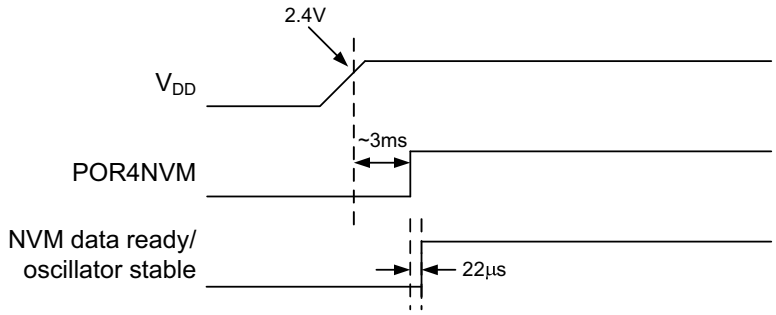


Figure 19. Power on Reset Timing Diagram

When NVM data is ready, the oscillator must be stable at the same time. If the oscillator power on is controlled by auto power on signals such as delay cells, ADC, or PWM, the oscillator will need a maximum of 5µs to become stable.

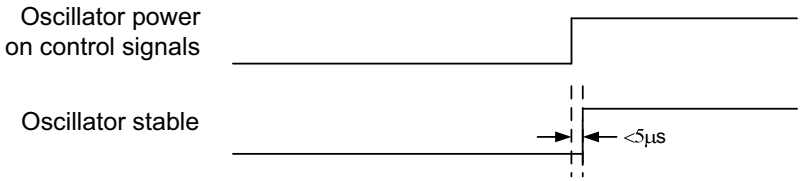


Figure 20. Stable Oscillator wait time

15.0 RC Oscillator (RC OSC)

The RC Oscillator (RC OSC) of the SLG46200 provides an internal clock to the ADC, PWM, DLYs and Counters. It has a frequency range of 43kHz – 7.8MHz which can be adjusted by setting V_{REF} and I_{BIAS}.

15.1 RC Oscillator Functional Diagram

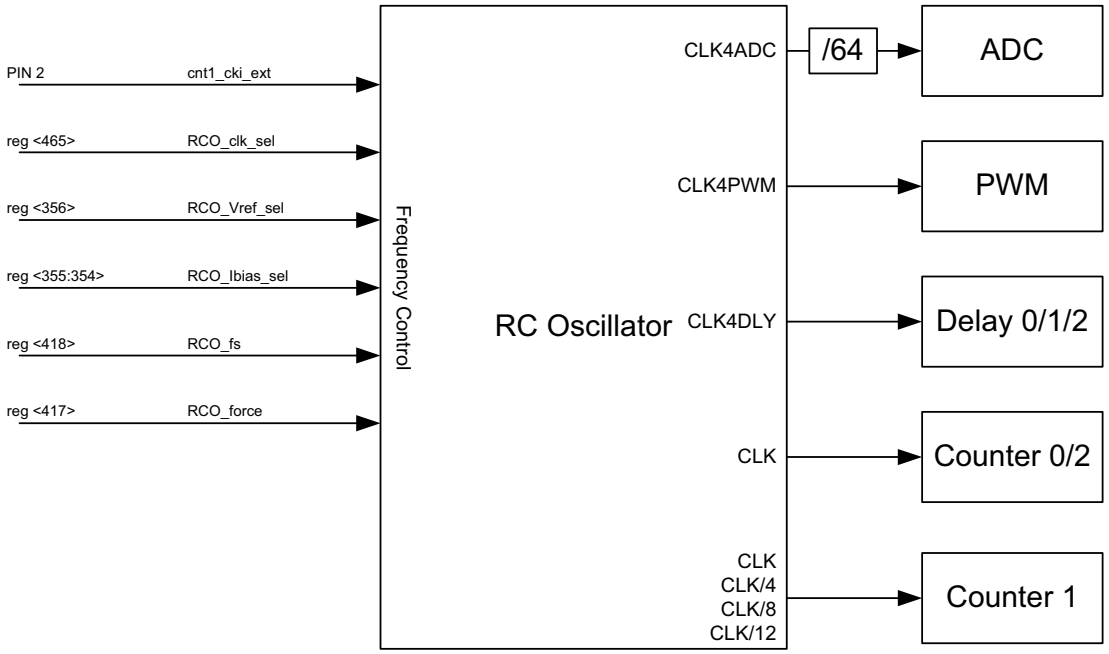


Figure 21. RC Oscillator Functional Diagram

15.2 RCO Frequency Control

The RCO produces an output timing signal that has a pulse width of 5 or 10ns depending on the clock frequency.

If Clock Frequency > 1MHz, then the pulse width is set to 5ns

If Clock Frequency < 1MHz, then the pulse width is set to 10ns

The frequency is set based on the *RCO_Vref_sel*, *RCO_Ibias_sel* and the *RCO_fs* signals. The following table shows the various output frequencies of the four registers.

15.3 RC OSC Frequency Selection

Table 15. RC OSC Frequency Selection

RCO_Vref_sel	RCO_Ibias_sel		RCO_fs	Frequency (kHz)
reg <356>	reg <355>	reg <354>	reg <418>	
0	0	0	0	43
0	0	0	1	384
0	0	1	0	85
0	0	1	1	625
0	1	0	0	160
0	1	0	1	950
0	1	1	0	800
0	1	1	1	4800
1	0	0	0	128
1	0	0	1	870
1	0	1	0	240
1	0	1	1	1290
1	1	0	0	440
1	1	0	1	1750
1	1	1	0	2100
1	1	1	1	7812

15.4 RC OSC Register Settings

Table 16. RC OSC Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
RCO_Ibias_sel	Internal OSC Current Select	<355:354>	00: 0.5µA 01: 1.0µA 10: 2.0µA 11: 10.0µA
RCO_Vref_sel	Internal OSC V_{REF} Select	<356>	0: 1.5V 1: 0.5V
RCO_force	Force Oscillator Power On	<417>	0: Auto Power On from Delay Cell 1: Force Power On
RCO_fs	Oscillator Frequency Band Select	<418>	0: Low frequency 1: High frequency
RCO_clk_sel	Clock Source Select	<465>	0: Internal OSC 1: External clock

16.0 Counters (CNT)

There are three configurable 14-bit counters in the SLG46200. CNT2's input can be sourced from the NVM, the ADC, or the S2P, while CNT0 and CNT1's input can be sourced from the connection matrix. The clock can be sourced from either the internal RC Oscillator (with data divider for CNT1) or from another connection matrix output.

The counters output their data to either the PWM or to the S2P. FSM functions include: count UP, count DOWN, KEEP, LOAD ONCE, and LOAD DATA (taken from either registers, ADC, or S2P). The three counters can also function as frequency dividers, FSM (CNT2), or PWM ramp (CNT1), while captured data is outputted to S2P.

When in count DOWN mode, the count UP/DOWN, KEEP, and LOAD signals in CNT0 and CNT1 are tied to ground and the RC OSC should be forced ON for counter work.

16.1 Counter Functional Diagram

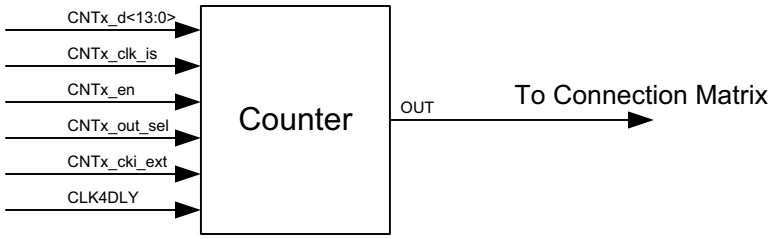


Figure 22. Counter Functional Diagram

16.2 Counter Timing

Each of the counters behave as a frequency divider, where the output clock (Div_clk_out) is result of the input clock (CLK_IN) being divided by the value of the Counter Control Data (CNTx_d<13:0> +1).

For CNT0:

$$div\_clk\_out0 = F_{CLK\_IN} / (reg<432:419> + 1)$$

For CNT1:

$$div\_clk\_out1 = F_{CLK\_IN} / (reg<446:433> + 1)$$

For CNT2:

$$div\_clk\_out2 = F_{CLK\_IN} / (reg<460:447> + 1)$$

Note: For proper functionality of each Counter cell, each respective CNTx_d<13:0> must have a value of greater than '1'.

An example waveform is shown below where the output clock goes high for only one of the input clock's cycles over a time period that is equal to the Counter Control Data (CNTx_d<13:0> +1).

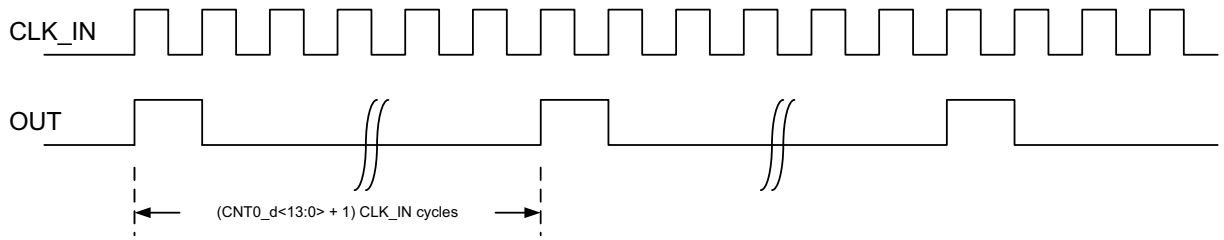


Figure 23. Counter Behavior

16.3 CNT2 as a Finite State Machine (FSM)

CNT2 can be used as a Finite State Machine, which has features for UP/DOWN/KEEP control and loading data (LOAD) select.

- When UP/DOWN = 1: CNT2 is in up-counting mode, the Q value will count from 0 to 16383. When Q reaches 16383, the Div_clk_out2 generates a single clock cycle pulse.
- When UP/DOWN = 0: CNT2 is in down-counting mode, the Q value will count from the loaded data value (based on reg<460:447> + 1) to 0. When Q reaches 0, the Div_clk_out2 generates a single clock cycle pulse.
- When KEEP = 1: Q will stay at its current value.
- The Loading Data (LOAD) is only used for down-counting mode. When the Div_clk_out2 is high, the data is then loaded in the counter.

16.4 FSM (CNT2) Functional Diagram

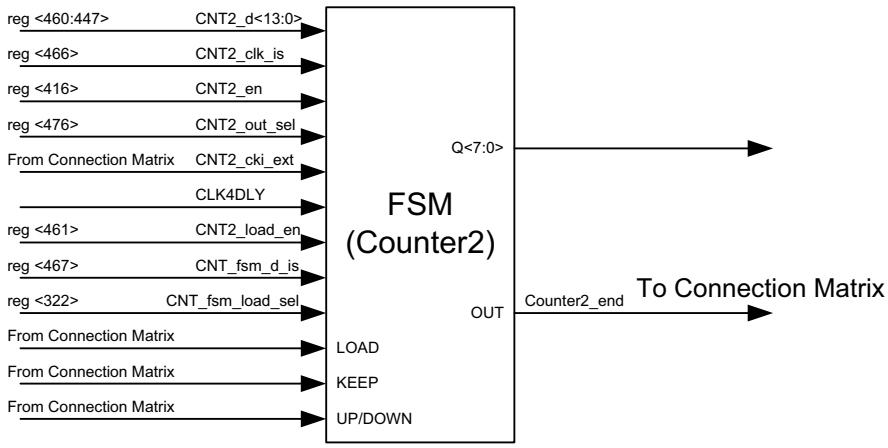


Figure 24. FSM (CNT2) Functional Diagram

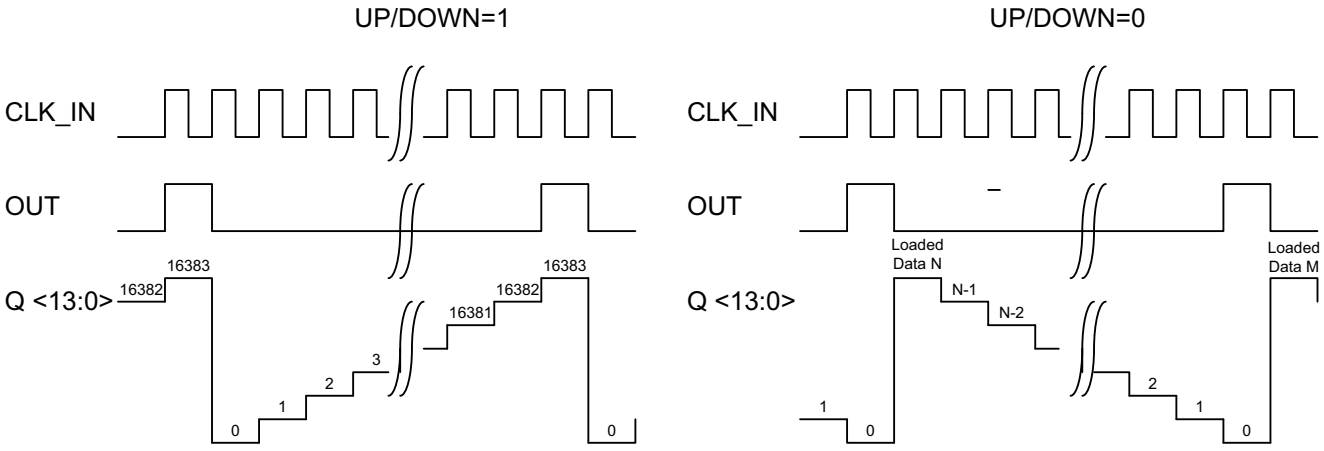


Figure 25. FSM Behavior

16.5 Counter Register Settings

Table 17. Counter Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
CNT_fsm_load_sel	CNT2 14-bit input data selection for FSM	<322>	0: From NVM reg<460:447> 1: 6 most significant bits are tied to “0” and the 8 less significant bits are sourced from S2P or ADC (controlled by reg<467>)
CNT0_en	CNT0 Enable (Force CNT0 power on)	<414>	0: Auto power on 1: Force power on
CNT1_en	CNT1 Enable (Force CNT1 power on)	<415>	0: Auto Power On 1: Force power on
CNT2_en	CNT2 Enable (Force CNT2 power on)	<416>	0: Auto power on 1: Force power on
CNT0_d<13:0>	CNT0 Control Data	<432:419>	1-16384: (delay time = (counter control data + 1) / freq)
CNT1_d<13:0>	CNT1 Control Data	<446:433>	1-16384: (delay time = (counter control data + 1) / freq)
CNT2_d<13:0>	CNT2 Control Data	<460:447>	1-16384: (delay time = (counter control data + 1) / freq)
CNT2_load_en	CNT2 Load Signal	<461>	0: Off 1: Enable
CNT0_clk_is	CNT0 Input Clock Source Select	<462>	0: From internal oscillator clock 1: From matrix
CNT1_clk_is	CNT1 Input Clock Source Select	<465:463>	000: Internal oscillator clock 001: Internal oscillator clock divided by 12 010: Internal oscillator clock divided by 4 011: CNT2 over flow signal 1X0: From matrix 1X1: From matrix divided by 8 and synchronized by internal clock
CNT2_clk_is	CNT2 Input Clock Source Select	<466>	0: Internal oscillator clock 1: From CNT0 output
CNT_fsm_d_is	Data Source Select for FSM (CNT2)	<467>	0: From external source (though S2P module) 1: From internal ADC output
CNT0_out_sel	CNT0 Output Select	<474>	0: Delay output 1: Counter output
CNT1_out_sel	CNT1 Output Select	<475>	0: Delay output 1: Counter output
CNT2_out_sel	CNT2 Output Select	<476>	0: Delay output 1: Counter output

17.0 Delay Cells (DLY)

There are three Delay Cells in the SLG46200. The time delay cells can be cascaded with one another to achieve longer time delays. Each delay cell can be triggered from a rising edge transition, a falling edge transition, or a transition in either direction.

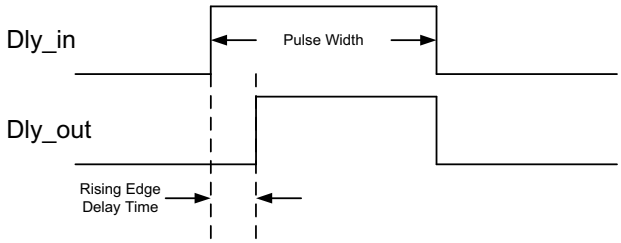


Figure 26. Delay Cells - Rising Edge

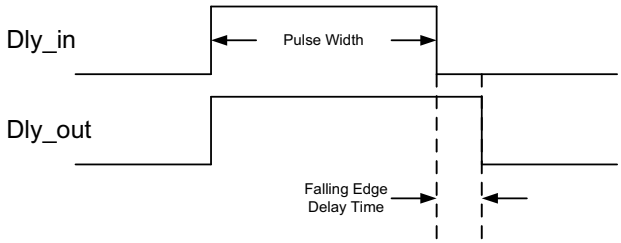


Figure 27. Delay Cells - Falling Edge

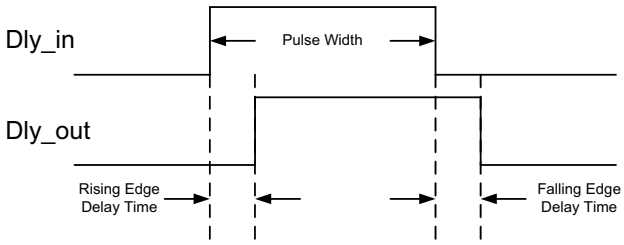


Figure 28. Delay Cells - Rising and Falling Edge

The clock frequency and counter data are used to set the output delay to a value between 0.5µs to 380ms (4.5s for DLY1). Each time delay cell's input and output can be sourced from any user defined signal in the SLG46200.

DLY1 is shared with the PWM while DLY2 is shared with S2P in parallel to serial mode.

17.1 Delay Cells Functional Diagram

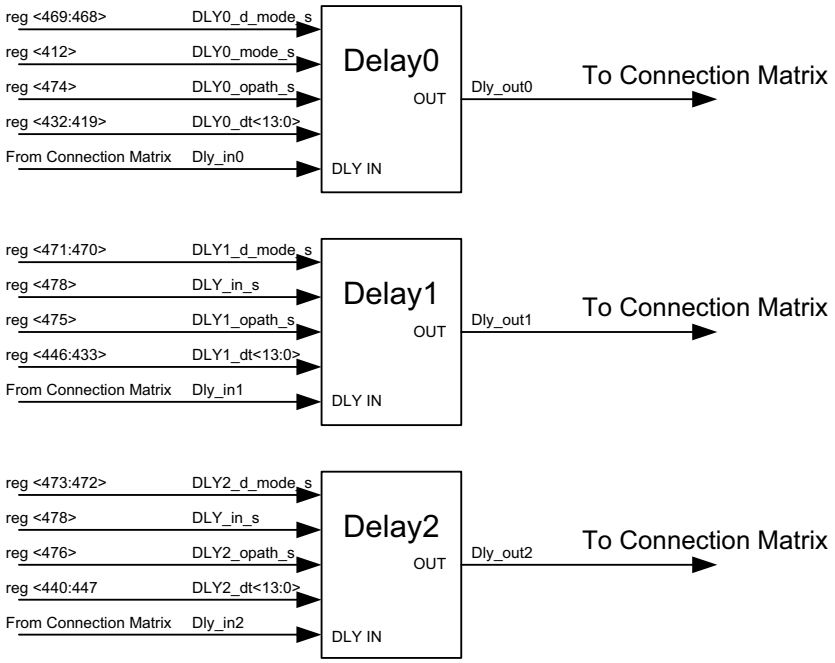


Figure 29. Delay Cells Functional Diagram

17.2 Delay Timing

The delay timing of each logic cell is determined by the frequency of the RC Oscillator and the Delay Time Control registers which use Counter data values: reg<432:419> (CNT0 data) for DLY0 , reg<446:433> (CNT1 data) for DLY1, reg<460:447> (CNT2 data) for DLY2. The formulas below list the timing delay equations for each logic cell;

For DLY0:

$$T_{DLY0} = (1/F_{OSC}) * (reg<432:419> + 1)$$

For DLY1:

$$T_{DLY1} = (1/F_{OSC}) * (reg<446:433> + 1)$$

For DLY2:

$$T_{DLY2} = (1/F_{OSC}) * (reg<460:447> + 1)$$

Note: In order for these equations above to be valid the pulse width must be larger than the total rising and falling edge delay times. Also, for proper functionality of each Delay cell, each respective CNTx_d<13:0> must have a value of greater than '1'.

17.3 Delay Cells Register Settings

Table 18. Delay Cells Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
DLY0_dt<13:0>	DLY0 - Delay Time Control	<432:419>	1 - 16384: (delay time = (counter data + 1)/freq)
DLY1_dt<13:0>	DLY1 - Delay Time Control	<446:433>	1 - 16384: (delay time = (counter data + 1)/freq)
DLY2_dt<13:0>	DLY2 - Delay Time Control	<460:447>	1 - 16384: (delay time = (counter data + 1)/freq)
DLY0_d_mode_s	DLY0 Mode Select	<469:468>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
DLY1_d_mode_s	DLY1 Mode Select	<471:470>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
DLY2_d_mode_s	DLY2 Mode Select	<473:472>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
DLY0_opath_s	DLY0 Output Path Select	<474>	0: DLY0 output 1: CNT0 output
DLY1_opath_s	DLY1 Output Path Select	<475>	0: DLY1 output 1: CNT1 output
DLY2_opath_s	DLY2 Output Path Select	<476>	0: DLY2 output 1: CNT2 output
DLY_in_s	DLY1 and DLY2 Input Source Enable	<478>	0: Disable DLY1 and DLY2 inputs 1: Enable DLY1 and DLY2 inputs from connection matrix

18.0 Combinatorial Logic

Combinatorial logic is supported via seven Lookup Tables (LUTs) within the SLG46200. There are two 2-bit LUTs, four 3-bit LUTs and one 4-bit LUT.

Inputs/Outputs for the seven LUTs are configured from the connection matrix with specific logic functions being defined by the state of NVM bits. The outputs of the seven LUTs can be configured to user defined functions or the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

18.1 2-Bit LUT

The two 2-bit LUTs within the SLG46200 each take in two input signals from the connection matrix and produce a single output.

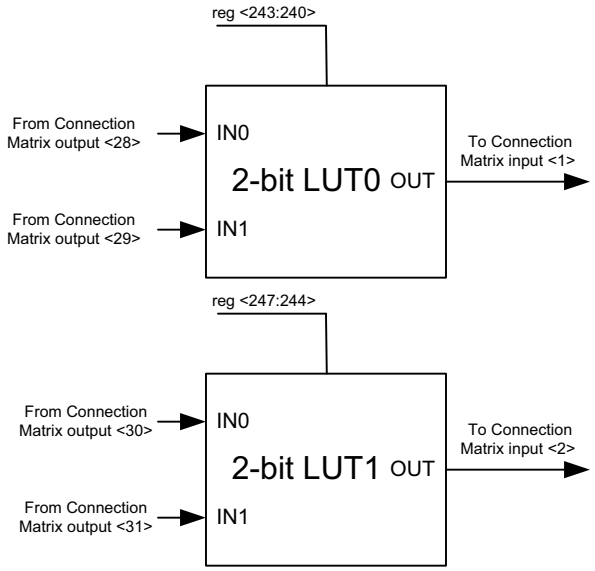


Figure 30. 2-bit LUTs

Table 19. 2-bit LUT0 Truth Table.

IN1	IN0	OUT
0	0	reg <240>
0	1	reg <241>
1	0	reg <242>
1	1	reg <243>

Table 20. 2-bit LUT1 Truth Table.

IN1	IN0	OUT
0	0	reg <244>
0	1	reg <245>
1	0	reg <246>
1	1	reg <247>

Each 2-bit LUT uses a 4-bit register signal to define their output functions;

2-Bit LUT0 is defined by reg<243:240>

2-Bit LUT1 is defined by reg<244:244>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 2-bit LUT logic cells.

Table 21. 2-bit LUT0/LUT1 Standard Digital Functions.

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

18.2 3-Bit LUT

The four 3-bit LUTs within the SLG46200 each take in three input signals from the connection matrix and produce a single output.

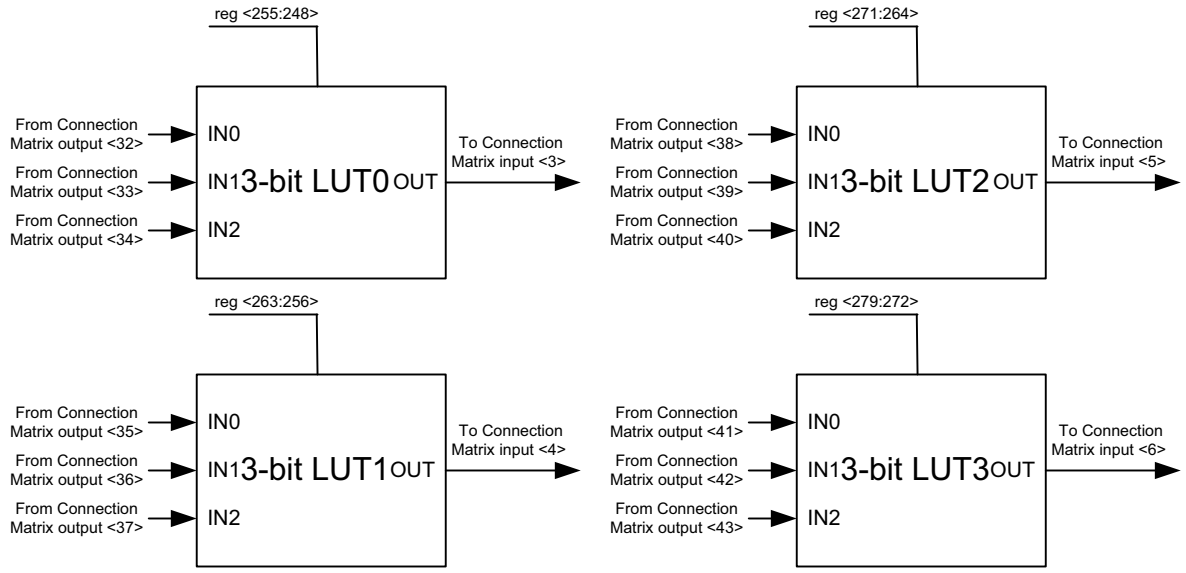


Figure 31. 3-bit LUTs

Table 22. 3-bit LUT0 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <248>
0	0	1	reg <249>
0	1	0	reg <250>
0	1	1	reg <251>
1	0	0	reg <252>
1	0	1	reg <253>
1	1	0	reg <254>
1	1	1	reg <255>

Table 23. 3-bit LUT1 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <256>
0	0	1	reg <257>
0	1	0	reg <258>
0	1	1	reg <259>
1	0	0	reg <260>
1	0	1	reg <261>
1	1	0	reg <262>
1	1	1	reg <263>

Table 24. 3-bit LUT2 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <264>
0	0	1	reg <265>
0	1	0	reg <266>
0	1	1	reg <267>
1	0	0	reg <268>
1	0	1	reg <269>
1	1	0	reg <270>
1	1	1	reg <271>

Table 25. 3-bit LUT3 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <272>
0	0	1	reg <273>
0	1	0	reg <274>
0	1	1	reg <275>
1	0	0	reg <276>
1	0	1	reg <277>
1	1	0	reg <278>
1	1	1	reg <279>

Each 3-bit LUT uses an 8-bit register signal to define their output functions;

3-Bit LUT0 is defined by reg<255:248>

3-Bit LUT1 is defined by reg<263:256>

3-Bit LUT2 is defined by reg<271:264>

3-Bit LUT3 is defined by reg<279:272>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 26. 3-bit LUT0/LUT1/LUT2/LUT3 Standard Digital Functions.

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

18.3 4-Bit LUT

The one 4-bit LUT within the SLG46200 has takes in four input signals from the connection matrix and produces a single output.

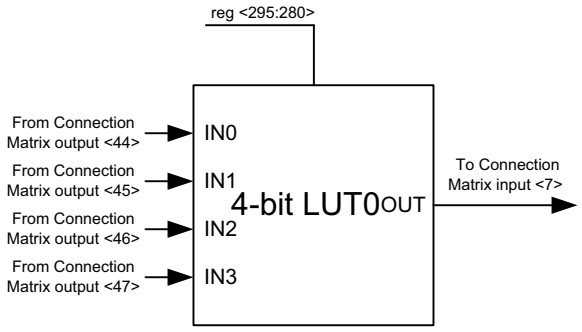


Figure 32. 4-bit LUT

Table 27. 4-bit LUT0 Truth Table.

IN3	IN2	IN1	IN0	OUT
0	0	0	0	reg <280>
0	0	0	1	reg <281>
0	0	1	0	reg <282>
0	0	1	1	reg <283>
0	1	0	0	reg <284>
0	1	0	1	reg <285>
0	1	1	0	reg <286>
0	1	1	1	reg <287>
1	0	0	0	reg <288>
1	0	0	1	reg <289>
1	0	1	0	reg <290>
1	0	1	1	reg <291>
1	1	0	0	reg <292>
1	1	0	1	reg <293>
1	1	1	0	reg <294>
1	1	1	1	reg <295>

The 4-bit LUT uses a 16-bit register signal to define the output function;

4-Bit LUT0 is defined by reg<295:280>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within the 4-bit LUT logic cell.

Table 28. 4-bit LUT0 Standard Digital Functions.

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

19.0 Digital Storage Elements (DFFs/LATCHes)

There are three DFF/LATCHes logic cells within the SLG46200 available for design. The source and destination of the inputs and outputs for the three DFF/LATCHes are configured from the connection matrix.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

DFF: CK is rising edge triggered, then Q = D; otherwise Q will not change

Latch: if CK = 0, then Q = D

if CK = 1, then Q will not change

19.1 DFF/LATCH Functional Diagram

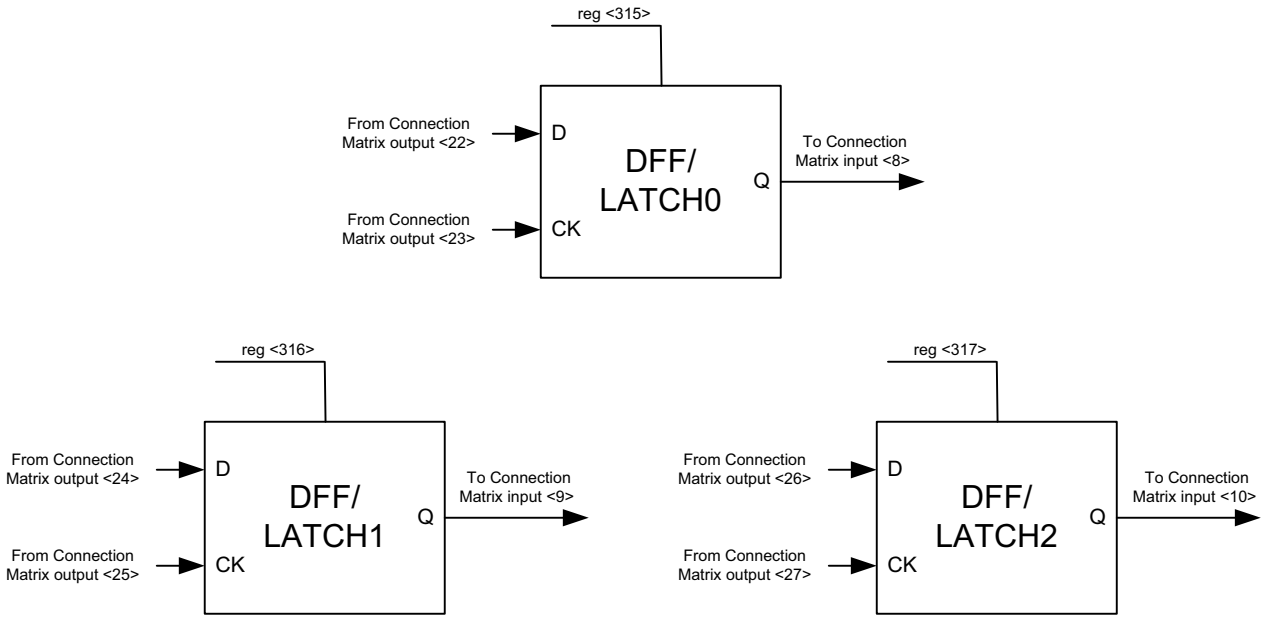


Figure 33. DFF/LATCH Functional Diagram

19.2 DFF/LATCH Selection

Each of the three DFF/LATCH logic cells has a selection bit that is used to define if the logic cell will be used as a D Flip-Flop or a Latch within the design. Those control bits are shown in the table below.

19.3 DFF/LATCH Register Settings

Table 29. DFF/LATCH Register Settings

Signal Function	Register Bit Address	Register Definition
DFF/LATCH0 Selection	<315>	0: DFF 1: LATCH
DFF/LATCH1 Selection	<316>	0: DFF 1: LATCH
DFF/LATCH2 Selection	<317>	0: DFF 1: LATCH

20.0 Application Examples

20.1 System Reset

In the following application example, a system reset pulse can be generated from a command signal (from a microprocessor) or an external reset push button. The current reset state can be shown by adding a LED into the design. Implementing this function within the SLG46200 requires the use of an input buffer, an open drain LED output driver, a de-glitch filter, and a one-shot circuit. In this example the SLG46200 replaces up to four off-the-shelf components.

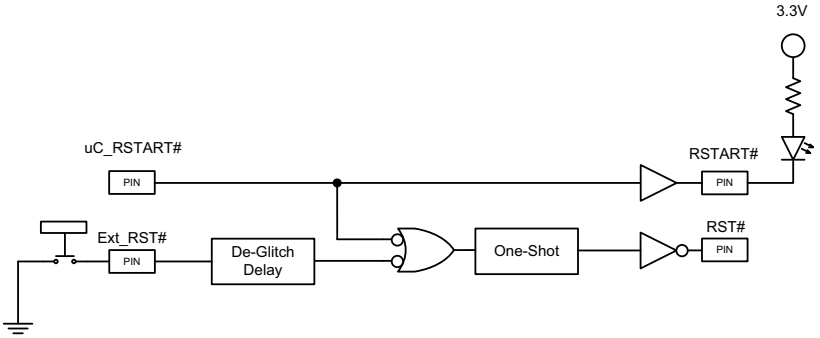


Figure 34. Example: System Reset

20.2 Combinatorial Logic

In this application example one SLG46200 is used to replace three discrete ‘1G’ SOT23-5 packaged logic components. The SLG46200’s 2mm X 2mm TDFN packaging of this function will result in significant space savings due to fewer components used in the final PCB design.

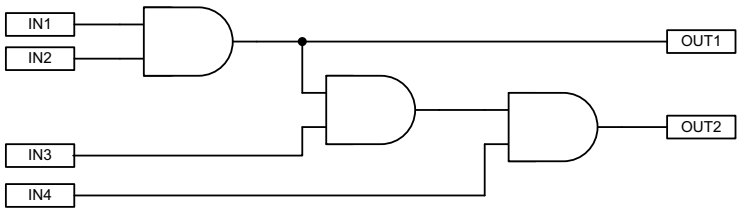


Figure 35. Example: Combinatorial Logic

20.3 Bi-Directional Pin Example

The example figure below shows how a Bi-Directional Pin can be set up in the GreenPAK 1 Designer tool by using an external signal for the Output Enable control signal.

The input to PIN 2 is controlled from an external signal, which is then used to control the Output Enable on PIN 3.

- When the signal on PIN 2 = “0”, then PIN 3 will act as a Digital Input. In this example, the signal from PIN3 is going to the logic cell (LUT2.1 in this case).

- When the signal on PIN 2 = “1”, then PIN 3 will act as a Push Pull Output with 1x current drive. In this example, a signal from CNT1/DLY1 will be sent from the SLG46200 to the external board.

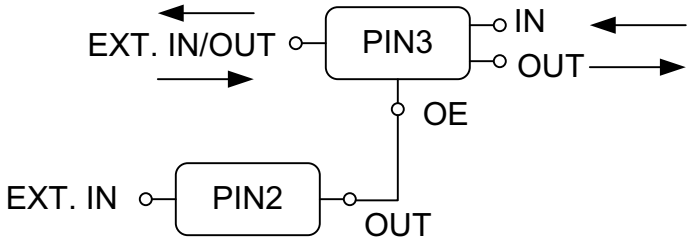


Figure 36. PIN 3 as a Bi-Directional Pin with PIN 2 as the OE Control

21.0 Development Tools

21.1 Software & Hardware

21.1.1 GreenPAK 1 Designer™

At the core of the GreenPAK development software suite is GreenPAK 1 Designer, graphical schematic design tool used to create circuit designs for the GreenPAK IC. GreenPAK 1 Designer requires no programming language or compiler.

GreenPAK designer software is available free of charge at http://www.silego.com/.

21.1.2 GreenPAK Programmer

GreenPAK Programmer is flexible enough and is used on the bench in development and also suitable for factory programming. GreenPAK Programmer operates directly from GreenPAK 1 Designer.

21.1.3 Minimum System Requirements

- CPU: 800MHz
- RAM: 128MB
- Graphics RAM: 32MB
- Free Hard Disk Space: 50MB

Silego's GreenPAK 1 Designer and Programmer software is supported in the following operating systems:

- 32-bit Microsoft Windows XP / Vista / 7
- 64-bit Microsoft Windows XP / Vista / 7
- Apple Mac OS X

21.2 Development Kits

The GreenPAK development kit is sold directly at the Silego Online Store. Please visit at http://store.silego.com/

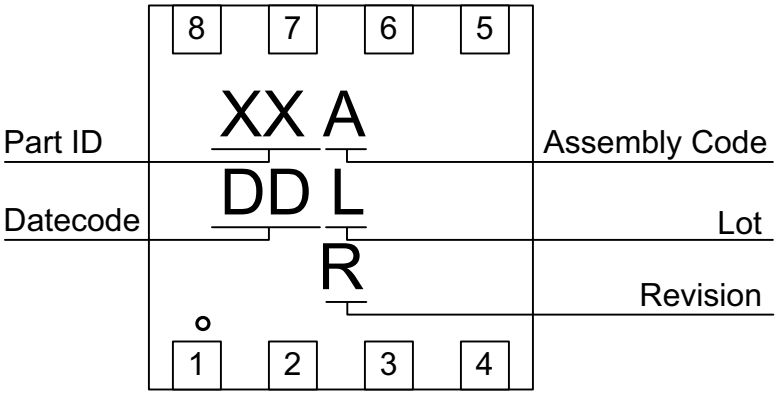
The GreenPAK Development kit is for prototyping and development with GreenPAK 1 Designer. The kit contains a USB Programming stick, USB extension cable and 50 SLG46200 samples. Everything needed for a circuit designer to start prototyping designs with the GreenPAK IC.

21.3 Project Examples

Additional GreenPAK examples designs are available on the Silego website free of charge. These designs can be downloaded and reviewed in the GreenPAK 1 Designer as a quick and efficient way to become familiar with the project development.

These examples can be found at http://support.silego.com/

22.0 Package Top Marking System Definition

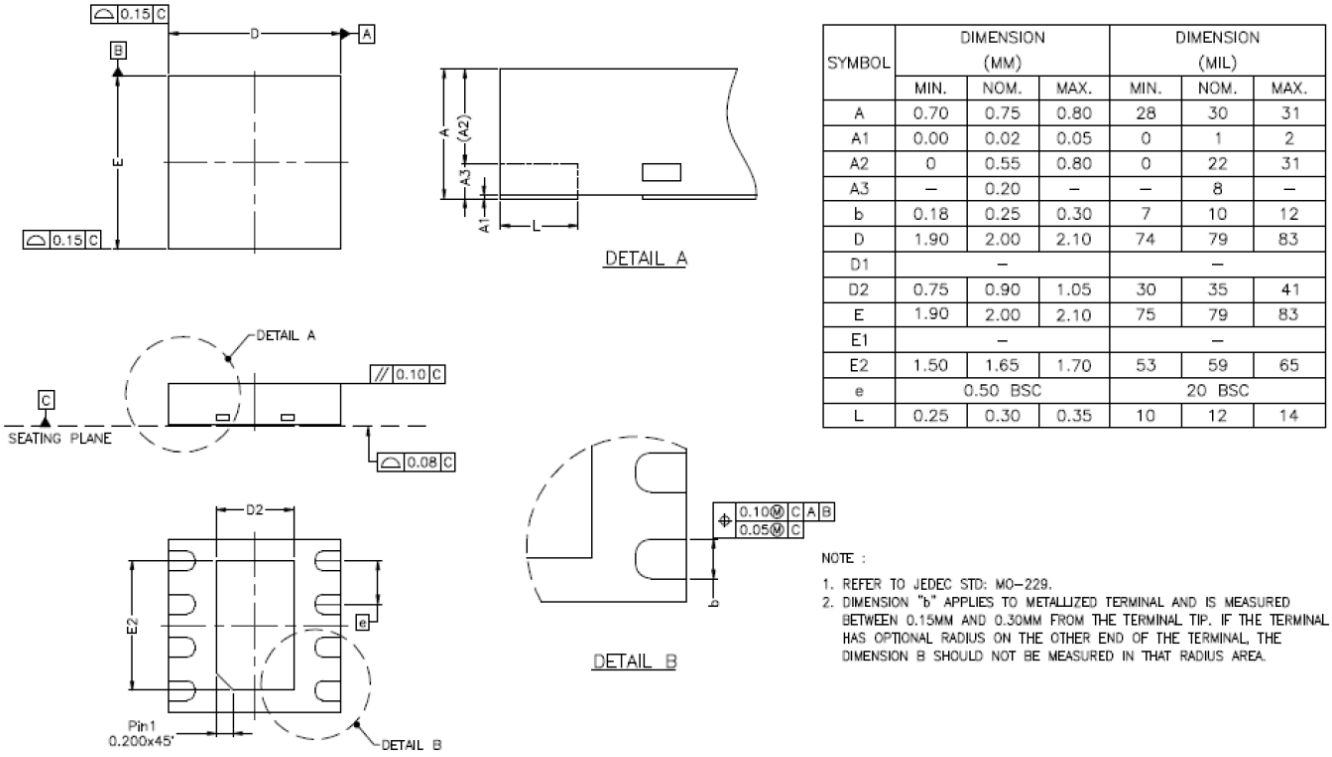


XX – Part ID Field: identifies the specific device configuration
A – Assembly Code Field: Assembly Location of the device.
DD – Date Code Field: Coded date of manufacture
L – Lot Code: Designates Lot #
R – Revision Code: Device Revision

23.0 Package Drawing and Dimensions

23.1 8 Lead TDFN Package

JEDEC MO-252, Variation W2020D



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	31
A1	0.00	0.02	0.05	0	1	2
A2	0	0.55	0.80	0	22	31
A3	–	0.20	–	–	8	–
b	0.18	0.25	0.30	7	10	12
D	1.90	2.00	2.10	74	79	83
D1		–			–	
D2	0.75	0.90	1.05	30	35	41
E	1.90	2.00	2.10	75	79	83
E1		–			–	
E2	1.50	1.65	1.70	53	59	65
e	0.50 BSC			20 BSC		
L	0.25	0.30	0.35	10	12	14

NOTE :

1. REFER TO JEDEC STD: MO–229.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

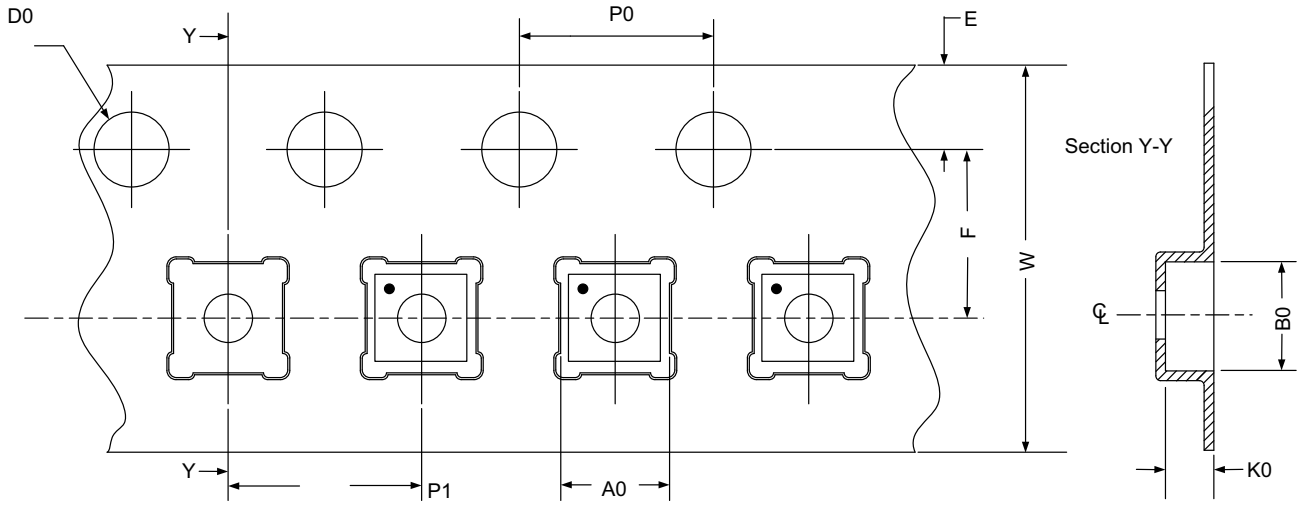
24.0 Tape and Reel Drawing and Specifications

24.1 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 8L Green	8	2 x 2 x 0.75	3,000	3,000	178 / 60	100	400	100	400	8	4

24.2 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L Green	2.3	2.3	1.05	4	4	1.55	1.75	3.5	8



Refer to EIA-481 specification

25.0 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.00 mm^3 (nominal). More information can be found at www.jedec.org.

26.0 Appendix - SLG46200 Register Definition

Bit Address	Definition
reg<4:0>	S2P input csb source selection (Connection matrix out0)
reg<9:5>	PWM power down source selection (Connection matrix out1)
reg<14:10>	PWM set source selection (Connection matrix out2)
reg<19:15>	ADC power down source selection (Connection matrix out3)
reg<24:20>	CNT0 external clock source selection (Connection matrix out4)
reg<29:25>	ACMP0 & ACMP1 power down (sig_in_CMP1_pdb) source selection (Connection matrix out5)
reg<34:30>	CNT2 keep source selection (Connection matrix out6)
reg<39:35>	CNT2 load source selection (Connection matrix out7)
reg<44:40>	CNT2 up source selection (Connection matrix out8)
reg<49:45>	DLY0 input selection (Connection matrix out9)
reg<54:50>	DLY1 or digital CMP source control input selection (Connection matrix out10)
reg<59:55>	DLY2 or digital CMP source control input selection (Connection matrix out11)
reg<64:60>	I/O PIN 3 input (digital out source) mux A port source selection (Connection matrix out12)
reg<69:65>	I/O PIN 4 input (digital out source) mux A port source selection (Connection matrix out13)
reg<74:70>	I/O PIN 6 input (digital out source) mux A port source selection (Connection matrix out14)
reg<79:75>	I/O PIN 7 digital out source selection (Connection matrix out15)
reg<84:80>	I/O PIN 8 digital out source selection (Connection matrix out16)
reg<89:85>	I/O PIN 3 output enable selection (Connection matrix out17)
reg<94:90>	I/O PIN 4 output enable selection (Connection matrix out18)
reg<99:95>	CNT2 external clock source selection (Connection matrix out19)
reg<104:100>	I/O PIN 7 output enable selection (Connection matrix out20)
reg<109:105>	I/O PIN 8 output enable selection (Connection matrix out21)
reg<114:110>	DFF0/LATCH0 data selection (Connection matrix out22)
reg<119:115>	DFF0/LATCH0 ck selection (Connection matrix out23)
reg<124:120>	DFF1/LATCH1 data selection (Connection matrix out24)
reg<129:125>	DFF1/LATCH1 ck selection (Connection matrix out25)
reg<134:130>	DFF2/LATCH2 data selection (Connection matrix out26)
reg<139:135>	DFF2/LATCH2 ck selection (Connection matrix out27)
reg<144:140>	2-bit LUT0 input0 (less significant bit) selection (Connection matrix out28)
reg<149:145>	2-bit LUT0 input1 (most significant bit) selection (Connection matrix out29)
reg<154:150>	2-bit LUT1 input0 (less significant bit) selection (Connection matrix out30)
reg<159:155>	2-bit LUT1 input1 (most significant bit) selection (Connection matrix out31)
reg<164:160>	3-bit LUT0 input0 (less significant bit) selection (Connection matrix out32)
reg<169:165>	3-bit LUT0 input1 selection (Connection matrix out33)
reg<174:170>	3-bit LUT0 input2 (most significant bit) selection (Connection matrix out34)
reg<179:175>	3-bit LUT1 input0 (less significant bit) selection (Connection matrix out35)
reg<184:180>	3-bit LUT1 input1 selection (Connection matrix out36)
reg<189:185>	3-bit LUT1 input2 (most significant bit) selection (Connection matrix out37)
reg<194:190>	3-bit LUT2 input0 (less significant bit) selection (Connection matrix out38)
reg<199:195>	3-bit LUT2 input1 selection (Connection matrix out39)
reg<204:200>	3-bit LUT2 input2 (most significant bit) selection (Connection matrix out40)
reg<209:205>	3-bit LUT3 input0(less significant bit) selection (Connection matrix out41)

Bit Address	Definition
reg<214:210>	3-bit LUT3 input1 selection (Connection matrix out42)
reg<219:215>	3-bit LUT3 input2(most significant bit) selection (Connection matrix out43)
reg<224:220>	4-bit LUT input0(less significant bit) selection (Connection matrix out44)
reg<229:225>	4-bit LUT input1 selection (Connection matrix out45)
reg<234:230>	4-bit LUT input2 selection (Connection matrix out46)
reg<239:235>	4-bit LUT input3(most significant bit) selection (Connection matrix out47)
reg<243:240>	2-bit LUT0 data
reg<247:244>	2-bit LUT1 data
reg<255:248>	3-bit LUT0 data
reg<263:256>	3-bit LUT1 data
reg<271:264>	3-bit LUT2 data
reg<279:272>	3-bit LUT3 data
reg<295:280>	4-bit LUT4 data
reg<298:296>	PIN 6 mode control 000: Digital in mode with Schmitt trigger 001: Digital in mode w/o Schmitt trigger 010: Low voltage digital in mode w/o Schmitt trigger (I/O pad supports input level 0.9V/1.2V/1.5V/1.8V) 011: Analog I/O mode 100: Digital out current double mode when OE=1 101: Open drain mode 110: Push pull mode OE=0, output tri-state; OE=1, output enable 111: Reserved
reg<300:299>	PIN 6 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<301>	PIN 6 pull up/down resistor 0: Pull down resistor 1: Pull up resistor
reg<304:302>	PIN 7 mode control 000: Digital in mode with Schmitt trigger 001: Digital in mode w/o Schmitt trigger 010: Low voltage digital in mode w/o Schmitt trigger (I/O pad supports input level 0.9V/1.2V/1.5V/1.8V) 011: Analog I/O mode 100: Digital out current double mode when OE=1 101: Open drain mode 110: Push pull mode OE=0, output tri-state; OE=1, output enable 111: Reserved
reg<306:305>	PIN 7 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<307>	PIN 7 pull up/down resistor 0: Pull down resistor 1: Pull up resistor
reg<310:308>	PIN 8 mode control 000: Digital in mode with Schmitt trigger 001: Digital in mode w/o Schmitt trigger 010: Low voltage digital in mode w/o Schmitt trigger (I/O pad supports input level 0.9V/1.2V/1.5V/1.8V) 011: Analog out mode 100: Digital out current double mode when oe=1 101: Open drain mode 110: Push pull mode OE=0, output tri-state; OE=1, output enable 111: Reserved

Bit Address	Definition
reg<312:311>	PIN 8 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<313>	PIN 8 pull up/down resistor 0: Pull down resistor 1: Pull up resistor
reg<314>	PIN 8 open drain x2 enable 0: Disable 1: Enable
reg<317:315>	3 DFFs or Latches selection 0: DFF function 1: Latch function
reg<318>	Source of digital comparators negative port selection control 0: DCOMP0 from reg<400:399>, DCOMP1 from reg<404:403> 1: From connection matrix out11 and out10
reg<319>	S2P clock enable control 0: Disable 1: Enable
reg<321:320>	PIN 2 mode control 00: Digital in mode with Schmitt trigger 01: Digital in mode w/o Schmitt trigger 10: Low voltage digital in mode w/o Schmitt trigger (I/O pad supports input level 0.9V/1.2V/1.5V/1.8V) 11: Reserved
reg<322>	CNT2 14-bit input data selection 0: From NVM reg<460:447> 1: 6 most significant bits tie 0 and 8 less significant bits from S2P or ADC (controlled by reg<467> 0: from S2P<15:0>, 1:from ADC)
reg<324:323>	PIN 2 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<325>	PIN 2 pull up/down resistor 0: Pull down resistor 1: Pull up resistor
reg<328:326>	PIN 3 mode control 000: Digital in mode with Schmitt trigger 001: Digital in mode w/o Schmitt trigger 010: Low voltage digital in mode w/o Schmitt trigger (I/O pad supports input level 0.9V/1.2V/1.5V/1.8V) 011: Reserved 100: Digital out current double mode when oe=1 101: Open drain mode 110: Push pull mode OE=0, output tri-state; OE=1, output enable 111: Reserved
reg<330:329>	PIN 3 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<331>	PIN 3 pull up/down resistor 0: Pull down resistor 1: Pull up resistor

Bit Address	Definition
reg<334:332>	PIN 4 mode control 000: Digital in mode with Schmitt trigger 001: Digital in mode w/o Schmitt trigger 010: Low voltage digital in mode w/o Schmitt trigger (I/O pad supports input level 0.9V/1.2V/1.5V/1.8V) 011: Analog in mode 100: Digital out current double mode when OE=1 101: Open drain mode 110: Push pull mode OE=0, output tri-state; OE=1, output enable 111: Reserved
reg<336:335>	PIN 4 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<337>	PIN 4 pull up/down resistor 0: Pull down resistor 1: Pull up resistor
reg<338>	PIN 4 open drain x2 enable 0: Disable 1: Enable
reg<339>	ADC analog input mux enable 0: Disable 1: Enable
reg<340>	ADC clock selection 0: Internal OSC 1: External clock (PIN 4)
reg<342:341>	V_{REF} selection 00: V_{BG} (1.796V) 01: External V_{REF} 10: Power divider
reg<343>	V_{REF} output enable 0: Disable 1: Enable
reg<344>	V_{REF} Power On 0: ACMP0_Vref off 1: Force V_{REF} output with ACMP0_Vref power ON
reg<345>	ACMP1's 0.5 gain enable 0: Bypass 1: Enable
reg<346>	ACMP0 input 1µA current output 0: Disable 1: Enable
reg<347>	ACMP0 low bandwidth enable 0: disable 1: enable
reg<348>	ACMP1 input 1µA current output 0: Disable 1: Enable
reg<349>	ACMP1 low bandwidth enable 0: Disable 1: Enable
reg<350>	ADC mode set 0: Single-end (PIN 6) 1: Differential model (PIN 6 and PIN 7)
reg<353:351>	ADC PGA gain control: 000 001 010 011 100 101 Single-ended: 0.5 1 2 4 8 16 (0.5x: w/o buffer) Differential: X 1 2 4 8 16

Bit Address	Definition
reg<355:354>	Internal OSC current select 00: 0.5µA 01: 1µA 10: 2µA 11: 10µA
reg<356>	Internal OSC V_{REF} select: 0: 1.5V 1: 0.5V
reg<357>	PGA gain to ACMP0 input enable 0: Disable 1: Enable
reg<361:358>	ACMP0 V_{REF} select: 0000: 50mV 1000: 600mV 0001: 100mV 1001: 700mV 0010: 150mV 1010: 800mV 0011: 200mV 1011: 900mV 0100: 250mV 1100: 1100mV 0101: 300mV 1101: 1300mV 0110: 400mV 1110: 1500mV 0111: 500mV 1111: Ext_Vref (PIN 8)
reg<362>	ADC's DAC V_{REF} feedback select 0: Normal 1: 0.5x gain
reg<366:363>	ACMP1 V_{REF} select: 0000: 50mV 1000: 600mV 0001: 100mV 1001: 700mV 0010: 150mV 1010: 800mV 0011: 200mV 1011: 900mV 0100: 250mV 1100: 1100mV 0101: 300mV 1101: 1300mV 0110: 400mV 1110: 1500mV 0111: 500mV 1111: Ext_Vref (PIN 8)
reg<367>	V_{REF} output buffer enable 0: V_{REF} output through buffer 1: V_{REF}output not through buffer
reg<368>	V_{REF} output source select 0: ACMP0's V_{REF} 1: VDD/2
reg<369>	ACMP0 hysteresis enable 0: Disable 1: Enable
reg<370>	ACMP1 hysteresis enable 0: Disable 1: Enable
reg<371>	ADC pseudo diff input enable under diff mode 0: Disable 1: Enable
reg<373:372>	PIN 3 digital out source selection 00/01: From connection matrix output <12> 10: S2P serial output data 11: ADC serial output data
reg<374>	S2P in/out mode control 0: S2P serial input mode 1: P2S serial output mode
reg<382:375>	Digital comparator negative port input (in2 of DCMP0 and in3 of DCMP1)
reg<390:383>	Digital comparator negative port input (in3 of DCMP0 and in4 of DCMP1)
reg<398:391>	Digital comparator negative port input (in4 of DCMP0 and in2 of DCMP1)

Bit Address	Definition
reg<400:399>	DCMP0 negative port selection control, which selected by reg<318> 00: S2P<15:8> 01: reg<382:375> 10: reg<390:383> 11: reg<398:391>
reg<401>	DCMP0 positive port selection 0: from S2P<7:0> 1: from ADC
reg<402>	DCMP0 & DCMP1 power down control 0: Power down 1: Normal operation
reg<404:403>	DCMP1 negative port selection control, which selected by reg<318> 00: S2P<7:0> 01: reg<390:383> 10: reg<398:391> 11: reg<382:375>
reg<405>	DCMP1 positive port selection 0: From S2P<15:8> 1: From ADC
reg<406>	PIN 6 output enable control 0: Disable 1: Enable
reg<408:407>	PWM input selection 00: from ADC 01: from S2P<15:8> 10: from FSM CNT2 outputs 11: DCMP1 negative input after 4 to 1 mux
reg<411:409>	PWM dead band selection 000: 8ns 100: 40ns 001: 16ns 101: 48ns 010: 24ns 110: 56ns 011: 32ns 111: 64ns
reg<412>	Reserved
reg<413>	PWM mode control 0: PWM output duty cycle 0 ~ 99.6% 1: PWM output duty cycle 0.39% ~ 100%
reg<414>	Force CNT0 power on 0: Auto power on 1: Force power on
reg<415>	Force CNT1 power on 0: Auto power on 1: Force power on
reg<416>	Force CNT2 power on 0: Auto power on 1: Force power on
reg<417>	Force oscillator power on 0: Auto power on from delay cell 1: Force power on
reg<418>	Oscillator frequency band select 0: Low frequency 1: High frequency
reg<432:419>	CNT0 control data 1-16384: (delay time = (counter control data + 1) / freq)
reg<446:433>	CNT1 control data 1-16384: (delay time = (counter control data + 1) / freq)
reg<460:447>	CNT2 control data 1-16384: (delay time = (counter control data + 1) / freq)

Bit Address	Definition
reg<461>	CNT2 load signal tied to Ground 0: Off 1: Enable
reg<462>	CNT0 input clock source select 0: Internal oscillator clock 1: From matrix
reg<465:463>	CNT1 input clock source select: 000: Internal oscillator clock 001: Internal oscillator clock divided by 12 010: Internal oscillator clock divided by 4 011: CNT2 overflow signal 1X0: From matrix 1X1: From matrix divided by 8 and synchronized by internal clock
reg<466>	CNT2 input clock source select 0: Internal oscillator clock 1: From CNT0 output
reg<467>	Data source select for FSM (CNT2) 0: From external (though S2P module) 1: From internal ADC output
reg<469:468>	Delay mode select for DLY0: 00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<471:470>	Delay mode select for DLY1: 00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<473:472>	Delay mode select for DLY2: 00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<474>	CNT0 and DLY0 output selection 0: Delay output 1: Counter output
reg<475>	CNT1 and DLY1 output selection 0: Delay output 1: Counter output
reg<476>	CNT2 and DLY2 output selection 0: Delay output 1: Counter output
reg<477>	PIN 4 digital out source selection 0: From connection matrix(out13) 1: ADC output clock
reg<478>	DLY1 And DLY2 Input Source Enable Control Signal 0: Disable DLY1 and DLY2 input 1: DLY1 input from connection matrix out10 and DLY2 input from connection matrix out11
reg<479>	Reserved

27.0 Revision History

Date	Version	Change
8/6/2014	1.24	Fixed ESD information
5/5/2014	1.23	Updated Pockets and Length values in Tape and Reel Spec
6/4/2013	1.22	Updated 3bit LUT and 4bit LUT Standard Digital Functions tables
5/28/2013	1.21	Adjusted VIH and VIL min and max values
3/1/2013	1.2	Fixed typo regarding register <466> CNT2 Input Clock Source Select
11/19/2012	1.19	Fixed typos in Section 12.9 (less than or equal signs)
7/16/2012	1.18	Editorial changes for clarification and typo fixes throughout Renamed Signal names to match GreenPAK Designer Software Moved Bi-Directional Pin example to Section 20.0
6/20/2012	1.17	Clarified ACMP power down operation Removed Application Example regarding time delay
6/8/2012	1.16	Updated Sections 16.2 and 17.2 Added note regarding minimum value of the register setting for the CNT/DLY cells
3/20/2012	1.14	Editorial changes for clarification and typo fixes throughout
1/30/2012	1.13	Editorial changes for clarification and typo fixes throughout Updated Section 11.x ADC
1/23/2012	1.12	Updated Section 11.9 ADC Outputs Updated Recommended Soldering Profile information
12/5/2011	1.11	Added Recommended Soldering Profile information
11/2/2011	1.1	Added Bi-Directional Pin Information
10/26/2011	1.09	Updated and clarified VIH/VIL specification
8/9/2011	1.07	Correct typos
2/9/2011	1.06	Clarified PWM output description
1/21/2011	1.04	Updated Block Diagram
11/19/2010	1.0	Production release.
11/18/2010	0.94	Added Current measurements to Section 5
11/15/2010	0.93	Updated Package Drawing and Tape and Reel Drawing
11/2/2010	0.9	Datasheet reorganization
9/14/2010	0.8	Fixed grammar and syntax added Analog Comparator Switching Characteristics
9/1/2010	0.77	Updated block diagram Added Appendix - Register Definition Added GreenPAK Design flowchart Typo fixes
8/23/2010	0.76	Fixed typos on Counters diagram
8/17/2010	0.75	Renamed AD_chmode_sel to AD_channel_sel in ADC

28.0 Silego Website & Support

28.1 Silego Technology Website

Silego Technology provides online support via our website at http://www.silego.com/.This web site is used as a means to make files and information easily available to customers.

For more information regarding Silego GreenPAK and other Silego Green products, please visit:

http://greenpak.silego.com/
http://greenfet.silego.com/
http://greenpak2.silego.com/
http://greenfet2.silego.com/
http://greenclk.silego.com/

Products are also available for purchase directly from Silego at the Silego Online Store at http://store.silego.com/.

28.2 Silego Technical Support

Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at info@silego.com.

For specific GreenPAK design or applications questions and support please send email requests to GreenPAK@silego.com

Users of Silego products can receive assistance through several channels:

28.2.1 Online Live Support

Silego Technology has live video technical assistance and sales support available at http://www.silego.com/. Please ask our live web receptionist to schedule a 1 on 1 training session with one of our application engineers.

28.2.2 Contact Your Local Sales Representative

Customers can contact their local sales representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. More information regarding your local representative is available at the Silego website or send a request to info@silego.com

28.2.3 Contact Silego Directly

Silego can be contacted directly via e-mail at info@silego.com or user submission form, located at the following weblink:

http://support.silego.com/

28.3 Other Information

The latest Silego Technology press releases, listing of seminars and events, listings of world wide Silego Technology offices and representatives are all available at http://www.silego.com/