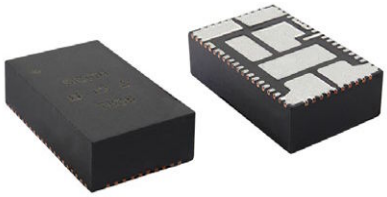
4.5 V to 18 V Input, 20 A microBRICK® DC/DC Regulator Module



LINKS TO ADDITIONAL RESOURCES

PowerCAD Design Tool | Evaluation Boards | Design Tools

DESCRIPTION

The SiC931 is a synchronous buck regulator module with integrated power MOSFETs and inductor. Its power stage is capable of supplying 20 A continuous current at up to 2 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.6 V from 4.5 V to 18 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiC931's architecture supports ultrafast transient response with minimum output capacitance and tight ripple regulation at very light load. The device is internally compensated and no external ESR network is required for loop stability purposes. The device also incorporates a power saving scheme that significantly increases light load efficiency.

The regulator integrates a full protection feature set, including output over voltage protection (OVP), cycle by cycle over current protection (OCP) short circuit protection (SCP) and thermal shutdown (OTP). It also has UVLO and a user programmable soft start.

The SiC931 is available in lead (Pb)-free power enhanced PowerPAK® MLP60-A6 package in 10.6 mm x 6.5 mm x 3 mm dimensions.

APPLICATIONS

- 5 V and 12 V input rail POLs
- Desktop, notebooks, server, and industrial computing
- Industrial and automation
- consumer electronics

FEATURES

RoHS COMPLIANT
HALOGEN FREE

- Versatile
  - Operation from 4.5 V to 18 V input voltage
  - Adjustable output voltage down to 0.6 V
  - Output voltage tracking and sequencing with pre-bias start up
  - ± 1 % output voltage accuracy from -40 °C to +125 °C
- Highly efficient
  - 95 % peak efficiency
  - 1 µA supply current at shutdown
  - 50 µA operating current, not switching
- Highly configurable
  - Four programmable switching frequencies available: 600 kHz, 1 MHz, 1.5 MHz, and 2 MHz
  - Adjustable soft start and adjustable current limit
  - Programmable modes of operation: forced continuous conduction or power save mode
- Robust and reliable
  - Cycle-by-cycle current limit
  - Output overvoltage protection
  - Output undervoltage / short circuit protection with auto retry

  -Power good flag and over temperature protection
- High power density
  - Integration of high current output inductor
  - 10.6 mm x 6.5 mm x 3 mm low profile MLP package
- Ease of use
  - Minimum peripheral components
  - All ceramic capacitors for input and output
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

TYPICAL APPLICATION CIRCUIT AND EFFICIENCY

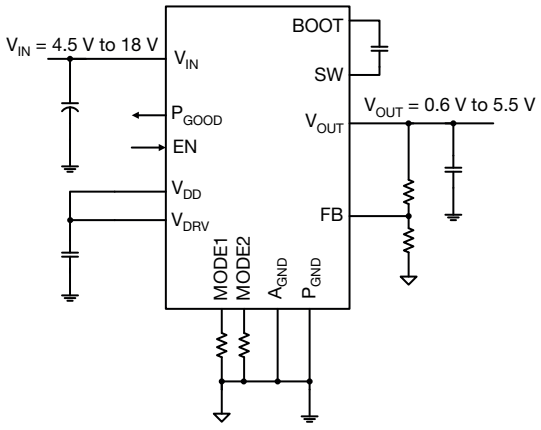


Fig. 1 - Typical Application Circuit

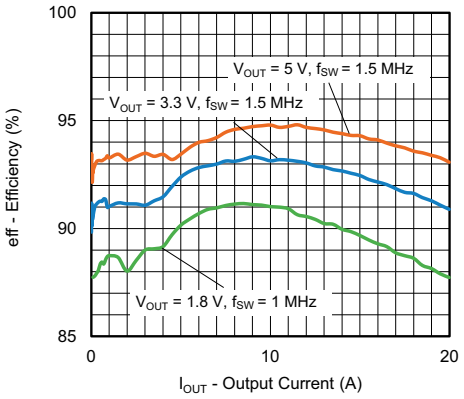


Fig. 2 - Efficiency vs. Output Current (V_{IN} = 12 V, Power Save Mode enabled)

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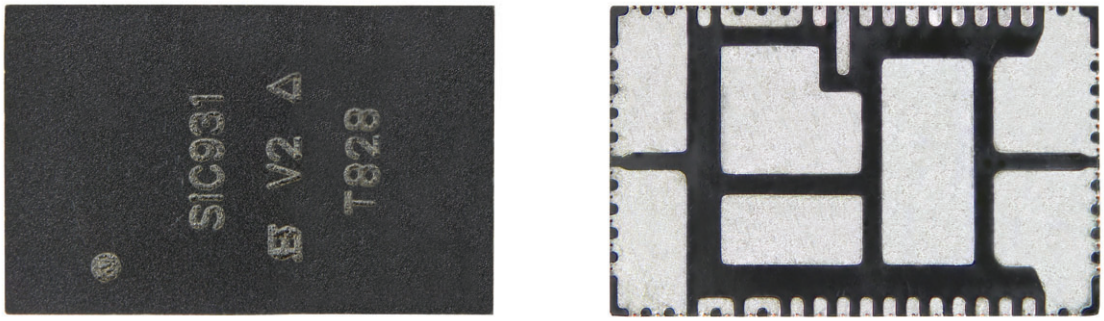
PIN CONFIGURATION



Top view Bottom view

Fig. 3 - Top View and Bottom View

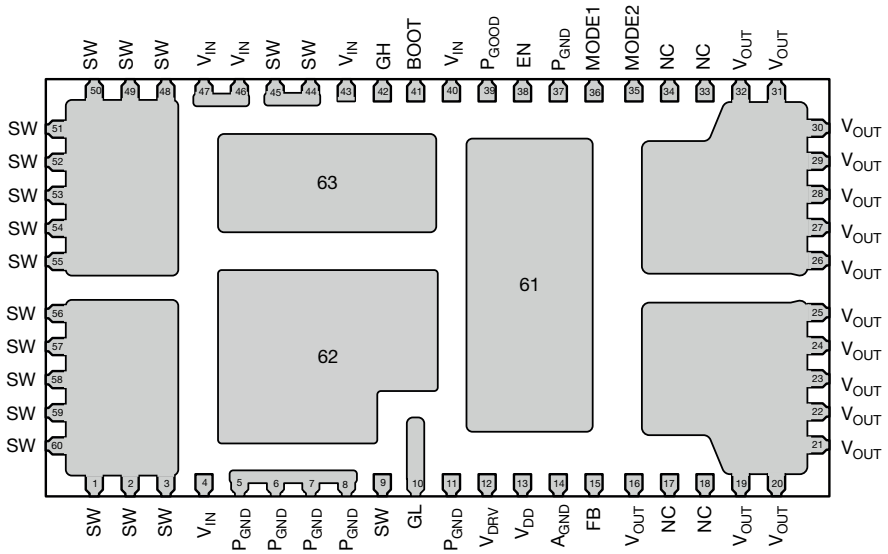


Fig. 4 - Pin Configuration (Top Transparent View)

PIN DESCRIPTION		
PIN NUMBER	**SYMBOL**	**DESCRIPTION**
1 to 3, 9, 44, 45, 48 to 60	SW	Switching node
4, 43, 46, 47, 63	V_{IN}	Power input
5 to 8, 11, 37, 62	P_{GND}	Power ground
10	GL	Low side power MOSFET gate signal
12	V_{DRV}	Supply voltage for internal gate driver. Connect a 2.2 µF decoupling capacitor to P_{GND}
13	V_{DD}	Supply voltage for internal logic. Connect a 1 µF decoupling capacitor to A_{GND}
14, 61	A_{GND}	Analog ground
15	FB	Output voltage feedback pin; connect to V_{OUT} through a resistor divider network
16, 19 to 32	V_{OUT}	Output voltage sense pin
17, 18, 33, 34	NC	Not internally connected
35	MODE2	Soft start and current limit selection; connect a resistor to V_{DD} or A_{GND} per Table 2
36	MODE1	Operating mode and switching frequency selection; connect a resistor to V_{DD} or A_{GND} per Table 1
38	EN	Enable pin
39	P_{GOOD}	Power good open drain output
40	V_{CIN}	Input to internal 5 V LDO. Recommend to connect to V_{IN} pins
41	BOOT	Bootstrap pin. Connect 100 nF capacitor between BOOT and SW for high side driver supply

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	DESCRIPTION
42	GH	High side power MOSFET gate signal

ORDERING INFORMATION

PART NUMBER	PART MARKING	V_{DD}, V_{DRV}	LIGHT LOAD MODE	OPERATION JUNCTION TEMPERATURE	PACKAGE	PACKAGING	MINIMUM ORDER QUANTITY
SiC931BED-T1-GE3	SiC931B	Internal	Power saving	-40 °C to +125 °C	PowerPAK MLP60-A6	Tape and reel	3000
SiC931BED-Y1-GE3	SiC931B	Internal	Power saving	-40 °C to +125 °C	PowerPAK MLP60-A6	Tray	210

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

ELECTRICAL PARAMETER	CONDITIONS	LIMITS	UNIT
V_{IN}	Reference to P_{GND}	-0.3 to +25	V
V_{OUT}	Reference to P_{GND}	-0.3 to +22	
V_{DD} / V_{DRV}	Reference to P_{GND}	-0.3 to +6	
SW / PHASE	Reference to P_{GND}	-0.3 to +25	
SW / PHASE (AC)	100 ns; reference to P_{GND}	-8 to +30	
BOOT	Reference to P_{GND}	-0.3 to +31	
BOOT to SW		-0.3 to +6	
A_{GND} to P_{GND}		-0.3 to +0.3	
EN	Reference to A_{GND}	-0.3 to +25	
All other pins	Reference to A_{GND}	-0.3 to +6	
Temperature			
Junction temperature	T_J	-40 to +150	°C
Storage temperature	T_{STG}	-65 to +150	
Power Dissipation			
Junction-to-ambient thermal impedance ($R_{\theta JA}$)		16	°C/W
Junction-to-case thermal impedance ($R_{\theta JC}$)		2	
Maximum power dissipation	Ambient temperature = 25 °C	7.75	W
ESD Protection			
Electrostatic discharge protection	Human body model	4000	V
	Charged device model	1000	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (all voltages referenced to A_{GND}, P_{GND} = 0 V)

PARAMETER	MIN.	TYP.	MAX.	UNIT
Input voltage (V_{IN})	4.5	-	18	V
Logic supply voltage, gate driver supply voltage (V_{DD}, V_{DRV})	4.5	5	5.5	
Enable (EN)	0	-	18	
Output voltage (V_{OUT})	0.6	-	5.5	
Temperature				
Recommended ambient temperature	-40 to +105			°C
Operating junction temperature	-40 to +125			

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ELECTRICAL SPECIFICATIONS (V_{IN} = 12 V, V_{EN} = 5 V, T_J = -40 °C to +125 °C, unless otherwise stated)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Power Supplies						
V_{DD} supply	V_{DD}	V_{IN} = 6 V to 18 V	4.75	5	5.25	V
V_{DD} UVLO threshold, rising	V_{DD_UVLO}		3.3	3.6	3.9	
V_{DD} UVLO hysteresis	$V_{DD_UVLO_HYST}$		-	300	-	mV
Maximum V_{DD} current	I_{DD}	V_{IN} = 6 V to 18 V	3	-	-	mA
V_{DRV} supply	V_{DRV}	V_{IN} = 6 V to 18 V	4.75	5	5.25	V
Maximum V_{DRV} current	I_{DRV}	V_{IN} = 6 V to 18 V	50	-	-	mA
Input current	I_{IN}	Non-switching, V_{FB} > 0.6 V	-	75	125	µA
Shutdown current	I_{IN_SHDN}	V_{EN} = 0 V	-	0.5	3	
Controller and Timing						
Feedback voltage	V_{FB}	T_J = 25 °C	597	600	603	m/V
		T_J = -40 °C to +125 °C (1)	594	600	606	
V_{FB} input bias current	I_{FB}		-	2	-	nA
Minimum on-time	$t_{ON_MIN.}$		-	40	50	ns
t_{ON} accuracy	$t_{ON_ACCURACY}$		-10	-	10	%
On-time range	t_{ON_RANGE}		65	-	2250	ns
Minimum off-time	$t_{OFF_MIN.}$		205	250	305	
Fault Protections						
Over current protection (inductor valley current)	I_{OCP}	T_J = -10 °C to +125 °C	-20	-	20	%
Output OVP threshold	V_{OVP}	V_{FB} with respect to 0.6 V reference	-	20	-	
Output UVP threshold	V_{UVP}		-	-80	-	
Over temperature protection	T_{OTP_RISING}	Rising temperature	-	150	-	°C
	T_{OTP_HYST}	Hysteresis	-	25	-	
Power Good						
Power good output threshold	$V_{FB_RISING_VTH_OV}$	V_{FB} rising above 0.6 V reference	-	20	-	%
	$V_{FB_FALLING_VTH_UV}$	V_{FB} falling below 0.6 V reference	-	-10	-	
Power good hysteresis	V_{FB_HYST}		-	45	-	mV
Power good on resistance	R_{ON_PGOOD}		-	14	20	Ω
Power good delay time	t_{DLY_PGOOD}		15	25	35	µs
EN / MODE / Ultrasonic Threshold						
EN logic high level	V_{EN_H}		1.6	-	-	V
EN logic low level	V_{EN_L}		-	-	0.4	
EN pull down resistance	R_{EN}		-	-	-	MΩ
Switching Frequency						
MODE1 (switching frequency)	R_{MODE1}	f_{SW} = 600 kHz	-	51	55	kΩ
		f_{SW} = 1 MHz	90	100	110	
		f_{SW} = 1.5 MHz	180	200	220	
		f_{SW} = 2 MHz	450	499	-	
Soft Start						
Soft start time	t_{ss}	Connect R_{MODE2} between MODE2 and A_{GND}	1.8	3	4.2	ms
		Connect R_{MODE2} between MODE2 and V_{DD}	3.6	6	8.4	
Over Current Protection						
MODE2 (over current protection)	R_{MODE2}	I_{OCP} = 32 A	450	499	-	kΩ
		I_{OCP} = 24.8 A	180	200	220	
		I_{OCP} = 17.3 A	90	100	110	
		I_{OCP} = 9.6 A	-	51	55	

Note
(1) Guaranteed by design

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FUNCTIONAL BLOCK DIAGRAM

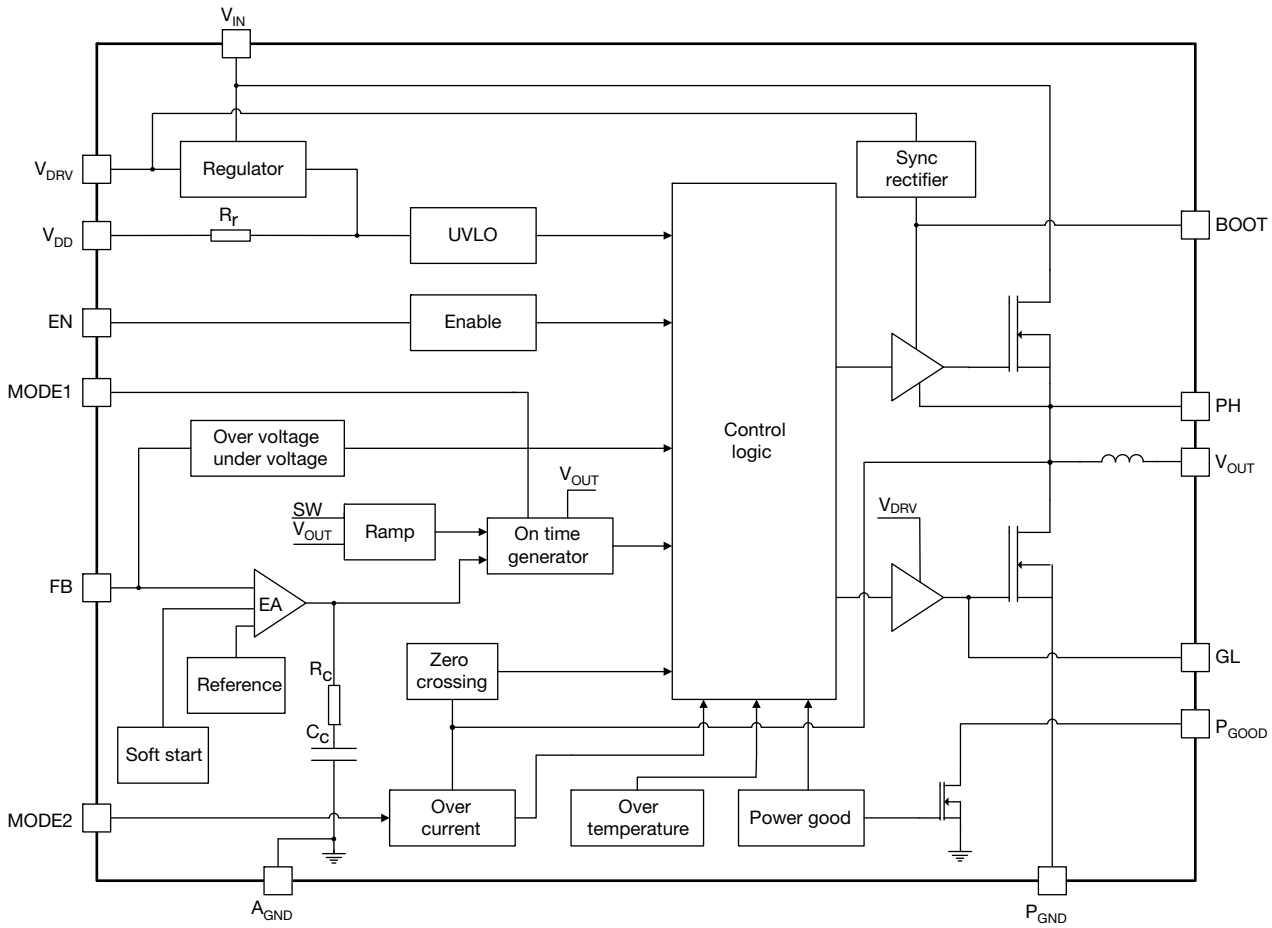

Fig. 5 - Functional Block Diagram

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OPERATIONAL DESCRIPTION

Device Overview

SiC931 is a high efficiency synchronous buck regulator capable of delivering up to 20 A continuous current. The device has user programmable switching frequency of 600 kHz, 1 MHz, 1.5 MHz, and 2 MHz. The control scheme delivers fast transient response and minimizes the number of external components. Thanks to the internal ramp information, no high ESR output bulk or virtual ESR network is required for the loop stability. This device also incorporates a power saving feature that enables diode emulation mode and frequency fold back as the load decreases.

SiC931 has a full set of protection and monitoring features:

- Over current protection in pulse-by-pulse mode
- Output over voltage protection
- Output under voltage protection with device latch
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power good open drain output

This device is available in MLP60-A6 package to deliver high power density and minimize PCB area.

Power Stage

SiC931 integrates a high performance power stage with both high side and low side MOSFETs and a 220 nH output inductor. The power stage is optimized to achieve up to 95 % efficiency with 1.5 MHz switching frequency.

The input voltage (V_{IN}) can go up to 18 V and down to as low as 4.5 V for power conversion. An internal LDO converts input voltage from V_{CIN} to V_{DD} for controller and driver power supply. There is no need to connect an external 5 V bias.

Control Mechanism

SiC931 employs an advanced voltage - mode COT control mechanism. During steady-state operation, feedback voltage (V_{FB}) is compared with internal reference (0.6 V typ.) and the amplified error signal (V_{COMP}) is generated at the internal comp node. An internally generated ramp signal and V_{COMP} feed into a comparator. Once V_{RAMP} crosses V_{COMP}, an on-time pulse is generated for a fixed time. During the on-time pulse, the high side MOSFET will be turned on. Once the on-time pulse expires, the low side MOSFET will be turned on after a dead time period. The low side MOSFET will stay on for a minimum duration equal to the minimum off-time ($t_{OFF_MIN.}$) and remains on until V_{RAMP} crosses V_{COMP}. The cycle is then repeated.

Fig. 6 illustrates the basic block diagram for VM-COT architecture. In this architecture the following is achieved:

- The reference of a basic ripple control regulator is replaced with a high again error amplifier loop
- This establishes two parallel voltage regulating feedback paths, a fast and slow path
- Fast path is the ripple injection which ensures rapid correction of the transient perturbation
- Slow path is the error amplifier loop which ensures the DC component of the output voltage follows the internal accurate reference voltage

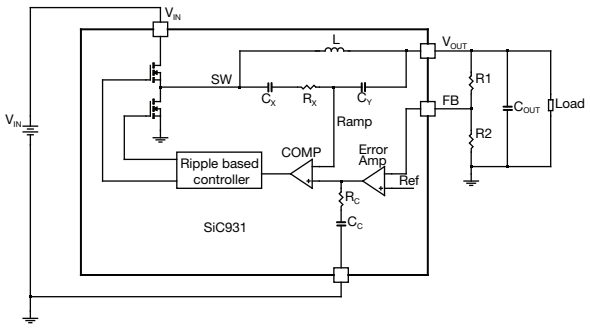

Fig. 6 - VM-COT Block Diagram

All components for RAMP signal generation and error amplifier compensation required for the control loop are internal to the IC, see Fig. 6. In order for the device to cover a wide range of V_{OUT} operation, the internal RAMP signal components (R_X, C_X, C_Y) are automatically selected depending on the V_{OUT} voltage and switching frequency. This method allows the RAMP amplitude to remain constant throughout the V_{OUT} voltage range, achieving low jitter and fast transient Response. The error amplifier internal compensation consists of a resistor in series with a capacitor (R_{COMP}, C_{COMP}).

Fig. 7 demonstrates the basic operational waveforms:

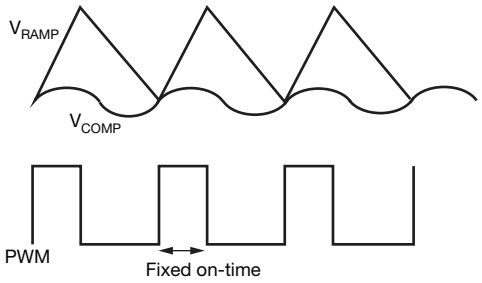

Fig. 7 - VM-COT Operational Principle

Light Load Condition

To improve efficiency at light-load condition, SiC931 provides a set of innovative implementations to eliminate LS recirculating current and switching losses. The internal zero crossing detector monitors SW node voltage to determine when inductor current starts to flow negatively. In power saving mode, as soon as inductor valley current crosses zero, the device deploys diode emulation mode by turning off low side MOSFET. If load further decreases, switching frequency is reduced proportional to load condition to save switching losses while keeping output ripple within tolerance. The switching frequency is set by the controller to maintain regulation. There is no minimum switching frequency limitation.

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Mode Setting, Over Current Protection, Switching Frequency, and Soft Start Selection

The SiC931 has a low pin count, minimal external components, and offers the user flexibility to choose soft start times, current limit settings, switching frequencies and to enable or disable the light load mode. Two MODE pins, MODE1 and MODE2, are user programmable by connecting a resistor from MODEx to V_{DD} or A_{GND}, allowing the user to choose various operating modes. This is best explained in the tables below.

TABLE 1 - MODE1 CONFIGURATION SETTINGS

OPERATION	CONNECTION	f_{SWITCH} (kHz)	R_{MODE1} (kΩ)
Skip	To A_{GND}	600	51
		1000	100
		1500	200
		2000	499
Forced CCM	To V_{DD}	600	51
		1000	100
		1500	200
		2000	499

TABLE 2 - MODE2 CONFIGURATION SETTINGS

SOFT-START TIME	CONNECTION	I_{LIMIT} (%)	R_{MODE2} (kΩ)
3 ms	To A_{GND}	30	51
		54	100
		78	200
		100 (32 A)	499
6 ms	To V_{DD}	30	51
		54	100
		78	200
		100 (32 A)	499

OUTPUT MONITORING AND PROTECTION FEATURES

Output Over Current Protection (OCP)

SiC931 has pulse-by-pulse over current limit control. The inductor current is monitored during low side MOSFET conduction time through $R_{DS(on)}$ sensing. After a pre-defined blanking time, the inductor current is compared with an internal OCP threshold. If inductor current is higher than OCP threshold, high side MOSFET is kept off until the inductor current falls below OCP threshold.

OCP is enabled immediately after V_{DD} passes UVLO rising threshold.

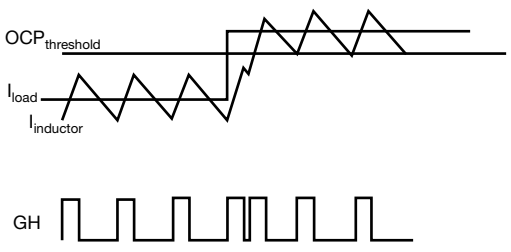

Fig. 8 - Over-Current Protection Illustration

Output Undervoltage Protection (UVP)

UVP is implemented by monitoring the FB pin. If the voltage level at FB drops below 0.12 V for more than 25 µs, a UVP event is recognized and both high side and low side MOSFETs are turned off. After a duration equivalent to 20 soft start periods, the IC attempts to re-start. If the fault condition still exists, the above cycle will be repeated.

UVP is active after the completion of soft start sequence.

Output Overvoltage Protection (OVP)

OVP is implemented by monitoring the FB pin. If the voltage level at FB rising above 0.72 V, a OVP event is recognized and both high side and low side MOSFETs are turned off. Normal operation is resumed once FB voltage drop below 0.68 V.

OVP is active after V_{DD} passes UVLO rising threshold.

Over-Temperature Protection (OTP)

OTP is implemented by monitoring the junction temperature. If the junction temperature rises above 150 °C, a OTP event is recognized and both high side and low MOSFETs are turned off. After the junction temperature falls below 115 °C (35 °C hysteresis), the device restarts by initiating a soft start sequence.

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Sequencing of Input / Output Supplies

SiC931 has no sequencing requirements on its supplies or enables (V_{IN}, V_{DD}, V_{DRV}, EN).

Enable

The SiC931 has an enable pin to turn the part on and off. Driving the pin high enables the device, while driving the pin low disables the device.

The EN pin is internally pulled to A_{GND} by a 5 MΩ resistor to prevent unwanted turn on due to a floating GPIO.

Pre-Bias Start-Up

In case of pre-bias startup, output is monitored through FB pin. If the sensed voltage on FB is higher than the internal reference ramp value, control logic prevents high side and low side MOSFETs from switching to avoid negative output voltage spike and excessive current sinking through low side MOSFET.

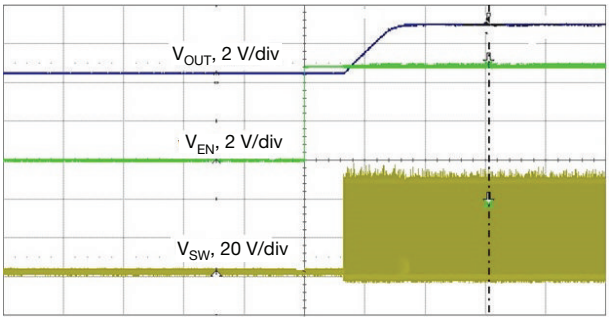

Fig. 9 - Pre-Bias Start-Up

Power Good

SiC931's power good is an open-drain output. Pull P_{GOOD} pin high through a > 10 kΩ resistor to use this signal. Power good window is shown in the below diagram. If voltage on FB pin is out of this window, P_{GOOD} signal is de-asserted by pulling down to A_{GND}. To prevent false triggering during transient events, P_{GOOD} has a 25 µs blanking time.

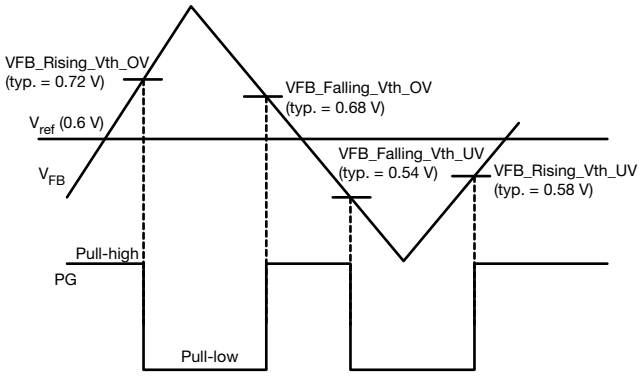

Fig. 10 - P_{GOOD} Window Diagram

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ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{sw} = 500 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 10 µF x 6, unless otherwise noted)

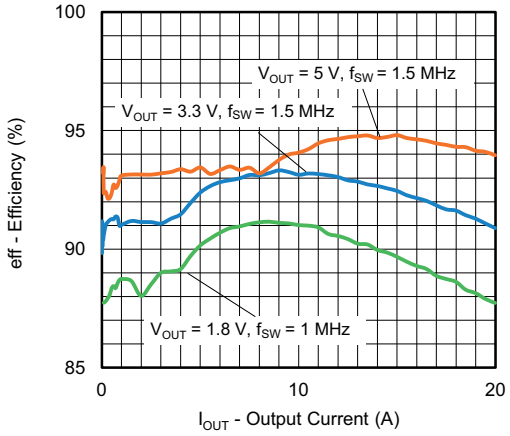

Fig. 11 - Efficiency vs. Output Current (V_{IN} = 12 V, f_{sw} = 1.5 MHz, Power Save Mode)

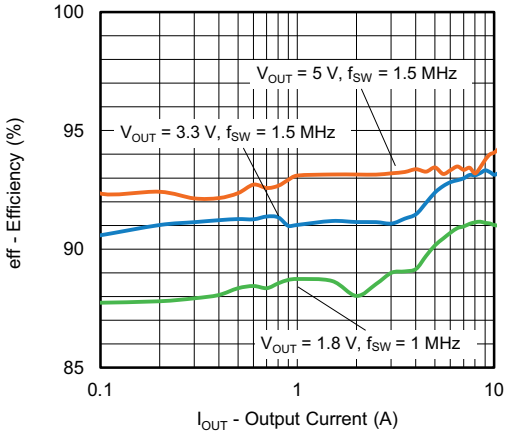

Fig. 14 - Efficiency vs. Output Current (V_{IN} = 12 V, f_{sw} = 1.5 MHz, Light Load)

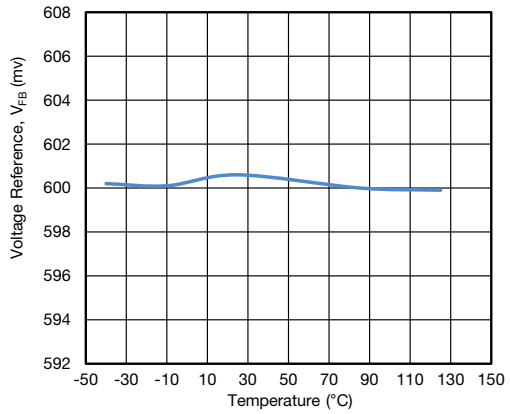

Fig. 12 - Voltage Reference vs. Junction Temperature

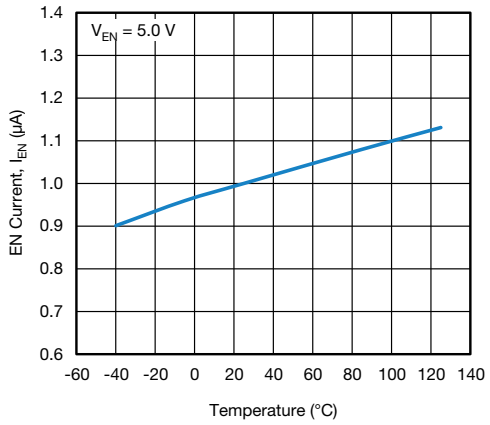

Fig. 15 - EN Current vs. Junction Temperature

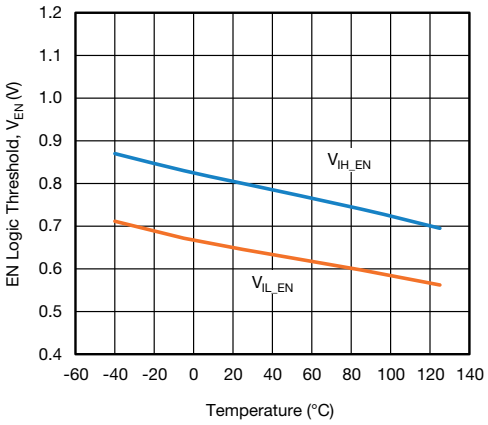

Fig. 13 - EN Logic Threshold vs. Junction Temperature

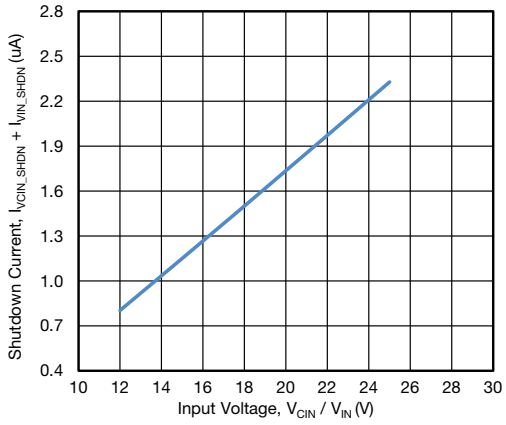

Fig. 16 - Shutdown Current vs. Input Voltage

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ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{sw} = 500 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 10 µF x 6, unless otherwise noted)

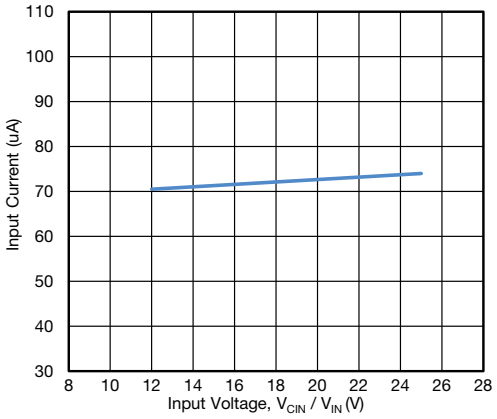

Fig. 17 - Input Current vs. Input Voltage

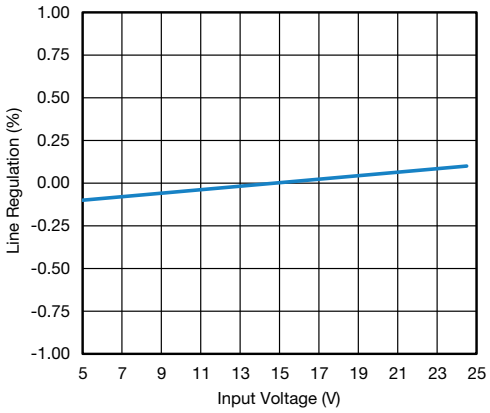

Fig. 20 - Line Regulation vs. Input Voltage

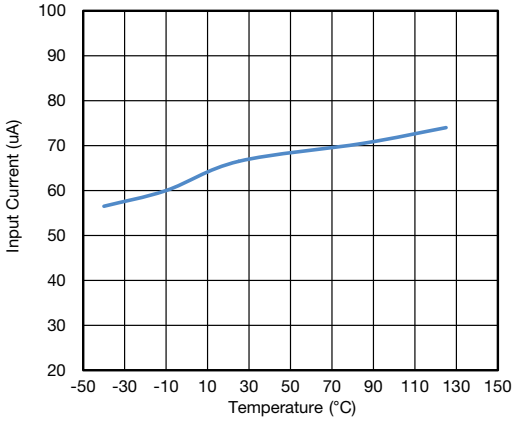

Fig. 18 - Input Current vs. Junction Temperature

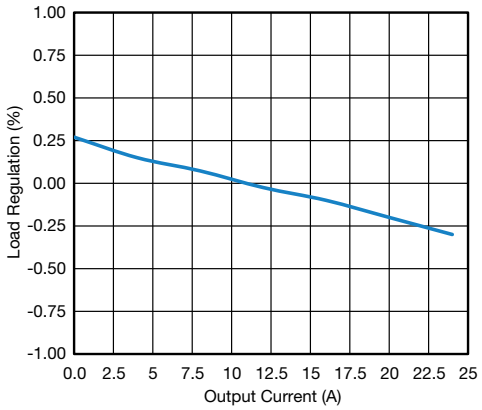

Fig. 21 - Load Regulation vs. Output Current

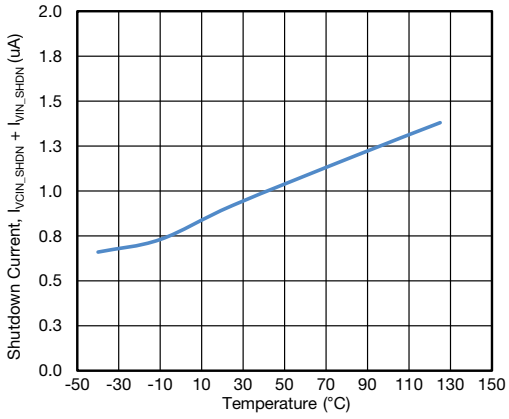

Fig. 19 - Shutdown Current vs. Junction Temperature

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ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, 25 A full load, f_{sw} = 600 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 2.2 µF x 3, unless otherwise noted)

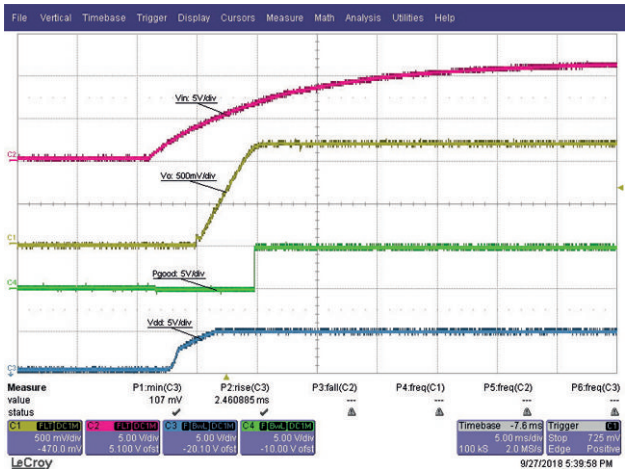

Fig. 22 - Startup with V_{IN}, t = 5 ms/div

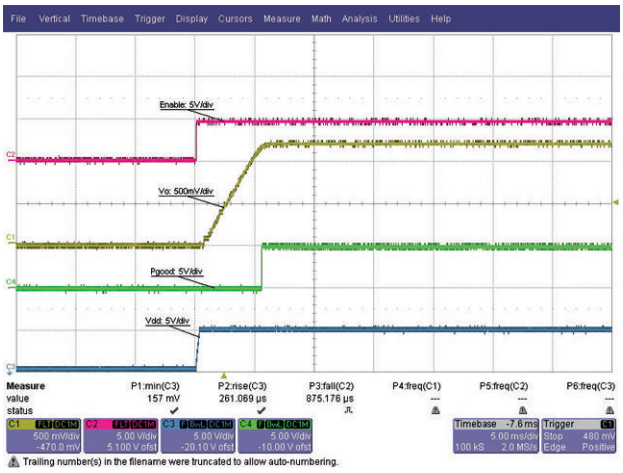

Fig. 25 - Startup with EN, t = 5 ms/div

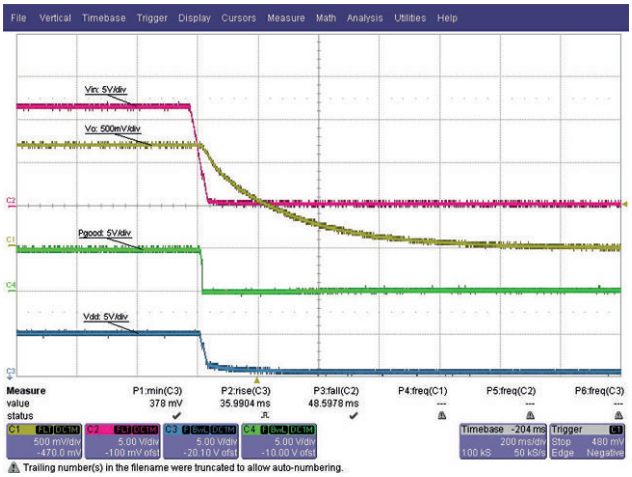

Fig. 23 - Shut down with V_{IN}, t = 200 ms/div

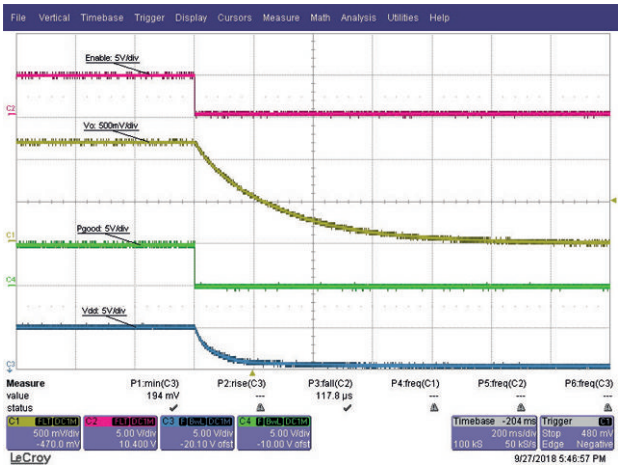

Fig. 26 - Shut down with EN, t = 200 ms/div

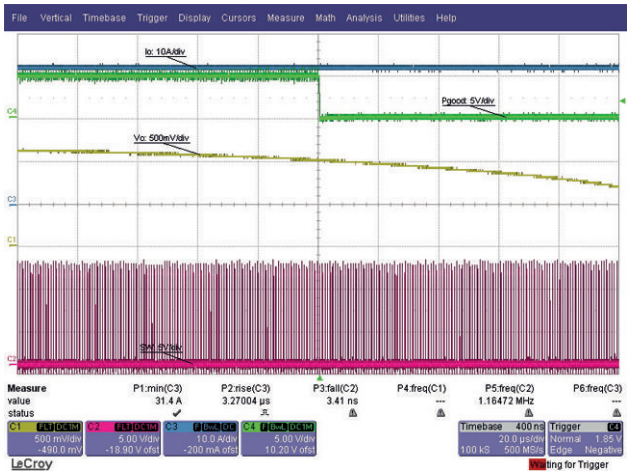

Fig. 24 - Overcurrent Protection Behavior, t = 20 µs/div

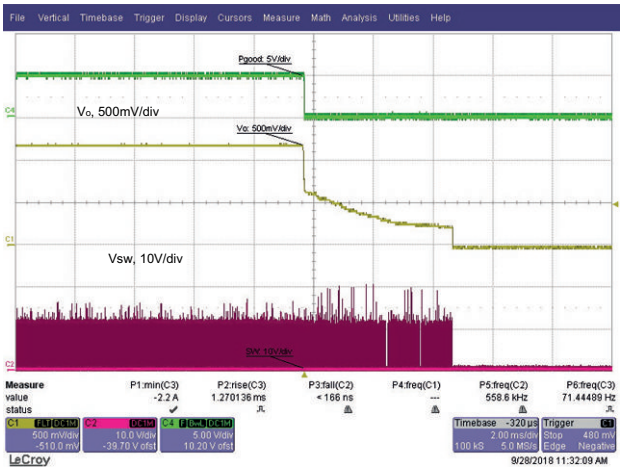

Fig. 27 - Output Undervoltage Protection Behavior, t = 2 ms/div

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ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, 25 A full load, f_{sw} = 600 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 2.2 µF x 3, unless otherwise noted)

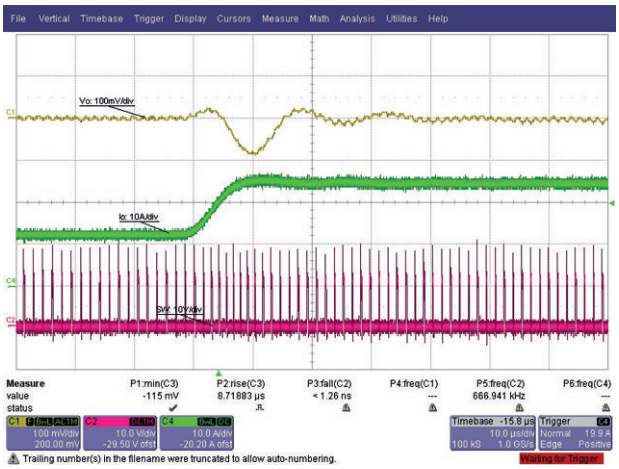

Fig. 28 - Load Step, 12 A to 24 A, 1 A/µs, t = 10 µs/div

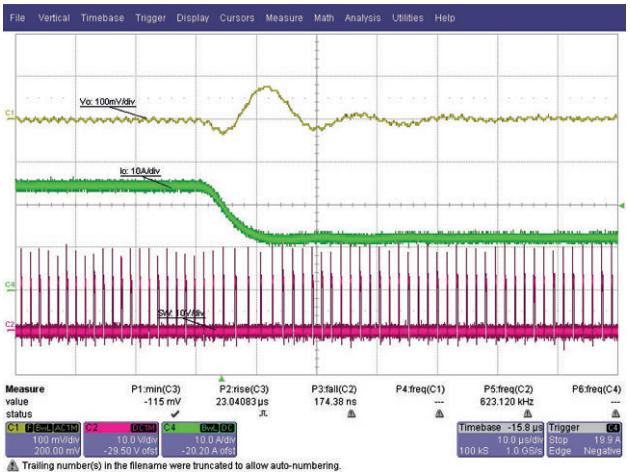

Fig. 31 - Load Release, 24 A to 12 A, 1 A/µs, t = 10 µs/div

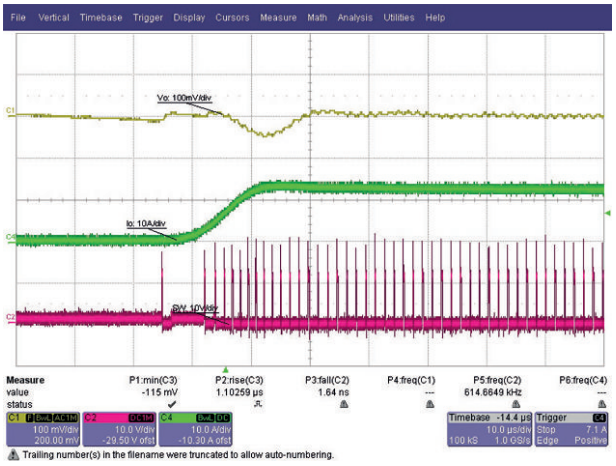

Fig. 29 - Load Step, 0.1 A to 12 A, 1 A/µs, t = 10 µs/div
Skip Mode Enabled

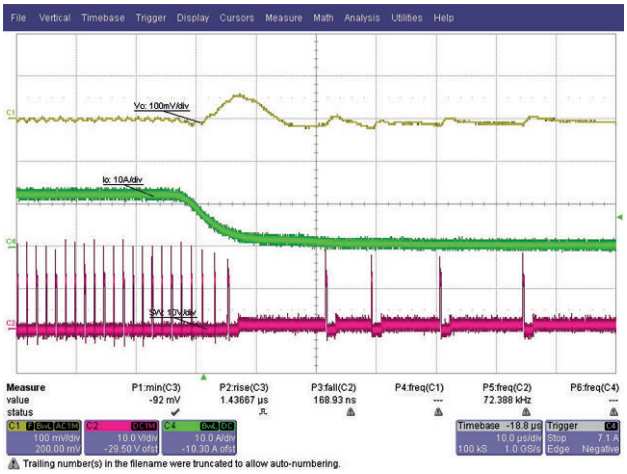

Fig. 32 - Load Release, 12 A to 0.1 A, 1 A/µs, t = 20 µs/div
Skip Mode Enabled

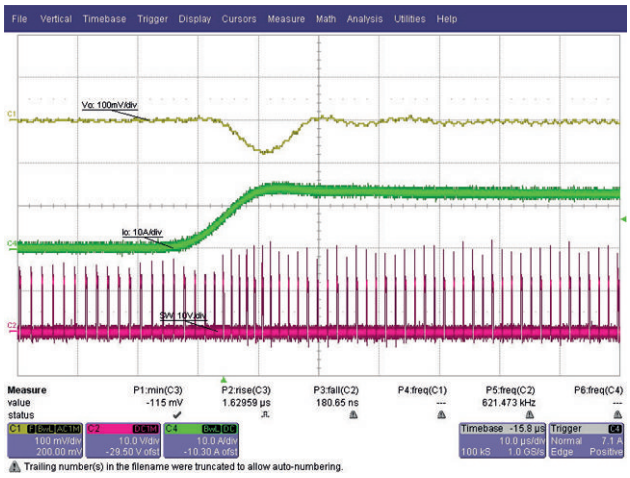

Fig. 30 - Load Step, 0.1 A to 12 A, 1 A/µs, t = 10 µs/div
Forced Continuous Conduction Mode

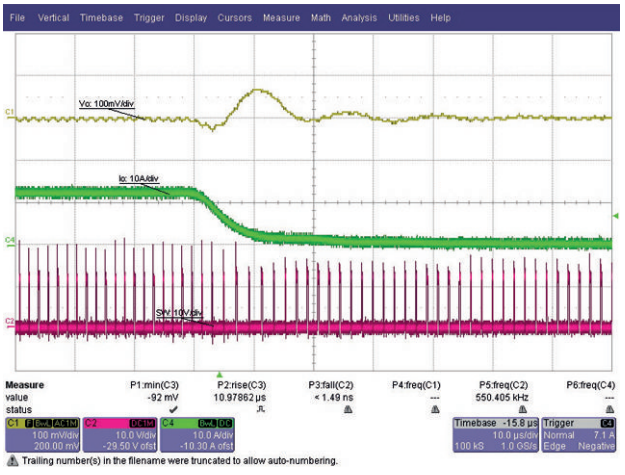

Fig. 33 - Load Release, 12 A to 0.1 A, 1 A/µs, t = 10 µs/div
Forced Continuous Conduction Mode

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ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, 25 A full load, f_{sw} = 600 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 2.2 µF x 3, unless otherwise noted)

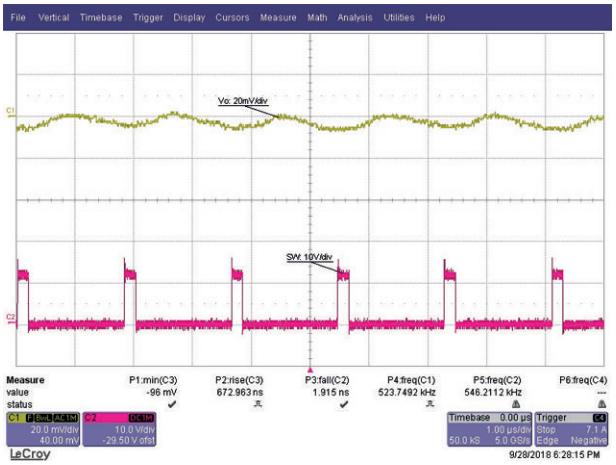

Fig. 34 - Output Ripple, 0.1 A, t = 1 µs/div
Forced Continuous Conduction Mode

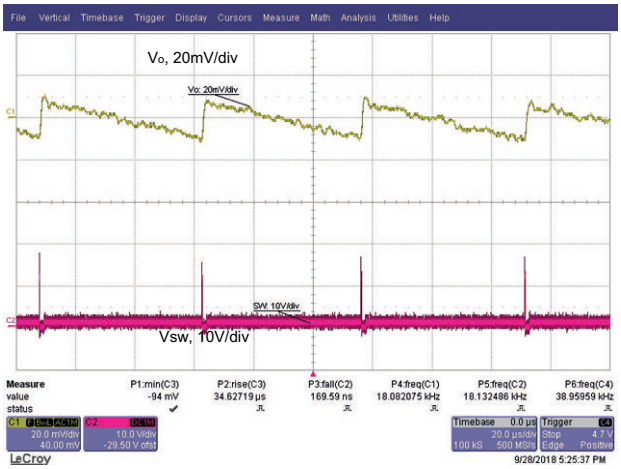

Fig. 35 - Output Ripple, 0.1 A, t = 20 µs/div
Skip Mode Enabled

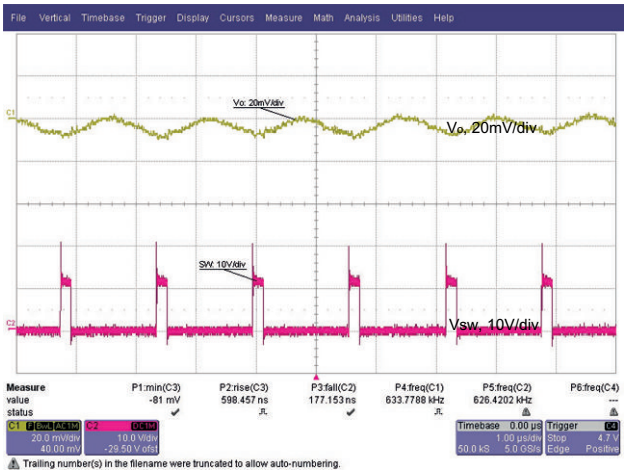

Fig. 36 - Output Ripple, 12 A, t = 1 µs/div
Forced Continuous Conduction Mode

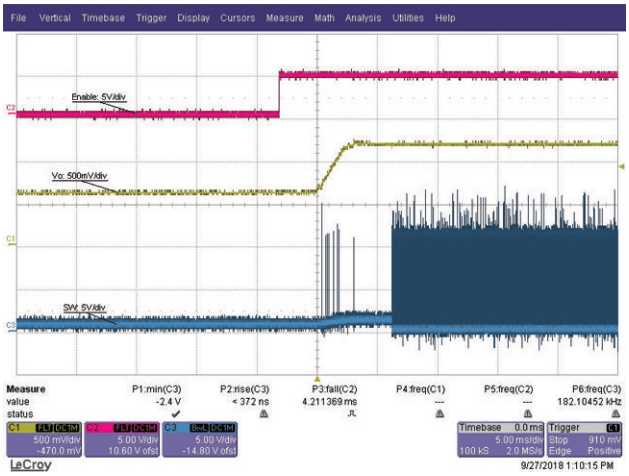

Fig. 37 - Prebias Start Up

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EXAMPLE SCHEMATIC

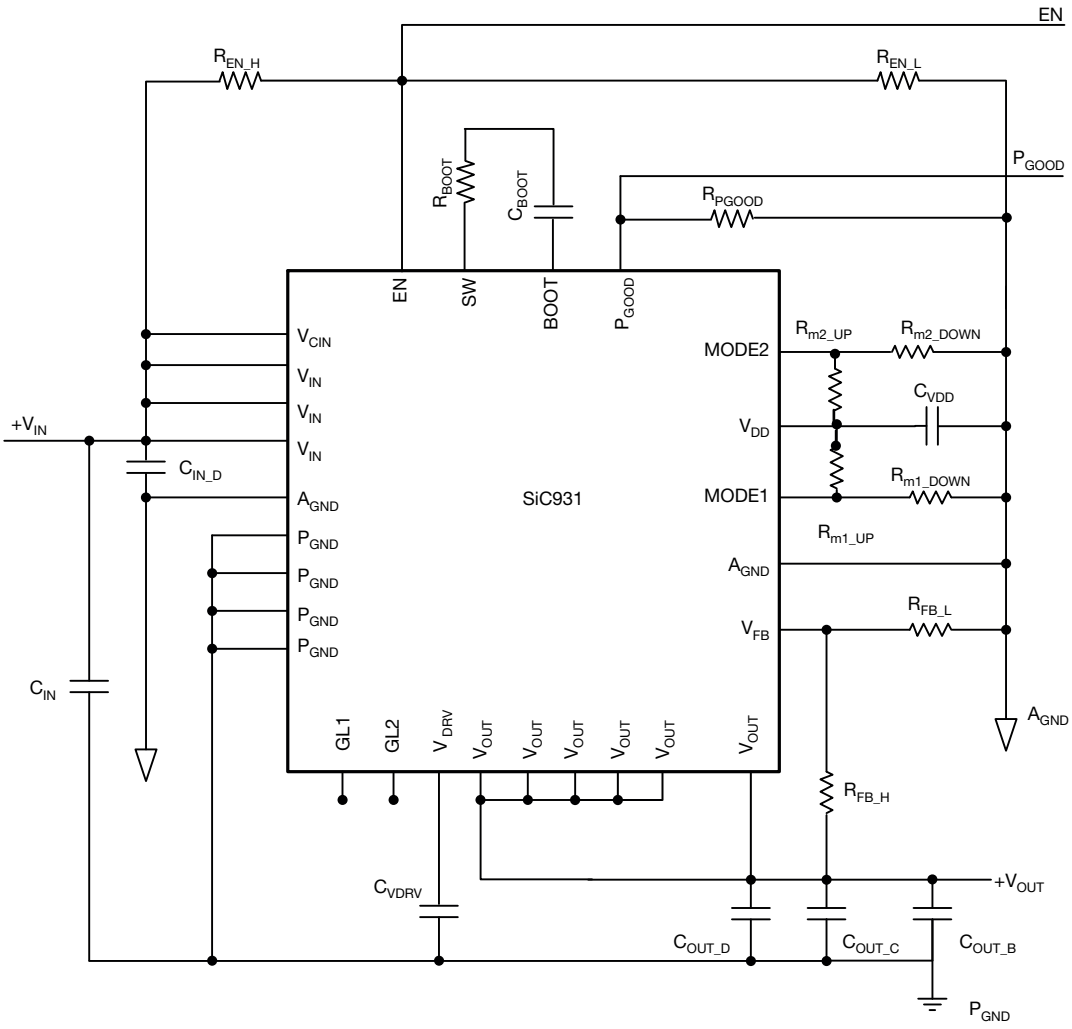

Fig. 38 - Application Schematic

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EXTERNAL COMPONENT SELECTION

This section explains external component selection for the SiC931 family of regulators. Component reference designators in any equation refer to the schematic shown in Fig. 38.

Output Voltage Adjustment

If a different output voltage is needed, simply change the value of V_{OUT} and solve for $R_{_FB_H}$ based on the following formula:

$$R_{_FB_H} = \frac{R_{_FB_L}(V_{OUT} - V_{FB})}{V_{FB}}$$

Where V_{FB} is 0.6 V for the SiC931. $R_{_FB_L}$ should be a maximum of 10 kΩ to prevent V_{OUT} from drifting at no load.

Capacitor Selection

The output capacitors are chosen based upon required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. A change in the output ripple voltage will lead to a change in DC voltage at the output.

For instance, the design goal for output voltage ripple is 3 % (45 mV for V_{OUT} = 1.5 V) with ripple current of 4.43 A. The maximum ESR value allowed is shown by the following equation.

$$ESR_{MAX.} = \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{45\ mV}{4.43\ A}$$

$$ESR_{MAX.} = 10.2\ m\Omega$$

The output capacitance is usually chosen to meet transient requirements. A worst-case load release (from maximum load to no load) at the moment of peak inductor current, determines the required capacitance. If the load release is instantaneous (maximum load to no load in less than 1 µs) the output capacitor must absorb all the inductor's stored energy. The output capacitor can be calculated according to the following equation.

$$C_{OUT_MIN.} = \frac{L_O(I_{OUT} + 0.5 \times I_{RIPPLE_{MAX.}})^2}{V_{PK}^2 - V_{OUT}^2}$$

Where I_{OUT} is the output current, $I_{RIPPLE_MAX.}$ is the maximum ripple current, V_{PK} is the peak V_{OUT} during load release, V_{OUT} is the output voltage. L_O is the internal output inductor of 220 nH.

The duration of the load release is determined by V_{OUT} and the inductor. During load release, the voltage across the inductor is approximately $-V_{OUT}$, causing a down-slope or falling di/dt in the inductor. If the di/dt of the load is not much larger than di/dt of the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor; therefore a smaller capacitance can be used.

Under this circumstance, the following equation can be used to calculate the needed capacitance for a given rate of load release (di_{LOAD}/dt).

$$C_{OUT} = \frac{\frac{L \times I_{PK}^2}{V_{OUT}} - (I_{PK} \times I_{RELEASE}) \times \frac{dT}{di_{LOAD}}}{2(V_{PK} - V_{OUT})}$$

$$I_{PK} = I_{RELEASE} + \left(\frac{1}{2} \times I_{RIPPLE_{MAX.}}\right)$$

Where I_{PK} is the peak inductor current, $I_{RIPPLE_MAX.}$ is the maximum peak to peak inductor current, $I_{RELEASE}$ is the maximum load release current, V_{PK} is the peak V_{OUT} during load release, di_{LOAD}/dt is the rate of load release.

If the load step does not meet the requirement, increasing the crossover frequency can help by adding feed forward capacitor (C_{FF}) in parallel to the upper feedback resistor to generate another zero and pole. Placing the geometrical mean of this pole and zero around the crossover frequency will result in faster transient response. f_Z and f_P are the generated zero and pole, see equations below.

$$f_Z = \frac{1}{2\pi \times R_{FB1} \times C_{FF}}$$

$$f_P = \frac{1}{2\pi \times (R_{FB1} \,//\, R_{FB2}) \times C_{FF}}$$

Where R_{FB1} is the upper feedback resistor, R_{FB2} is the lower feedback resistor C_{FF} is the feed forward capacitor, f_Z is the zero from feed forward capacitor, f_P is the pole frequency generated from the feed forward capacitor.

A calculator is available to assist user to obtain the value of the feed forward capacitance value.

From the calculator, obtain the crossover frequency (f_C). Use the equation below for the calculation of the feed forward capacitance value.

$$f_C = \sqrt{(f_Z \times f_P)}$$

$$C_{FF} = \frac{1}{2\pi \times (f_C \times \sqrt{(R_{FB1} \times (R_{FB1} \,//\, R_{FB2}))})}$$

As the internal RC compensation of the SiC931 works with a wide range of output LC filters, the SiC931 offers stable operation for a wide range of output capacitance, making the product versatile and usable in a wide range of applications.

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Input Capacitance

In order to determine the minimum capacitance the input voltage ripple needs to be specified; $V_{CINPKPK} \leq 500$ mV is a suitable starting point. This magnitude is determined by the final application specification. The input current needs to be determined for the lowest operating input voltage,

$$I_{CIN(RMS)} = I_O \times \sqrt{D \times (1 - D) + \frac{1}{12} \times \left(\frac{V_{OUT}}{L \times f_{sw} \times I_{OUT}}\right)^2 \times (1 - D)^2 \times D}$$

The minimum input capacitance can then be found,

$$C_{IN_min.} = I_{OUT} \times \frac{D \times (1 - D)}{V_{CINPKPK} \times f_{sw}}$$

If high ESR capacitors are used, it is good practice to also add low ESR ceramic capacitance. A 4.7 µF ceramic input capacitance is a suitable starting point.
Care must be taken to account for voltage derating of the capacitance when choosing an all ceramic input capacitance.

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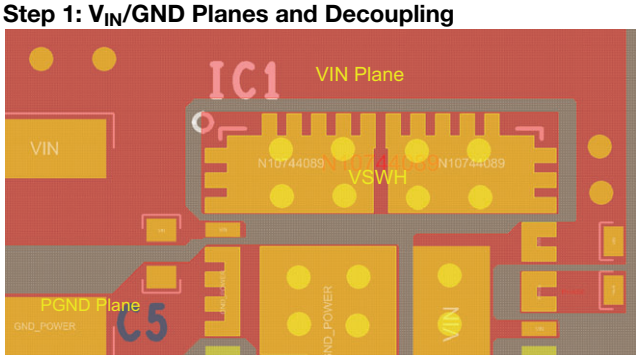
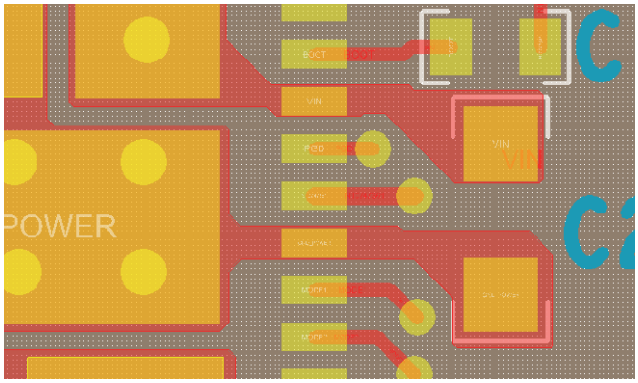
PCB LAYOUT RECOMMENDATIONS

Step 1: V_{IN}/GND Planes and Decoupling



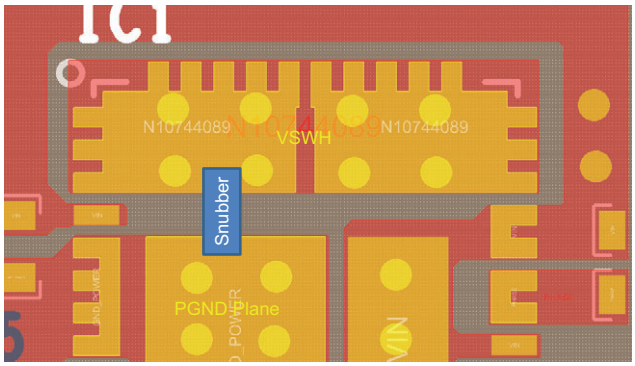
1. Layout V_{IN} and P_{GND} planes as shown above. V_{IN} can be fed from both sides to get better connection. VSWH is surrounded by V_{IN} plane, switching noise can be shielded
2. Ceramic capacitors should be placed right between V_{IN} and P_{GND}, and very close to the device for best decoupling effect
3. Difference values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210 + 0603
4. Smaller capacitance value, closer to device V_{IN} pin(s) –better high frequency noise absorbing

Step 2: V_{CIN} Pin



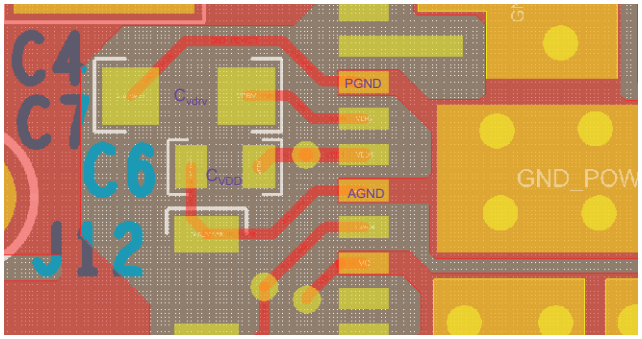
1. V_{CIN} (pin 40) is the input pin for both internal LDO and Ton block. t_{ON} time varies based on input voltage. It is necessary to have short connection to V_{IN} paddle

Step 3: VSWH Node



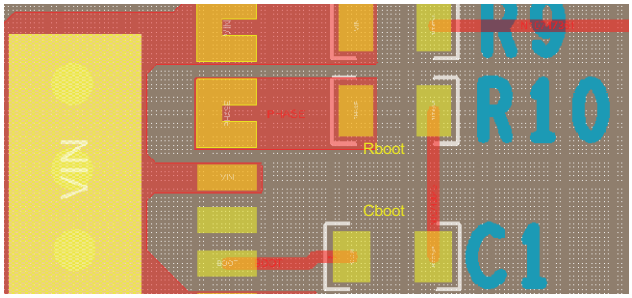
1. Switching node is located on the top of the package. If any snubber network is required, place the components on the bottom side as shown above

Step 4: V_{DD}/V_{DRV} Input Filter



1. C_{VDD} cap should be placed between pin13 and pin 14 (the A_{GND} of driver IC) to achieve best noise filtering
2. C_{VDRV} cap should be placed close to V_{DRV} (pin12) and P_{GND} (pin 11) to reduce effects of trace impedance and provide maximum instantaneous driver current for low side MOSFET during switching cycle

Step 5: BOOT Resistor and Capacitor Placement



1. These components need to be placed very close to SiC931, right between PHASE (pin 44, 45) and BOOT (pin 41)
2. In order to reduce parasitic inductance, it is recommended to use 0402 chip size for the resistor and the capacitor

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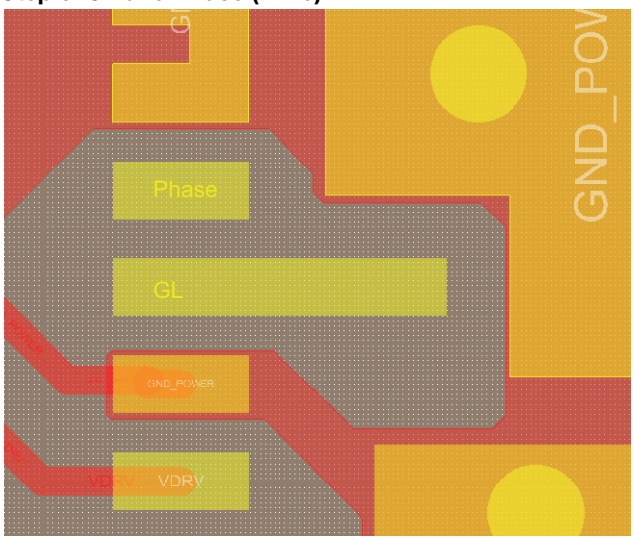
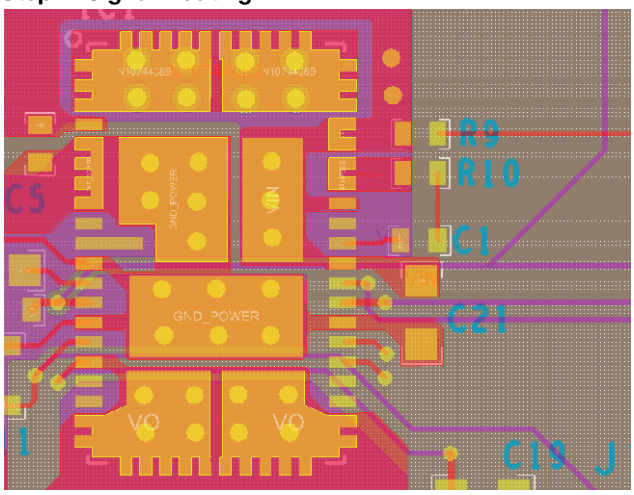
Step 6: GL and Phase (Pin 9)



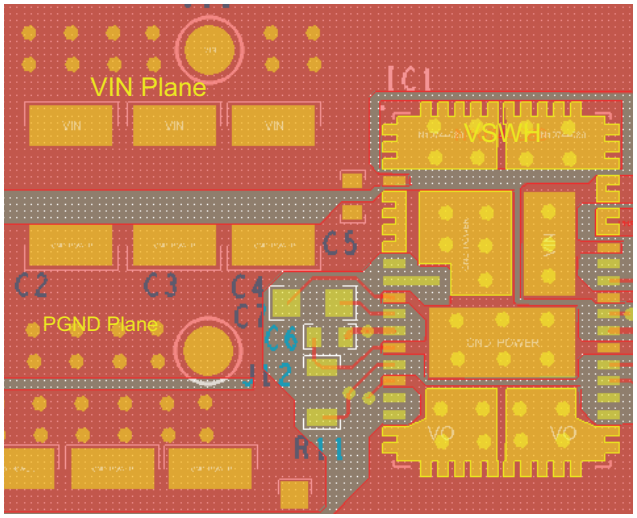
1. GL (pin10) and phase (pin 9) are located on the left side of the device and used for packing purpose. These 2 pins can be left floating

Step 7: Signal Routing



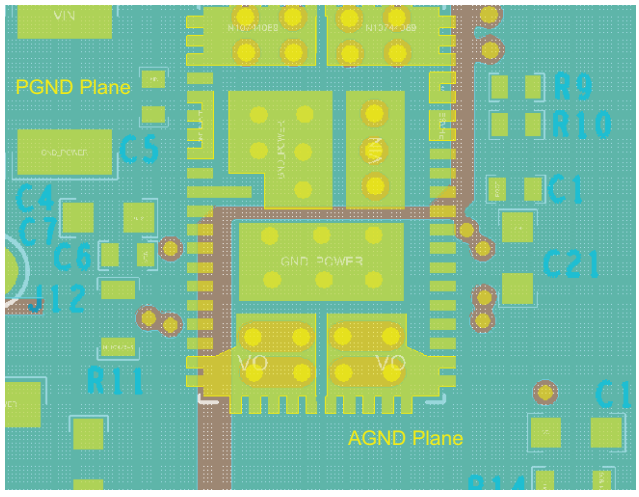
1. Separate the small analog signal from high current path. As shown above, the high current paths with high dv/dt, di/dt are placed on the top left side of the IC, while the small control signals are placed on the bottom right side of the IC. All the components for small analog signal should be placed closer to IC with minimum trace length
2. Pin 14 is considered as IC analog ground, which should have single connection to power ground
3. Output return signal can be routed through inner layer

Step 8: Adding thermal relief Vias and duplicate power path plane



1. Thermal relief Vias can be added on the V_{IN} and P_{GND} pads to utilize inner layers for high-current and thermal dissipation
2. To achieve better thermal performance, additional Vias can be put on V_{IN} and P_{GND} plane. It is also necessary to duplicate the V_{IN} and Ground Plane at bottom layer to maximize the power dissipation capability from PCB
3. 8 mil drill for pads and 10 mils drill for plane can be the optional Via size. The Vias on pad may drain solder during assembly and cause assembly issue. Please consult with the assembly house for guideline

Step 9: Ground Layer



1. It is recommended to make the whole inner 1 layer (next to Top layer) ground plane
2. This ground plane provides shielding between noise source on top layer and signal trace within inner layer
3. The ground plane can be broken into two section as P_{GND} and A_{GND}

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PRODUCT SUMMARY	
Part number	SiC931
Description	20 A, 4.5 V to 18 V input, 600 kHz, 1 MHz, 1.5 MHz, 2 MHz, synchronous buck regulator with power save mode and internal 5 V bias
Input voltage min. (V)	4.5
Input voltage max. (V)	18
Output voltage min. (V)	0.6
Output voltage max. (V)	5.5
Continuous current (A)	20
Switch frequency min. (kHz)	600
Switch frequency max. (kHz)	2000
Pre-bias operation (yes / no)	Yes
Internal bias reg. (yes / no)	Yes
Compensation	Internal
Enable (yes / no)	Yes
P_{GOOD} (yes / no)	Yes
Over current protection	Yes
Protection	OVP, OCP, UVP/SCP, OTP, UVLO
Light load mode	Power save
Peak efficiency (%)	95
Package type	PowerPAK MLP60-A6
Package size (W, L, H) (mm)	10.6 x 6.5 x 3
Status code	1
Product type	microBRICK® (step down regulator)
Applications	Computers, consumer, industrial, healthcare, networking

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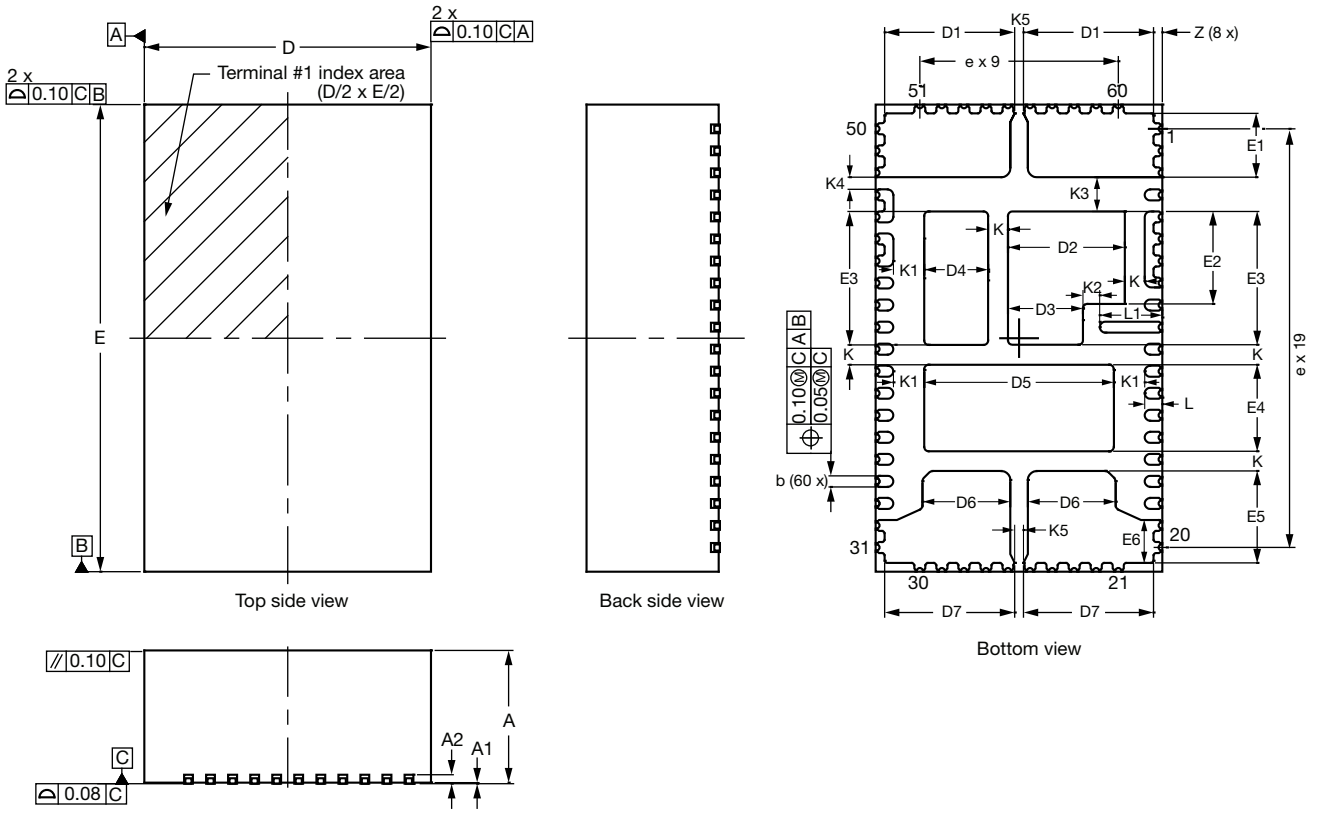
PowerPAK® MLP60-A6C Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	2.95	3.00	3.05	0.116	0.118	0.120
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 ref.			0.008 ref.		
b (4)	0.20	0.25	0.30	0.008	0.010	0.012
D	6.40	6.50	6.60	0.252	0.256	0.260
D1	2.85	2.95	3.05	0.112	0.116	0.120
D2	2.55	2.65	2.75	0.100	0.104	0.108
D3	1.60	1.70	1.80	0.063	0.067	0.071
D4	1.35	1.45	1.55	0.053	0.057	0.061
D5	4.20	4.30	4.40	0.165	0.169	0.173
D6	1.89	1.99	2.09	0.074	0.078	0.082
D7	2.85	2.95	3.05	0.112	0.116	0.120
E	10.50	10.60	10.70	0.413	0.417	0.421
E1	1.35	1.45	1.55	0.053	0.057	0.061
E2	2.00	2.10	2.20	0.079	0.083	0.087
E3	2.93	3.03	3.13	0.115	0.119	0.123
E4	1.86	1.96	2.06	0.073	0.077	0.081
E5	1.99	2.09	2.19	0.078	0.082	0.086
E6	0.88	0.98	1.08	0.035	0.039	0.043

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DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
K		0.45 ref.			0.018 ref.	
K1		0.70 ref.			0.028 ref.	
K2		0.38 ref.			0.015 ref.	
K3		0.78 ref.			0.031 ref.	
K4		0.28 ref.			0.011 ref.	
K5		0.20 ref.			0.008 ref.	
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	1.32	1.42	1.52	0.052	0.056	0.060
e		0.50 BSC			0.020 BSC	
Z		0.20 ref.			0.008 ref.	
ECN: T19-0039-Rev. B, 04-Mar-2019 DWG: 6072						

Notes

(1) Use millimeters as the primary measurement
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994
(3) N is the number of terminals, Nd is the number of terminals in x-direction, Ne is the number of terminals in y-direction
(4) Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
(5) The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
(6) Exact shape and size of this feature is optional
(7) Package warpage max. 0.08 mm
(8) Applied only for terminals

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