# CURRENT SENSE LATCH

# DESCRIPTION

This monolithic integrated circuit is an analog latch device with digital reset. It was specifically designed to provide pulse-by-pulse current limiting for switch-mode power supply systems, but many other applications are also feasible. Its function is to provide a latching switch action upon sensing an input threshold voltage, with reset accomplished by an external clock signal. This device can be interfaced directly with many kinds of pulse width modulating control IC's, including the SG1524, SG1525A, and SG1527A.

The input threshold for the latch circuit is 100mV, which can be referenced either to ground or to a wide-ranging positive voltage. There are high and low-going output signals available, and both the supply voltage and clock signal can be taken directly from an associated PWM control chip.

With delays in the range of 200 nanoseconds, this latch circuit is ideal for fast reaction sensing to provide overall current limiting, short circuit protection, or transformer saturation control.

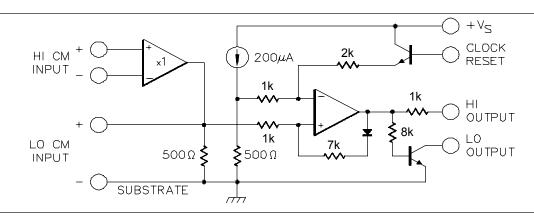
# **BLOCK DIAGRAM**

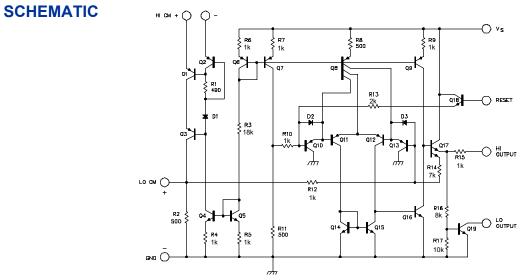
# **FEATURES**

- Current Sensing with 100mV Threshold
- Common-mode Input at Ground or to 40V
- Complementary Outputs
- Automatic Reset from PWM Clock
- 180ns Delay
- Interface Direct to SG1524, SG1525A, SG1527A

# **HIGH RELIABILITY FEATURES**

- Available To MIL-STD-883, ¶ 1.2.1
- Available to DSCC Standard Microcircuit Drawing (SMD)
- MSC-AMS Level "S" Processing Available
- Radiation Data Available







#### ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, V <sub>s</sub>	25V
HI CM Input Voltage	
LO Output "off" Voltage	
LO Output "on" current	

Note 1. Values beyond which damage may occur.

### **THERMAL DATA**

Y Package:
Thermal Resistance-Junction to Case, θ <sub>JC</sub> 50°C/W
Thermal Resistance-Junction to Ambient, $\theta_{IA}$ 130°C/W
M Package:
Thermal Resistance-Junction to Case, $\theta_{JC}$
Thermal Resistance-Junction to Ambient, $\theta_{IA}$
D Package:
Thermal Resistance-Junction to Ambient, $\theta_{JA}$ 120°C/W

#### **RECOMMENDED OPERATING CONDITIONS** (Note 2)

Input Supply Voltage, V <sub>s</sub>	5.0V
HI CM Input Voltage	
LO Output "off" Voltage	5V to 40V
LO Output "on" Current	. 0 to 10mA
Reset LO Voltage	

Note 2. Range over which the device is functional.

#### **ELECTRICAL CHARACTERISTICS**

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1549 with -55°C  $\leq$  T<sub>A</sub>  $\leq$  125°C, SG2549 with  $-25^{\circ}C \le T_{a} \le 85^{\circ}C$ , SG3549 with  $0^{\circ}C \le T_{a} \le 70^{\circ}C$ , and  $V_{s} = 5V$ . Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG	SG1549/2549			SG3549		
Farameter	Test conditions	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
Supply Section								
Supply Current	pply Current $V_{PIN 8} = 5V$ 2		3		2	5	mA	
	$V_{\text{PIN 8}} = 20 \text{V}$	V <sub>PIN 8</sub> = 20V 10 15			10	15	mA	
LO CM Input Section (Note 3	3)							
Threshold Voltage	Pin 1 & 2 shorted, $T_A = 25^{\circ}C$	80	100	120	80	100	120	mV
-	pin 1 & 2 shorted	70	100	130	70	100	130	mV
Input Impedance	$V_{PIN3} = 50 \text{mV}, T_A = 25^{\circ}\text{C}$	400	500	600	400	500	600	Ω
	$V_{PIN3} = 50 \text{mV}$	300	500	700	300	500	700	Ω
HI CM Input Section (Note 3	3)							
Threshold Voltage	$V_{CM} = 2V$ , Pin 3 open, $T_{A} = 25^{\circ}C$	80	100	120	80	100	120	mV
	$V_{CM} = 2V$ , Pin 3 open, $T_A = 25^{\circ}C$ $V_{CM} = 40V$ , Pin 3 open, $T_A = 25^{\circ}C$	80	100	120	80	100	120	mV
	V <sub>CM</sub> = 2V, Pin 3 open	70	100	130	70	100	130	mV
	V <sub>CM</sub> = 40V, Pin 3 open	70	100	130	70	100	130	mV
Input Current	$V_{PIN1} = V_{PIN2} = 40V$					200	300	μΑ
Clock Reset Section								
Min. Trigger Voltage			2.0	2.5		2.0	2.5	V
Input Current	$V_{PIN7} = 4V$		20	40		20	40	μA

Note 3. Input threshold voltages and supply current are directly proportional to supply voltage,  $V_s$ .

# Hermetic (Y Package) ..... 150°C

**Operating Junction Temperature** 

Plastic (N Package)150°C	
Storage Temperature Range65°C to 150°C	
RoHS Peak Package Solder Reflow Temp (40 sec. max. exp.) 260°C (+0, -5)	

Note A. Junction Temperature Calculation:  $T_{_J} = T_{_A} + (P_{_D} \ x \ \theta_{_{JA}}).$  Note B. The above numbers for  $\theta_{_{JC}}$  are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The  $\,\theta_{_{J\!A}}$  numbers are meant to be guidelines for the thermal performance of the device/pcboard system. All of the above assume no ambient airflow.

Reset HI Voltage	2.5V to 5.0V
Operating Ambient Temperature Range	
SG1549Y	-55°C to 125°C
SG2549D or M	25°C to 85°C
SG3549D or M	0°C to 70°C



#### ELECTRICAL CHARACTERISTICS (Continued)

 $(V_{c} = 5V, and over recommended operating temperature, unless otherwise specified.)$ 

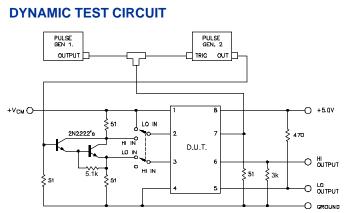
Parameter	Test Conditions	SG1549/2549			SG3549			Units
Falameter	Test conditions		Тур.	Max.	Min.	Тур.	Max.	Units
HI Output Section	HI Output Section							
Off Voltage			0	0.1		0	0.1	V
On Voltage	I <sub>L</sub> = 1mA	2.8	3.2		2.8	3.2		V
LO Output								
Off Leakage	$V_{PIN5} = 40V$		.01	1.0		.01	1.0	μΑ
On Voltage	I_=5mA		.3	0.5		.3	0.5	V

# TYPICAL SWITCHING CHARACTERISTICS (Note 4)

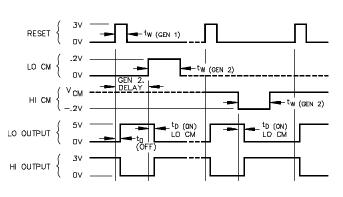
 $(V_{S} = 5V, T_{A} = 25^{\circ}C)$ 

Parameter	Test Conditions		SG1549 Series			
Falalletei			Тур.	Max.	Units	
Reset Minimum Pulse Width (T <sub>w1</sub> )	Amplitude = 3.0V		150	300	ns	
Delay from Reset to LO Output (T <sub>D(OFF)</sub> )	$R_1 = 470\Omega$ to $V_s$		300	600	ns	
LO Input Minimum Pulse Width (T <sub>w2</sub> )	LO CM Amplitude = 200mV		50	300	ns	
Delay from LO Input to LO Output (T <sub>D(ON)</sub> )	LO CM Amplitude = 200mV, $R_1 = 470\Omega$ to $V_s$		180	360	ns	
Delay from HI Input to LO Output (T	Amplitude = 200mV, $V_{CM} = 5V$		300	900	ns	
Delay from HI Output to LO Output	LO CM Input = 200mV		30	60	ns	

Note 4: These parameters, although guaranteed, are not tested in production.



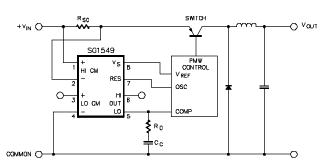
## **SWITCHING WAVEFORMS**

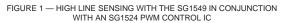


#### **APPLICATION NOTES**

HIGH LINE SENSING - The SG1549 will provide current sensing in the positive supply line in the typical SG1524 single-ended switching regulator application shown in Figure 1. The HI CM sense circuitry can be used with input voltages between 2 and 40 volts.

A value for R<sub>sc</sub> is determined by dividing the 100mV input threshold by the peak current desired. High-frequency noise, or switching transients, can usually be eliminated by a small capacitor between pins 3 and 4. Current control may be accomplished by either the HI OUTPUT pin connected to the SG1524's Shutdown pin, or the LO OUTPUT pin connected directly to the Compensation Terminal. In either case, activation of the current sense latch will tend to discharge the compensation capacitor, C<sub>c</sub>, which may cause slow recovery from pulse limiting. If this feature is desired, the LO OUTPUT pin may be used to discharge a soft-start network instead of coupling directly to the SG1524. If it is not desired, the use of a small value of  $C_c$ , and perhaps a diode across  $R_c$ , will enhance recovery.







#### APPLICATION NOTES (continued)

Another method of introducing the current shutdown signal is shown in Figure 2 where the SG1524 is used to activate a constant drive current to the high-current switch, in this case an SM600. The 2N2222 forms a constant current generator when driven from the SG1524's 5.0 volt reference through a 1k resistor. This transistor is then switched off by the LO OUTPUT transistor in the SG1549, achieving the fastest response to the output of the regulator.

**LOW LINE SENSING -** In many types of feed-forward or push-pull converters, current protection may be provided by sensing in an emitter resistor referenced to ground on the primary side of an output transformer. The fast-reacting SG1549 can easily sense secondary overload as reflected back to the primary and, additionally, provide protection from unbalanced transformer saturation.

When using the LO CM inputs, the HI CM inputs should be shorted together. While the LO CM inputs may be connected directly across a sense resistor,  $R_{sc}$ , a small low-pass filter as shown in Figure 3 is often required to eliminate high frequency transients. It must be remembered that the  $500\Omega$  input impedance at the LO CM terminals will cause the use of R1 to increase the effective threshold; however, this also offers the possibility of an easily adjustable threshold by incorporating a potentiometer at the input.

Coupling the output signal from the SG1549 to the control chip may be done in several ways including the use of either the Compensation or Shutdown pins on the SG1524 as described earlier.

Another convenient way to tie the output of the SG1549 into the PWM control in higher power applications is by using the SG1627 Dual Interface Driver and connecting the LO OUTPUT terminal of the

SG1549 directly to the two Non-Inverting inputs of the SG1627 as shown in Figure 4.

And finally, keep in mind that the LO OUTPUT terminal of the SG1549 will easily drive most high-speed optical couplers should some type of isolation between current sense and shutdown control be required.

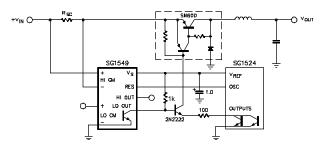
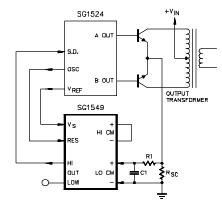


FIGURE 2 — CURRENT CONTROL FOR A BUCK REGULATOR WITH CONSTANT DRIVE CURRENT





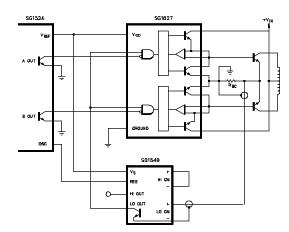


FIGURE 4 — POWER BOOST AND CURRENT CONTROL WITH THE SG1627



#### CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
	SG1549Y-883B	-55°C to 125°C	
8-PIN CERAMIC DIP	SG1549Y-DESC	-55°C to 125°C	
Y - PACKAGE	SG1549Y	-55°C to 125°C	
8-PIN PLASTIC DIP	SG2549M	-25°C to 85°C	+ LO CM INPUT ☐ 3 6 ☐ HI OUTPUT — LO CM INPUT ☐ 4 5 ☐ LO OUTPUT
M - PACKAGE	SG3549M	0°C to 70°C	M Package: RoHS / Pb-free 100% Matte Tin Lead Finish M Package: RoHS Compliant / Pb-free Transition DC: 0503
	SG2549D	-25°C to 85°C	N.C. + HI CM INPUT 2 13 +VS - HI CM INPUT 3 12 CLOCK RESET + LO CM INPUT 4 11 HI OUTPUT - LO CM INPUT 5 10 LO OUTPUT
14-PIN SOIC D - PACKAGE	SG3549D	0°C to 70°C	N.C. N.C. N.C. N.C. Top View D Package: 0440 RoHS / Pb-free 100% Matte Tin Lead Finish

Note 1. Contact factory for DESC product availability.

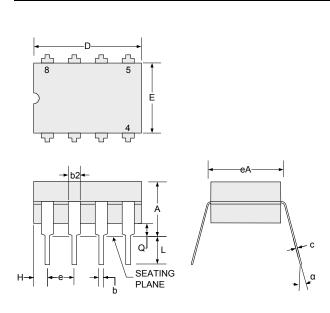
Note 2. All parts are viewed from the top.

Note 3. Hermetic Y Package uses Pb37/Sn63 hot solder dip lead finish, contact factory for availability of a RoHS version.



## PACKAGE OUTLINE DIMENSIONS

Controlling dimensions are in inches, metric equivalents are shown for general information.

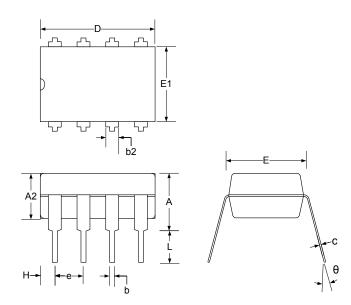


DIM	MILLIM	ETERS	INCHES		
DIN	MIN	MAX	MIN	MAX	
Α	4.32	5.08	0.170	0.200	
b	0.38	0.51	0.015	0.020	
b2	1.04	1.65	0.045	0.065	
С	0.20	0.38	0.008	0.015	
D	9.52	10.29	0.375	0.405	
E	5.59	7.11	0.220	0.280	
е	2.54 BSC		0.10	) BSC	
eA	7.37	7.87	0.290	0.310	
Н	0.63	1.78	0.025	0.070	
L	3.18	4.06	0.125	0.160	
α	-	15°	-	15°	
Q	0.51	1.02	0.020	0.040	

#### Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 5 - Y 8-Pin CERDIP Package Dimensions



DIM	MILLIM	IETERS	INC	HES
DIN	MIN	MAX	MIN	MAX
Α	-	5.08	-	0.200
A2	3.30	Тур.	1.30	Тур.
b	0.38	0.51	0.145	0.020
b2	0.76	1.65	0.030	0.065
с	0.20	0.38	0.008	0.015
D	-	10.16	-	0.400
E	7.62 BSC		0.300	BSC
е	2.54	BSC	0.100	BSC
E1	6.10	6.86	0.240	0.270
L	3.05	-	0.120	-
θ	0°	15°	0°	15°

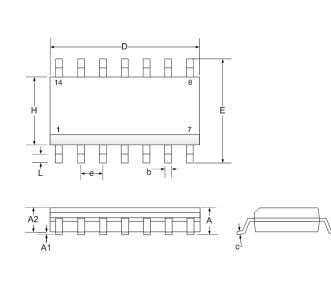
#### Note:

Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.





# PACKAGE OUTLINE DIMENSIONS (continued)



DIM	MILLIM	ETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	1.35	1.75	0.053	0.069	
A1	0.10	0.25	0.004	0.010	
A2	1.25	1.52	0.049	0.060	
b	0.33	0.51	0.013	0.020	
С	0.19	0.25	0.007	0.010	
D	8.54	8.74	0.336	0.344	
E	5.79	6.20	0.228	0.244	
е	1.27	BSC	0.050	) BSC	
Н	3.81	4.01	0.150	0.158	
L	0.40	1.27	0.016	0.050	
θ	0°	8°	0°	8°	
*LC	-	0.010	-	0.004	

\*Lead Co-planarity

#### Note:

Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage



θ



#### Microsemi Corporate Headquarters One Enterprise, Aliso Viejo, CA 92656 USA

Within the USA: +1 (800) 713-4113 Outside the USA: +1 (949) 380-6100 Sales: +1 (949) 380-6136 Fax: +1 (949) 215-4996

#### E-mail: sales.support@microsemi.com

© 2015 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi Corporation (MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,600 employees globally. Learn more at www.microsemi.com.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.