6A, 2MHz, High Efficiency Synchronous Step-Down Converter

General Description

The RT8073 is a high efficiency PWM step-down converter and capable of delivering 6A output current over a wide input voltage range from 2.9V to 5.5V.

The RT8073 provides accurate regulation for a variety of loads with an ±1% reference voltage at room temperature. For reducing inductor size, it provides up to 2MHz switching frequency. The efficiency is maximized through the integrated 50mΩ for high side, 35mΩ for low side MOSFETs and 250μA typical supply current.

The RT8073 features over current protection, frequency fold back function in shorted circuit, hiccup mode under voltage protection and over temperature protection.

The RT8073 is available in SOP-8 (Exposed Pad) and WDFN-12L 3x3 packages.

Ordering Information

RT8073□□

- Package Type
  - SP : SOP-8 (Exposed Pad-Option 2)
  - QW : WDFN-12L 3x3 (W-Type) (Exposed Pad-Option 1)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

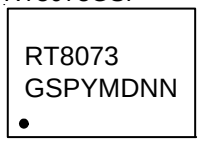
- **Integrated 50mΩ and 35mΩ MOSFETs**
- **6A Output Current**
- **High Efficiency Up to 95%**
- **2.9V to 5.5V Input Range**
- **Adjustable PWM Frequency : 300kHz to 2MHz**
- **0.8V ±1% Reference Voltage**
- **Adjustable External Soft-Start**
- **Power Good Indicator (WDFN-12L 3x3 only)**
- **Over Current Protection**
- **Under Voltage Protection**
- **Over Temperature Protection**
- **SOP-8 (Exposed Pad) and 12-Lead WDFN Packages**
- **RoHS Compliant and Halogen Free**

Applications

- Low Voltage, High Density Power Systems
- Distributed Power Systems
- Point-of-Load Conversions

Marking Information

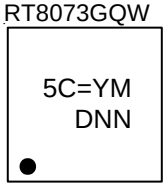
RT8073GSP



RT8073GSP : Product Number

YMDNN : Date Code

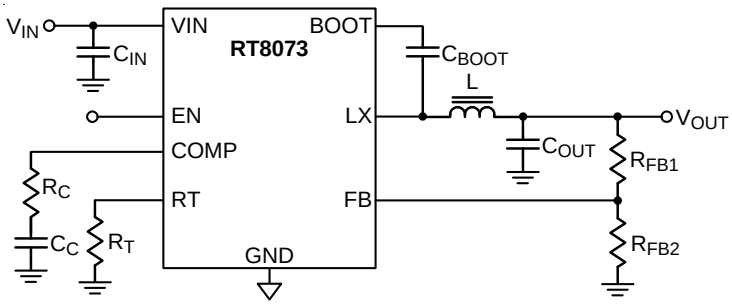
RT8073GQW



5C= : Product Code

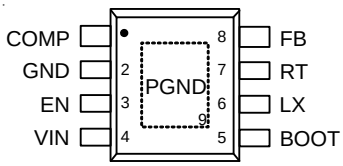
YMDNN : Date Code

Simplified Application Circuit

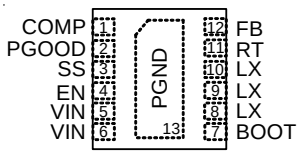


Pin Configuration

(TOP VIEW)



SOP-8 (Exposed Pad)



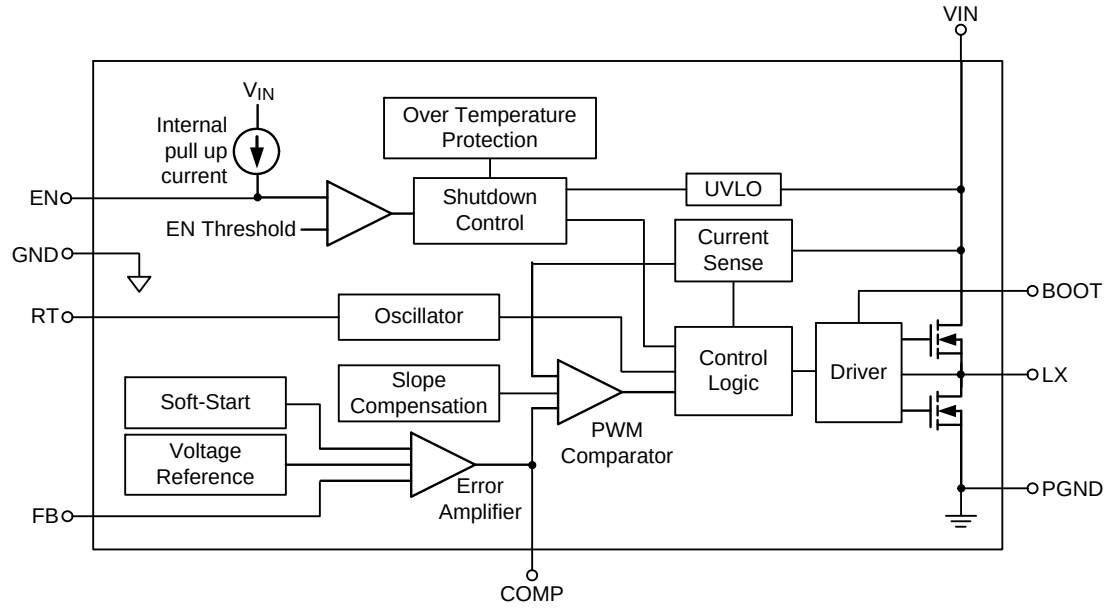
WDFN-12L 3x3

Functional Pin Description

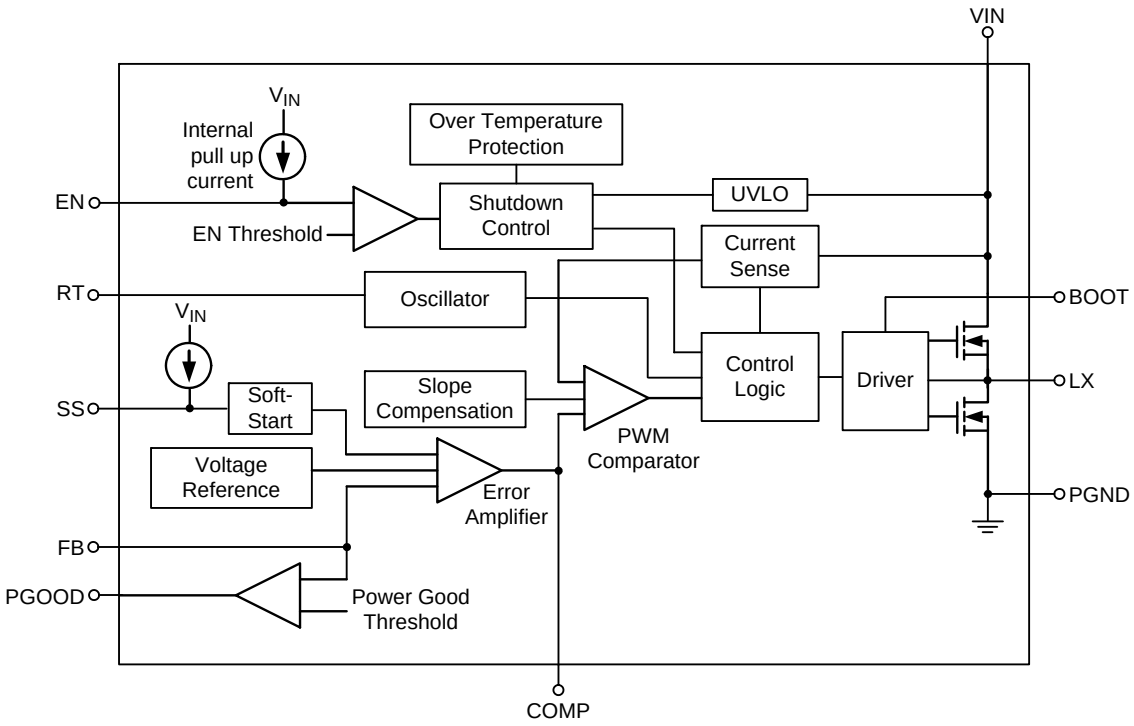
Pin No.		Pin Name	Pin Function
SOP-8 (Exposed Pad)	WDFN-12L 3x3		
1	1	COMP	Compensation Node.
2	--	GND	Analog Ground.
3	4	EN	Chip Enable. Externally pulled high to enable and pulled low to disable this chip, and it is internally pulled up to high when the pin is floating.
4	5, 6	VIN	Power Input.
5	7	BOOT	Bootstrap Supply for High Side Gate Driver.
6	8, 9, 10	LX	Switch Node.
7	11	RT	Frequency Setting.
8	12	FB	Feedback Voltage Input.
9	13 (Exposed Pad)	PGND	Power Ground. The exposed pad must be shouldered to a large PCB and connected to PGND for maximum power dissipation.
--	2	PGOOD	Power Good Indicator with Open Drain Output. It is high impedance when the output voltage is regulated. It is internally pulled low when the chip is shutdown, thermal shutdown or VIN is under UVLO threshold.
--	3	SS	Soft-Start Control.

Functional Block Diagram

For SOP-8 (Exposed Pad) Package



For WDFN-12L 3x3 Package



Operation

The RT8073 is a current mode synchronous step-down DC/DC converter with two integrated power MOSFETs. It can deliver up to 6A output current from a 2.9V to 5.5V input supply. The RT8073's current mode architecture allows the transient response to be optimized over a wide input voltage and load range. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up.

Error Amplifier

The error amplifier adjusts COMP voltage by comparing the feedback signal (V_{FB}) from the output voltage with the internal 0.8V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, the COMP voltage then rises to allow higher inductor current to match the load current.

Oscillator (OSC)

The frequency of the oscillator is adjustable by an external resistor connected between the RT pin and GND. The available switching frequency range is from 300kHz to 2MHz.

PGOOD Comparator

When the feedback voltage (V_{FB}) rises above 94% or falls below 106% of reference voltage, the PGOOD open drain output will be high impedance. The PGOOD open drain output will be internally pulled low when the feedback voltage (V_{FB}) falls below 90% or rises above 110% of reference voltage.

Soft-Start (SS)

An internal current source charges an external capacitor to build the soft-start ramp voltage (V_{SS}). The V_{FB} voltage will track the V_{SS} during soft-start interval. The chip will use internal soft-start if the SS pin is floating. The nominal internal soft-start time is 800µs.

Over Temperature Protection (OTP)

The RT8073 implements an internal over temperature protection. When junction temperature is higher than 165°C, it will stop switching operation. Once the junction temperature decreases below 145°C, the RT8073 will automatically resume switching.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 6.5V
- BOOT to LX ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to (V_{IN} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 2.041W
  WDFN-12L 3x3 ---------- 1.667W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 49°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
  WDFN-12L 3x3, θ_{JA} ---------- 60°C/W
  WDFN-12L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 2.9V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, C_{IN} = 10µF, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply							
Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	--	2.6	2.8	V
Quiescent Current		I_Q	Active, V_{FB} = 0.9V, Not switching	--	250	--	µA
Shutdown Current		I_{SHDN}		--	2	5	µA
Voltage Reference							
Voltage Reference		V_{REF}		0.792	0.8	0.808	V
Enable							
EN Input Voltage	Logic-High	V_{IH}		1.5	--	5.5	V
	Logic-Low	V_{IL}		--	--	0.4	
Switching Frequency Setting							
Switching Frequency		f_{OSC}		300	--	2000	kHz
			R_T = 28.7kΩ	--	1400	--	
			RT pin is floating	--	300	--	
Minimum On-Time				--	80	--	ns
Minimum Off-Time				--	60	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
MOSFET						
High Side MOSFET On-resistance		V_{IN} = 5V, BOOT – LX = 5V	--	50	--	mΩ
Low Side MOSFET On-resistance		V_{IN} = 5V	--	35	--	mΩ
Current Limit						
Current Limit Threshold			7	9	--	A
Power Good						
Power Good Range (WDFN-12L 3x3 only)		V_{FB} Rising (Good)	--	94	--	% V_{REF}
		V_{FB} Falling (Fault)	--	90	--	
		V_{FB} Rising (Fault)	--	110	--	
		V_{FB} Falling (Good)	--	106	--	
Over Temperature Protection						
Thermal Shutdown		Rising	--	165	--	°C
Thermal Shutdown Hysteresis			--	20	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

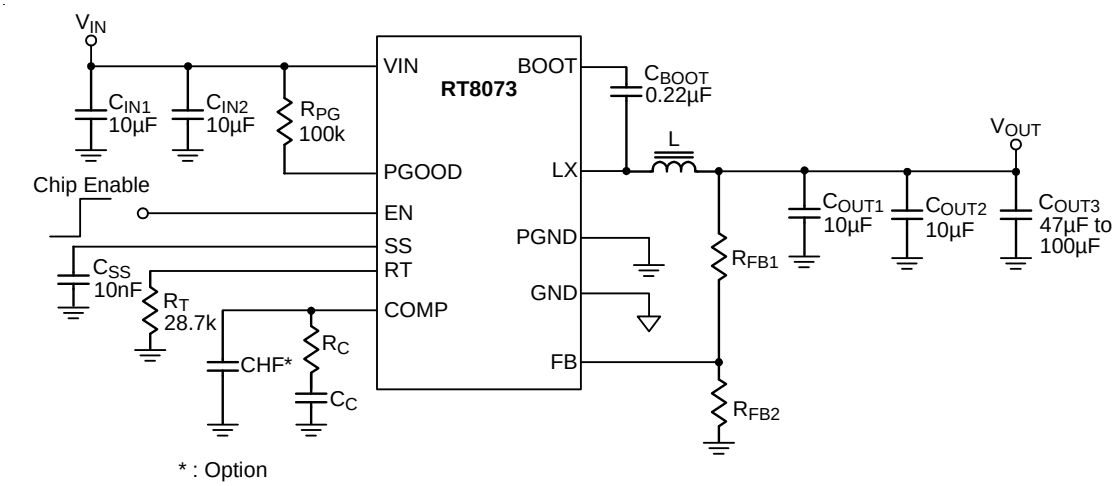
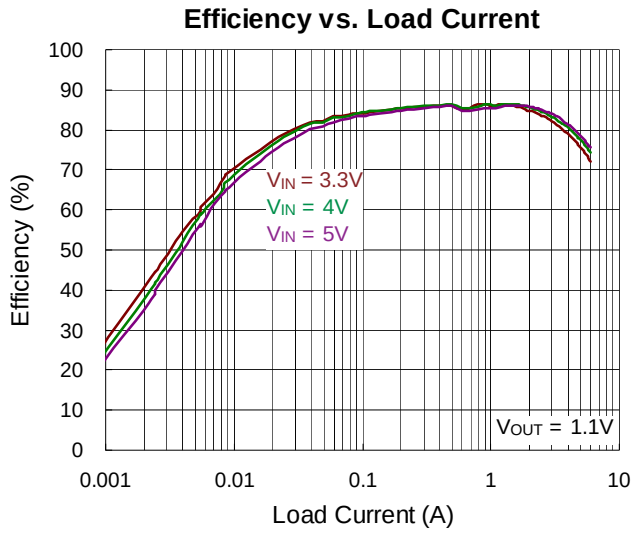
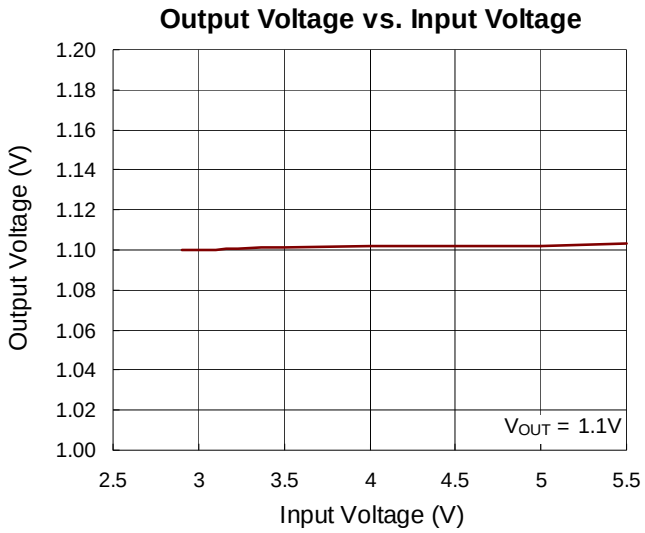


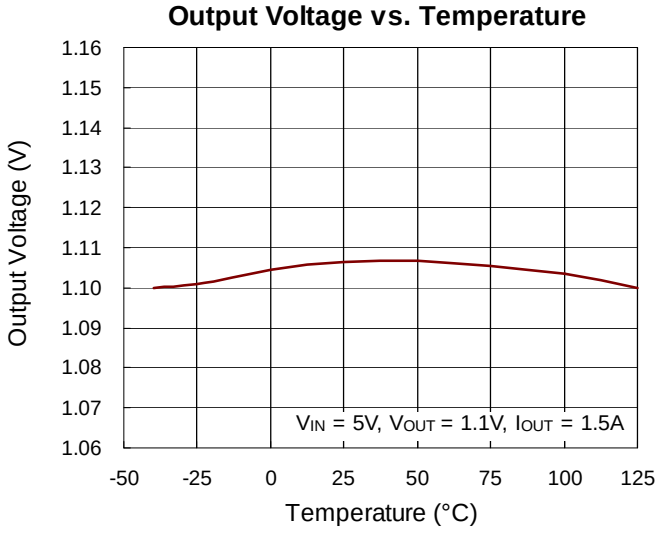
Table 1. Recommended Component Selection

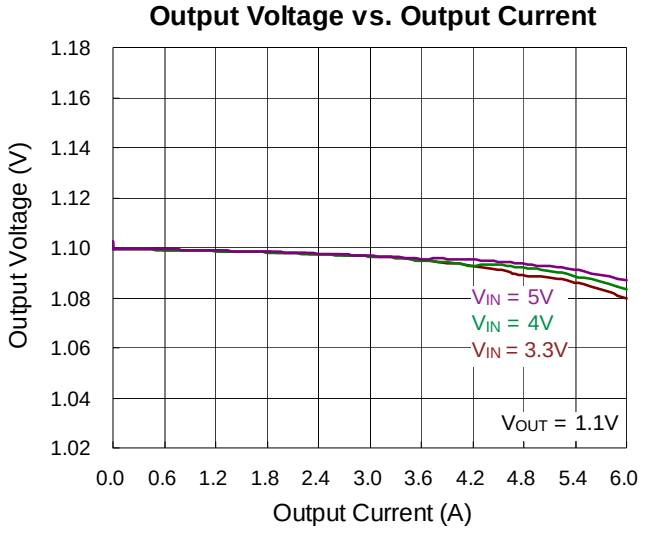
V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	R_C (kΩ)	C_C (nF)	L (µH)	C_{OUT}
3.3	3.75	1.2	33	0.33	0.47	Cer. 20µF + E-Cap 100µF
2.5	2.55	1.2	24	0.47	0.47	Cer. 20µF + E-Cap 100µF
1.8	1.5	1.2	18	0.56	0.47	Cer. 20µF + E-Cap 100µF
1.5	1.05	1.2	15	0.68	0.33	Cer. 20µF + E-Cap 100µF
1.2	2.55	5.1	12	1	0.33	Cer. 20µF + E-Cap 100µF
1	1.27	5.1	10	1	0.33	Cer. 20µF + E-Cap 100µF

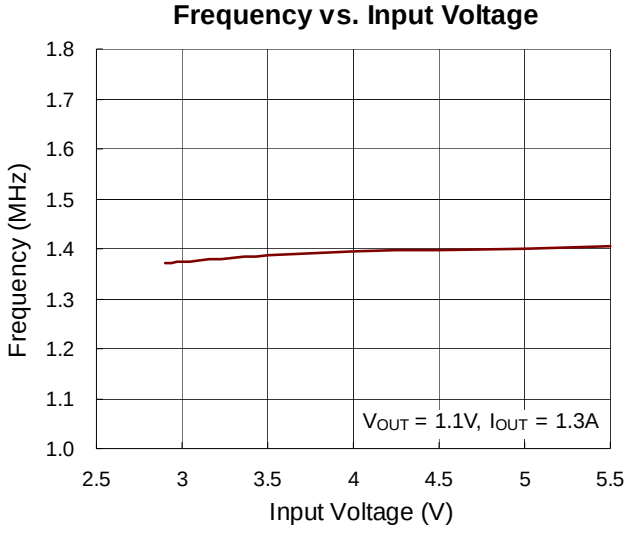
Typical Operating Characteristics

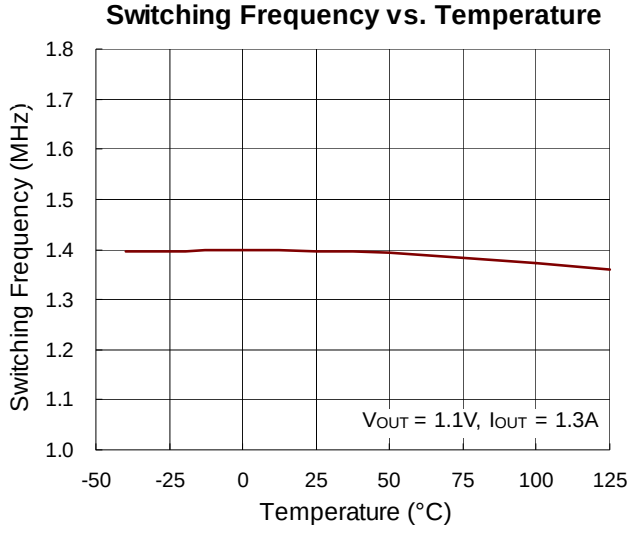




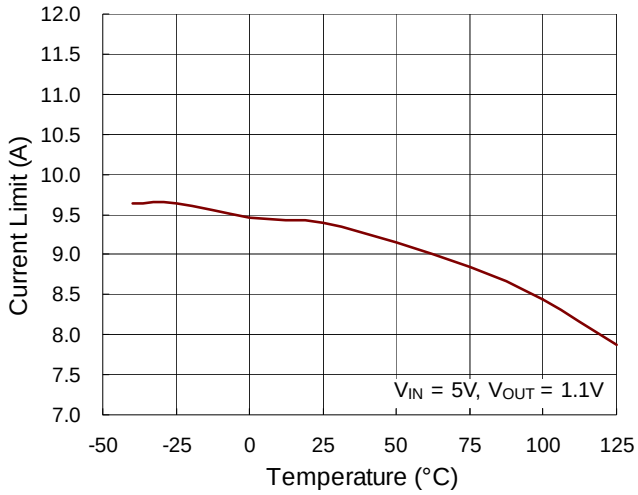




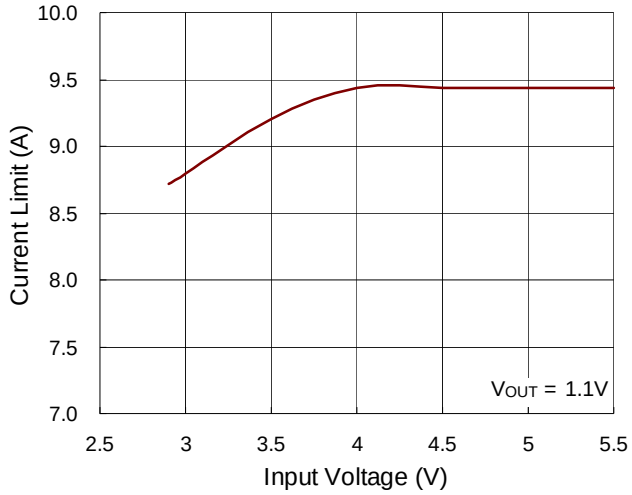




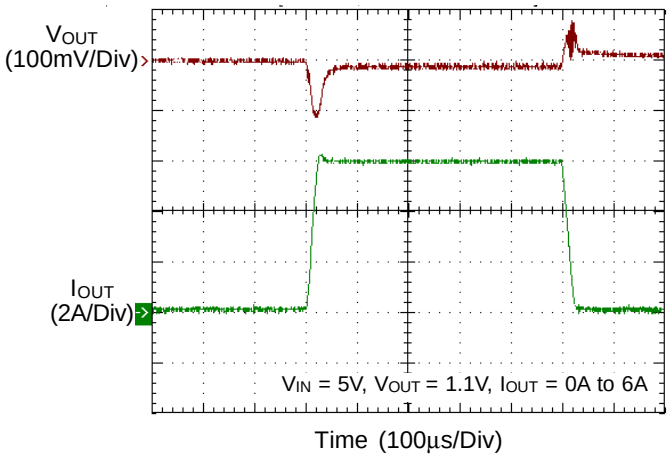
Current Limit vs. Temperature



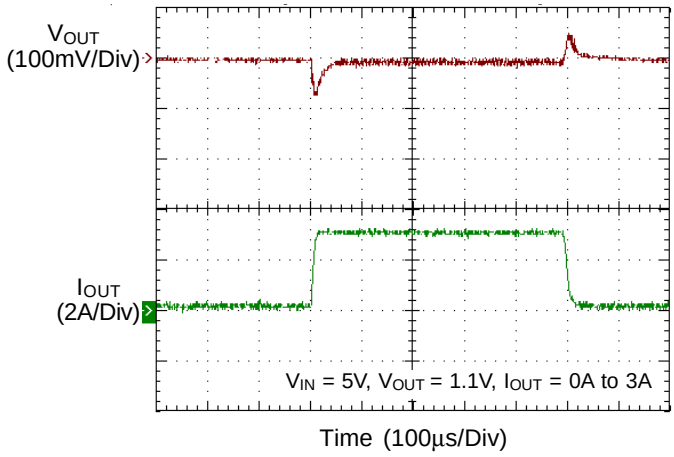
Current Limit vs. Input Voltage



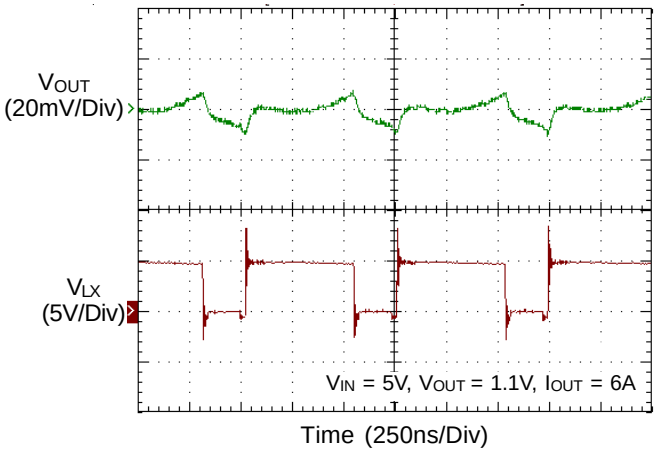
Load Transient Response



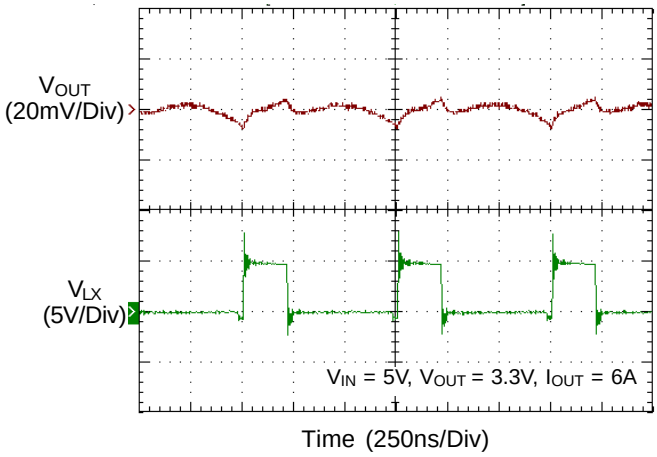
Load Transient Response



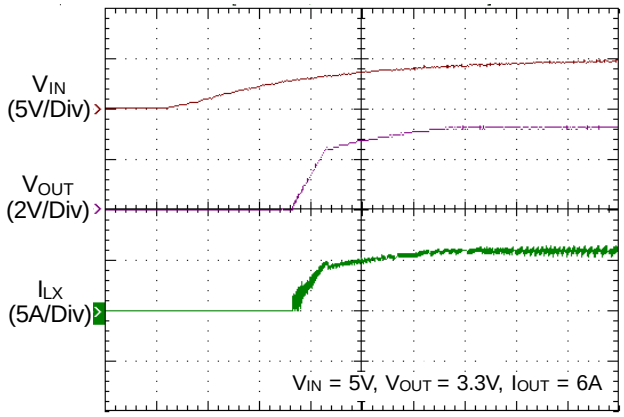
Output Ripple Voltage



Output Ripple Voltage

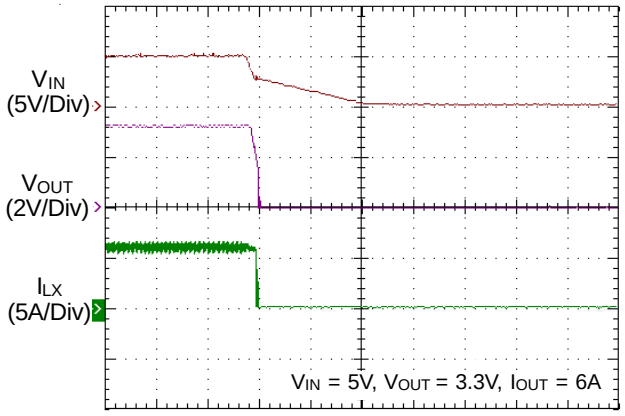


Power On from VIN



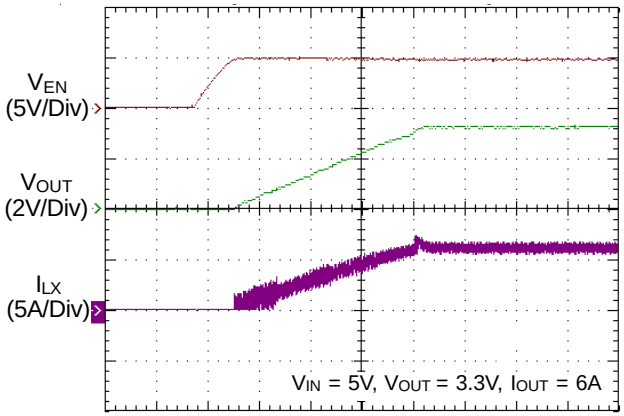
Time (1ms/Div)

Power Off from VIN



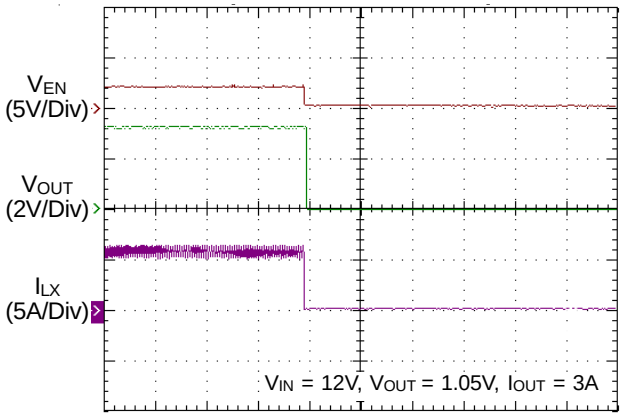
Time (10ms/Div)

Power On from EN



Time (250µs/Div)

Power Off from EN



Time (10ms/Div)

Application Information

The basic RT8073 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where V_{REF} equals to 0.8V (typical)

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

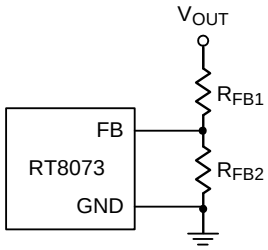


Figure 1. Setting the Output Voltage

Soft-Start (SS)

An internal current source charges an external capacitor to build the soft-start ramp voltage (V_{SS}). The V_{FB} voltage will track the V_{SS} during soft-start interval. The chip will use internal soft-start if the SS pin is floating. The nominal internal soft-start time is 800µs.

With external soft-start, the typical soft-start time can be calculated as following equation :

t_{SS} (ms) = 0.1 x C_{SS} (nF)

For example, if C_{SS} = 10nF, the soft-start time is 1ms.

Operating Frequency

Selection of the operating frequency is a tradeoff between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequency improves efficiency by reducing internal gate charge and switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The operating frequency of the RT8073 is determined by an external resistor that is connected between the SHDN/RT pin and GND. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator. The RT resistor value can be determined by examining the frequency vs. RT curve. Although frequency as high as 2MHz is possible, the minimum on-time of the RT8073 imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 80ns. Therefore, the minimum duty cycle is equal to 100 x 80ns x f (Hz).

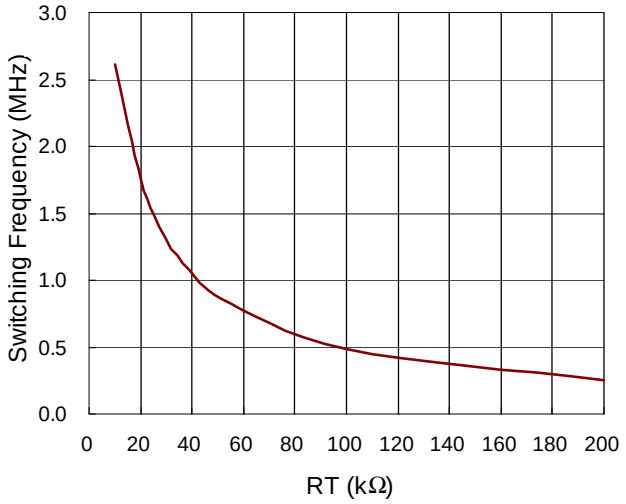


Figure 2

Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the RT8073 quiescent current drops to lower than 2µA. Driving the EN pin high (>1.5V, 5.5V) will turn on the device again. For external timing control, the EN pin can also be externally pulled high by adding a R_{EN} resistor and C_{EN} capacitor from the VIN pin (see Figure 3).

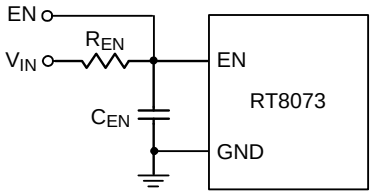


Figure 3. Enable Timing Control

An external MOSFET can be added to implement digital control on the EN pin when no system voltage above 1.5V is available, as shown in Figure 4. In this case, the pull-up resistor, R_{EN}, is connected between V_{IN} and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin.

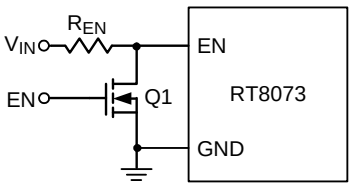


Figure 4. Digital Enable Control Circuit

Hiccup Mode

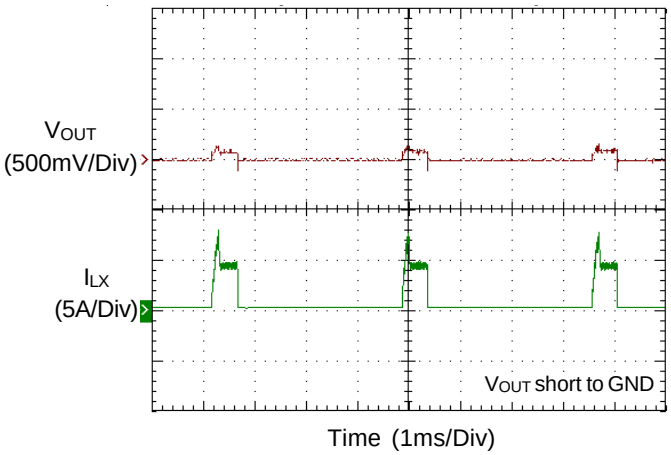


Figure 5. Hiccup Mode Under Voltage Protection

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, the maximum inductor peak current is reduced when slope compensation is added. In the RT8073, however, separated inductor current signals are used to monitor over current condition. This keeps the maximum output current relatively constant regardless of duty cycle.

Hiccup Mode

For the RT8073, it provides Hiccup Mode Under Voltage Protection (UVP). When the output is shorted to ground, the UVP function will be triggered to shut down switching operation. If the under voltage condition remains for a period, the RT8073 will retry automatically. When the under voltage condition is removed, the converter will resume operation. The UVP is disabled during soft-start period.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current can reduce not only the ESR losses in the output capacitors but also the output voltage ripple. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.4(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 (Exposed Pad) packages, the thermal resistance, θ_{JA}, is 49°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-12L 3x3 packages, the thermal resistance, θ_{JA}, is 60°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (49°C/W) = 2.041W for SOP-8 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (60°C/W) = 1.667W for WDFN-12L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curves in Figure 6 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

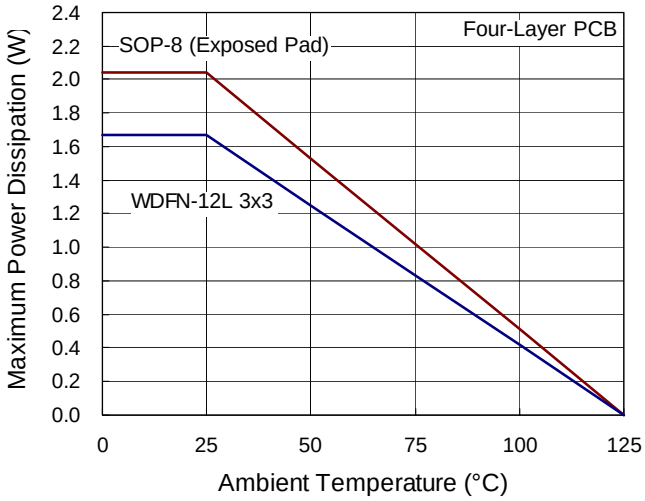


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of RT8073.

- A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small-signal components returning to the GND pin at one point that is then connected to the PGND pin close to the IC. The exposed pad should be connected to GND.
- Connect the terminal of the input capacitor(s), C_{IN}, as close as possible to the VIN pin. This capacitor provides the AC current into the internal power MOSFETs.
- LX node is with high frequency voltage swing and should be kept within small area. Keep all sensitive small-signal nodes away from the LX node to prevent stray capacitive noise pick-up.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components.
- Connect the FB pin directly to the feedback resistors. The resistor divider must be connected between V_{OUT} and GND.

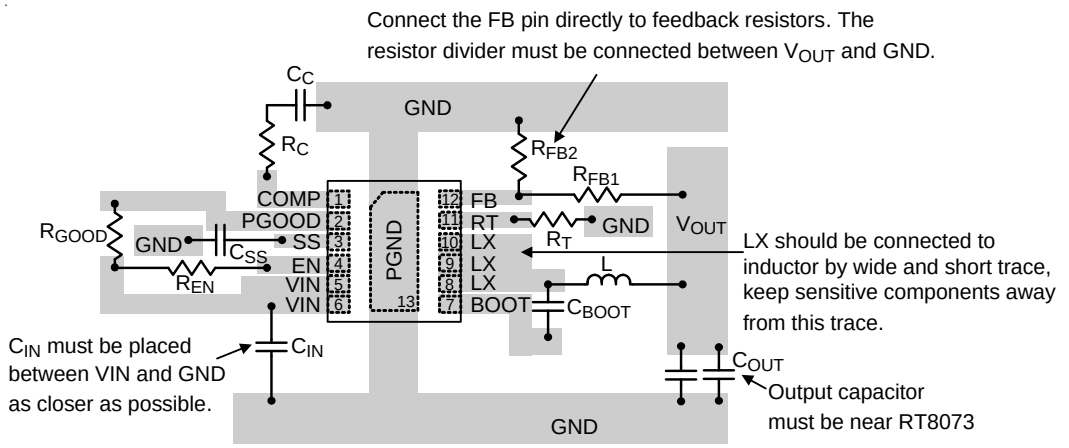


Figure 7. PCB Layout Guide for WDFN-12L 3x3

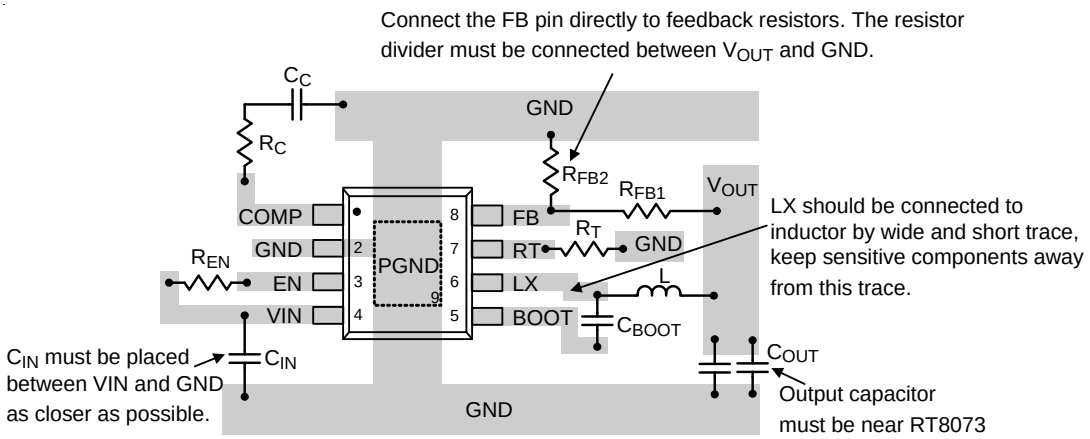


Figure 8. PCB Layout Guide for SOP-8 (Exposed Pad)

Recommended component selection for Typical Application

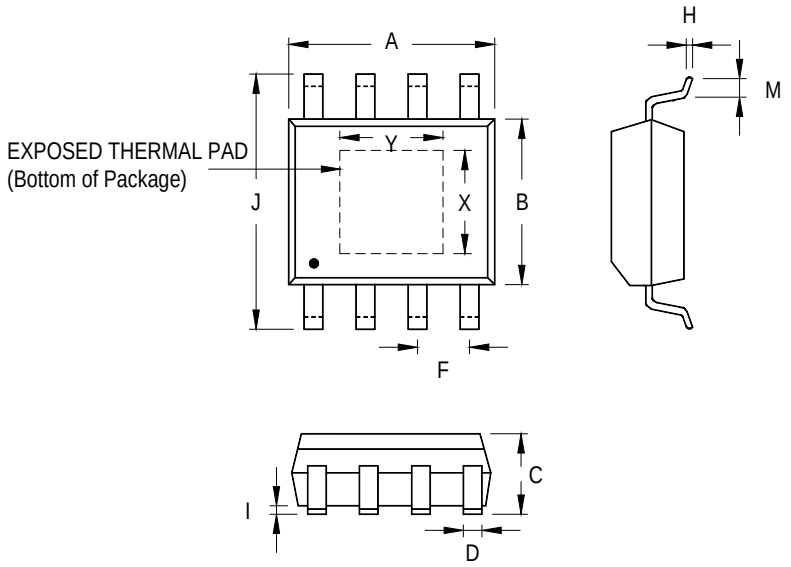
Table 2. Inductors

Component Supplier	Series	Inductance (μH)	DCR (mΩ)	Current Rating (A)	Case Size
Wurth Elektronik	No.744308033	0.33	0.37	27	1070
Wurth Elektronik	No.744355147	0.47	0.67	30	1365

Table 3. Capacitors for C_{IN} and C_{OUT}

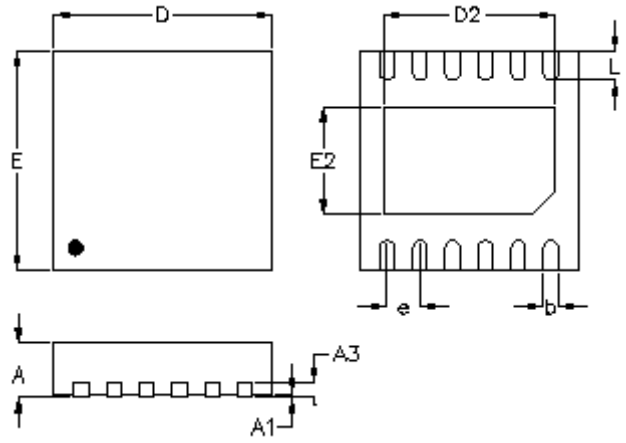
Component Supplier	Part No.	Capacitance (μF)	Case Size
TDK	C3225X5R0J226M	22	1210
TDK	C2012X5R0J106M	10	0805
Panasonic	ECJ4YB0J226M	22	1210
Panasonic	ECJ4YB1A106M	10	1210
TAIYO YUDEN	LMK325BJ226ML	22	1210
TAIYO YUDEN	JMK316BJ226ML	22	1206
TAIYO YUDEN	JMK212BJ106ML	10	0805

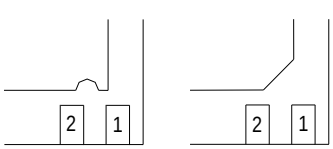
Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.250	0.006	0.010
D		2.950	3.050	0.116	0.120
D2	Option1	2.300	2.650	0.091	0.104
	Option2	1.970	2.070	0.078	0.081
E		2.950	3.050	0.116	0.120
E2	Option1	1.400	1.750	0.055	0.069
	Option2	1.160	1.260	0.046	0.050
e		0.450		0.018	
L		0.350	0.450	0.014	0.018

W-Type 12L DFN 3x3 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789