NB3L8504S

2.5 V / 3.3 V 1:4 Differential Input to LVDS Fanout Buffer / Translator

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Description

The NB3L8504S is a differential 1:4 LVDS fanout buffer/translator with OE control for each differential output. The differential inputs which can be driven by either a differential or single−ended input, can accept various logic level standards such as LVPECL, LVDS, HSTL, HCSL and SSTL. These signals are then translated to four identical LVDS copies of the input up to 700 MHz. As such, the NB3L8504S is ideal for Clock distribution applications that require low skew.

The NB3L8504S is offered in the TSSOP−16 package.

Features

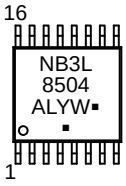
- Four Differential LVDS Outputs
- Each Differential Output has OE Control
- 700 MHz Maximum Output Frequency
- 660 ps Max Output Rise and Fall Times, LVCMOS
- Translates Differential Input to LVDS Levels
- Additive Phase Jitter RMS: < 100 fs Typical
- 50 ps Maximum Output Skew
- 350 ps Maximum Part−to−part Skew
- 1.3 ns Maximum Propagation Delay
- Operating Range: V_{CC} = 2.5 V ± 5% or 3.3 V ± 10%
- −40°C to +85°C Ambient Operating Temperature
- 16−Pin TSSOP, 4.4 mm x 5.0 mm x 0.925 mm
- These are Pb−Free Devices

Applications

- Telecom
- Ethernet
- Networking
- SONET

TSSOP−16
DT SUFFIX
CASE 948F

MARKING DIAGRAM*



A	=	Assembly Location
L	=	Wafer Lot
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

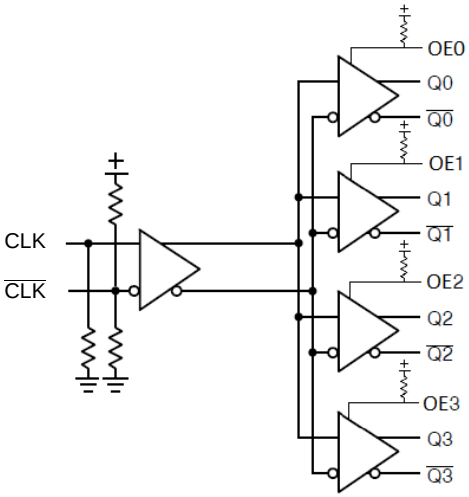


Figure 1. Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

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Table 1. PIN DESCRIPTIONS AND CHARACTERISTICS

Pin	Name	I/O	Description
1	OE0	LVTTL/LVCMOS Input	Output Enable pin for Q0, $\overline{Q0}$ outputs. Defaults High when left open; internal pull−up resistor.
2	OE1	LVTTL/LVCMOS Input	Output Enable pin for Q1, $\overline{Q1}$ outputs. Defaults High when left open; internal pull−up resistor.
3	OE2	LVTTL/LVCMOS Input	Output Enable pin for Q2, $\overline{Q2}$ outputs. Defaults High when left open; internal pull−up resistor.
4	VDD	Power	3.3 V / 2.5 V Positive Supply Voltage.
5	GND	Power	3.3 V / 2.5 V Negative Supply Voltage.
6	CLK	Multi−Level Input	Non−inverting differential Clock input. Defaults Low when left open; internal pull−down resistor.
7	$\overline{CLK}$	Multi−Level Input	Inverting differential Clock input. Defaults to VDD/2 when left open; internal pull−up and pull−down resistors.
8	OE3	LVTTL/LVCMOS Input	Output Enable pin for Q3, $\overline{Q3}$ outputs. Defaults High when left open; internal pull−up resistor.
9	$\overline{Q3}$	LVDS Output	Inverting differential Clock output.
10	Q3	LVDS Output	Non−inverting differential Clock output.
11	$\overline{Q2}$	LVDS Output	Inverting differential Clock output.
12	Q2	LVDS Output	Non−inverting differential Clock output.
13	$\overline{Q1}$	LVDS Output	Inverting differential Clock output.
14	Q1	LVDS Output	Non−inverting differential Clock output.
15	$\overline{Q0}$	LVDS Output	Inverting differential Clock output.
16	Q0	LVDS Output	Non−inverting differential Clock output.

1. All VDD and GND pins must be externally connected to a power supply for proper operation.

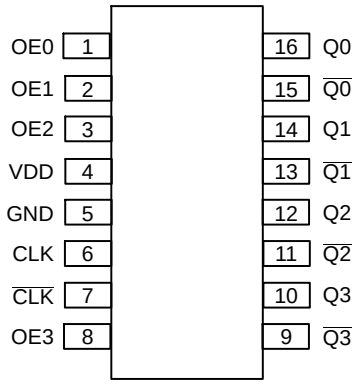


Figure 2. NB3L8504S Pinout, 16−pin TSSOP (Top View)

Table 2. OUTPUT ENABLE FUNCTION TABLE

OE[3:0]	Outputs – Q[0:3], $\overline{Q}$[0:3]
LOW	High Impedance
HIGH (Default)	Active

Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
R_{PU} − Input Pull−up Resistor R_{PD} − Input Pull−down Resistor		50 kΩ 50 kΩ
C_{IN} − Input Capacitance		4 pF
R_{IN} − Input Impedance		10 kΩ
Moisture Sensitivity (Note 2)	TSSOP−16	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		371
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition		Rating	Unit
V_{DD}		GND = 0 V		4.6	V
V_{IN}		GND = 0 V		−0.5 to V_{DD} +0.5	V
I_{out}	Continuous Current Surge Current	LVDS Outputs		10 15	mA mA
I_{OSC}	Output Short Circuit Current Line−to−Line (Q to $\overline{Q}$) Line−to−GND (Q or $\overline{Q}$ to GND)	 Q or $\overline{Q}$ Q to $\overline{Q}$ to GND	 Continuous Continuous	 12 24	 mA mA
T_A	Operating Temperature Range	TSSOP−16		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 lfpm 500 lfpm	TSSOP−16 TSSOP−16	138 108	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	TSSOP−16	33 − 36	°C/W
T_{sol}	Wave Solder (Pb−Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS V_{DD} = 2.5 V ± 5% or 3.3 V ± 10%; GND = 0 V; T_A = −40°C to 85°C

Symbol	Characteristic		Min	Typ	Max	Unit
POWER SUPPLY / CURRENT (Note 4)						
V_{DD}	Power Supply Voltage	V_{DD} = 3.3 V V_{DD} = 2.5 V	2.97 2.375	3.3 2.5	3.63 2.625	V
I_{DD}	Power Supply Current for V_{DD}			41	50	mA
LVDS OUTPUTS (Note 5)						
V_{OD}	Differential Output Voltage (Figure 12) (Notes 6 and 7)		250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change (Figure 12) (Notes 6 and 7)				50	mV
V_{OS}	Offset Voltage (Figure 13) (Notes 6 and 7)		1075	1250	1375	mV
ΔV_{OS}	V_{OS} Magnitude Change (Figure 13) (Notes 6 and 7)				50	mV
V_{OH}	Output HIGH Voltage			1425	1600	mV
V_{OL}	Output LOW Voltage		900	1075		mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figure 5 & 6) (Note 11)						
V_{IHD}	Differential Input HIGH Voltage		500		V_{DD} – 850	mV
V_{ILD}	Differential Input LOW Voltage		−300		V_{IHD} – 150	mV
V_{ID}	Differential Input Voltage (V_{IHD} – V_{ILD})		150		1300	mV
V_{IHCMR}	Input Common Mode Voltage Range (Differential Configuration) (Note 10) (Figure 7)		GND + 0.5		V_{DD} – 850	mV
I_{IH}	Input HIGH Current, V_{DD} = V_{IN} = 3.63 V	CLK, $\overline{CLK}$			150	μA
I_{IL}	Input LOW Current, V_{DD} = 3.63 V, V_{IN} = 0 V	CLK $\overline{CLK}$	−5 −150			μA
LVCMOS – OE Control Inputs						
V_{IH}	Input HIGH Voltage		2.0		V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		−0.3		0.8	V
I_{IH}	Input HIGH Current, V_{DD} = V_{IN} = 3.63 V				5	μA
I_{IL}	Input LOW Current, V_{DD} = 3.63 V, V_{IN} = 0 V		−150			μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input pins open and output pins loaded with R_L=100 Ω across differential.
5. LVDS outputs require 100 Ω receiver termination resistor between diff. pair. See Figure 14.
6. VOS max + ½ VOD max. Also see Figures 12 and 13.
7. VOS min − ½ VOD max. Also see Figures 12 and 13.
8. V_{IH}, V_{IL}, Vth, and V_{ISE} parameters must be complied with simultaneously.
9. Vth is applied to the complementary input when operating in single−ended mode.
10. V_{IHCMR} max varies 1:1 with V_{DD}, V_{IHCMR} min varies 1:1 with GND.
11. V_{IHD}, V_{ILD}, V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.

Table 6. AC CHARACTERISTICS V_{DD} = 2.5 V ± 5% or 3.3 V ± 10%; GND = 0 V; T_A = −40°C to 85°C (Note 12) (Figure 10)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{MAX}	Input Clock Frequency $V_{OUTPP} \geq 250$ mV @ $V_{INPPmax}$			700	MHz
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \leq 700$ MHz (See Figure 3)	250	350		mV
tpd	Differential Input to Differential Output Propagation Delay at f_{MAX} @ V_{DD} = 3.3 V	0.9		1.3	ns
$t_{jit}(\phi)$	Additive Phase Jitter RMS (Figure 4) Integration Range:12 kHz − 20 MHz f_{out} = 156.25 MHz f_{out} = 100 MHz		0.07 0.10	0.08 0.105	ps
$t_{SKEW(o-o)}$	Output−to−output Skew (Note 14) (Figure 8)			50	ps
$T_{SKEW(pp)}$	Part−to−part Skew (Note 14)			350	ps
t_r / t_f	Output Rise/Fall Times @ 50 MHz, 20% − 80%	180	350	660	ps
t_{DC}	Output Clock Duty Cycle (Input Duty Cycle = 50%)	45	50	55	%
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 13)	150		1300	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

12. Measured by forcing a 50% duty cycle clock source. All LVDS output loading with an external R_L = 100 Ω across Q & $\overline{Q}$.
13. $V_{INPP(max)}$ cannot exceed V_{DD}. Input voltage swing is a single−ended measurement operating in differential mode.
14. Skew is measured between outputs under identical transition at 50 MHz.

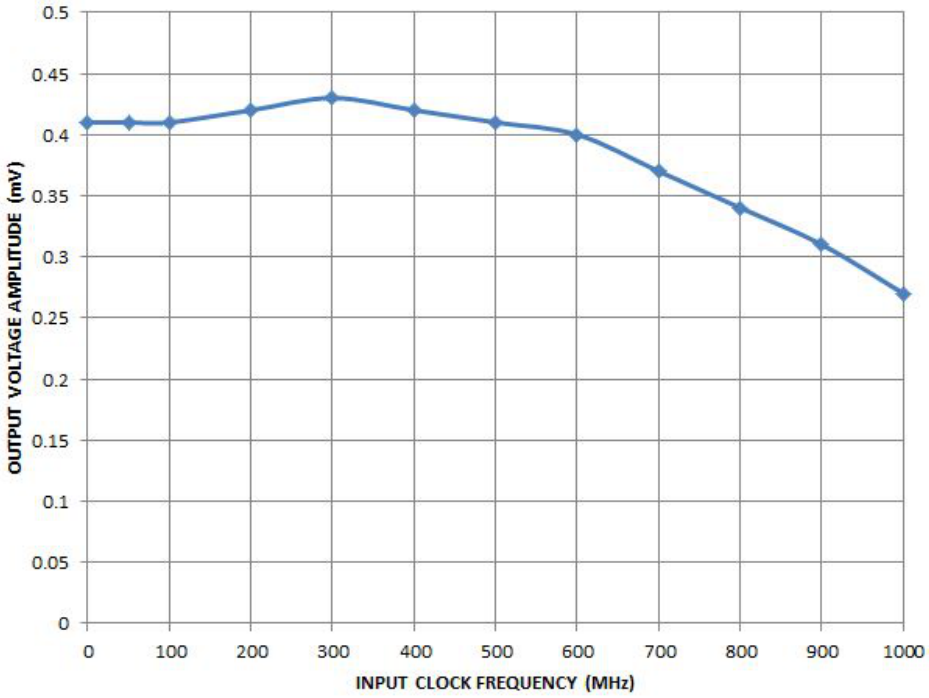


Figure 3. Output Voltage Amplitude (V_{OUTPP}) vs. Input Clock Frequency (f_{in}) and Temperature (@ V_{DD} = 2.5 V)

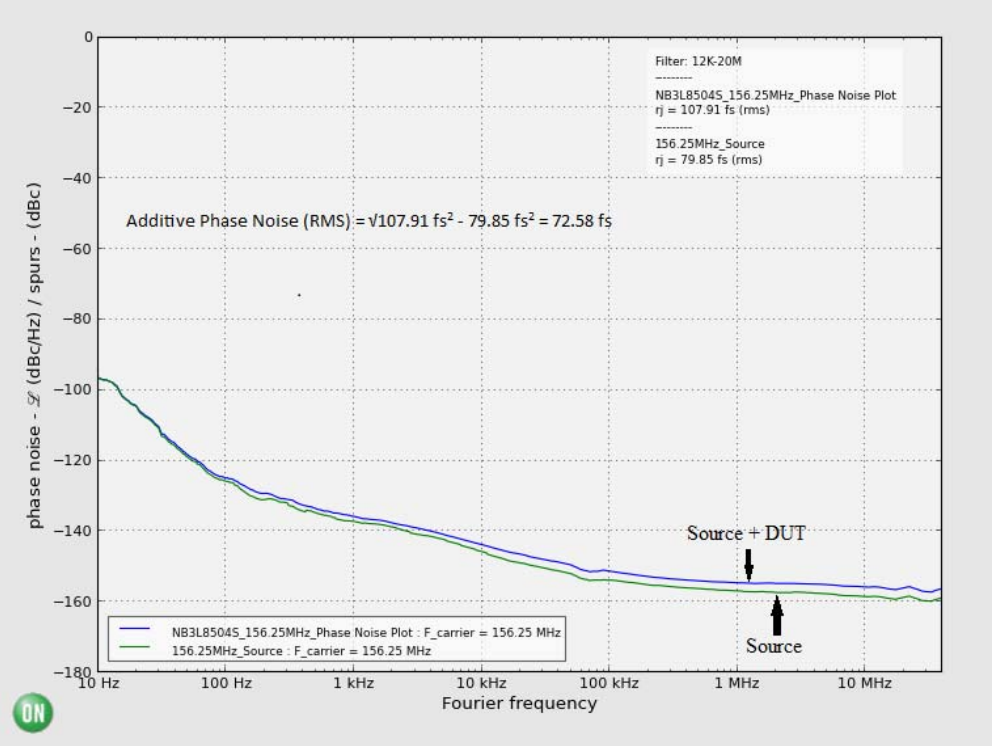


Figure 4. Additive Phase Jitter

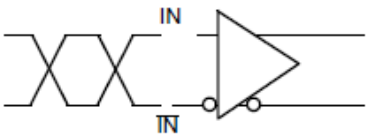


Figure 5. Differential Inputs Driven Differentially

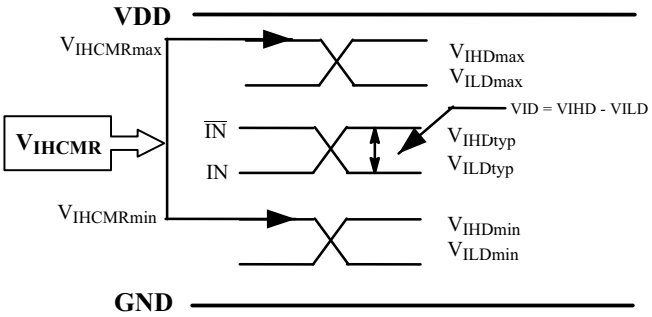


Figure 7. VIHCMR Diagram

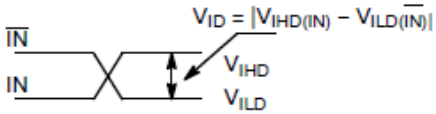


Figure 6. Differential Inputs Driven Differentially

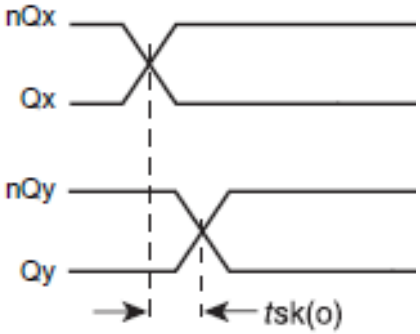


Figure 8. Output−to−Output Skew

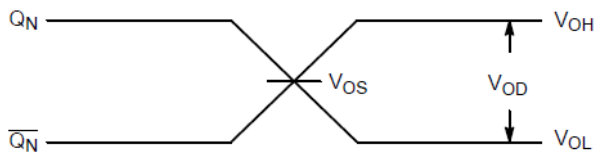


Figure 9. LVDS Output

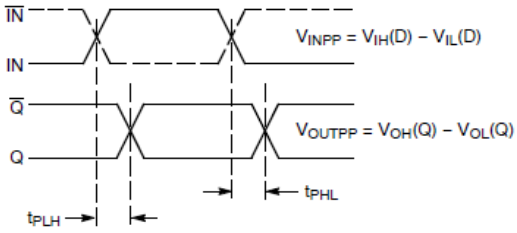


Figure 10. AC Reference Measurements

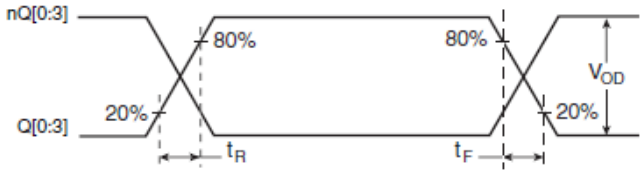


Figure 11. LVDS Output

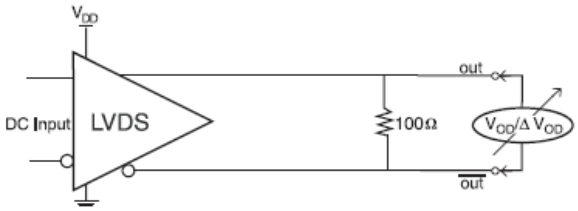


Figure 12. V_{OD} and ΔV_{OD}

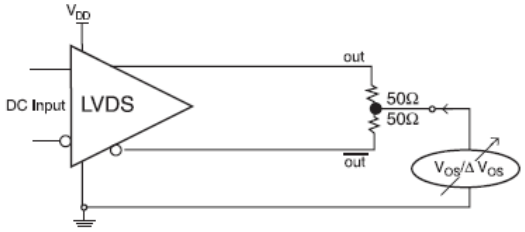


Figure 13. V_{OS} and ΔV_{OS}

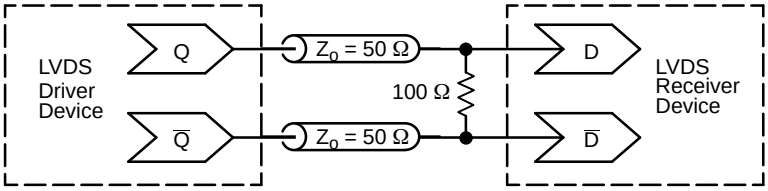


Figure 14. Typical LVDS Termination for Output Driver and Device Evaluation

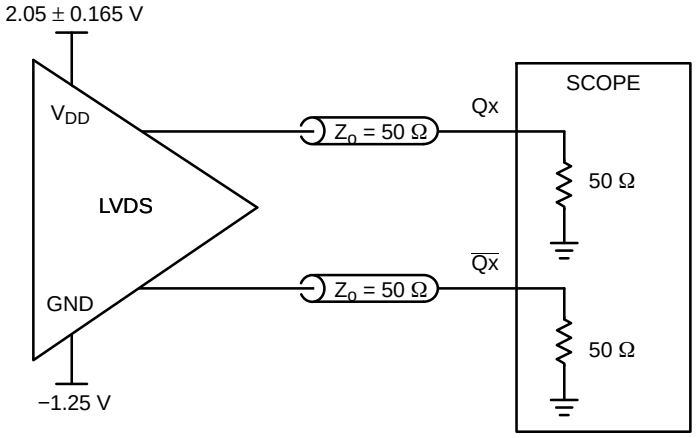


Figure 15. Typical Test Setup and Termination for Evaluation. The V_{DD} = 2.05 V ±0.165 V and GND of −1.25 Split Supply Allows a Direct Connection to an Oscilloscope 50 Ω Input Module

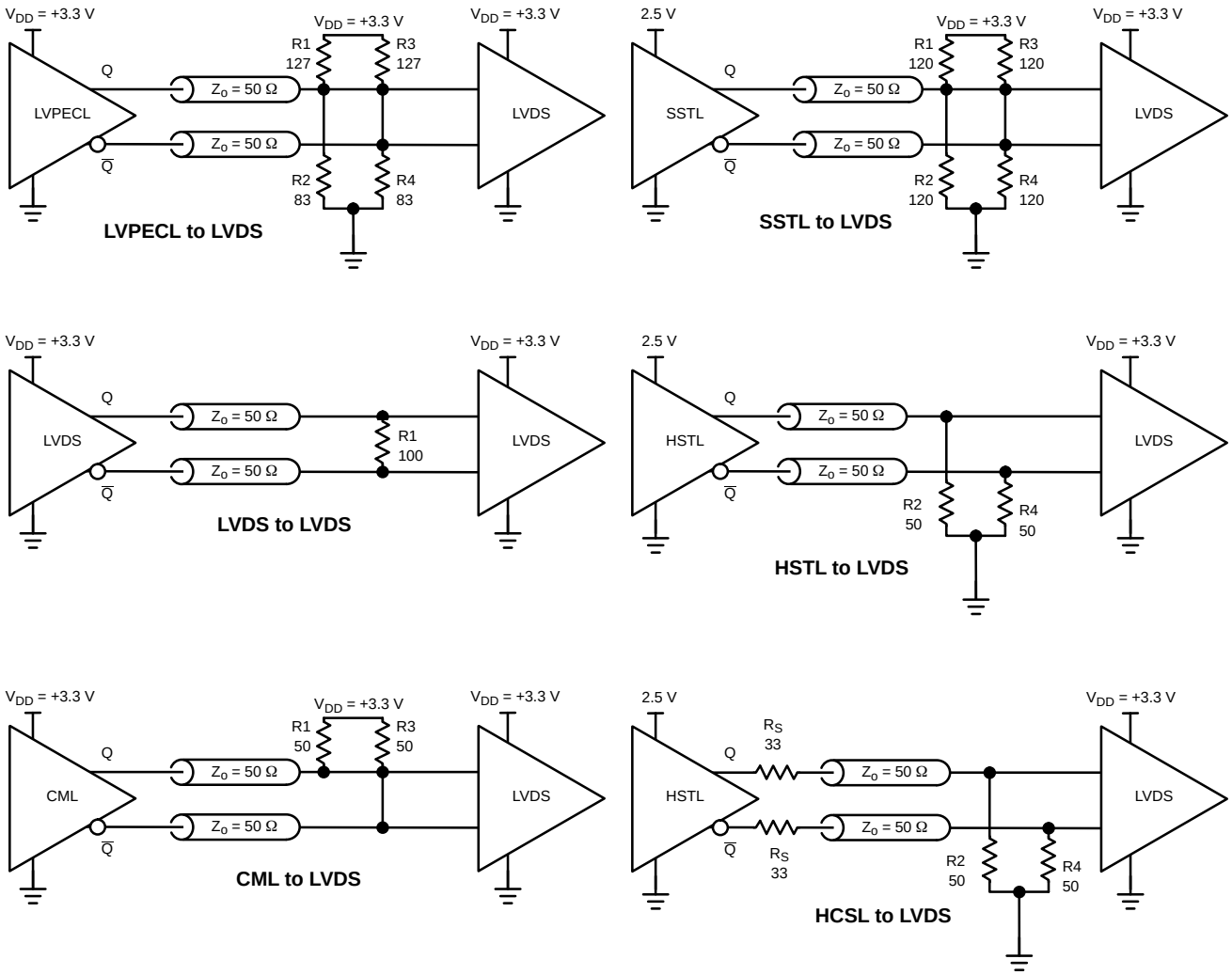


Figure 16. Differential Input Interface from LVPECL, CML, LVDS, HSTL, SSTL or HCSL

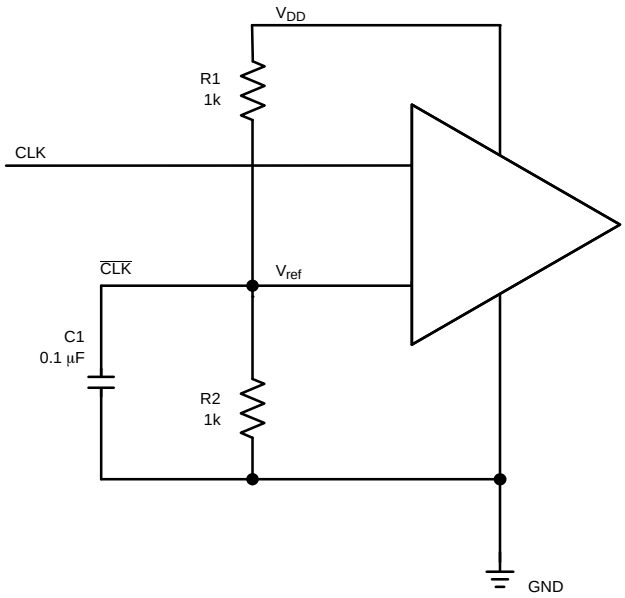


Figure 17. Differential Input Driven Single−ended

Differential Clock Input to Accept Single−ended Input

Figure 17 shows how the CLK input can be driven by a single−ended Clock signal. C1 is connected to the V_{ref} node as a bypass capacitor. Locate these components close the device pins. R1 and R2 must be adjusted to position V_{ref} to the center of the input swing on CLK.

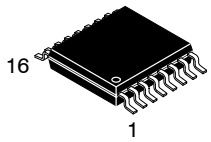
Table 7. ORDERING INFORMATION

Device	Package	Shipping
NB3L8504SDTG	TSSOP−16 (Pb−Free)	96 Units / Tube
NB3L8504SDTR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

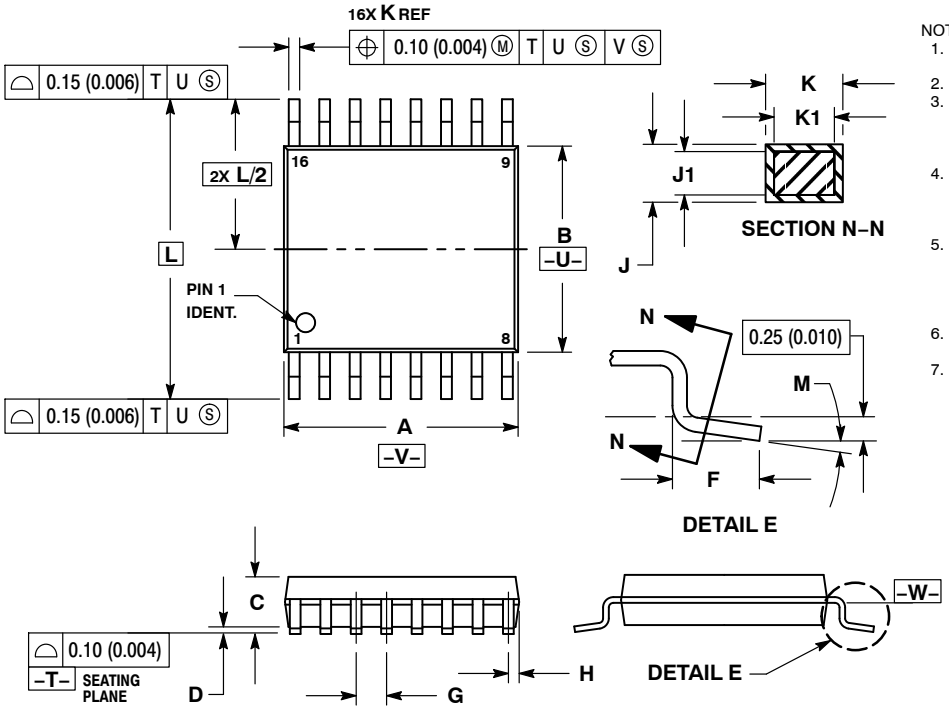
ON Semiconductor®



SCALE 2:1

TSSOP−16
CASE 948F−01
ISSUE B

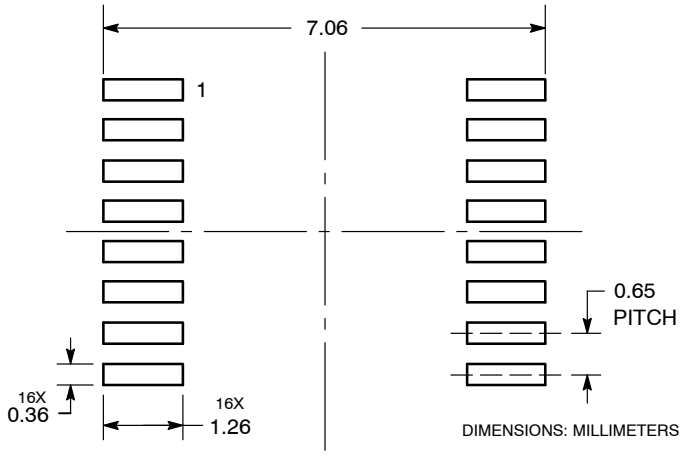
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

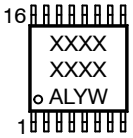
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	TSSOP−16	PAGE 1 OF 1

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