MP8003A

IEEE 802.3af/at, PoE, Powered Device, Interface Controller

DESCRIPTION

The MP8003A is an IEEE, 802.3af/at, Power over Ethernet (PoE) compliant, powered device (PD), interface controller. The MP8003A has all the functions of IEEE 802.3af/at, including detection, 1-event and 2-event classification, input current control, and a 100V hot-swap MOSFET.

The MP8003A sets the inrush current limit at about 120mA during start-up and switches to 840mA when the output pass MOSFET is turned on completely. A PG signal set to high indicates when the output is fully charged and pulls low when the output drops under the overload condition. The MP8003A also provides a T2P signal when it is connected to Type-2 power sourcing equipment (PSE).

An auxiliary power input detector (AUX) provides a smooth power switch from PSE to an auxiliary wall adapter. The MP8003A also features built-in thermal protection and a wide-input UVLO hysteresis.

The MP8003A is available in a QFN-10 (3mmx3mm) package.

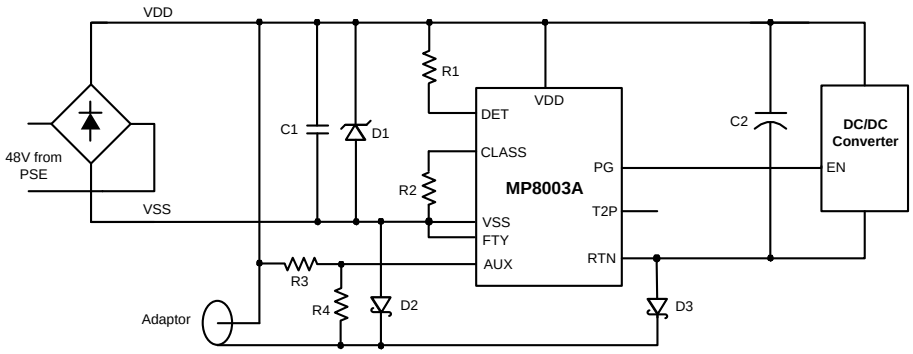
FEATURES

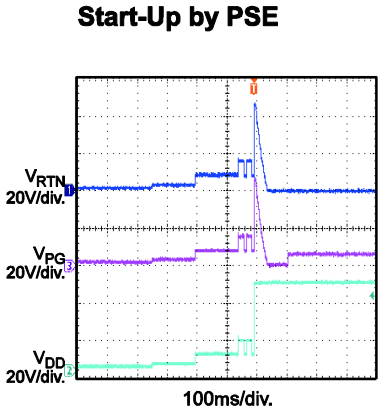
- Compatible with 802.3af/at Specifications
- 100V, 0.48Ω Integrated Pass Switch
- 120mA Inrush Current Limit
- 840mA Operation Current Limit
- 2-Event Classification
- Auxiliary Adapter O-Ring Power Supply
- Self-Driving Power Good Inductor
- Open-Drain Type-2 PSE Indicator
- Over-Temperature Protection (OTP)
- Available in QFN-10 (3mmx3mm) Package

APPLICATIONS

- IEEE 802.3af/at-Compliant Devices
- Security Cameras
- VoIP Phones
- WLAN Access Points
- IoT Devices

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8003AGQ	QFN-10 (3mmx3mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP8003AGQ–Z)

TOP MARKING

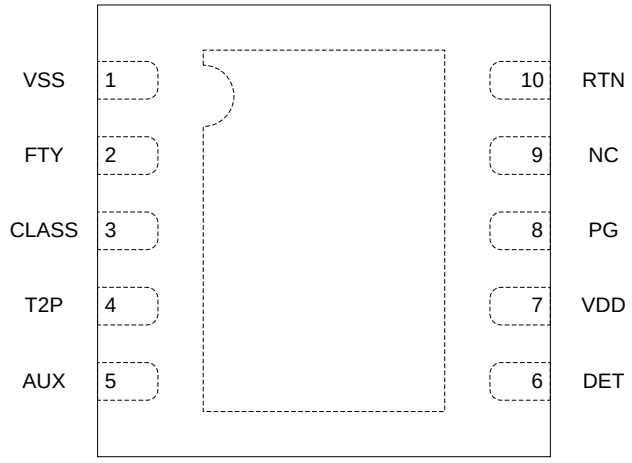
ANUY

LLL

ANU: Product code of MP8003AGQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-10 (3mmx3mm)

ABSOLUTE MAXIMUM RATINGS (1)

VDD, RTN, DET, T2P, AUX to VSS ..... -0.3V to +100V
CLASS, FTY to VSS ..... -0.3V to +6.5V
PG to RTN ..... -0.3V to +6.5V
AUX to VDD ..... -6.5V to +0.3V (2)
T2P sinking current 10mA
AUX sinking current ..... -5mA (2)
PG sinking current 1mA (3)
Continuous power dissipation (T_A = +25°C) (4) 2.5W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (5)

Supply voltage (V_{DD}) ..... 0V to 57V
T2P sinking current 5mA
Maximum AUX sinking current ..... -3mA (2)
Maximum PG sinking current 0.6mA (3)
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-10 (3mmx3mm)	50	12 ...	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) When VDD to the adapter ground voltage is high, the AUX-VDD voltage may exceed -6.5V if the divider resistor is not appropriate. In this condition, VDD clamps the -6.5V voltage on AUX, but the current should be limited by the external resistor.
3) If PG is pulled up higher than 6.5V externally, the pull-up current should be limited. Refer to the Power Good (PG) Indicator Signal section on page 14 for more details.
4) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD = 48V, all voltages are with respect to VSS, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Detection						
Detection on	V_{DET-ON}	V_{DD} rising		1.9		V
Detection off	$V_{DET-OFF}$	V_{DD} rising		11		V
DET leakage current	I_{DET-LK}	V_{DET} = V_{DD} = 57V, measure I_{DET}		0.1	5	µA
Bias current		V_{DD} = 10.1V, float DET, not in mark event, measure I_{SUPPLY}			12	µA
Detection current	I_{DET}	V_{DD} = 2.5V, measure I_{SUPPLY}	96	99	102	µA
		V_{DD} = 10.1V, measure I_{SUPPLY}	395	410	425	µA
Classification						
Classification stability time				90		µs
V_{CLASS} output voltage	V_{CLASS}	13V < V_{DD} < 21V 1mA < I_{CLASS} < 42mA	1.1	1.16	1.21	V
Classification current	I_{CLASS}	13 ≤ V_{VDD} ≤ 21V, guaranteed by V_{CLASS}				
		R_{CLASS} = 578Ω, 13V ≤ V_{DD} ≤ 21V	1.8	2	2.4	mA
		R_{CLASS} = 110Ω, 13V ≤ V_{DD} ≤ 21V	9.9	10.55	11.3	
		R_{CLASS} = 62Ω, 13V ≤ V_{DD} ≤ 21V	17.7	18.7	19.8	
		R_{CLASS} = 41.2Ω, 13V ≤ V_{DD} ≤ 21V	26.6	28.15	29.7	
		R_{CLASS} = 28.7Ω, 13V ≤ V_{DD} ≤ 21V	38.2	40.4	42.6	
Classification lower threshold	V_{CL-ON}	Regulator turns on, V_{DD} rising	11.8	12.5	13	V
Classification upper threshold	V_{CL-OFF}	Regulator turns off, V_{DD} rising	21	22	23	V
Classification hysteresis	V_{CL-HYS}	Low-side hysteresis		0.8		V
		High-side hysteresis		0.5		
Mark event reset threshold	V_{MARK-L}		4.5	5	5.5	V
Max mark event voltage	V_{MARK-H}		11	11.5	12	V
Mark event current	I_{MARK}		0.5	1.5	2	mA
Mark event resistance	R_{MARK}	2-point measure at 7V and 10V			12	kΩ
IC supply current during classification	$I_{IN-CLASS}$	V_{DD} = 17.5V, CLASS floating		220	300	µA
CLASS leakage current	$I_{LEAKAGE}$	V_{CLASS} = 0V, V_{DD} = 57V			1	µA
UVLO						
VDD turn on threshold	$V_{DD-VSS-R}$	V_{DD} rising	35	37.5	40	V
VDD turn off threshold	$V_{DD-VSS-F}$	V_{DD} falling	29	31	33	V
VDD UVLO hysteresis	$V_{DD-VSS-HYS}$		4.9			V
IC supply current during operation	I_{IN}			450		µA

ELECTRICAL CHARACTERISTICS *(continued)*

VDD = 48V, all voltages are with respect to VSS, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pass Device and Current Limit						
On resistance	R_{ON-RTN}	I_{RTN} = 600mA		0.48		Ω
Leakage current	I_{RTN-LK}	V_{DD} = V_{RTN} = 57V		1	15	μA
Current limit	I_{LIMIT}	V_{RTN} = 1V	720	840	920	mA
Inrush limit	I_{INRUSH}	V_{RTN} = 2V		120		mA
Inrush current termination		V_{RTN} falling		1.2		V
Inrush to operation mode delay	T_{DELAY}		80	100		ms
Current foldback threshold		V_{RTN} rising		10		V
Foldback deglitch time		V_{RTN} rising to inrush current foldback		1		ms
T2P						
T2P output low voltage		I_{T2P} = 2mA, respect to VSS		0.1	0.3	V
T2P high leakage current		V_{T2P} = 48V			1	μA
AUX						
AUX high threshold voltage(7)		Respect to VDD			-2.3	V
AUX low threshold voltage(7)		Respect to VDD	-0.6			V
AUX leakage current		V_{DD} - V_{AUX} = 6V			2	μA
PG						
PG output high voltage		PG floating		5.5		V
PG source current		PG = high, force PG = 4V	7			μA
PG pull-down resistance		PG is logic low, pull PG up to 1V		1000		kΩ
Thermal Shutdown						
Thermal shutdown temperature(8)	T_{SD}			150		°C
Thermal shutdown hysteresis(8)	T_{HYS}			20		°C

NOTES:

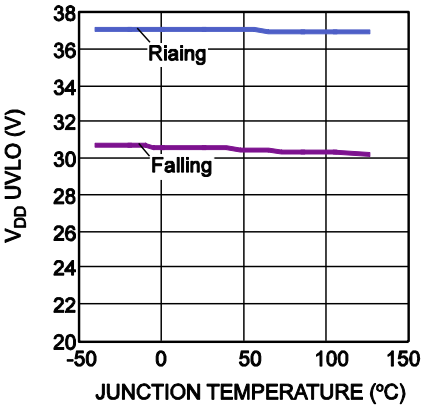
7) VDD - AUX > 2.3V, IC enable adapter input. If VDD - AUX < 0.6V, IC enables the PSE input. Refer to the Wall Power Adapter Detection and Operation section on page 12 for the AUX setting.

8) Guaranteed by engineering sample characterization.

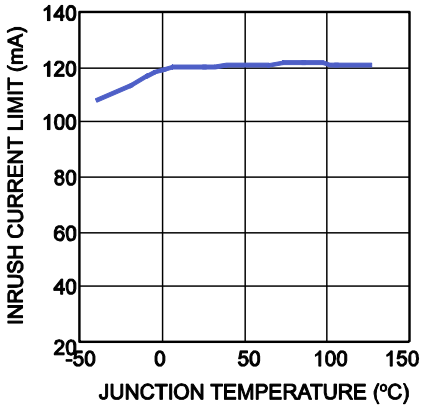
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = (VDD - VSS) = 48V, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω, T_A = 25°C, unless otherwise noted.

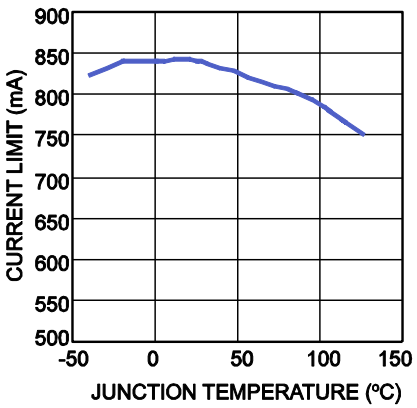
V_{DD} UVLO vs. Junction Temperature



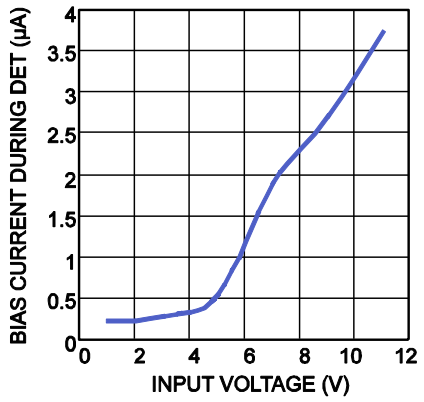
Inrush Current Limit vs. Junction Temperature



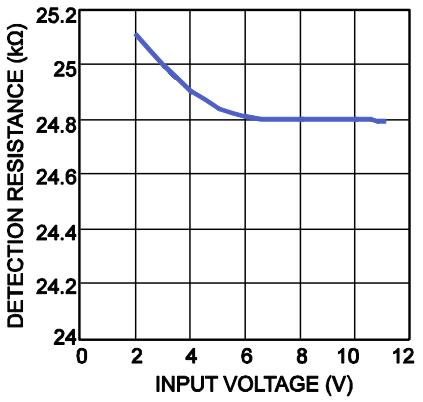
Current Limit vs. Junction Temperature



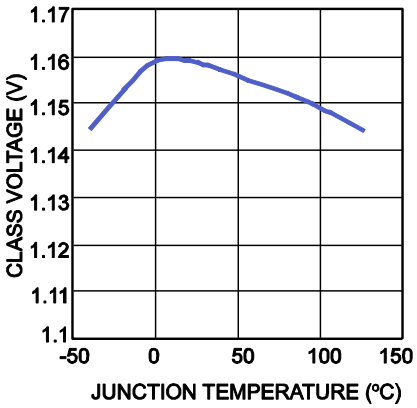
Bias Current during Detection vs. Input Voltage



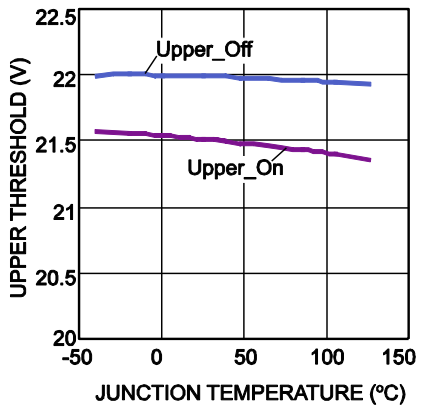
Detection Resistance vs. Input Voltage



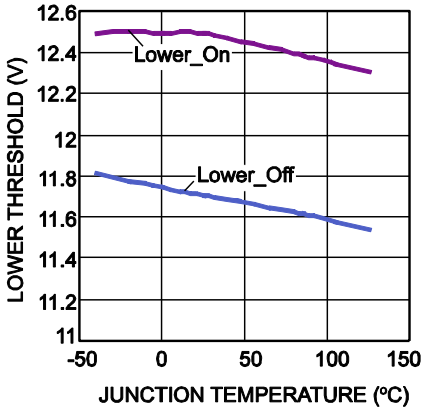
Class Voltage vs. Junction Temperature



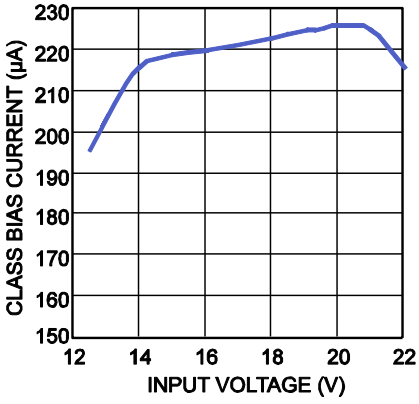
Class Upper Threshold vs. Junction Temperature



Class Lower Threshold vs. Junction Temperature



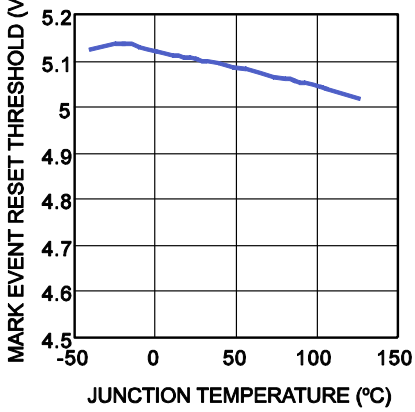
Class Bias Current vs. Input Voltage



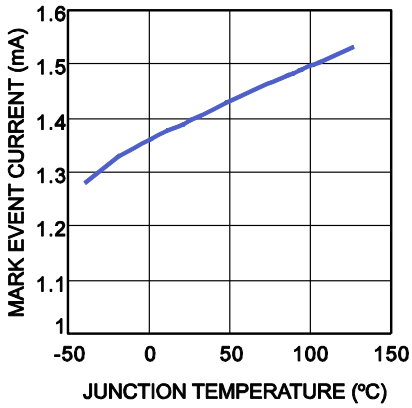
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = (VDD - VSS) = 48V, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω, T_A = 25°C, unless otherwise noted.

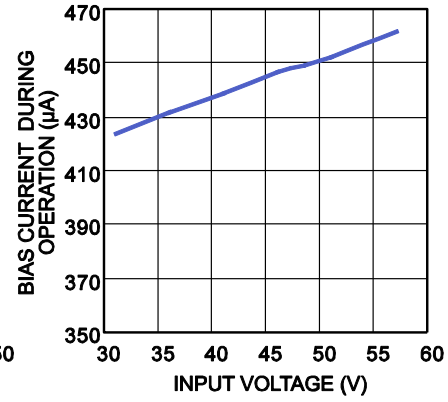
Mark Event Reset Threshold vs. Junction Temperature



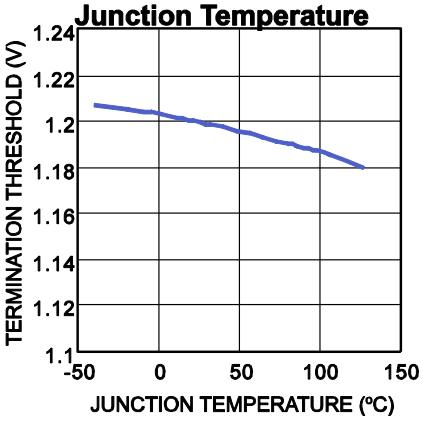
Mark Event Current vs. Junction Temperature



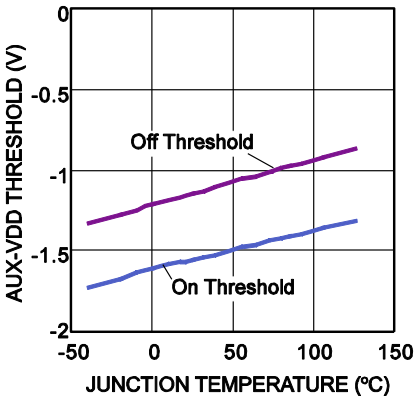
Bias Current during Operation vs. Input Voltage



Inrush Current Termination Threshold vs. Junction Temperature



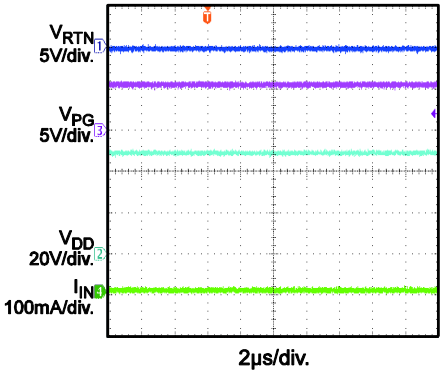
AUX-VDD Threshold vs. Junction Temperature



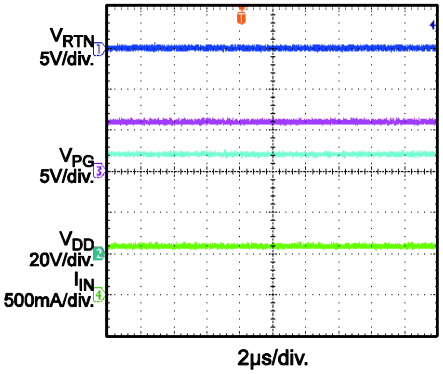
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = (VDD - VSS) = 48V, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω, T_A = 25°C, unless otherwise noted.

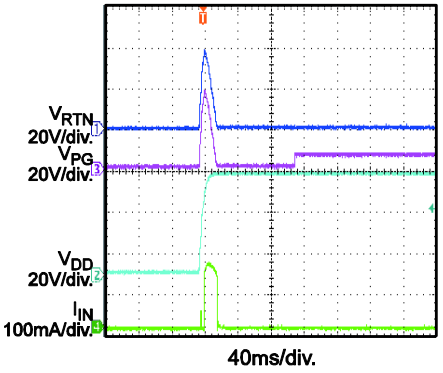
Steady State
I_{OUT} = 0A



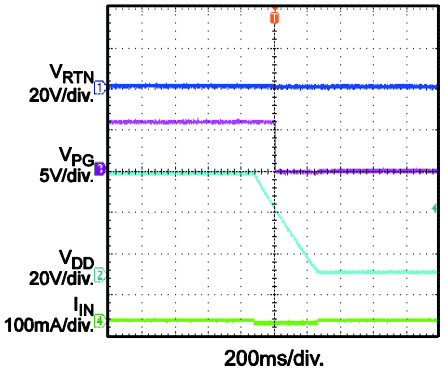
Steady State
I_{OUT} = 0.6A



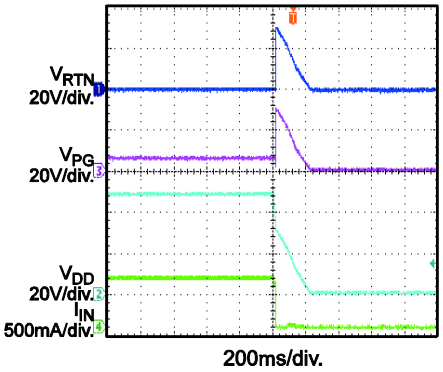
V_{DD} Start-Up
I_{OUT} = 0A



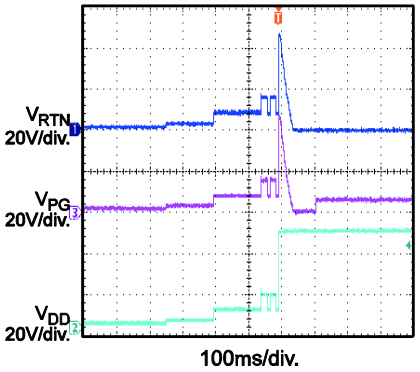
V_{DD} Shutdown
I_{OUT} = 0A



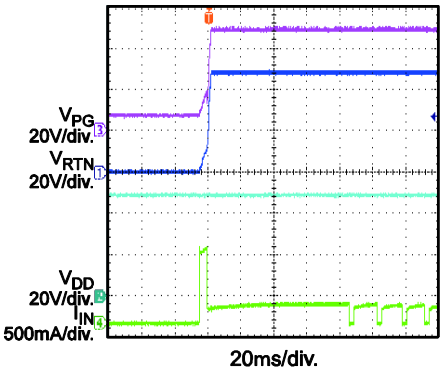
V_{DD} Shutdown
I_{OUT} = 0.6A



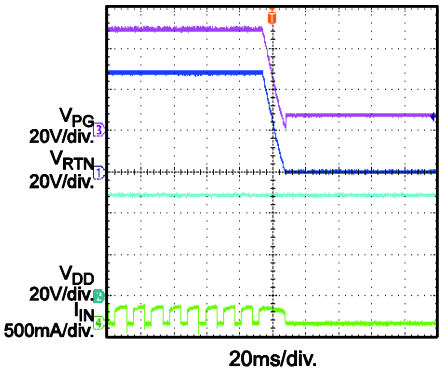
Start-Up by PSE



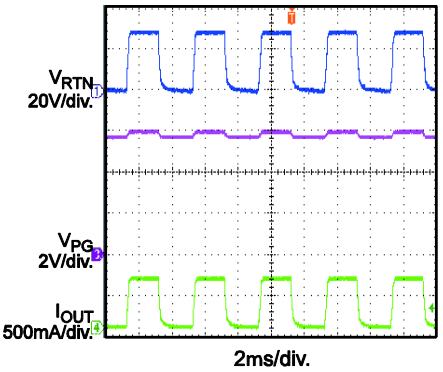
OCP Entry
I_{OUT} = 0A to 1A



OCP Recovery
I_{OUT} = 1A to 0A



Load Transient
I_{OUT} = 0A to 0.6A



PIN FUNCTIONS

PIN#	Name	Description
1	VSS	**Negative power supply terminal from the PoE input power rail.**
2	FTY	**Factory use only.** FTY must be connected to VSS during application.
3	CLASS	**Power class.** Connect resistor from CLASS to VSS to program the classification current.
4	T2P	**Type-2 PSE indictor, open-drain output.** T2P is pulled low to VSS to indicate the presence of a Type-2 PSE or if AUX is enabled.
5	AUX	**Auxiliary power input detector.** Use AUX for adapter auxiliary power applications. Drive VDD - AUX higher than 2.3V to disable the hot-swap MOSFET and CLASS function and force T2P and PG active.
6	DET	**Detection.** Connect a 24.9kΩ resistor between VDD and DET for PoE detection.
7	VDD	**Positive power supply terminal from the PoE input power rail.**
8	PG	**PD supply power good indicator.** The PG signal can be used to enable the downstream DC/DC converter. PG is pulled up by an internal current source in output-high condition and can be floated during application.
9	NC	**No connection.** NC is not connected internally, but can be connected to VSS and the exposed thermal pad during layout.
10	RTN	**Drain of PD hot-swap MOSFET.** Connect the next stage DC/DC converter's power return terminal to RTN.

BLOCK DIAGRAM

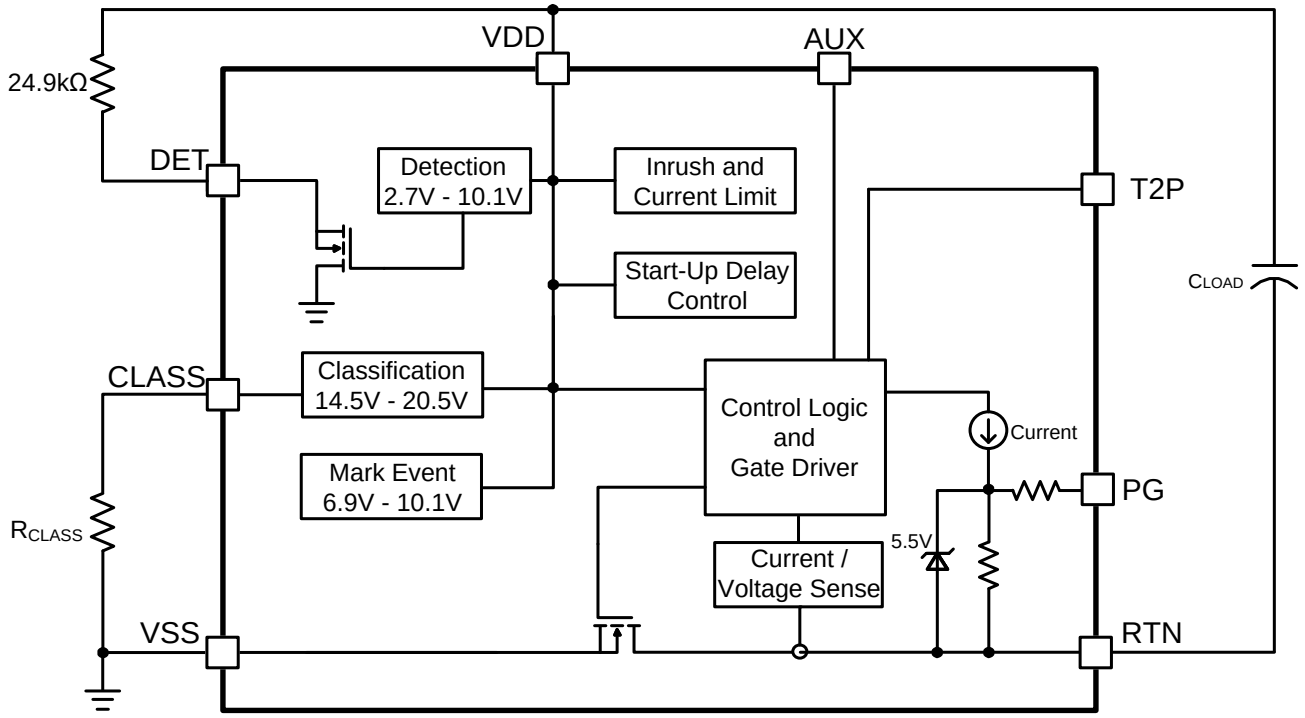


Figure 1: Functional Block Diagram

OPERATION

Compared with IEEE 802.3af, the IEEE 802.3at standard establishes a higher power allocation for Power over Ethernet (PoE) while maintaining backwards compatibility with existing IEEE 802.3af systems. Power sourcing equipment (PSE) and powered devices (PD) are distinguished as Type-1 (complying with IEEE 802.3af power levels) or Type-2 (complying with the IEEE 802.3at power levels). The IEEE 802.3af/at standard establishes a method of communication between PD and PSE with detection, classification, and event mark.

The MP8003A is an IEEE 802.3af/at PoE PD interface. The MP8003A operates as a safety device that supplies voltage only when the power sourcing equipment recognizes a unique, tightly specified resistance at the end of an unknown length of Ethernet cable. If the PSE sees the correct load, then it increases the applied voltage further to enter the classification operation range and switch on the nominal 48V power to the load. Figure 2 shows the typical PD interface power operation sequence.

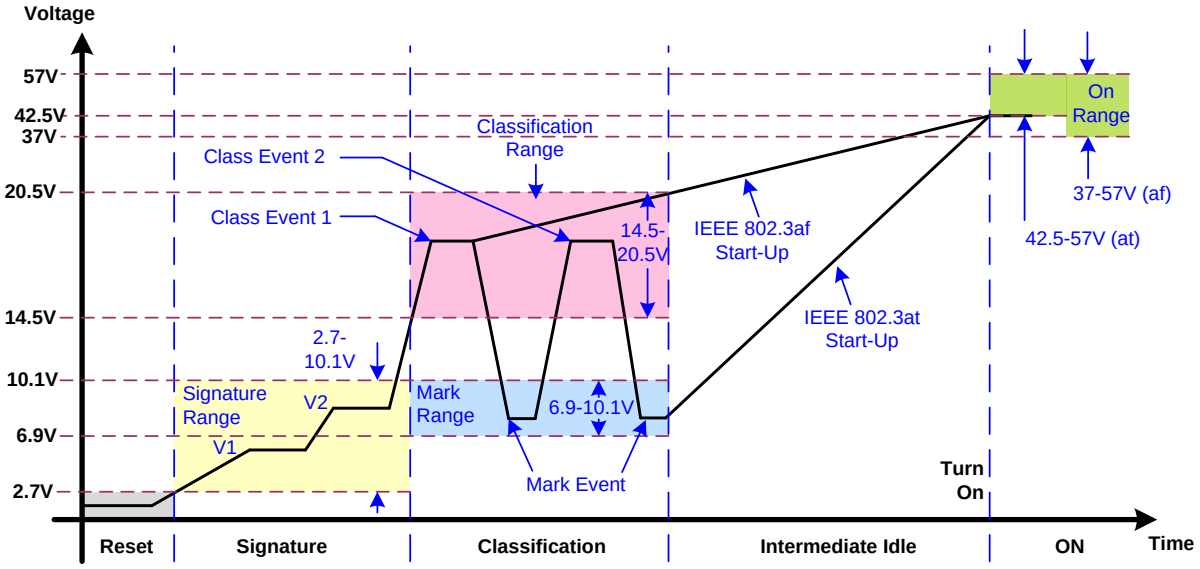


Figure 2: PD Interface Operation Description

Detection

R_{DET} connected between DET and VDD is presented as a load to the PSE in detection mode. When the PSE applies two safe voltages between 2.7V to 10.1V while measuring the change in current drawn to determine the load resistance. A 24.9kΩ (1%) resistor between VDD and DET is recommended to present one correct signature. The valid signature resistance seen from the power interface (PI) is between 23.7kΩ and 26.3kΩ.

The detection resistance seen from the PI is the result of the input bridge resistance in series with the VDD load. The input bridge resistance is cancelled partially by the effective leakage resistance during detection.

Classification

The classification mode can specify the expected load range of the device under power to the PSE so that the PSE can distribute power intelligently to as many loads as it can within its maximum current capability. The classification mode is active between 14.5V and 20.5V. The MP8003A presents a current in classification mode (see Table 1).

Table 1: Class Resistor Selection

Class	Max Input Power to PD (W)	Classification Current (mA)	R_{CLASS} (Ω)
0	12.95	2	578
1	3.84	10.55	110
2	6.49	18.7	62
3	12.95	28.15	41.2
4	25.5	40.4	28.7

2-Event Classification

The MP8003A can be used as a Type-1 PD class 0-3 (as shown in Table 1). It also distinguishes class 4 with 2-event classification.

In 2-event classification, the Type-2 PSE reads the power classification twice. Figure 2 shows an example of a 2-event classification. The first classification event occurs when the PSE presents a voltage between 14.5V to 20.5V to the MP8003A, and the MP8003A presents a class-4 load current. The PSE then drops the input voltage into the mark voltage range of 6.9V to 10.1V signaling the first mark event. The MP8003A presents a load current between 0.5mA to 2mA in the mark event voltage range.

The PSE repeats this sequence, signaling the second classification and second mark event. The PSE then applies power to the MP8003A, which charges up the downstream DC/DC input capacitor (C2) with a controlled inrush current. When C2 is fully charged, T2P presents an active low signal with respect to VSS after T_{DELAY}. The T2P output becomes inactive when the MP8003A input voltage (VDD) falls below UVLO (see Figure 3).

Under-Voltage Lockout (UVLO) and Current Limit

When the PD voltage is powered by PSE, and VDD is higher than the turn-on threshold, the hot-swap switch starts passing a limited current (I_{INRUSH}) to charge the downstream DC/DC converter's input capacitor. The start-up charging current is around 120mA.

If RTN drops below 1.2V, the hot-swap current limit switches to 840mA. After the T_{DELAY} from UVLO begins, the MP8003A asserts the PG signal and switches from start-up mode to normal operation mode. The PG signal can enable the downstream DC/DC converter directly.

If VDD - VSS drops below the input falling UVLO threshold, the hot-swap MOSFET is disabled.

If the output current overloads on the internal pass MOSFET, the current limit works, and V_{RTN} - VSS rises. If V_{RTN} rises above 10V for longer than 1ms or rises above 20V, the current limit reverts to the inrush value and pulls down PG simultaneously.

Figure 3 shows the current limit, PG, and T2P work logic during start-up from the PSE power supply.

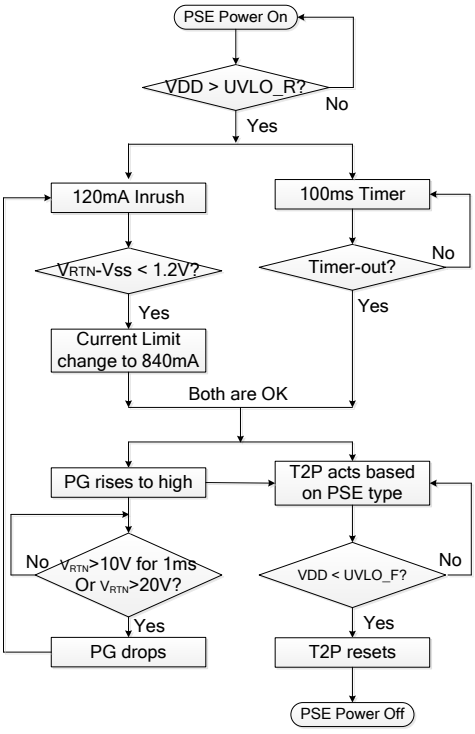


Figure 3: Start-Up Sequence

Wall Power Adapter Detection and Operation

For applications where an auxiliary power source such as a wall adapter is used to power the device, the MP8003A features wall power adapter detection (see Figure 4). Once the input voltage (VDD - VSS) exceeds about 11.5V, the MP8003A enables wall adapter detection. The wall power adapter detection resistor divider is connected from VDD to the negative terminal of an adapter. D_{ADP3} in Figure 4 is added for more accurate hysteresis. There is a -2.3V turn-on voltage from AUX to VDD for adapter detection.

The adapter is detected when Equation (1) is met:

$$V_{DD} - V_{AUX} = (V_{ADP} - V_{DADP3}) \times \frac{R_{ADPUP}}{R_{ADPUP} + R_{ADPDOWN}} > 2.3V \quad (1)$$

Where V_{ADP} is the adapter voltage, V_{DADP3} is the Zener voltage, and R_{ADPUP} and $R_{ADPDOWN}$ are the AUX divider resistors from the adapter power.

If applied adapter voltage is much higher than the design adapter voltage, the VDD - V_{AUX} voltage is high. If the applied adapter voltage is higher than 6.5V, the MP8003A inner circuit clamps the VDD - V_{AUX} voltage at 6.5V. A current then flows out through AUX. The current should be limited below 3mA by an external resistor (R_{ADPUP}/$R_{ADPDOWN}$ or R_T from the resistor divider to AUX).

To make the MP8003A work stably with adapter power, one Schottky diode (D_{ADP1}, D2 in the schematic on page 1) is required between the negative terminal of the adapter and VSS. D_{ADP2} (D3 in the schematic on page 1) is used to block reverse current between the adapter and PSE power source. When a wall adapter is detected, the internal MOSFET between RTN and VSS turns off, the classification current is disabled, and T2P becomes active. The PG signal is active when the adapter power is detected so that it can enable the downstream DC/DC converter, even if the input hot-swap MOSFET is disabled.

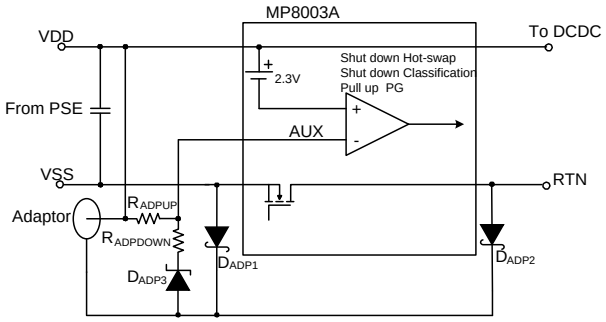


Figure 4: Adapter Power Detection

Power Good Indicator (PG)

The PG signal is driven by the internal current source. After T_{DELAY} from UVLO starts, and RTN drops to 1.2V, or a wall power adapter is detected, the PG signal is pulled high to indicate the output power condition and enable the downstream DC/DC converter. Figure 3 shows the PG logic when powered from PSE. PG is high if the adapter is detected.

Thermal Shutdown

The MP8003A has a temperature protection circuit. When the junction temperature exceeds 150°C, the IC shuts down. The IC recovers with limited inrush current if the junction temperature drops below 130°C.

APPLICATION INFORMATION

Detection Resistor

In detection mode, a resistor connected between DET and VDD is required as a load to the PSE. The resistance is calculated as $\Delta V/\Delta I$ with an acceptable range of 23.7kΩ to 26.3kΩ. Use a typical value of 24.9kΩ as a detection resistor.

Classification Resistor

To distribute power to as many loads as possible from PSE, a resistor between CLASS and VSS is used to classify the PD power level, which draws a fixed current set by the classification resistor. The supplied power set by the classification resistor is shown in Table 1. The typical voltage on CLASS is 1.16V in the classification range and produces about 47mW of power loss on the CLASS resistor, even in class-4 condition.

Protection TVS

To limit the input transient voltage within the absolute maximum ratings, a TVS across the rectified voltage (VDD - VSS) must be used. A SMAJ58A TVS or equivalent is recommended for general indoor applications. Outdoor transient levels or special applications require additional protection.

PD Input Capacitor

A 0.05μF to 0.12μF input bypass capacitor from VDD to VSS is needed for IEEE 802.3at standard specifications. Typically, a 0.1μF, 100V, ceramic capacitor is sufficient.

Wall Power Adapter Detection Circuit

When an auxiliary power source, such as a wall power adapter, is used to power the device, the divider resistors, R_{ADPUP}, $R_{ADPDOWN}$, and D_{ADP3} should be chosen to satisfy Equation (1) for correct wall power adapter detection (see Figure 5).

R_{ADPUP} with a typical 3kΩ value is recommended to balance power loss and D_{ADP1} and D_{ADP2} leakage current discharge.

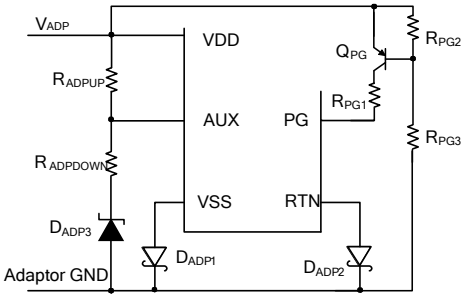


Figure 5: Wall Adapter Detection Circuit

One small Schottky diode with a 100V voltage rating, such as BAT46W, is suggested for D_{ADP1}, typically. The voltage rating of D_{ADP2} must also be 100V or higher, while the current rating must be higher than the load current. A low voltage drop Schottky diode, such as SS1H10, is recommended to reduce conduction power loss. The MP8003A enables wall adapter detection when VDD is 11.5V. If one adapter power with a lower voltage rating (such as 10V) is used to power the converter, one external PG pull-up circuit is necessary to enable the downstream DC/DC converter.

Power Good (PG) Indicator Signal

The MP8003A integrates one PG indicator. Since PG is pulled high through an internal pull-up current source when the logic is high, it can be used to enable the downstream DC/DC converter without an external pull-up circuit. PG disables the internal pull-up current and is pulled low through a 1MΩ internal resistor when PG is in a logic-low state. If there is a low resistance pulling down on EN of the downstream converter, some external PG pull-up current is needed. The MP8003A can provide 7μA of pull-up current. If PG is pulled up higher than the 5.5V power source, the PG sink current should be limited to protect the internal clamp Zener diode. Normally, an input current 0.6mA or lower on PG is suggested.

If one adapter power less than 11.5V is connected to supply the converter, the PG function cannot work with such a low input. The external PG pull-up circuit is recommended (see Figure 5). Typically, Q_{PG} requires a V_{CE} voltage higher than 100V, such as BSS63LT1. Choose R_{PG2} = 7.5kΩ and R_{PG3} = 100kΩ for a 12V adapter with some adapter regulation margin, and choose R_{PG1} = 100kΩ to limit the PG sink current.

T2P Indicator Connection

T2P is an active-low, open-drain output which indicates the presence of a Type-2 PSE or adapter power. An optocoupler is used as the interface from T2P to the circuitry on the output of the converter, typically (see Figure 6). A high-gain optocoupler and a high-impedance receiver (i.e.: CMOS) are recommended.

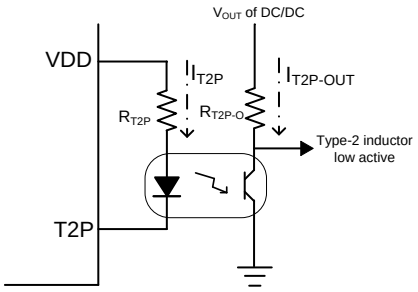


Figure 6: T2P Inductor Circuit

Considering the T2P sinking current (typically 2mA), the T2P output low voltage 0.1V, and the diode forward voltage drop, choose R_{T2P} to be 23.7kΩ. Suppose V_{OUT} of the DC/DC converter is 12V. To match the typical 48V input, choose R_{T2P-O} = 20kΩ based on the CRT, though it may vary with temperature, LED bias current, and aging.

If using an LED from VDD to T2P to indicate T2P activity, the R_{T2P}'s resistance can be higher to match the LED's max current and reduce power loss.

PCB Layout Guidelines

Efficient layout of the PoE front end should guarantee solid performance, low power loss, and no EMI/ESD problems. The spacing between VDD (48V) and VSS must comply with safety standards such as IEC60950. For best results, refer to Figure 7 and follow the guidelines below.

1. Ensure that all component placement follows the power flow from RJ-45 to the Ethernet transformer to the diode bridges to TVS to the 0.1μF capacitor to the DC/DC converter input bulk capacitor.
2. Make all leads as short as possible with wide power traces.
3. Place the MP8003A local ground planes referenced to VSS.
4. Place the next-stage DC/DC converter ground planes referenced to RTN.
5. Connect the exposed pad to VSS, since it is used to heat sink the part to the circuit board traces.
6. Place large copper traces and vias on the exposed pad and VSS trace for thermal dissipation.

Figure 7 shows the recommended component placement for the MP8003A based on the schematic on page 1.

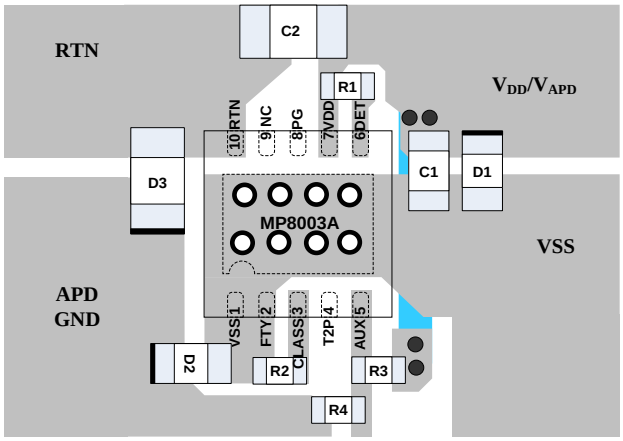


Figure 7: Recommended Layout

Design Example

Table 2 is a design example following the application guidelines for the following specifications.

Table 2: Design Example

VDD - VSS	48V
R_{DET}	24.9kΩ
R_{CLASS}	28.7Ω
$V_{ADAPTER}$	12V

The typical application circuit in Figure 8 shows the detailed application schematic, and is the basis for the Typical Performance Characteristics section. Typically, the device is powered by PSE (VDD - VSS = 48V). When an adapter voltage above 9.6V is present, the internal MOSFET between RTN and VSS turns off. Instead, the device is powered by the adapter regardless of what the PSE voltage is. For more detailed device applications, please refer to the related evaluation board datasheet.

TYPICAL APPLICATION CIRCUITS

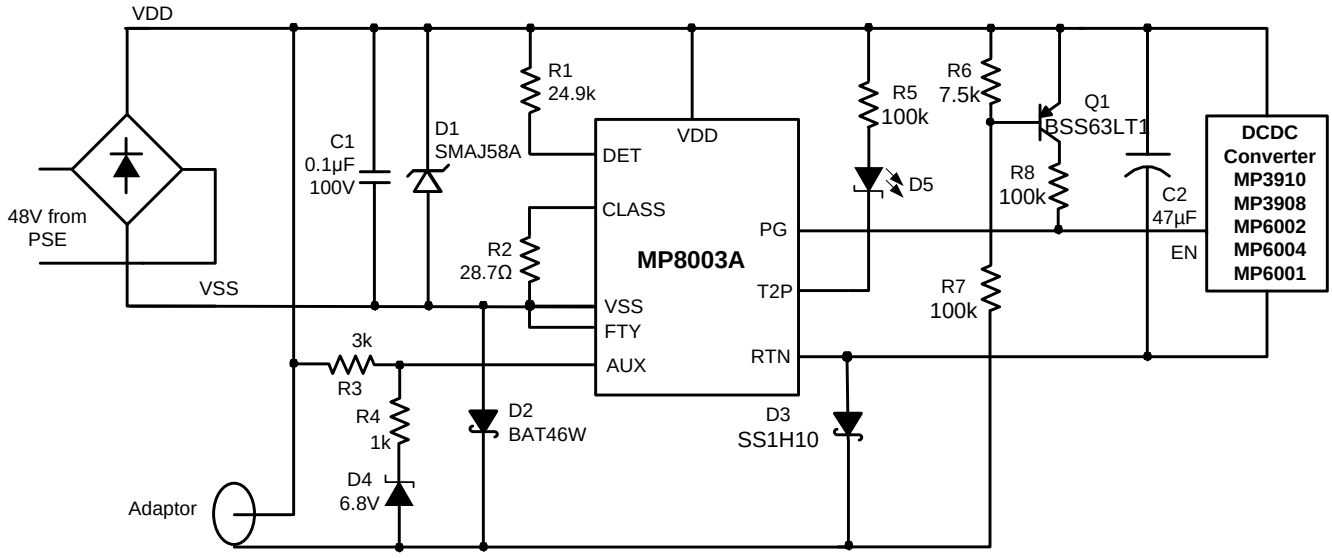


Figure 8: Typical Application Circuit, VDD - VSS = 48V, $V_{ADAPTER}$ = 12V

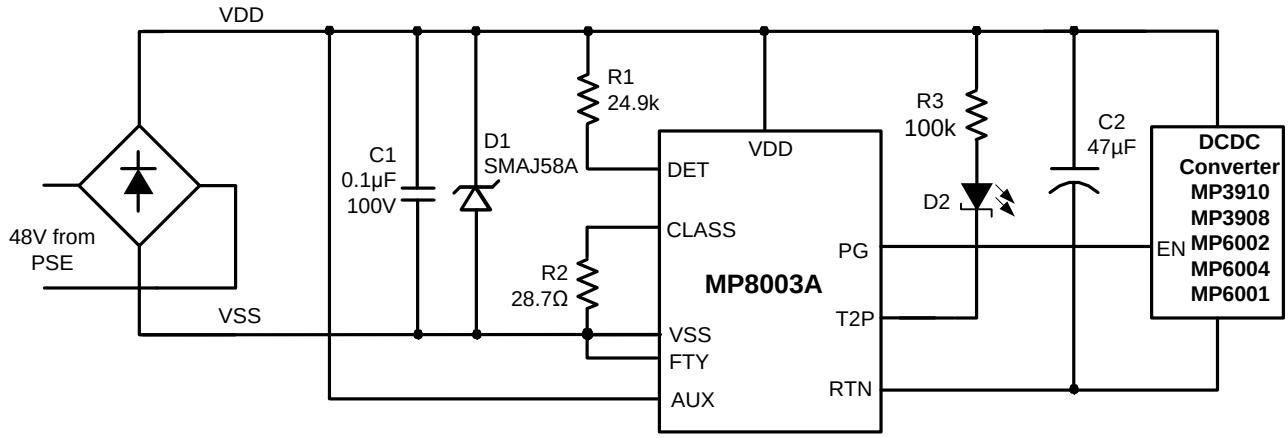
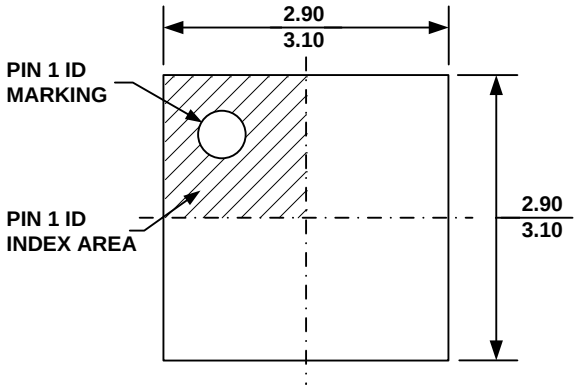


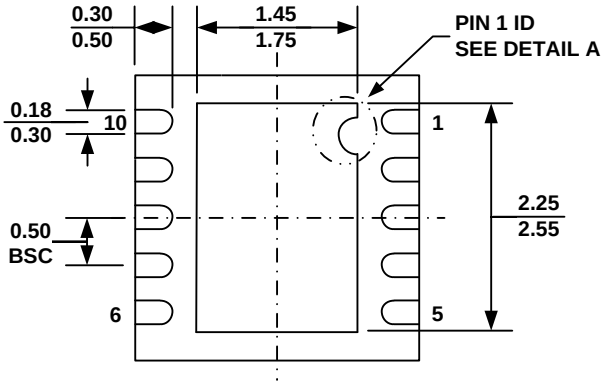
Figure 9: Typical Application Circuit, VDD - VSS = 48V, No Adapter Input

PACKAGE INFORMATION

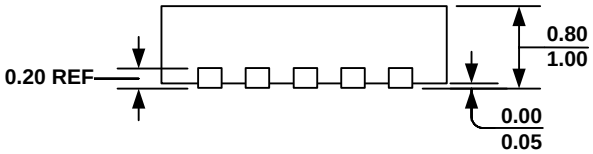
QFN-10 (3mmx3mm)



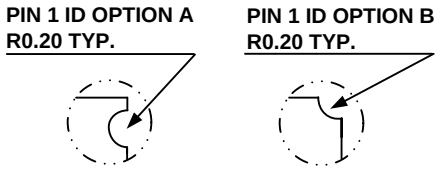
TOP VIEW



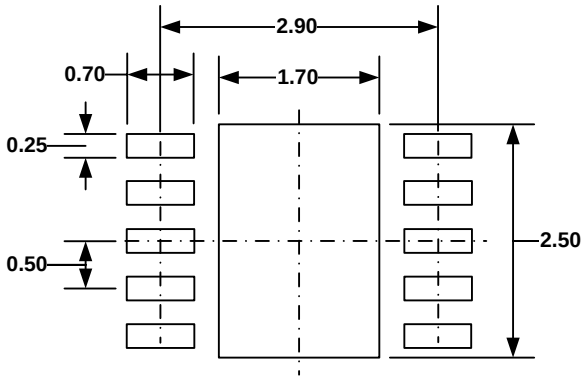
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.