AN-2072 LMH6522 Evaluation Board

1 General Description

The LMH6522EVAL evaluation board, Figure 1, is designed to aid in the characterization of Texas Instruments High Speed LMH6522 Digital Controlled Variable Gain Amplifier (DVGA).

Use the evaluation board as a guide for high frequency layout and as a tool to aid in device testing and characterization.

2 Basic Operation

The LMH6522 DVGA has differential inputs and differential outputs. The evaluation board has been designed to easily interface with 50Ω single ended test equipment. The LMH6522EVAL evaluation board is shipped with input and output transformers installed to convert the DVGA differential inputs and outputs to single ended signal paths. As built, the signal path uses the IN+ and OUT− marked connectors. The IN− and OUT+ signal paths are grounded. The signal paths are fully symmetrical.

To preserve proper bias voltages there are DC blocking capacitors on both the input and output signal traces. The input pins of the LMH6522 will self bias to approximately mid supply (2.5V). The output pins need to be biased to near ground potential. Inductors are installed on the evaluation board to provide proper output biasing. The bias current is approximately 36 mA per output pin. Capacitors between the amplifier and the output transformer will prevent offset currents from flowing through the transformer primary coil. Many transformers will show increased distortion products when there is a DC current flowing through the primary coil.

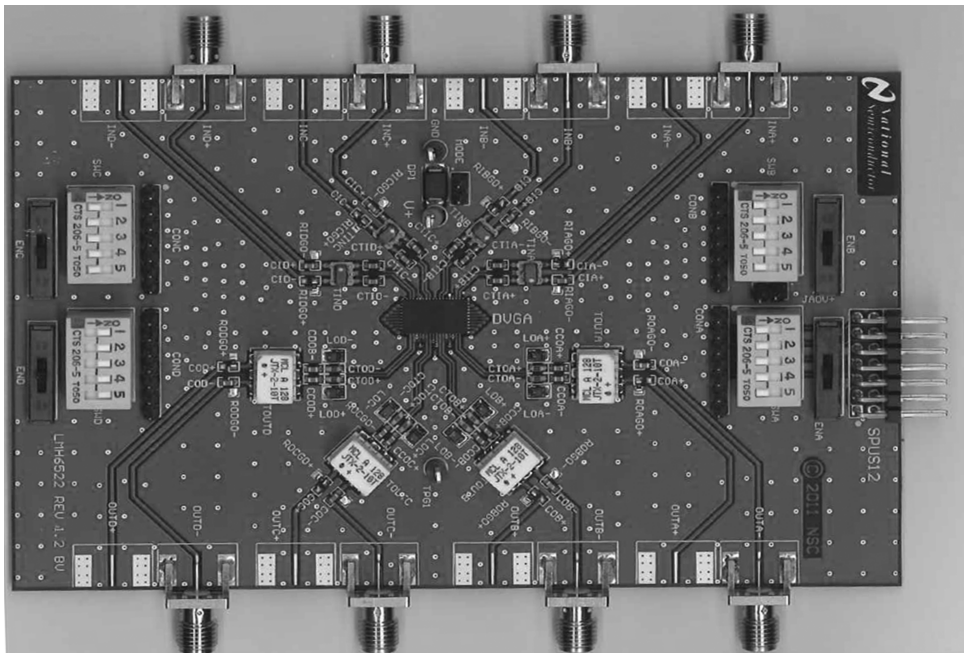


Figure 1. LMH6522EVAL Evaluation Board

Transformers TINA– TIND can provide both impedance matching as well as single ended to differential conversion. The board is shipped with 2:1 impedance ratio transformers (1.4:1 Voltage ratio) that will match 50Ω equipment with the 100Ω input impedance of the LMH6522 DVGA .

On the output side of the board are transformers TOUTA -TOUTD. The output transformers were chosen to provide a good compromise between distortion performance and physical size. The LMH6522 is capable of driving a wide range of load impedances. A 200 Ω load impedance was chosen for the evaluation board to emulate performance with a 100 Ω back terminated filter. Other configurations are possible with minor rework of the evaluation board.

Capacitors CCOA± through CCOD± are installed to isolate the DVGA outputs from the output transformer primary windings. The output resistors are 40.2 Ω matching resistors. The output impedance of the LMH6522 amplifier is very low (10Ω @ 50MHz), and the 40.2 Ω resistors provide termination for the 100 Ω load presented by the transformer when the evaluation board is connected to 50 Ω test equipment. The JTX–2–10T output transformers have a 1:2 impedance ratio.

The LMH6522 DVGA is configured to have a maximum gain of 26dB. The transformers and matching resistors contribute a loss of approximately 7.5 dB. Gain through the board should measure approximately 18.6 dB.

Zoomed in portions of the input and output schematics are shown above in Figure 2 and Figure 3. These schematics show that the evaluation board, as shipped, has been built with single ended inputs and outputs. The full signal path schematic is shown in Figure 10 and the full evaluation board schematic, including the digital control portions is available in .PDF format upon request.

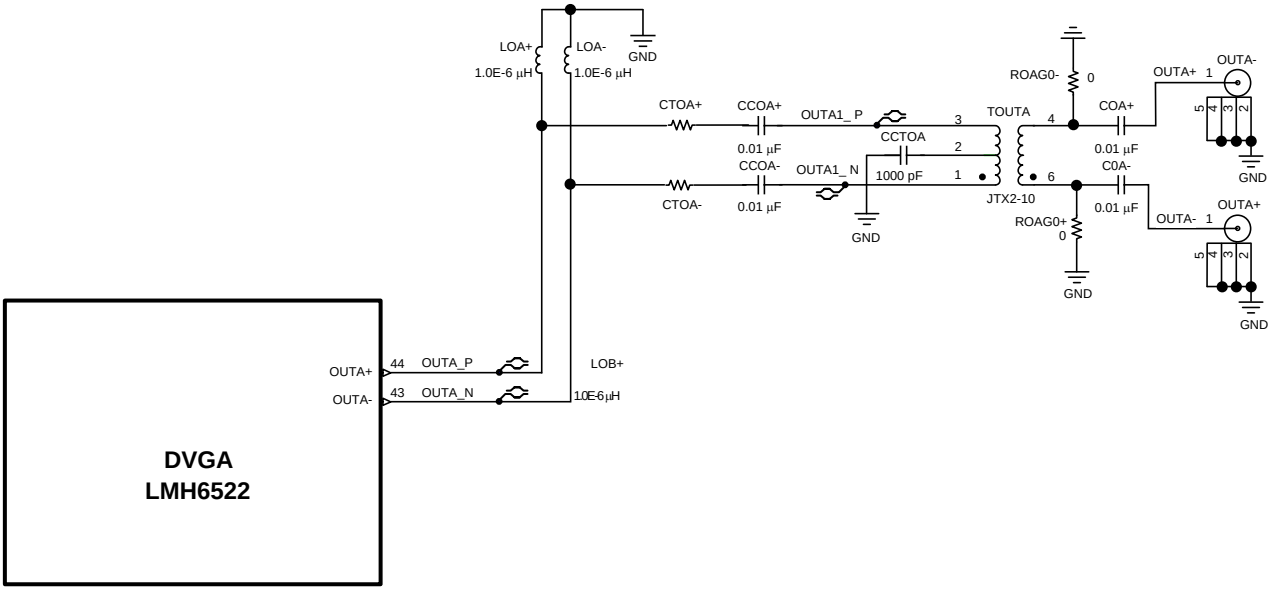


Figure 2. Output Schematic

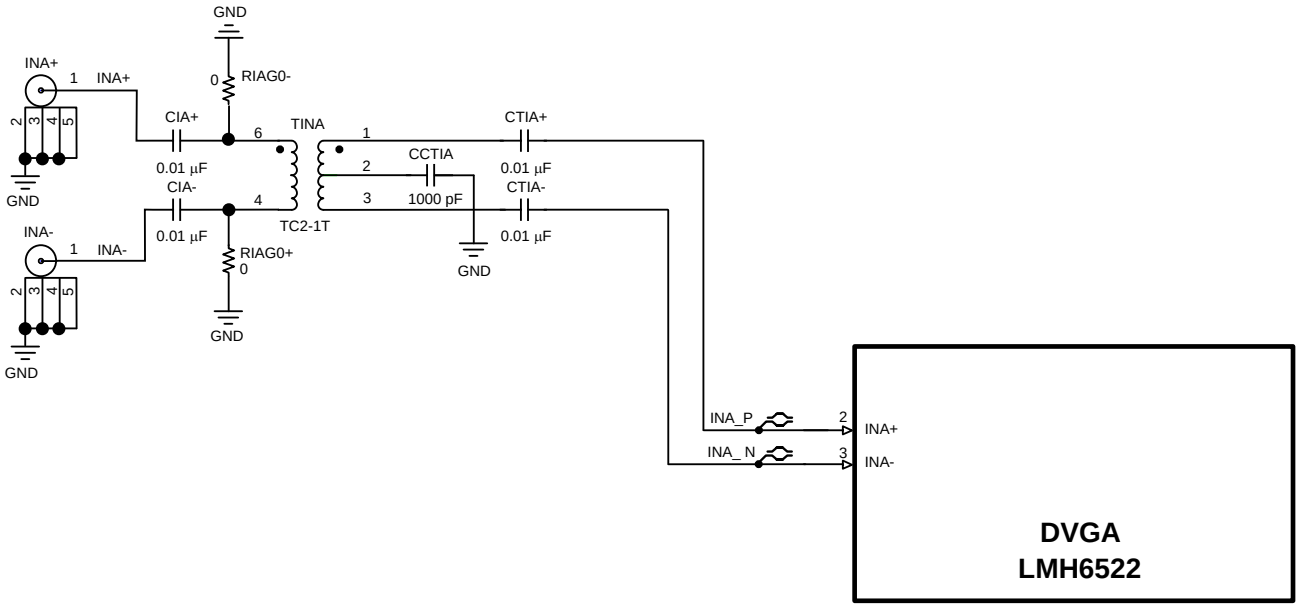


Figure 3. Input Schematic

3 Using with Differential Sources or Loads

The LMH6522EVAL board was designed to be easily modified by the customer for fully differential operation. To modify the board for differential operation it is necessary to remove the transformers and the resistors that ground the unused signal paths. Next, add coupling capacitors on the IN- and OUT+ signal lines, and finally place shorting jumpers across the appropriate transformer pads. At this point the LMH6522EVAL board will be configured for a 100 Ω differential signal path.

Other load conditions can also be easily matched by placing appropriate components on existing pads on the evaluation board. When changing components remember to keep the input path AC coupled so that the input common mode voltage is preserved.

4 Gain Control

For ease of use, banks of DIP switches are set up to control gain settings. For high speed interfacing to a logic analyzer there are also 0.1" header strips. The pin functions for these headers are shown in Table 1. For detailed instructions on the pin functions, see *LMH6522 High Performance Quad DVGA* (SNOSB53).

The dip switches settings will impact the on-board impedance for the J1 header pins. With the dip switches should be set to the OPEN position the header pins are unterminated. When the dip switches are closed the header pins are terminated with 49.9 Ω resistors. This would be the preferred setting for most high speed signal interfaces. For the absolute maximum voltage and current ratings of the digital pins, see the device-specific data sheet.

Table 1. Header Jack Pin Assignments (CONA. CONB, CONC, COND) (Pin 1 is pin closest to input connectors)

Header Pin	Parallel Function
1	Address bit 0
2	Address bit 1
3	Address bit 2
4	Address bit 3
5	Address bit 4
6	Ground
7	Enable (Tri State Pin)

5 SPI™ Compatible Gain Control Using the SPISU2 Card

The LMH6522_EVAL board can easily be controlled in the serial mode using a Texas Instruments SPISU2 USB to SPI controller card. This card and the required software are available on the TI website. Directions for installing the USB control software and evaluation board drivers are in the user's guide available in the document, SNLU086.

To use the SPI card, the LMH6522 DVGA must be put into serial mode. This is done by placing a shorting block on the MODE jumper pins which are located near the power connectors in the center of the board. Once this shorting block is in place the switches on the SWA switch block all need to be put in the OFF position. If the switches are in the ON position the digital lines will be grounded and the SPISU2 card will not be able to communicate with the DVGA.

Once the SPUSI2 board drivers and TinyI2CSPI software are installed, connect the SPUSI2 board directly onto the LMH6522_EVAL double-row header (J1) by aligning pin 1 as shown in Figure 4. Plug the USB cable into the SPISU2 card and the host PC. Start the TinyI2CSPI software and load the LMH6522 profile as shown in Figure 5. Additional commands can be generated by changing the data in the MOSI column. For details on the data to be sent to the DVGA registers, see the LMH6522 data sheet (SNOSB53). The example SPI commands are a good starting point for generating the desired commands.

SPISU2 Header Pins	Serial Function
1	Chip Select
2	Ground
3	Clock
4	N/A
5	Serial Data Out (MISO)
6	N/A
7	Serial Data IN (MOSI)
8 -14	N/A

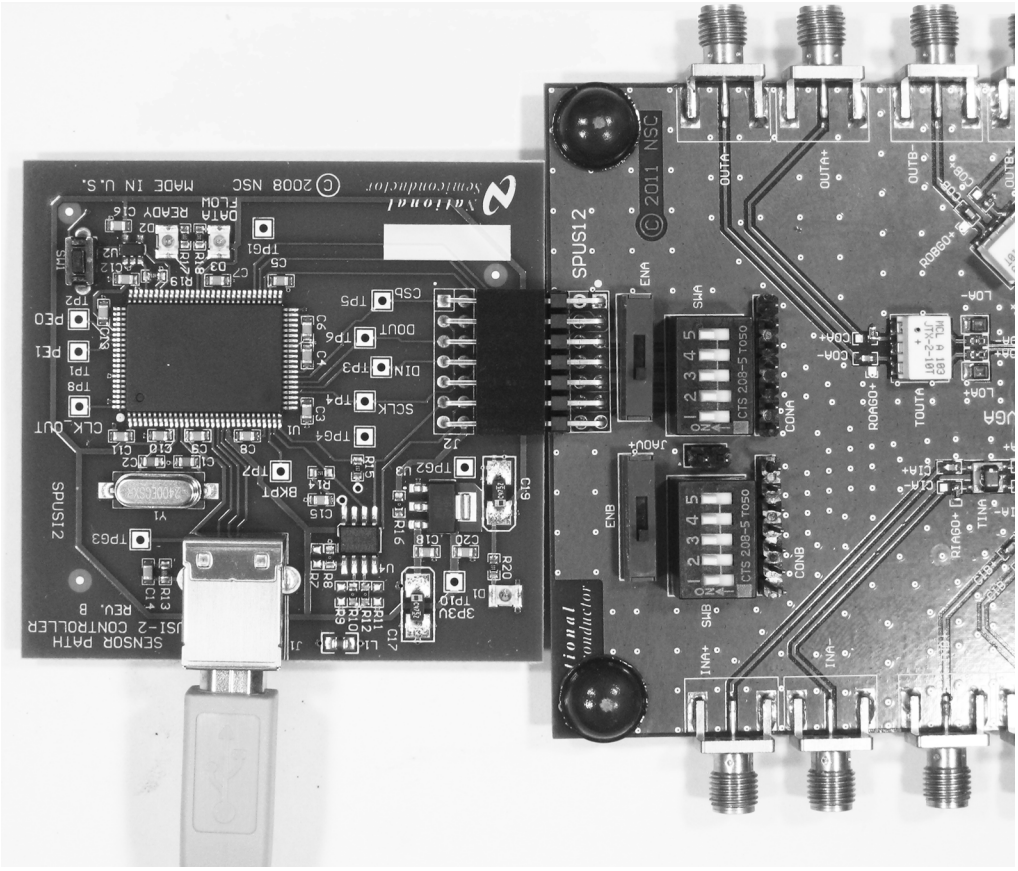
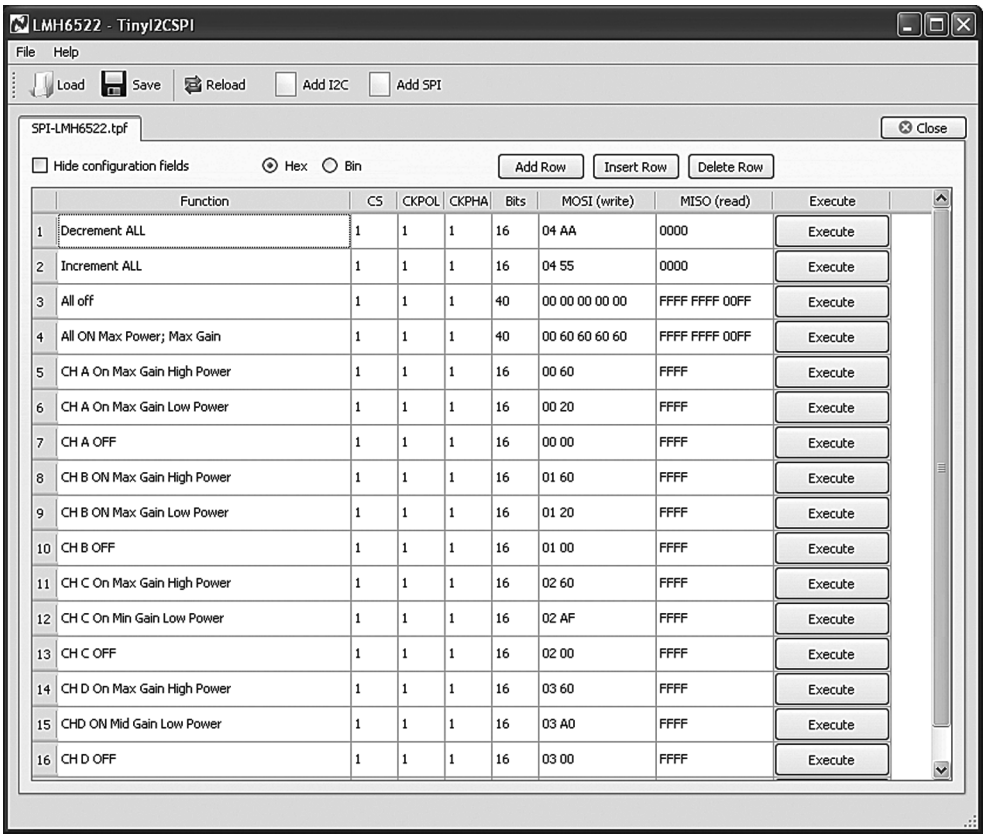


Figure 4. SPISU2 Card Connected to LMH6522EVAL Board



	Function	CS	CKPOL	CKPHA	Bits	MOSI (write)	MISO (read)	Execute
1	Decrement ALL	1	1	1	16	04 AA	0000	Execute
2	Increment ALL	1	1	1	16	04 55	0000	Execute
3	All off	1	1	1	40	00 00 00 00 00	FFFF FFFF 00FF	Execute
4	All ON Max Power; Max Gain	1	1	1	40	00 60 60 60 60	FFFF FFFF 00FF	Execute
5	CH A On Max Gain High Power	1	1	1	16	00 60	FFFF	Execute
6	CH A On Max Gain Low Power	1	1	1	16	00 20	FFFF	Execute
7	CH A OFF	1	1	1	16	00 00	FFFF	Execute
8	CH B ON Max Gain High Power	1	1	1	16	01 60	FFFF	Execute
9	CH B ON Max Gain Low Power	1	1	1	16	01 20	FFFF	Execute
10	CH B OFF	1	1	1	16	01 00	FFFF	Execute
11	CH C On Max Gain High Power	1	1	1	16	02 60	FFFF	Execute
12	CH C On Min Gain Low Power	1	1	1	16	02 AF	FFFF	Execute
13	CH C OFF	1	1	1	16	02 00	FFFF	Execute
14	CH D On Max Gain High Power	1	1	1	16	03 60	FFFF	Execute
15	CHD ON Mid Gain Low Power	1	1	1	16	03 A0	FFFF	Execute
16	CH D OFF	1	1	1	16	03 00	FFFF	Execute

Figure 5. TinyI2CSPI Settings

6 Additional Design Tools

The RD-179: High-IF Sub-sampling Receiver Subsystem board (SP16160CH1RB) is also available. This reference design includes the ADC16DV160 ADC, the LMH6517 DVGA, and the LMK04031B precision clock conditioner. Power regulation, filters and controlled impedance board layout are all provided in this reference design. Please visit the TI website for further details.

7 Board Layout

The LMH6522EVAL board has been designed to provide excellent signal integrity and has been thermally enhanced to provide for excellent heat dissipation. The LMH6522EVAL board has balanced differential signal traces as well as provision for using single ended test equipment.

The LMH6522 DVGA dissipates approximately 2.4W of power. To keep the amplifier cool, the LMH6522EVAL board uses eight layers of copper, many of which are solid ground planes connected directly to the LMH6522 exposed thermal pad. This provides excellent heat dissipation and eliminates the need for a heat sink. The board design files (in GERBER) format are available upon request.

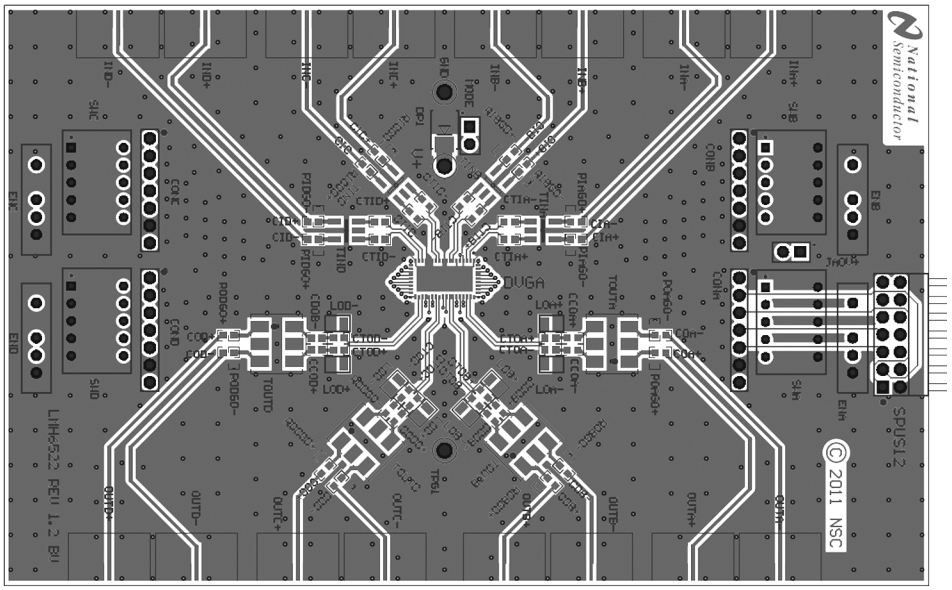


Figure 6. Evaluation Board Top Layer

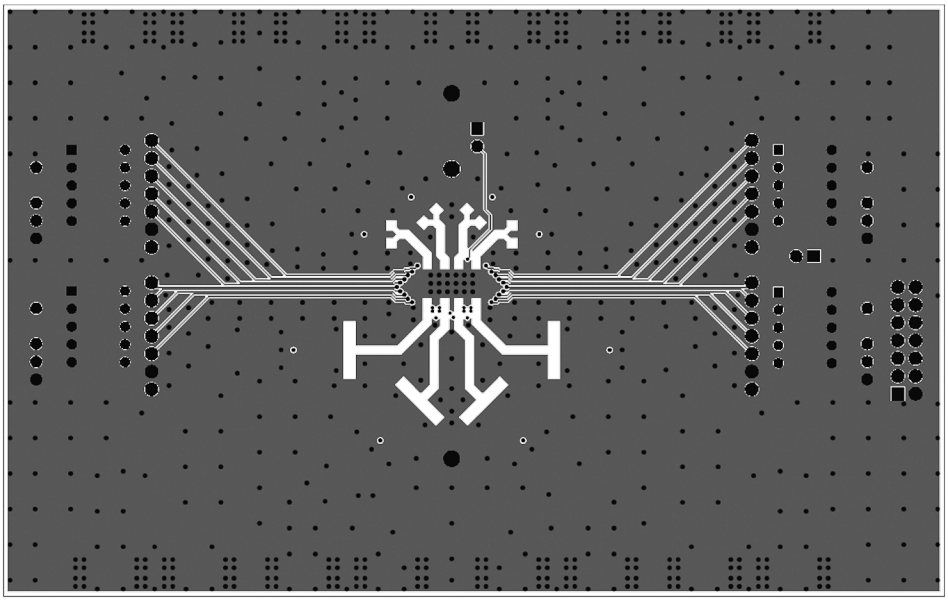


Figure 7. Layout Layer 2 (Showing Metal Removed from Under Input and Output Pins)

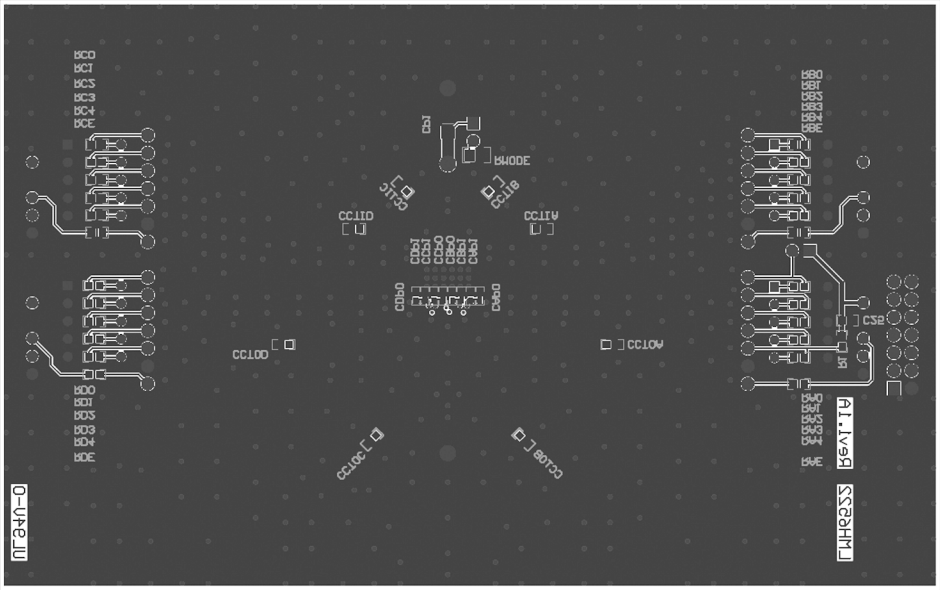


Figure 8. Evaluation Board Bottom Layer

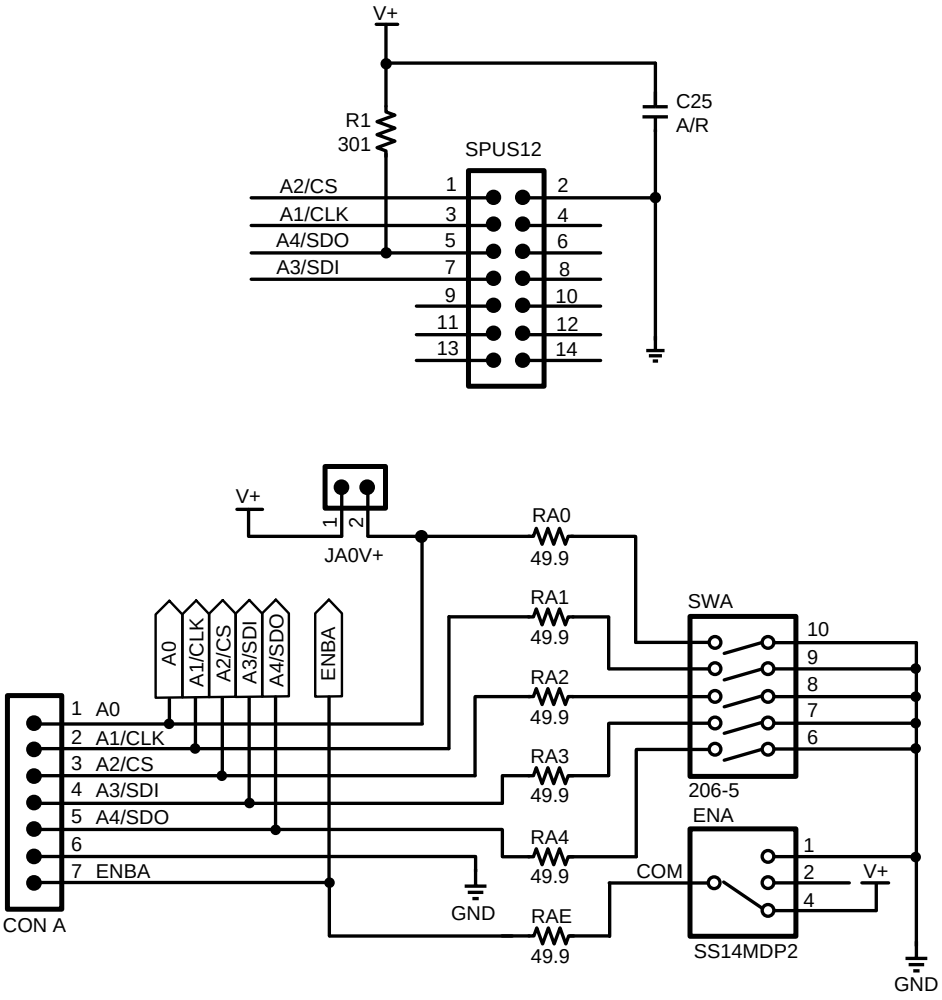


Figure 9. Logic Header Schematic

8 Signal Path Schematic

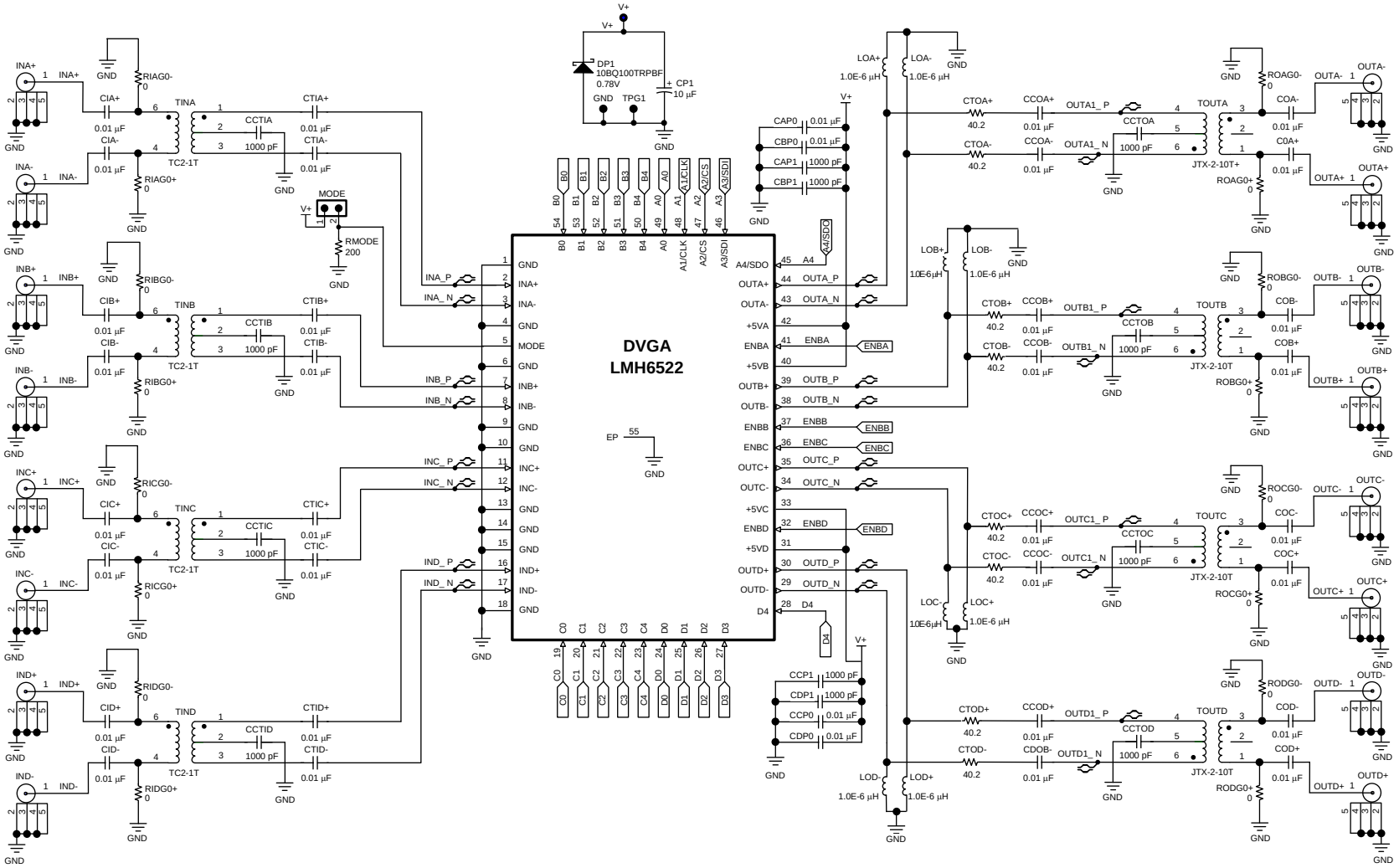


Figure 10. Signal Path Schematic

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