User's Guide

LM3000 Buck Controller Evaluation Module User's Guide

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1 Introduction

The LM3000 evaluation board is designed to provide the design engineer with a fully functional power converter-based solution using the LM3000 dual output emulated current mode controller. This evaluation board provides two output voltages of 3.3 V and 1.2 V. The 3.3-V output is designed to handle a maximum current of 8 A, whereas the 1.2-V output has a maximum current capability of 15 A. The switching frequency for the converter is set at 500 kHz. The gate signals for each output voltage will be 180 degree out of phase from each other. The printed circuit board consists of four layers of FR4 material with 2-ounce copper on top and bottom layer and 1-ounce copper for internal layers. This user's guide contains the evaluation board schematic, bill of materials (BOM), and a quick setup procedure. Refer to the *LM3000 Dual Synchronous Emulated Current-Mode Controller* data sheet for complete circuit design information.

The performance of the evaluation board is as follows:

Input Range	6 V to 18 V
Output voltage 1 (VO1)	3.3 V
Output current 1	0 A to 8 A
Output voltage 2 (VO2)	1.2 V
Output current 2	0 A to 15 A
Switching frequency	500 kHz
Load regulation	1%
Board size	2.68 × 3.146 × 0.068 inches

2 Powering and Loading Considerations

Read this entire page prior to attempting to power the evaluation board.

2.1 Quick Setup Procedure

1. Set the input power supply current limit to 10 A. Turn off the input power supply. Connect the input power supply to the VIN terminal. Make sure to connect power supply ground to each GND1 and GND2 terminals in order to provide a short path for input current to return to the power supply.
2. Connect the load with an 8-A capability on VO1 and 15-A capability on VO2. Connect the positive terminal to VO1 and VO2 and negative terminal to GND1 and GND2.
3. Connect a secondary power supply to EN1 and EN2 terminals. Set the power supply voltage to 5 V. The ground return for this power supply should be connected to GND terminal. Since the evaluation board is configured such that V_{OUT2} tracks V_{OUT1}, V_{OUT2} cannot be turned on without turning on V_{OUT1}. Different configuration can be required in order to turn on VOUT2 independently. This will be discussed later in Section 3.3.
4. Set V_{IN} to 12 V with no load being applied. Turn on the input power supply followed by the secondary power supply in order to power up the enable pins. The output voltage should be in regulation with a value of 3.3 V on VO1 and 1.2 V on VO2.
5. Slowly increase the load in each output into its maximum output current while monitoring the output voltages in each channel. The output voltages should also be in regulation at each respective maximum output current.
6. Slowly vary the input voltages from 6 V and 18.5 V. Both output voltages should remain in regulation with a nominal value of 3.3 V on VO1 and 1.2 V on VO2.

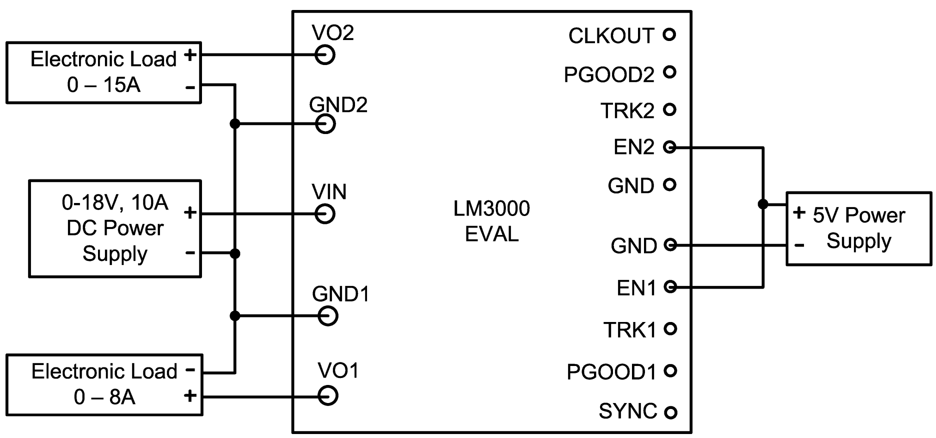

Figure 2-1. Basic Test Setup for LM3000EVAL Board

3 Board Configuration

3.1 External Clock Synchronization

A SYNC terminal has been provided in this evaluation board in order to synchronize the converter to an external clock or other fixed frequency signal from 200 kHz to 1.5 MHz. Refer to the *LM3000 Dual Synchronous Emulated Current-Mode Controller* data sheet for complete information.

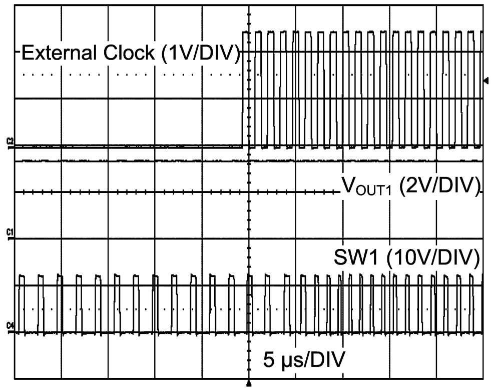

Figure 3-1. Synchronization at 3.3-V Output

3.2 CLKOUT

A CLKOUT terminal provides an external clock signal 90 degrees out of phase with the main clock. This clock signal can be used to synchronize a second LM3000.

3.3 Tracking

The LM3000 evaluation board is configured such that VOUT2 tracks VOUT1, while VOUT1 voltage increases with a rate determined by the value of C17, the soft-start capacitor for VOUT1 (Condition 1). This configuration will not allow VOUT2 to be turned on independently without turning on VOUT1. In order to track VOUT1, the TRK2 pin should be connected to a divider junction between R14 and R15 through R26.

When both outputs are used to track an external source (Condition 2), then R25, R26, and R28 should be left open and a 10-Ω resistor should be added into R24 and R27.

If no tracking feature is required, both TRK1 and TRK2 should then be tied to VDD in order to soft start each output voltage based on a soft-start capacitor value (Condition 3). This can be done by keeping R24, R26, and R27 open while adding a 10-Ω resistor onto R25 and R28.

Please note that the slew rate of track signal should be lower than the soft-start slew rate, which is set by soft-start capacitor value.

The following are the summary of different tracking configuration on the LM3000EVAL board:

Condition	R24	R25	R26	R27	R28
1	Open	10 Ω	10 Ω	Open	Open
2	10 Ω	Open	Open	10 Ω	Open
3	Open	10 Ω	Open	Open	10 Ω

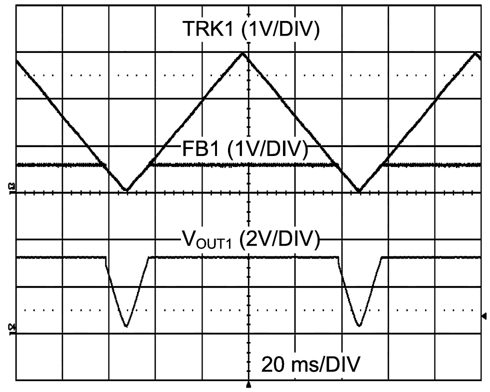

Figure 3-2. Tracking with an External Ramp for 3.3-V Output

3.4 Output Voltage Ripple

Output voltage ripple measurement should be taken directly across the output capacitor C21 or C22. Care has to be taken to minimize the loop area between the scope probe tip and the ground lead in order to minimize noise in the measurement. This can be achieved by removing the spring tip of the probe and ground lead and then wire a bare wire around the scope probe shaft. The bare wire should be in contact with the probe shaft because this is the “new” ground lead for the probe. The measurement can be taken by connecting the bare wire onto the ground side of the capacitor and the probe tip onto the other side of the capacitor. Figure 3-3 shows a diagram of this measurement technique.

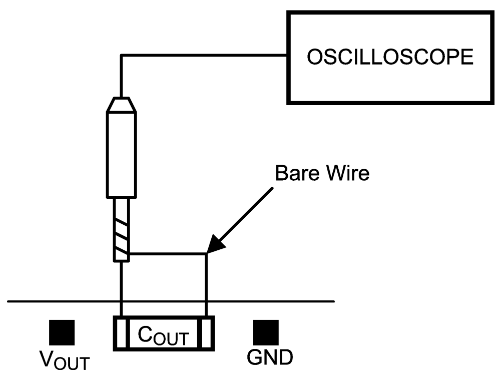

Figure 3-3. Output Voltage Ripple Measurement Setup

4 Typical Performance Waveforms

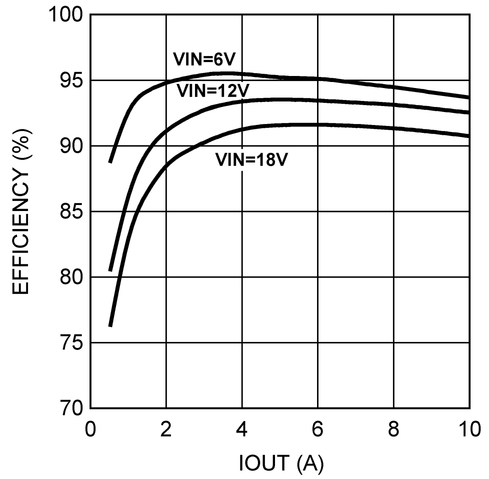

Figure 4-1. Efficiency of 3.3-V Output at 500 kHz

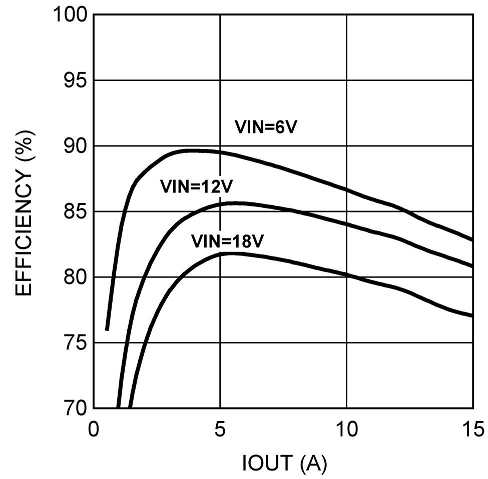

Figure 4-2. Efficiency of 1.2-V Output at 500 kHz

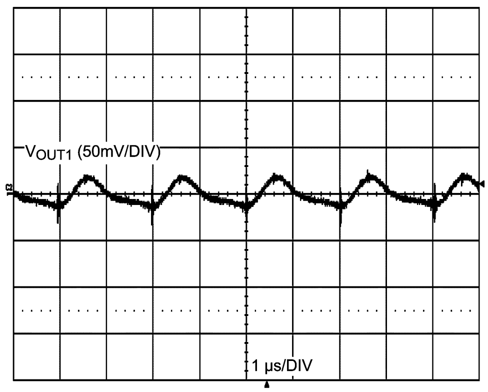

Figure 4-3. Output Ripple Voltage for 3.3-V Output at 8-A Load

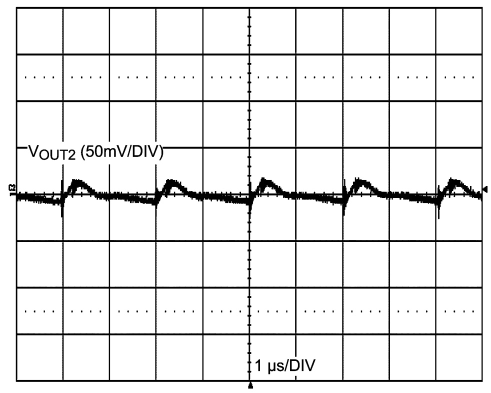

Figure 4-4. Output Ripple Voltage for 1.2-V Output at 15-A Load

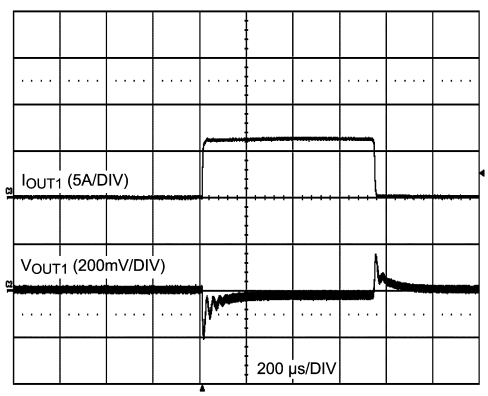

Figure 4-5. Output Load Transient from 0 A to 6 A for 3.3-V Output

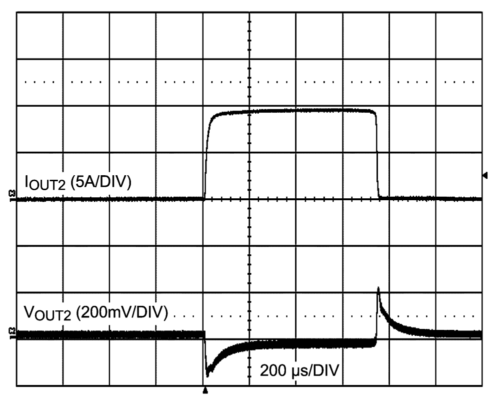

Figure 4-6. Output Load Transient from 0 A to 10 A for 1.2-V Output

5 Evaluation Board Schematic

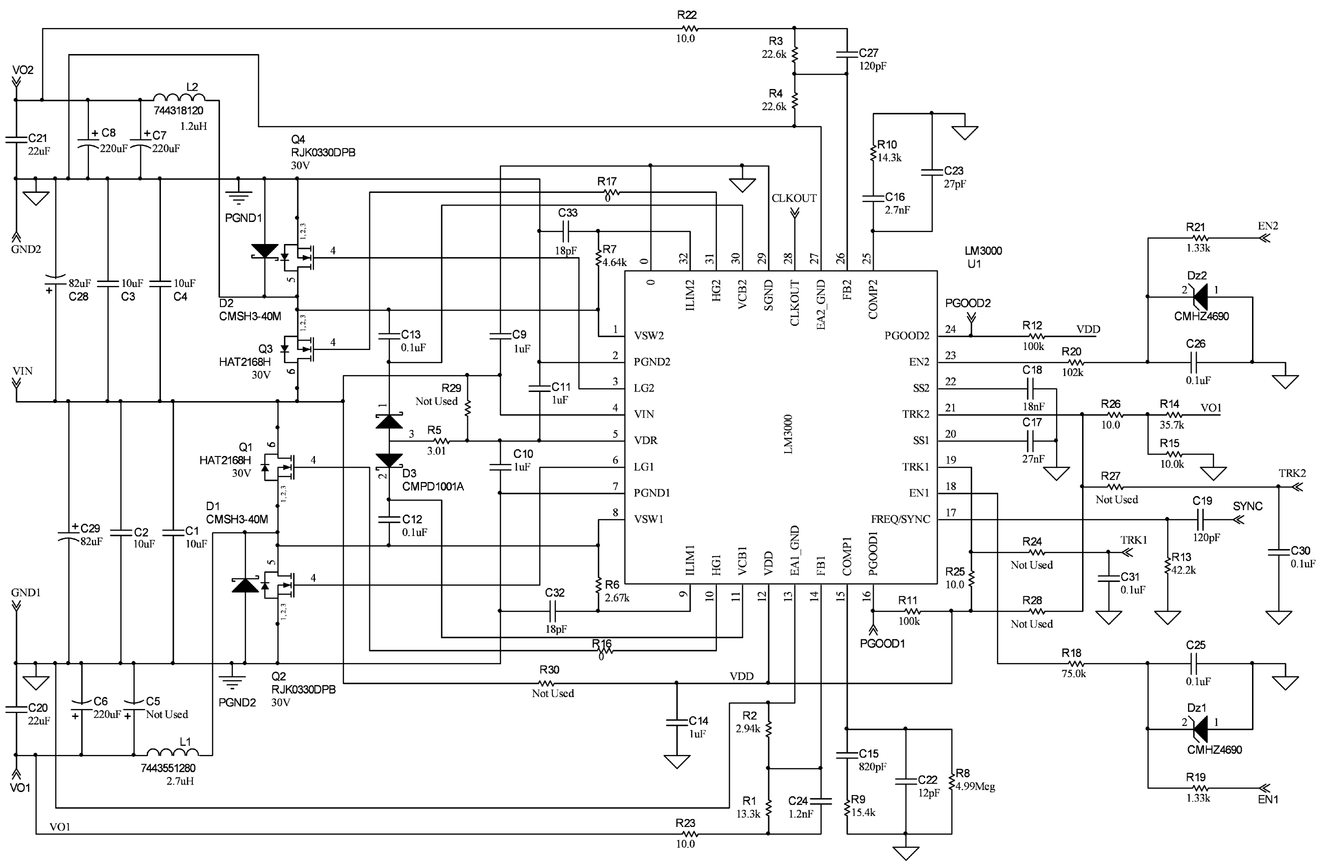

Figure 5-1. Evaluation Board Full Schematic

6 Bill of Materials

Table 6-1. Bill of Materials

ID	Part Number	Type	Size	Parameters	Qty	Vendor
C1, C2, C3, C4	GRM31CR6E106KA12L	Capacitor, Ceramic	1206	10 µF, 25 V, X5R, 10%	4	Murata
C5			7343-43	Not Used	0	
C6,C7, C8	EEF-UE0G221R	Capacitor, Polymer	7343-43	220 µF, 4 V, 12 mΩ	3	Panasonic
C9, C10, C11, C14	GRM188R61E105KA12D	Capacitor, Ceramic	0603	1 µF, 25 V, X5R, 10%	4	Murata
C12, C13, C30, C31	GRM188R71E104KA01D	Capacitor, Ceramic	0603	0.1 µF, 25 V, X7R, 10%	4	Murata
C15	VJ0603Y821KXXA	Capacitor, Ceramic	0603	820 pF, 25 V, X7R, 10%	1	Vishay
C16	VJ0603Y272KXXA	Capacitor, Ceramic	0603	2.7 nF, 25 V, X7R, 10%	1	Vishay
C17	06035C273KAT2A	Capacitor, Ceramic	0603	0.027 µF, 50 V, X7R, 10%	1	AVX
C18	VJ0603Y183KXXA	Capacitor, Ceramic	0603	18 nF, 25 V, X7R, 10%	1	Vishay
C19	VJ0603A121JXAA	Capacitor, Ceramic	0603	120 pF, 50 V, COG, 5%	1	Vishay
C20, C21	GRM31CR60J226KE19L	Capacitor, Ceramic	1206	22 µF, 6.3 V, X5R, 10%	2	Murata
C22	VJ0603A120KXAA	Capacitor, Ceramic	0603	12 pF, 50 V, COG, 5%	1	Vishay
C23	06031A270KAT2A	Capacitor, Ceramic	0603	27 pF, 100 V, COG, 10%	1	AVX
C24	06035C122KAT2A	Capacitor, Electrolytic	0603	1200 pF, 50 V, X7R, 10%	1	AVX
C25,C26	GRM188R71C104KA01D	Capacitor, Ceramic	0603	0.1 µF, 16 V, X7R, 10%	2	Murata
C27	06035A121JAT2A	Capacitor, Ceramic	0603	120 pF, 50 V, COG, 5%	1	AVX
C28, C29	EEEFK1H151P	Capacitor, Aluminum	10x10.2 mm	150 µF, 50 V, 670 mA	2	Panasonic
C32, C33	06031A180KAT2A	Capacitor, Ceramic	0603	18 pF, 100 V, COG, 10%	2	AVX
D1, D2	CMSH3-40M	Diode, Schottky	SMA	3 A, 40 V	2	Central Semiconductor
D3	CMPD1001A	Diode, Switching	SOT-23	250 mA, 90 V	1	Central Semiconductor
Dz1, Dz2	CMHZ4690	Diode, Zener	SOD-123	5.6 V, 500 mW	2	Central Semiconductor
L1	7443551280	Inductor		2.8 µH, 20 A, 3.8 mΩ	1	Wurth Elektronik
L2	744318120	Inductor		1.2 µH, 22 A, 1.79 mΩ	1	Wurth Elektronik
Q1, Q3	HAT2168H	N-CH MOSFET	LF-PAK	30 A, 30 V, 6 mΩ	2	Renesas Technology
Q2, Q4	RJK0330DPB	N-CH MOSFET	LF-PAK	45A, 30V, 2.1 mΩ	2	Renesas Technology
R1	CRCW060313k3FKEA	Resistor	0603	13.3 kΩ, 1%	1	Vishay
R2	CRCW06032k94FKEA	Resistor	0603	2.94 kΩ, 1%	1	Vishay
R3, R4	CRCW060322k6FKEA	Resistor	0603	22.6 kΩ, 1%	2	Vishay
R5	CRCW06033R01FNEA	Resistor	0603	3.01 Ω, 1%	1	Vishay
R6	CRCW06032k67FKEA	Resistor	0603	2.67 kΩ, 1%	1	Vishay
R7	CRCW06034k64FKEA	Resistor	0603	4.64 kΩ, 1%	1	Vishay
R8	CRCW06034M99FKEA	Resistor	0603	4.99 MΩ, 1%	1	Vishay
R9	CRCW060315k4FKEA	Resistor	0603	15.4 kΩ, 1%	1	Vishay
R10	CRCW060314k3FKEA	Resistor	0603	14.3 kΩ, 1%	1	Vishay
R11, R12	CRCW0603100kFKEA	Resistor	0603	100 kΩ, 1%	2	Vishay
R13	CRCW060342k2FKEA	Resistor	0603	42.2 kΩ, 1%	1	Vishay
R14	CRCW060335k7FKEA	Resistor	0603	35.7 kΩ, 1%	1	Vishay

Table 6-1. Bill of Materials (continued)

ID	Part Number	Type	Size	Parameters	Qty	Vendor
R15	CRCW060310k0FKEA	Resistor	0603	10 kΩ, 1%	1	Vishay
R16, R17	CRCW06030000Z0EA	Resistor	0603	0 Ω	2	Vishay
R18	CRCW060375k0FKEA	Resistor	0603	75 kΩ , 1%	1	Vishay
R19, R21	CRCW06031k33FKEA	Resistor	0603	1.33 kΩ, 1%	2	Vishay
R20	CRCW0603102kFKEA	Resistor	0603	102 kΩ, 1%	1	Vishay
R22, R23	CRCW040210R0FKED	Resistor	0402	10 Ω, 1%	2	Vishay
R24, R27, R28, R29, R30		Resistor	0603	Not Used		
R25, R26	CRC060310R0FKEA	Resistor	0603	10 Ω, 1%	2	Vishay
U1	LM3000	Controller	32 Lead WQFN		1	Texas Instruments
VIN, VO1, VO2, GND1, GND2	1514-2	Turret Terminal	0.090" diameter		5	Keystone
CLKOUT, PGOOD2, TRK2, EN2, GND	1573-2	Turret Terminal	0.072" diameter		5	Keystone
GND, EN1, TRK1, PGOOD1, SYNC	1573-2	Turret Terminal	0.072" diameter		5	Keystone

7 PCB Layout

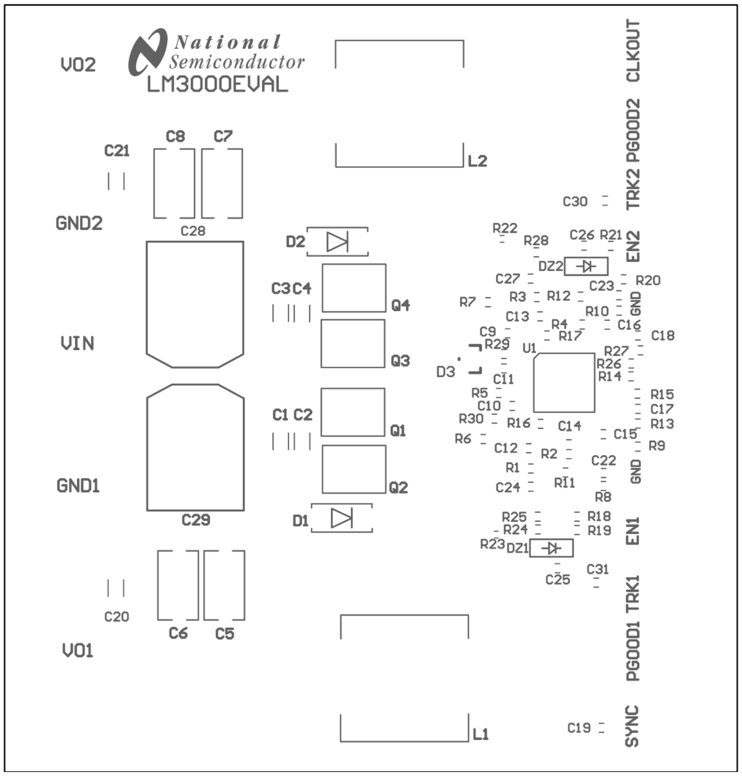

Figure 7-1. Top Overlay as Viewed from Top

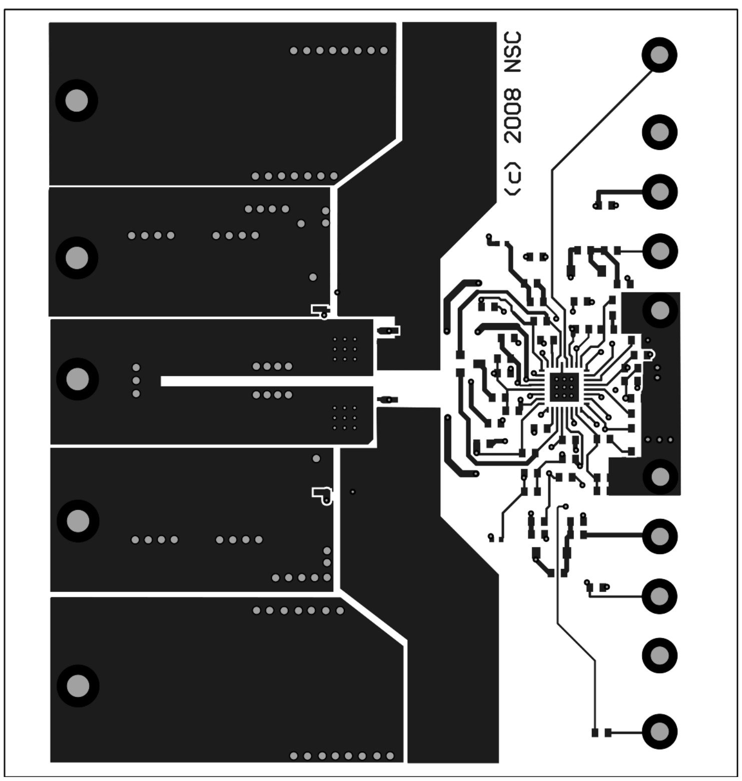

Figure 7-2. Top Layer as Viewed from Top

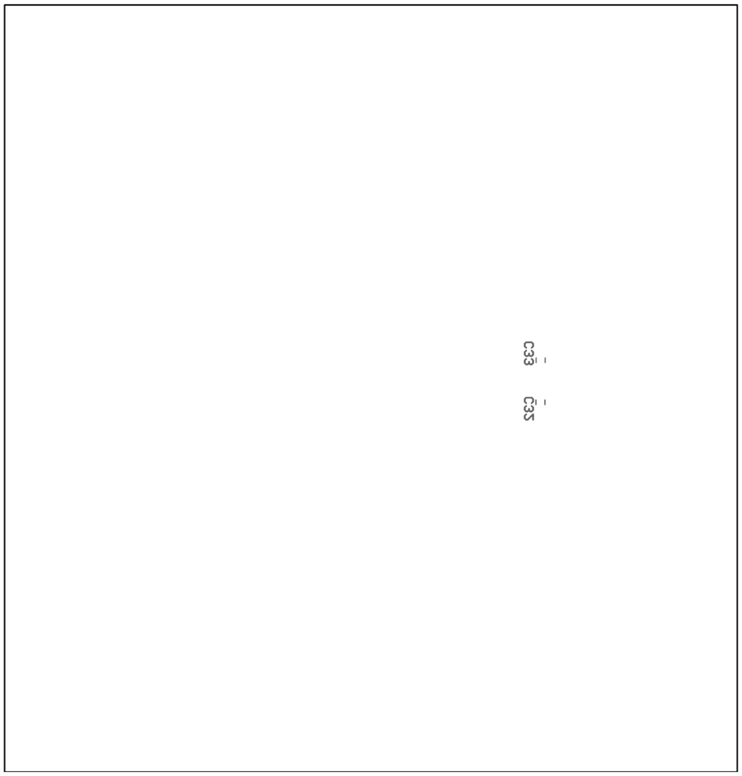

Figure 7-3. Bottom Overlay as Viewed from Top

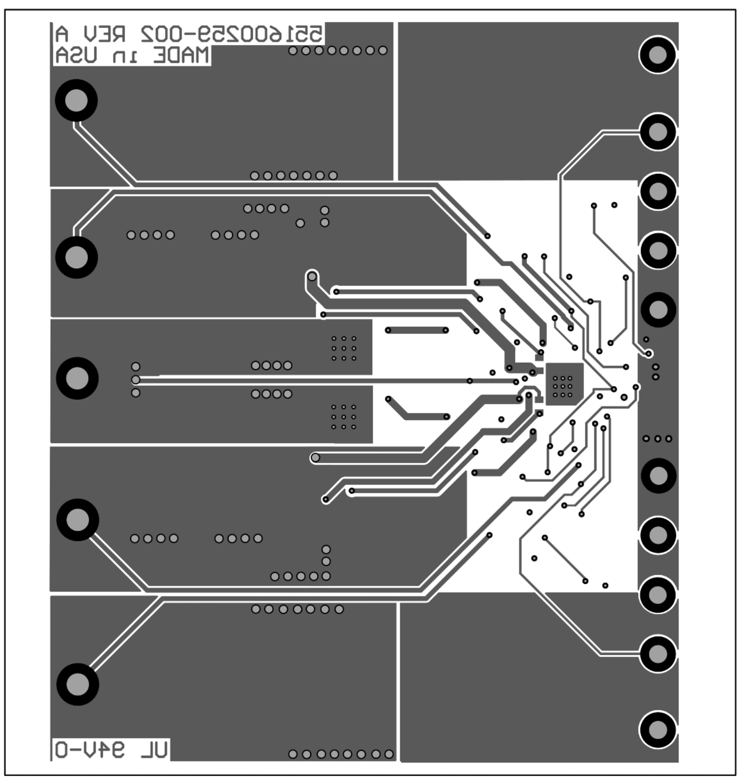

Figure 7-4. Bottom Layer as Viewed from Top

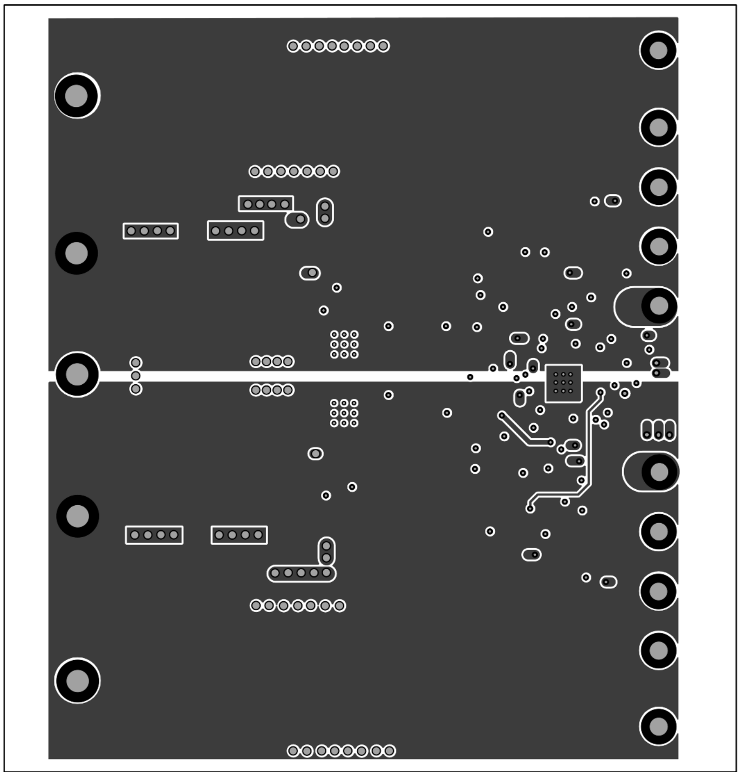

Figure 7-5. Internal Layer 1 as Viewed from Top

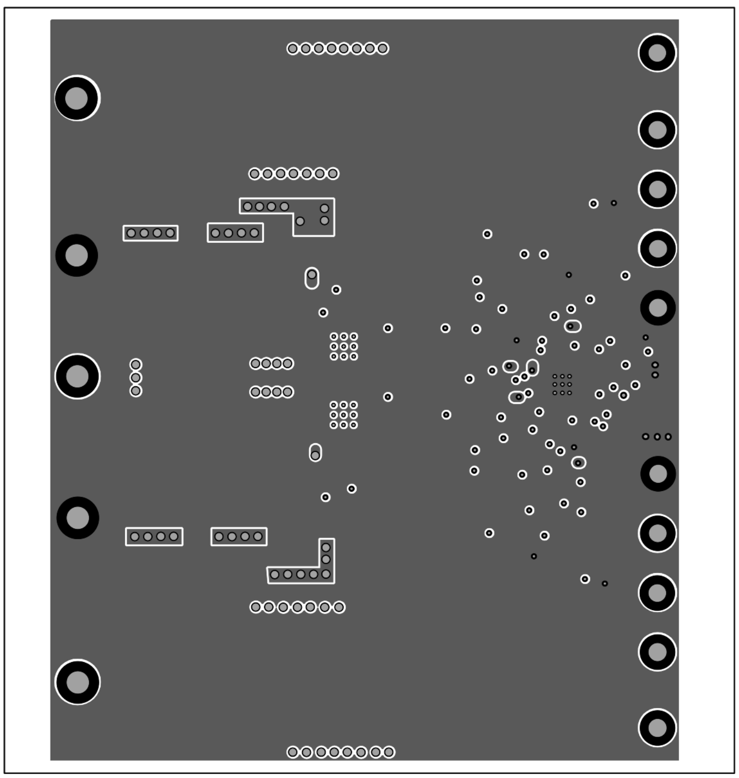

Figure 7-6. Internal Layer 2 as Viewed from Top

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2013) to Revision B (February 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title.. 2

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