ISL6261

Single-Phase Core Regulator for IMVP-6® Mobile CPUs

FN9251
Rev 1.00
Sep 27, 2006

The ISL6261 is a single-phase buck regulator implementing Intel® IMVP-6® protocol, with embedded gate drivers.

The heart of the ISL6261 is the patented R^3 Technology™, Intersil's Robust Ripple Regulator modulator. Compared with the traditional multi-phase buck regulator, the R^3 Technology™ has faster transient response. This is due to the R^3 modulator commanding variable switching frequency during a load transient.

Intel® Mobile Voltage Positioning (IMVP) is a smart voltage regulation technology effectively reducing power dissipation in Intel® Pentium processors. To boost battery life, the ISL6261 supports DPRSLRVR (deeper sleep) function and maximizes the efficiency via automatically changing operation modes. At heavy load in the active mode, the regulator commands the continuous conduction mode (CCM) operation. When the CPU enters deeper sleep mode, the ISL6261 enables diode emulation to maximize the efficiency at light load. Asserting the FDE pin of the ISL6261 in deeper sleep mode will further decrease the switching frequency at light load and increase the regulator efficiency.

A 7-bit digital-to-analog converter (DAC) allows dynamic adjustment of the core output voltage from 0.300V to 1.500V. The ISL6261 has 0.5% system voltage accuracy over temperature.

A unity-gain differential amplifier provides remote voltage sensing at the CPU die. This allows the voltage on the CPU die to be accurately measured and regulated per Intel® IMVP-6 specification. Current sensing can be implemented through either lossless inductor DCR sensing or precise resistor sensing. If DCR sensing is used, an NTC thermistor network will thermally compensates the gain and the time constant variations caused by the inductor DCR change.

Features

- Precision single-phase CORE voltage regulator
  - 0.5% system accuracy over temperature
  - Enhanced load line accuracy
- Internal gate driver with 2A driving capability
- Microprocessor voltage identification input
  - 7-Bit VID input
  - 0.300V to 1.500V in 12.5mV steps
  - Support VID change on-the-fly
- Multiple current sensing schemes supported
  - Lossless inductor DCR current sensing
  - Precision resistive current sensing
- Thermal monitor
- User programmable switching frequency
- Differential remote voltage sensing at CPU die
- Overvoltage, undervoltage, and overcurrent protection
- Pb-free plus anneal available (RoHS compliant)

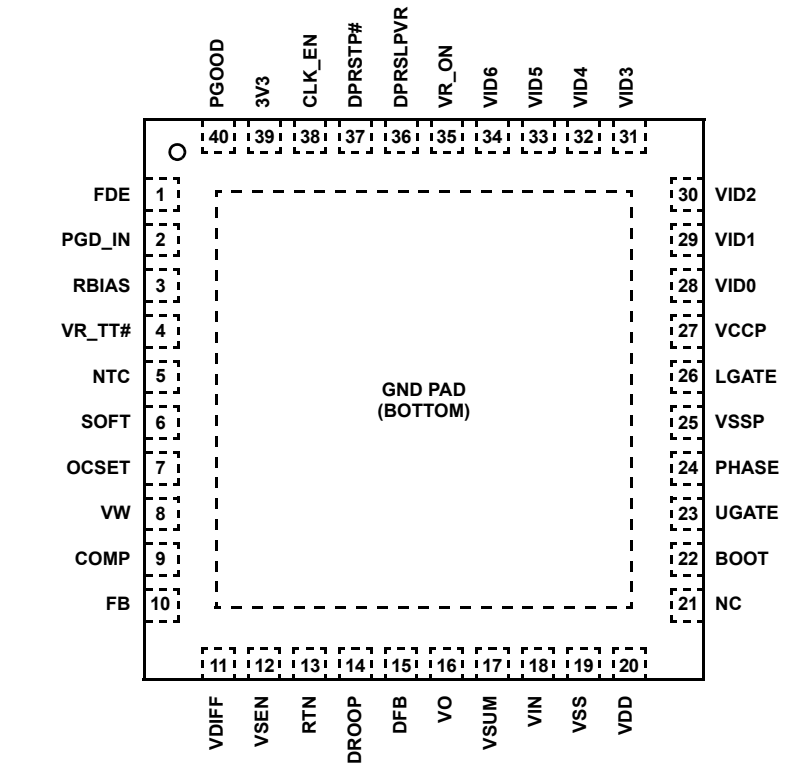
Ordering Information

PART NUMBER (NOTE)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-FREE)	PKG. DWG. #
ISL6261CRZ	ISL6261CRZ	-10 to +100	40 Ld 6x6 QFN	L40.6x6
ISL6261CRZ-T	ISL6261CRZ	-10 to +100	40 Ld 6x6 QFN, T&R	L40.6x6
ISL6261CR7Z	ISL6261CR7Z	-10 to +100	48 Ld 7x7 QFN	L48.7x7
ISL6261CR7Z-T	ISL6261CR7Z	-10 to +100	48 Ld 7x7 QFN, T&R	L48.7x7
ISL6261IRZ	ISL6261IRZ	-40 to +100	40 Ld 6x6 QFN	L40.6x6
ISL6261IRZ-T	ISL6261IRZ	-40 to +100	40 Ld 6x6 QFN, T&R	L40.6x6
ISL6261IR7Z	ISL6261IR7Z	-40 to +100	48 Ld 7x7 QFN	L48.7x7
ISL6261IR7Z-T	ISL6261IR7Z	-40 to +100	48 Ld 7x7 QFN, T&R	L48.7x7

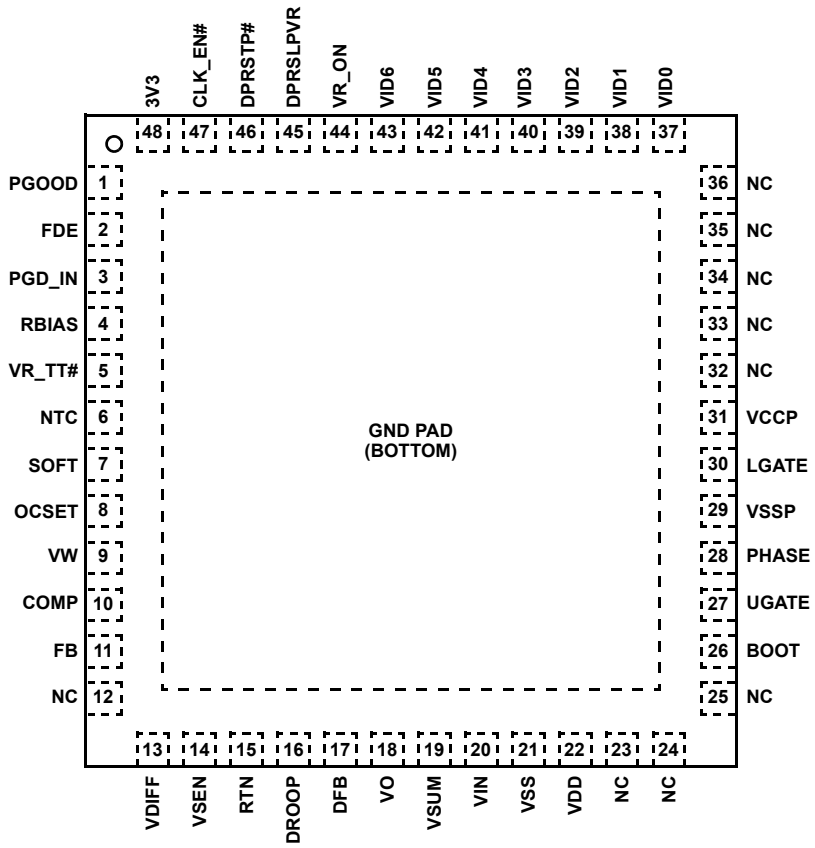
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

ISL6261
(40 LD QFN)



ISL6261
(48 LD QFN)



Absolute Maximum Ratings

Supply Voltage, VDD . . . . . -0.3 to +7V
Battery Voltage, VIN. . . . . .+28V
Boot Voltage (BOOT). . . . . -0.3V to +33V
Boot to Phase Voltage (BOOT-PHASE). . . . . -0.3V to +7V(DC)
. . . . . -0.3V to +9V(<10ns)
Phase Voltage (PHASE) . . . . . -7V (<20ns Pulse Width, 10µJ)
UGATE Voltage (UGATE) . . . . . PHASE-0.3V (DC) to BOOT
. . . . . PHASE-5V (<20ns Pulse Width, 10µJ) to BOOT
LGATE Voltage (LGATE) . . . . . -0.3V (DC) to VDD+0.3V
. . . . . -2.5V (<20ns Pulse Width, 5µJ) to VDD+0.3V
All Other Pins. . . . . -0.3V to (VDD +0.3V)
Open Drain Outputs, PGOOD, VR_TT# . . . . . -0.3 to +7V
HBM ESD Rating. . . . . >3kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
6x6 QFN Package (Notes 1, 2)	33	5.5
7x7 QFN Package (Notes 1, 2)	30	5.5

Maximum Junction Temperature . . . . . .+150°C
Maximum Storage Temperature Range. . . . . .-65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .+300°C

Recommended Operating Conditions

Supply Voltage, VDD . . . . . .+5V ±5%
Battery Voltage, VIN . . . . . .+5V to 21V
Ambient Temperature . . . . . .-10°C to +100°C
Junction Temperature . . . . . .-10°C to +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{DD} = 5V, T_A = -10°C to +100°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT POWER SUPPLY						
+5V Supply Current	I_{VDD}	VR_ON = 3.3V	-	3.1	3.6	mA
		VR_ON = 0V	-	-	1	µA
+3.3V Supply Current	I_{3V3}	No load on CLK_EN# pin	-	-	1	µA
Battery Supply Current at VIN pin	I_{VIN}	VR_ON = 0, VIN = 25V	-	-	1	µA
POR (Power-On Reset) Threshold	POR_r	V_{DD} Rising	-	4.35	4.5	V
	POR_f	V_{DD} Falling	3.85	4.1	-	V
SYSTEM AND REFERENCES						
System Accuracy	%Error (V_{cc_core})	No load, close loop, active mode, T_A = 0°C to +100°C, VID = 0.75-1.5V	-0.5	-	0.5	%
		VID = 0.5-0.7375V	-8	-	8	mV
		VID = 0.3-0.4875V	-15	-	15	mV
RBIAS Voltage	R_{RBIAS}	R_{RBIAS} = 147kΩ	1.45	1.47	1.49	V
Boot Voltage	V_{BOOT}		1.188	1.2	1.212	V
Maximum Output Voltage	V_{CC_CORE} (max)	VID = [0000000]	-	1.5	-	V
Minimum Output Voltage	V_{CC_CORE} (min)	VID = [1100000]	-	0.3	-	V
VID Off State		VID = [1111111]	-	0.0	-	V
CHANNEL FREQUENCY						
Nominal Channel Frequency	f_{SW}	R_{FSET} = 7kΩ, V_{comp} = 2V	-	333	-	kHz
Adjustment Range			200	-	500	kHz
AMPLIFIERS						
Droop Amplifier Offset			-0.3		0.3	mV
Error Amp DC Gain (Note 3)	A_{V0}		-	90	-	dB

Electrical Specifications V_{DD} = 5V, T_A = -10°C to +100°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amp Gain-Bandwidth Product (Note 3)	GBW	C_L = 20pF	-	18	-	MHz
Error Amp Slew Rate (Note 3)	SR	C_L = 20pF	-	5.0	-	V/µs
FB Input Current	$I_{IN(FB)}$		-	10	150	nA
SOFT-START CURRENT						
Soft-start Current	I_{SS}		-46	-41	-36	µA
Soft Geyserville Current	I_{GV}	|SOFT - REF|>100mV	±175	±200	±225	µA
Soft Deeper Sleep Entry Current	I_{C4}	DPRSLPVR = 3.3V	-46	-41	-36	µA
Soft Deeper Sleep Exit Current	I_{C4EA}	DPRSLPVR = 3.3V	36	41	46	µA
Soft Deeper Sleep Exit Current	I_{C4EB}	DPRSLPVR = 0V	175	200	225	µA
GATE DRIVER DRIVING CAPABILITY (Note 4)						
UGATE Source Resistance	$R_{SRC(UGATE)}$	500mA Source Current	-	1	1.5	Ω
UGATE Source Current	$I_{SRC(UGATE)}$	V_{UGATE_PHASE} = 2.5V	-	2	-	A
UGATE Sink Resistance	$R_{SNK(UGATE)}$	500mA Sink Current	-	1	1.5	Ω
UGATE Sink Current	$I_{SNK(UGATE)}$	V_{UGATE_PHASE} = 2.5V	-	2	-	A
LGATE Source Resistance	$R_{SRC(LGATE)}$	500mA Source Current	-	1	1.5	Ω
LGATE Source Current	$I_{SRC(LGATE)}$	V_{LGATE} = 2.5V	-	2	-	A
LGATE Sink Resistance	$R_{SNK(LGATE)}$	500mA Sink Current	-	0.5	0.9	Ω
LGATE Sink Current	$I_{SNK(LGATE)}$	V_{LGATE} = 2.5V	-	4	-	A
UGATE to PHASE Resistance	$R_{P(UGATE)}$		-	1.1	-	kΩ
GATE DRIVER SWITCHING TIMING (Refer to Timing Diagram)						
UGATE Turn-on Propagation Delay	t_{PDHU}	PV_{CC} = 5V, Output Unloaded	20	30	44	ns
LGATE Turn-on Propagation Delay	t_{PDHL}	PV_{CC} = 5V, Output Unloaded	7	15	30	ns
BOOTSTRAP DIODE						
Forward Voltage		V_{DDP} = 5V, Forward Bias Current = 2mA	0.43	0.58	0.67	V
Leakage		V_R = 16V	-	-	1	µA
POWER GOOD and PROTECTION MONITOR						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA	-	0.11	0.4	V
PGOOD Leakage Current	I_{OH}	P_{GOOD} = 3.3V	-1	-	1	µA
PGOOD Delay	tpgd	CLK_EN# Low to PGOOD High	5.5	6.8	8.1	ms
Overvoltage Threshold	O_{VH}	V_O rising above setpoint >1ms	160	200	240	mV
Severe Overvoltage Threshold	O_{VHS}	V_O rising above setpoint >0.5µs	1.675	1.7	1.725	V
OCSET Reference Current		I(Rbias) = 10µA	9.8	10	10.2	µA
OC Threshold Offset		DROOP rising above OCSET >120µs	-3.5		3.5	mV
Undervoltage Threshold (VDIFF-SOFT)	UV_f	V_O below set point for >1ms	-360	-300	-240	mV
LOGIC THRESHOLDS						
VR_ON, DPRSLPVR and PGD_IN Input Low	$V_{IL(3.3V)}$		-	-	1	V
VR_ON, DPRSLPVR and PGD_IN Input High	$V_{IH(3.3V)}$		2.3	-	-	V

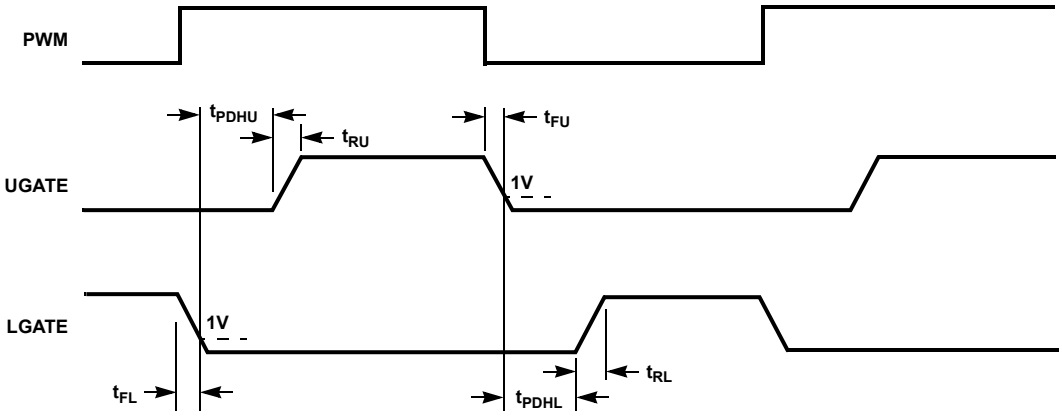
Electrical Specifications V_{DD} = 5V, T_A = -10°C to +100°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Leakage Current on VR_ON and PGD_IN	I_{IL}	Logic input is low	-1	0	-	µA
	I_{IH}	Logic input is high	-	0	1	µA
Leakage Current on DPRSLPVR	I_{IL_DPRSLP}	DPRSLPVR logic input is low	-1	0	-	µA
	I_{IH_DPRSLP}	DPRSLPVR logic input is high	-	0.45	1	µA
DAC(VID0-VID6), PSI# and DPRSTP# Input Low	$V_{IL(1.0V)}$		-	-	0.3	V
DAC(VID0-VID6), PSI# and DPRSTP# Input High	$V_{IH(1.0V)}$		0.7	-	-	V
Leakage Current of DAC(VID0-VID6) and DPRSTP#	I_{IL}	DPRSLPVR logic input is low	-1	0	-	µA
	I_{IH}	DPRSLPVR logic input is high	-	0.45	1	µA
THERMAL MONITOR						
NTC Source Current		NTC = 1.3V	53	60	67	µA
Over-temperature Threshold		V(NTC) falling	1.17	1.2	1.25	V
VR_TT# Low Output Resistance	R_{TT}	I = 20mA	-	5	9	
CLK_EN# OUTPUT LEVELS						
CLK_EN# High Output Voltage	V_{OH}	3V3 = 3.3V, I = -4mA	2.9	3.1	-	V
CLK_EN# Low Output Voltage	V_{OL}	$I_{CLK\_EN\#}$ = 4mA	-	0.18	0.4	V

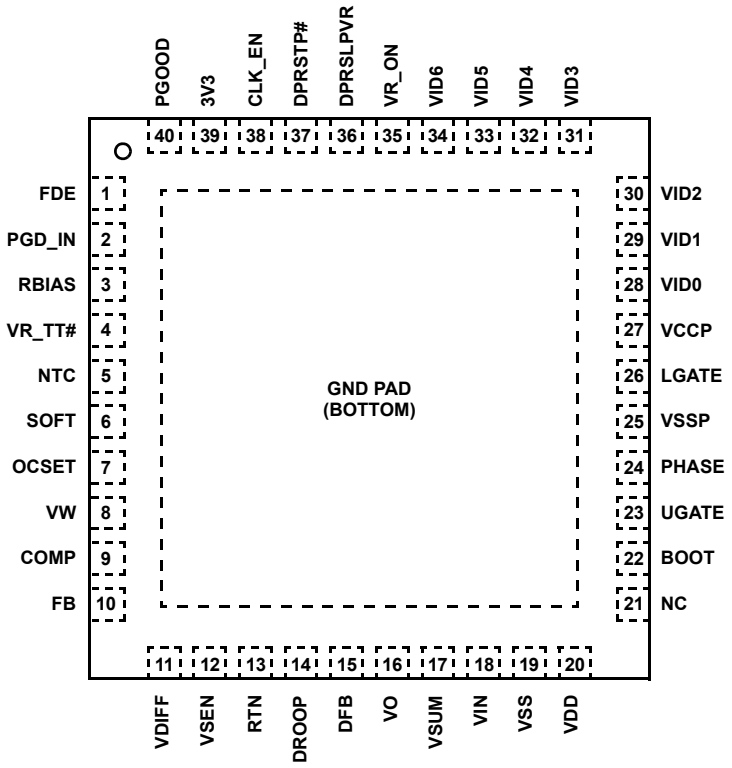
NOTES:

3. Guaranteed by characterization.
4. Guaranteed by design.

Gate Driver Timing Diagram



Functional Pin Description



FDE

Forced diode emulation enable signal. Logic high of FDE with logic low of DPRSTP# forces the ISL6261 to operate in diode emulation mode with an increased VW-COMP voltage window.

PGD_IN

Digital Input. Suggest connecting to MCH_PWRGD, which indicates that VCC_MCH voltage is within regulation.

RBIAS

A 147K resistor to VSS sets internal current reference.

VR_TT#

Thermal overload output indicator with open-drain output. Over-temperature pull-down resistance is 10.

NTC

Thermistor input to VR_TT# circuit and a 60µA current source is connected internally to this pin.

SOFT

A capacitor from this pin to GND pin sets the maximum slew rate of the output voltage. The SOFT pin is the non-inverting input of the error amplifier.

OCSET

Overcurrent set input. A resistor from this pin to VO sets DROOP voltage limit for OC trip. A 10µA current source is connected internally to this pin.

VW

A resistor from this pin to COMP programs the switching frequency (eg. 6.81K = 300kHz).

COMP

The output of the error amplifier.

FB

The inverting input of the error amplifier.

VDIFF

The output of the differential amplifier.

VSEN

Remote core voltage sense input.

RTN

Remote core voltage sense return.

DROOP

The output of the droop amplifier. DROOP-VO voltage is the droop voltage.

DFB

The inverting input of the droop amplifier.

VO

An input to the IC that reports the local output voltage.

VSUM

This pin is connected to one terminal of the capacitor in the current sensing R-C network.

VIN

Power stage input voltage. It is used for input voltage feed forward to improve the input line transient performance.

VSS

Signal ground. Connect to controller local ground.

VDD

5V control power supply.

BOOT

Upper gate driver supply voltage. An internal bootstrap diode is connected to the VCCP pin.

UGATE

The upper-side MOSFET gate signal.

PHASE

The phase node. This pin should connect to the source of upper MOSFET.

VSSP

The return path of the lower gate driver.

LGATE

The lower-side MOSFET gate signal.

VCCP

5V power supply for the gate driver.

NC

Not connected. Ground this pin in the practical layout.

VID0, VID1, VID2, VID3, VID4, VID5, VID6

VID input with VID0 as the least significant bit (LSB) and VID6 as the most significant bit (MSB).

VR_ON

VR enable pin. A logic high signal on this pin enables the regulator.

DPRSLPVR

Deeper sleep enable signal. A logic high indicates that the microprocessor is in Deeper Sleep Mode and also indicates a slow Vo slew rate with 41µA discharging or charging the SOFT cap.

DPRSTP#

Deeper sleep slow wake up signal. A logic low signal on this pin indicates that the microprocessor is in Deeper Sleep Mode.

CLK_EN#

Digital output for system PLL clock. Goes active 20µs after PGD_IN is active and Vcore is within 10% of boot voltage.

3V3

3.3V supply voltage for CLK_EN#.

PGOOD

Power good open-drain output. Needs to be pulled up externally by a 680 resistor to VCCP or 1.9k to 3.3V.

Function Block Diagram

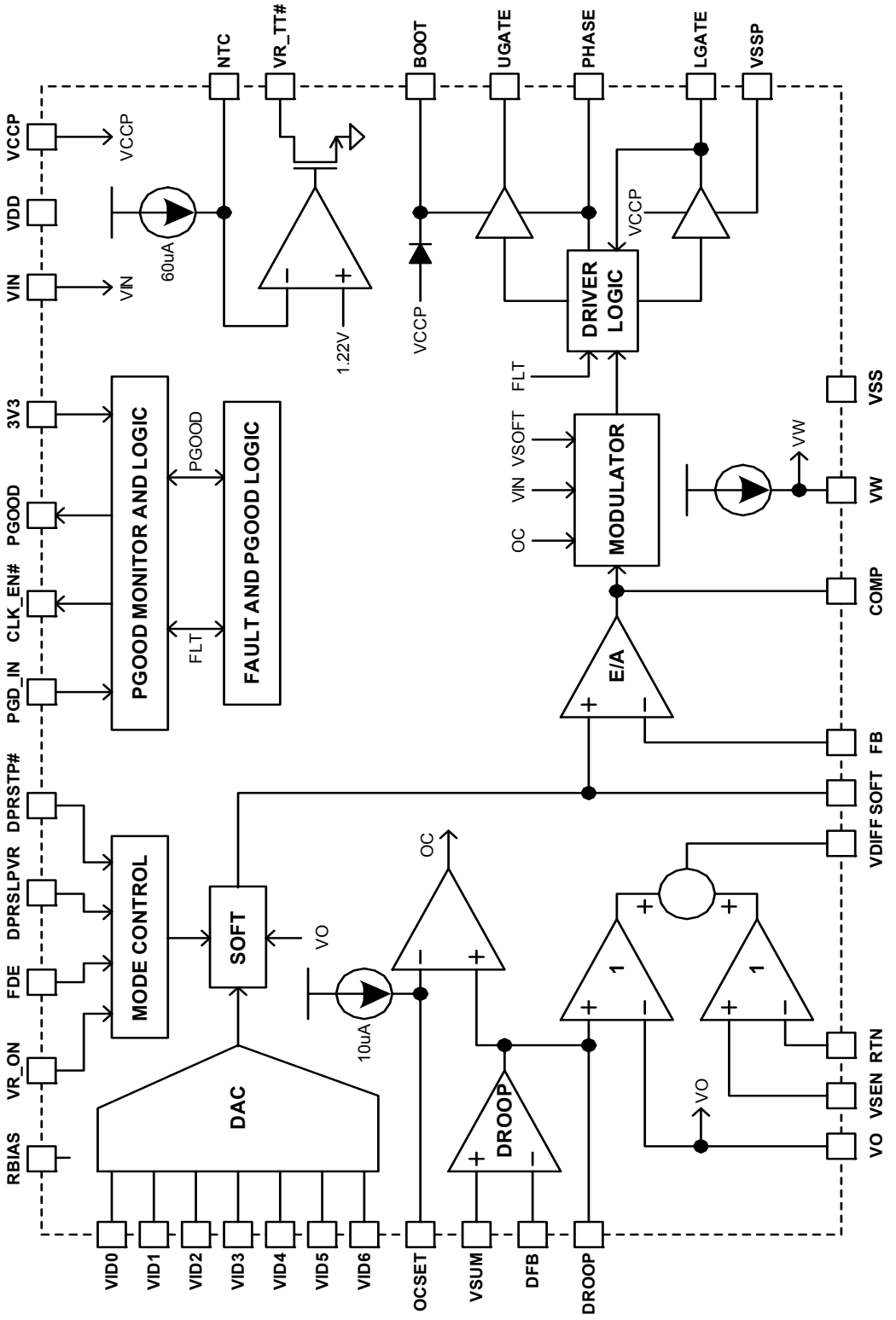


FIGURE 1. SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF ISL6261

Simplified Application Circuit for DCR Current Sensing

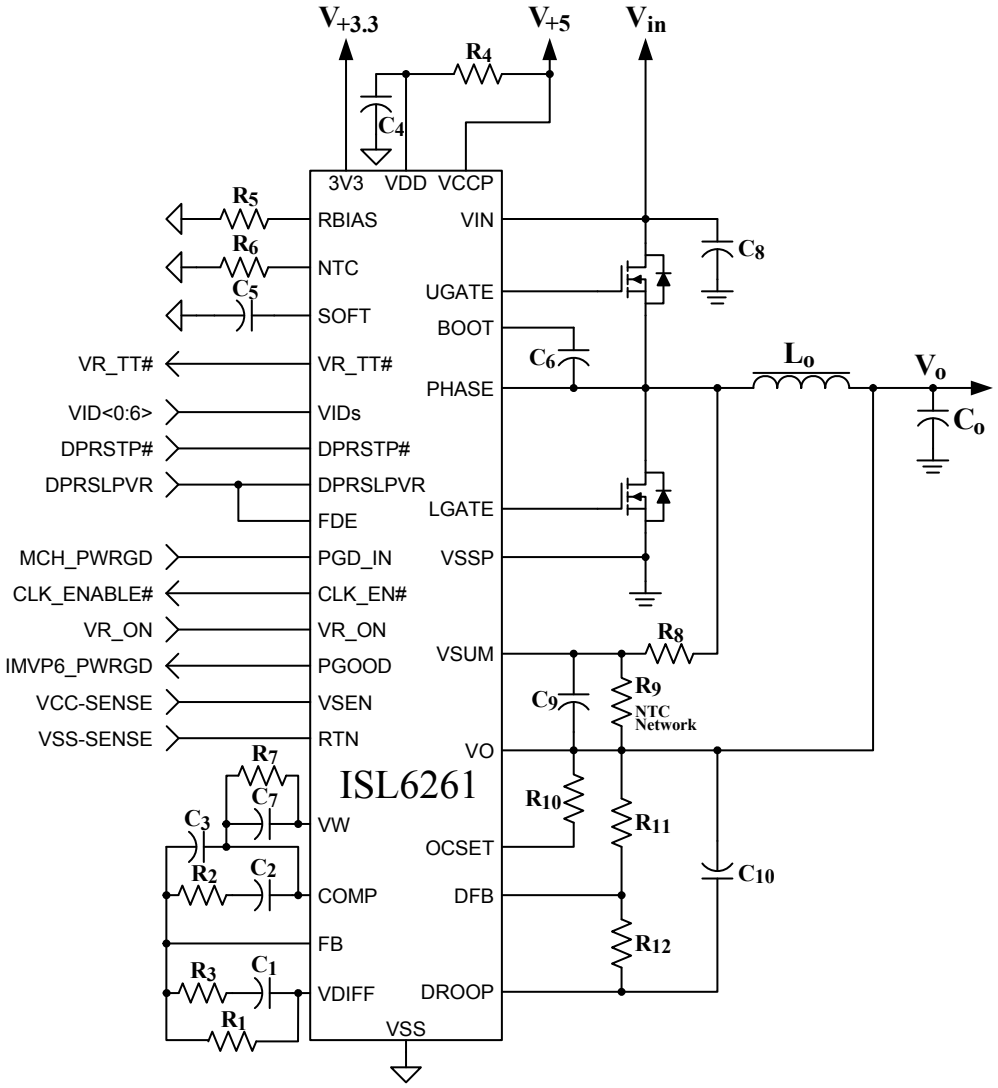


FIGURE 2. ISL6261-BASED IMVP-6® SOLUTION WITH INDUCTOR DCR CURRENT SENSING

Simplified Application Circuit for Resistive Current Sensing

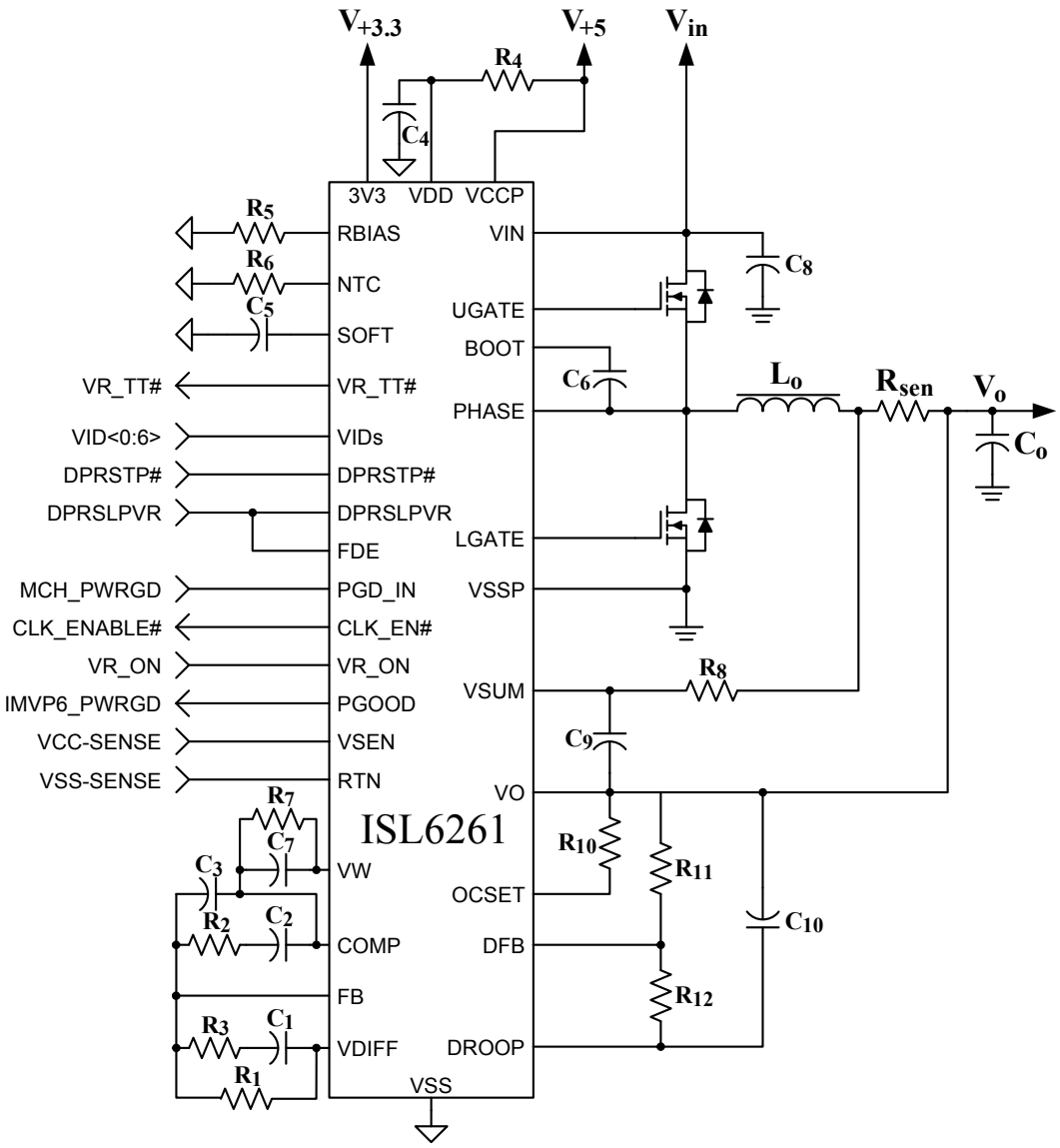


FIGURE 3. ISL6261-BASED IMVP-6® SOLUTION WITH RESISTIVE CURRENT SENSING

Theory of Operation

The ISL6261 is a single-phase regulator implementing Intel® IMVP-6® protocol and includes an integrated gate driver for reduced system cost and board area. The ISL6261 IMVP-6® solution provides optimum steady state and transient performance for microprocessor core voltage regulation applications up to 25A. Implementation of diode emulation mode (DEM) operation further enhances system efficiency.

The heart of the ISL6261 is the patented R^3 Technology™, Intersil's Robust Ripple Regulator modulator. The R^3™ modulator combines the best features of fixed frequency and hysteretic PWM controllers while eliminating many of their shortcomings. The ISL6261 modulator internally synthesizes an analog of the inductor ripple current and uses hysteretic comparators on those signals to establish PWM pulses. Operating on the large-amplitude and noise-free synthesized signals allows the ISL6261 to achieve lower output ripple and lower phase jitter than either conventional hysteretic or fixed frequency PWM controllers. Unlike conventional hysteretic converters, the ISL6261 has an error amplifier that allows the controller to maintain 0.5% voltage regulation accuracy throughout the VID range from 0.75V to 1.5V.

The hysteretic window voltage is with respect to the error amplifier output. Therefore the load current transient results in increased switching frequency, which gives the R^3™ regulator a faster response than conventional fixed frequency PWM regulators.

Start-up Timing

With the controller's VDD pin voltage above the POR threshold, the start-up sequence begins when VR_ON exceeds the 3.3V logic HIGH threshold. In approximately 100µs, SOFT and VO start ramping to the boot voltage of 1.2V. At startup, the regulator always operates in continuous current mode (CCM), regardless of the control signals. During this interval, the SOFT cap is charged by a 41µA current source. If the SOFT capacitor is 20nF, the SOFT ramp will be 2mV/µs for a soft-start time of 600µs. Once VO is within 10% of the boot voltage and PGD_IN is HIGH for six PWM cycles (20µs for 300kHz switching frequency), CLK_EN# is pulled LOW, and the SOFT cap is charged/discharged by approximate 200µA and VO slews at 10mV/µs to the voltage set by the VID pins. In approximately 7ms, PGOOD is asserted HIGH. Figure 4 shows typical startup timing.

PGD_IN Latch

It should be noted that PGD_IN going low will cause the converter to latch off. Toggling PGD_IN won't clear the latch. Toggling VR_ON will clear it. This feature allows the converter to respond to other system voltage outages immediately.

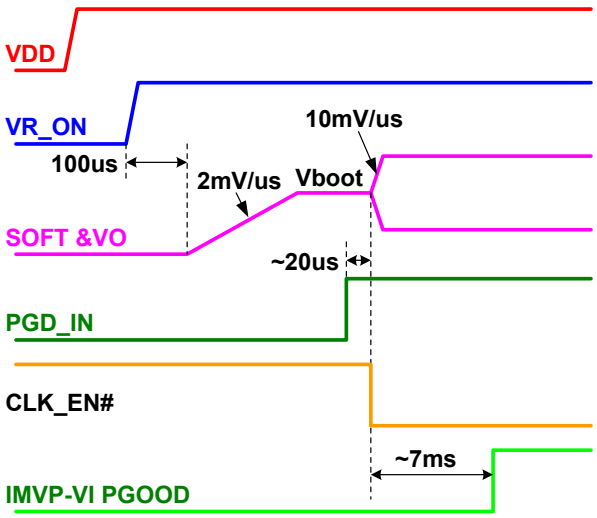


FIGURE 4. SOFT-START WAVEFORMS USING A 20nF SOFT CAPACITOR

Static Operation

After the startup sequence, the output voltage will be regulated to the value set by the VID inputs per Table 1, which is presented in the Intel® IMVP-6® specification. The ISL6261 regulates the output voltage with ±0.5% accuracy over the range of 0.7V to 1.5V.

A true differential amplifier remotely senses the core voltage to precisely control the voltage at the microprocessor die. VSEN and RTN pins are the inputs to the differential amplifier.

As the load current increases from zero, the output voltage droops from the VID value proportionally to achieve the IMVP-6® load line. The ISL6261 can sense the inductor current through the intrinsic series resistance of the inductors, as shown in Figure 2, or through a precise resistor in series with the inductor, as shown in Figure 3. The inductor current information is fed to the VSUM pin, which is the non-inverting input to the droop amplifier. The DROOP pin is the output of the droop amplifier, and DROOP-VO voltage is a high-bandwidth analog representation of the inductor current. This voltage is used as an input to a differential amplifier to achieve the IMVP-6® load line, and also as the input to the overcurrent protection circuit.

When using inductor DCR current sensing, an NTC thermistor is used to compensate the positive temperature coefficient of the copper winding resistance to maintain the load-line accuracy.

The switching frequency of the ISL6261 controller is set by the resistor R_{FSET} between pins VW and COMP, as shown in Figures 2 and 3.

TABLE 1. VID TABLE FROM INTEL IMVP-6 SPECIFICATION

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vo (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875

TABLE 1. VID TABLE FROM INTEL IMVP-6 SPECIFICATION (Continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vo (V)
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625

TABLE 1. VID TABLE FROM INTEL IMVP-6 SPECIFICATION (Continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vo (V)
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750

TABLE 1. VID TABLE FROM INTEL IMVP-6 SPECIFICATION (Continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vo (V)
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000

TABLE 2. CONTROL SIGNAL TRUTH TABLES FOR OPERATIONAL MODES OF ISL6261

	DPRSTP#	FDE	DPRSLPVR	OPERATIONAL MODE	VW-COMP WINDOW VOLTAGE INCREASE
Control Signal Logic	0	0	0	Forced CCM	0%
	0	0	1	Diode Emulation Mode	0%
	0	1	x	Enhanced Diode Emulation Mode	33%
	1	x	x	Forced CCM	0%

High Efficiency Operation Mode

The operational modes of the ISL6261 depend on the control signal states of DPRSTP#, FDE, and DPRSLPVR, as shown in Table 2. These control signals can be tied to Intel® IMVP-6® control signals to maintain the optimal system configuration for all IMVP-6® conditions.

DPRSTP# = 0, FDE = 0 and DPRSLPVR = 1 enables the ISL6261 to operate in diode emulation mode (DEM) by monitoring the low-side FET current. In diode emulation mode, when the low-side FET current flows from source to drain, it turns on as a synchronous FET to reduce the conduction loss. When the current reverses its direction trying to flow from drain to source, the ISL6261 turns off the low-side FET to prevent the output capacitor from discharging through the inductor, therefore eliminating the extra conduction loss. When DEM is enabled, the regulator works in automatic discontinuous conduction mode (DCM), meaning that the regulator operates in CCM in heavy load, and operates in DCM in light load. DCM in light load decreases the switching frequency to increase efficiency. This mode can be used to support the deeper sleep mode of the microprocessor.

DPRSTP# = 0 and FDE = 1 enables the enhanced diode emulation mode (EDEM), which increases the VW-COMP window voltage by 33%. This further decreases the switching frequency at light load to boost efficiency in the deeper sleep mode.

For other combinations of DPRSTP#, FDE, and DPRSLPVR, the ISL6261 operates in forced CCM.

The ISL6261 operational modes can be set according to CPU mode signals to achieve the best performance. There are two options: (1) Tie FDE to DPRSLPVR, and tie DPRSTP# and DPRSLPVR to the corresponding CPU mode signals. This configuration enables EDEM in deeper sleep mode to increase efficiency. (2) Tie FDE to “1” and DPRSTP# to “0” permanently, and tie DPRSLPVR to the corresponding CPU mode signal. This configuration sets the regulator in EDEM all the time. The regulator will enter DCM based on load current. Light-load efficiency is increased in both active mode and deeper sleep mode.

CPU mode-transition sequences often occur in concert with VID changes. The ISL6261 employs carefully designed mode-transition timing to work in concert with the VID changes.

The ISL6261 is equipped with internal counters to prevent control signal glitches from triggering unintended mode transitions. For example: Control signals lasting less than seven switching periods will not enable the diode emulation mode.

Dynamic Operation

The ISL6261 responds to VID changes by slewing to new voltages with a dv/dt set by the SOFT capacitor and the logic of DPRSLPVR. If C_{SOFT} = 20nF and DPRSLPVR = 0, the output voltage will move at a maximum dv/dt of ±10mV/µs for large changes. The maximum dv/dt can be used to achieve fast recovery from Deeper Sleep to Active mode. If C_{SOFT} = 20nF and DPRSLPVR = 1, the output voltage will move at a dv/dt of ±2mV/µs for large changes. The slow dv/dt into and out of deeper sleep mode will minimize the audible noise. As the output voltage approaches the VID command value, the dv/dt moderates to prevent overshoot. The ISL6261 is IMVP-6® compliant for DPRSTP# and DPRSLPVR logic.

Intersil R^3™ has an intrinsic voltage feed forward function. High-speed input voltage transients have little effect on the output voltage.

Intersil R^3™ commands variable switching frequency during transients to achieve fast response. Upon load application, the ISL6261 will transiently increase the switching frequency to deliver energy to the output more quickly. Compared with steady state operation, the PWM pulses during load application are generated earlier, which effectively increases the duty cycle and the response speed of the regulator. Upon load release, the ILS6261 will transiently decrease the switching frequency to effectively reduce the duty cycle to achieve fast response.

TABLE 3. FAULT-PROTECTION SUMMARY OF ISL6261

FAULT TYPE	FAULT DURATION PRIOR TO PROTECTION	PROTECTION ACTIONS	FAULT RESET
Overcurrent fault	120µs	PWM tri-state, PGOOD latched low	VR_ON toggle or VDD toggle
Way-Overcurrent fault	< 2µs	PWM tri-state, PGOOD latched low	VR_ON toggle or VDD toggle
Overvoltage fault (1.7V)	Immediately	Low-side FET on until Vcore < 0.85V, then PWM tri-state, PGOOD latched low (OV-1.7V always)	VDD toggle
Overvoltage fault (+200mV)	1ms	PWM tri-state, PGOOD latched low	VR_ON toggle or VDD toggle
Undervoltage fault (-300mV)	1ms	PWM tri-state, PGOOD latched low	VR_ON toggle or VDD toggle
Over-temperature fault (NTC<1.18)	Immediately	VR_TT# goes high	N/A

Protection

The ISL6261 provides overcurrent (OC), overvoltage (OV), undervoltage (UV) and over-temperature (OT) protections as shown in Table 3.

Overcurrent is detected through the droop voltage, which is designed as described in the “Component Selection and Application” section. The OCSET resistor sets the overcurrent protection level. An overcurrent fault will be declared when the droop voltage exceeds the overcurrent set point for more than 120µs. A way-overcurrent fault will be declared in less than 2µs when the droop voltage exceeds twice the overcurrent set point. In both cases, the UGATE and LGATE outputs will be tri-stated and PGOOD will go low.

The over-current condition is detected through the droop voltage. The droop voltage is equal to $I_{core} \times R_{droop}$, where R_{droop} is the load line slope. A 10µA current source flows out of the OCSET pin and creates a voltage drop across R_{OCSET} (shown as R_{10} in Figure 2). Overcurrent is detected when the droop voltage exceeds the voltage across R_{OCSET}. Equation 1 gives the selection of R_{OCSET}.

$$R_{OCSET} = \frac{I_{OC} \times R_{droop}}{10\mu A} \quad \text{(EQ. 1)}$$

For example: The desired over current trip level, I_{oc}, is 30A, R_{droop} is 2.1mΩ, Equation 1 gives R_{OCSET} = 6.3k.

Undervoltage protection is independent of the overcurrent limit. A UV fault is declared when the output voltage is lower than (VID-300mV) for more than 1ms. The gate driver outputs will be tri-stated and PGOOD will go low. Note that a practical core regulator design usually trips OC before it trips UV.

There are two levels of overvoltage protection and response. An OV fault is declared when the output voltage exceeds the VID by +200mV for more than 1ms. The gate driver outputs will be tri-stated and PGOOD will go low. The inductor current will decay through the low-side FET body diode. Toggling of VR_ON or bringing VDD below 4V will reset the fault latch. A way-overvoltage (WOV) fault is declared immediately when the output voltage exceeds 1.7V. The ISL6261 will latch PGOOD low and turn on the low-side FETs. The low-side FETs will remain on until the output voltage drops below approximately 0.85V, then all the FETs are turned off. If the output voltage again rises above 1.7V, the protection process repeats. This mechanism provides maximum protection against a shorted high-side FET while preventing the output from ringing below ground. Toggling VR_ON cannot reset the WOV protection; recycling VDD will reset it. The WOV detector is active all the time, even when other faults are declared, so the processor is still protected against the high-side FET leakage while the FETs are commanded off.

The ISL6261 has a thermal throttling feature. If the voltage on the NTC pin goes below the 1.2V over-temperature threshold, the VR_TT# pin is pulled low indicating the need for thermal throttling to the system oversight processor. No other action is taken within the ISL6261.

Component Selection and Application

Soft-Start and Mode Change Slew Rates

The ISL6261 commands two different output voltage slew rates for various modes of operation. The slow slew rate reduces the inrush current during startup and the audible noise during the entry and the exit of Deeper Sleep Mode. The fast slew rate enhances the system performance by achieving active mode regulation quickly during the exit of Deeper Sleep Mode. The SOFT current is bidirectional — charging the SOFT capacitor when the output voltage is commanded to rise, and discharging the SOFT capacitor when the output voltage is commanded to fall.

Figure 5 shows the circuitry on the SOFT pin. The SOFT pin, the non-inverting input of the error amplifier, is connected to ground through capacitor C_{SOFT}. I_{SS} is an internal current source connected to the SOFT pin to charge or discharge C_{SOFT}. The ISL6261 controls the output voltage slew rate by connecting or disconnecting another internal current source I_Z to the SOFT pin, depending on the state of the system, i.e. Startup or Active mode, and the logic state on the DPRSLPVR pin. The SOFT-START CURRENT section of the Electrical Specification Table shows the specs of these two current sources.

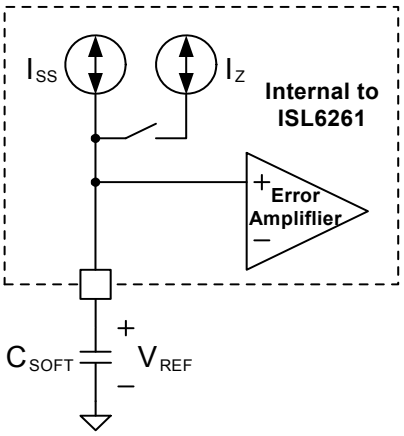


FIGURE 5. SOFT PIN CURRENT SOURCES FOR FAST AND SLOW SLEW RATES

I_{SS} is 41µA typical and is used during startup and mode changes. When connected to the SOFT pin, I_Z adds to I_{SS} to get a larger current, labelled I_{GV} in the Electrical Specification Table, on the SOFT pin. I_{GV} is typically 200µA with a minimum of 175µA.

The IMVP-6® specification reveals the critical timing associated with regulating the output voltage. SLEWRATE,

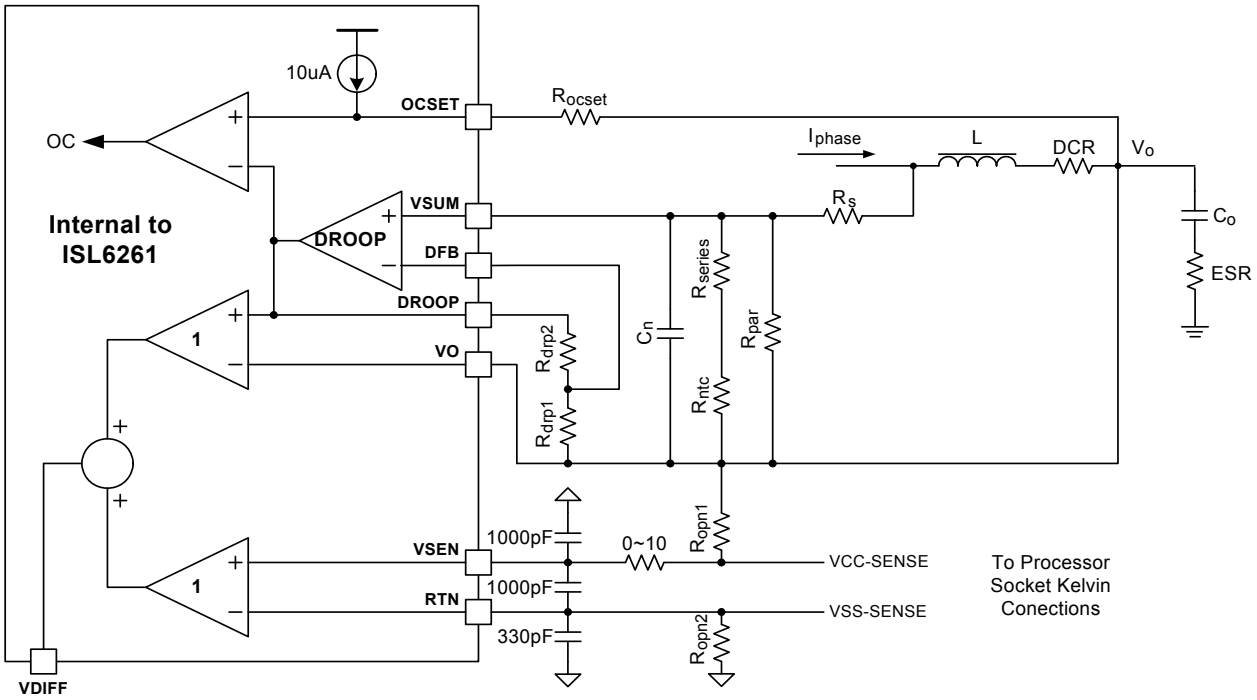


FIGURE 6. SIMPLIFIED VOLTAGE DROOP CIRCUIT WITH CPU-DIE VOLTAGE SENSING AND INDUCTOR DCR CURRENT SENSING

given in the IMVP-6® specification, determines the choice of the SOFT capacitor, C_{SOFT}, through the following equation:

$$C_{SOFT} = \frac{I_{GV}}{SLEWRATE} \quad \text{(EQ. 2)}$$

If SLEWRATE is 10mV/µs, and I_{GV} is typically 200µA, C_{SOFT} is calculated as

$$C_{SOFT} = 200\mu A/(10mV/\mu s) = 20nF \quad \text{(EQ. 3)}$$

Choosing 0.015µF will guarantee 10mV/µs SLEWRATE at minimum I_{GV} value. This choice of C_{SOFT} controls the startup slew rate as well. One should expect the output voltage to slew to the Boot value of 1.2V at a rate given by the following equation:

$$\frac{dV_{soft}}{dt} = \frac{I_{ss}}{C_{SOFT}} = \frac{41\mu A}{0.015\mu F} = 2.8\,mV/\mu s \quad \text{(EQ. 4)}$$

Selecting Rbias

To properly bias the ISL6261, a reference current needs to be derived by connecting a 147k, 1% tolerance resistor from the RBIAS pin to ground. This provides a very accurate 10µA current source from which OCSET reference current is derived.

Caution should used in layout: This resistor should be placed in the close proximity of the RBIAS pin and be connected to good quality signal ground. Do not connect any other components to this pin, as they will negatively impact the performance. Capacitance on this pin may create instabilities and should be avoided.

Startup Operation - CLK_EN# and PGOOD

The ISL6261 provides a 3.3V logic output pin for CLK_EN#. The system 3.3V voltage source connects to the 3V3 pin, which powers internal circuitry that is solely devoted to the CLK_EN# function. The output is a CMOS signal with 4mA sourcing and sinking capability. CMOS logic eliminates the need for an external pull-up resistor on this pin, eliminating the loss on the pull-up resistor caused by CLK_EN# being low in normal operation. This prolongs battery run time. The 3.3V supply should be decoupled to digital ground, not to analog ground, for noise immunity.

At startup, CLK_EN# remains high until 20µs after PGD_IN going high, and Vcc-core is regulated at the Boot voltage. The ISL6261 triggers an internal timer for the IMVP6_PWRGD signal (PGOOD pin). This timer allows PGOOD to go high approximately 7ms after CLK_EN# goes low.

Static Mode of Operation - Processor Die Sensing

Remote sensing enables the ISL6261 to regulate the core voltage at a remote sensing point, which compensates for various resistive voltage drops in the power delivery path.

The VSEN and RTN pins of the ISL6261 are connected to Kelvin sense leads at the die of the processor through the processor socket. (The signal names are Vcc_sense and Vss_sense respectively). Processor die sensing allows the voltage regulator to tightly control the processor voltage at the die, free of the inconsistencies and the voltage drops due to layouts. The Kelvin sense technique provides for extremely tight load line regulation at the processor die side.

These traces should be laid out as noise sensitive traces. For optimum load line regulation performance, the traces connecting these two pins to the Kelvin sense leads of the processor should be laid out away from rapidly rising voltage nodes (switching nodes) and other noisy traces. Common mode and differential mode filters are recommended as shown in Figure 6. The recommended filter resistance range is 0~10Ω so it does not interact with the 50k input resistance of the differential amplifier. The filter resistor may be inserted between VCC-SENSE and the VSEN pin. Another option is to place one between VCC-SENSE and the VSEN pin and another between VSS-SENSE and the RTN pin. The need of these filters also depends on the actual board layout and the noise environment.

Since the voltage feedback is sensed at the processor die, if the CPU is not installed, the regulator will drive the output voltage all the way up to damage the output capacitors due to lack of output voltage feedback. Ropn1 and Ropn2 are recommended, as shown in Figure 6, to prevent this potential issue. Ropn1 and Ropn2, typically ranging 20~100Ω, provide voltage feedback from the regulator local output in the absence of the CPU.

Setting the Switching Frequency - FSET

The R^3 modulator scheme is not a fixed frequency PWM architecture. The switching frequency increases during the application of a load to improve transient performance.

It also varies slightly depending on the input and output voltages and output current, but this variation is normally less than 10% in continuous conduction mode.

Resistor R_{fset} (R_7 in Figure 2), connected between the VW and COMP pins of the ISL6261, sets the synthetic ripple window voltage, and therefore sets the switching frequency. This relationship between the resistance and the switching frequency in CCM is approximately given by the following equation.

$$R_{fset}(k\Omega) = (period(\mu s) - 0.29) \times 2.33 \quad \text{(EQ. 5)}$$

In diode emulation mode, the ISL6261 stretches the switching period. The switching frequency decreases as the load becomes lighter. Diode emulation mode reduces the switching loss at light load, which is important in conserving battery power.

Voltage Regulator Thermal Throttling

Intel® IMVP-6® technology supports thermal throttling of the processor to prevent catastrophic thermal damage to the voltage regulator. The ISL6261A features a thermal monitor sensing the voltage across an externally placed negative temperature coefficient (NTC) thermistor. Proper selection and placement of the NTC thermistor allows for detection of a designated temperature rise by the system.

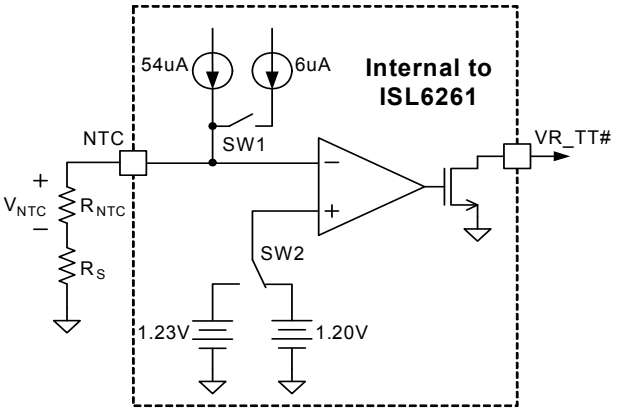


FIGURE 7. CIRCUITRY ASSOCIATED WITH THE THERMAL THROTTLING FEATURE

Figure 7 shows the circuitry associated with the thermal throttling feature of the ISL6261. At low temperature, SW1 is on and SW2 connects to the 1.20V side. The total current going into the NTC pin is 60µA. The voltage on the NTC pin is higher than 1.20V threshold voltage and the comparator output is low. VR_TT# is pulled up high by an external resistor. Temperature increase will decrease the NTC thermistor resistance. This decreases the NTC pin voltage. When the NTC pin voltage drops below 1.2V, the comparator output goes high to pull VR_TT# low, signalling a thermal throttle. In addition, SW1 turns off and SW2 connects to 1.23V, which decreases the NTC pin current by 6µA and increases the threshold voltage by 30mV. The VR_TT# signal can be used by the system to change the CPU operation and decrease the power consumption. As the temperature drops, the NTC pin voltage goes up. If the NTC pin voltage exceeds 1.23V, VR_TT# will be pulled high. Figure 8 illustrates the temperature hysteresis feature of VR_TT#. T_1 and T_2 (T_1>T_2) are two threshold temperatures. VR_TT# goes low when the temperature is higher than T_1 and goes high when the temperature is lower than T_2.

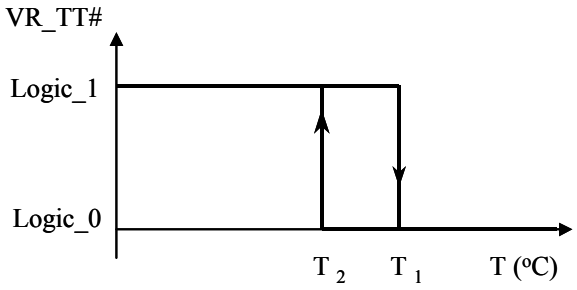


FIGURE 8. VR_TT# TEMPERATURE HYSTERISIS

The NTC thermistor's resistance is approximately given by the following formula:

$$R_{NTC}(T) = R_{NTCTo} \cdot e^{b \cdot (\frac{1}{T+273} - \frac{1}{To+273})} \quad \text{(EQ. 6)}$$

T is the temperature of the NTC thermistor and b is a constant determined by the thermistor material. T_o is the reference temperature at which the approximation is derived. The most commonly used T_o is 25°C. For most commercial NTC thermistors, there is b = 2750k, 2600k, 4500k or 4250k.

From the operation principle of VR_TT#, the NTC resistor satisfies the following equation group:

$$R_{NTC}(T_1) + R_s = \frac{1.20V}{60\mu A} = 20k\Omega \quad \text{(EQ. 7)}$$

$$R_{NTC}(T_2) + R_s = \frac{1.23V}{54\mu A} = 22.78k\Omega \quad \text{(EQ. 8)}$$

From Equation 7 and Equation 8, the following can be derived:

$$R_{NTC}(T_2) - R_{NTC}(T_1) = 2.78k\Omega \quad \text{(EQ. 9)}$$

Substitution of Equation 6 into Equation 9 yields the required nominal NTC resistor value:

$$R_{NTCTo} = \frac{2.78k\Omega \cdot e^{b \cdot (\frac{1}{T_o+273})}}{e^{b \cdot (\frac{1}{T_2+273})} - e^{b \cdot (\frac{1}{T_1+273})}} \quad \text{(EQ. 10)}$$

In some cases, the constant b is not accurate enough to approximate the resistor value; manufacturers provide the resistor ratio information at different temperatures. The nominal NTC resistor value may be expressed in another way as follows:

$$R_{NTCTo} = \frac{2.78k\Omega}{\overset{\Lambda}{R}_{NTC}(T_2) - \overset{\Lambda}{R}_{NTC}(T_1)} \quad \text{(EQ. 11)}$$

where $\overset{\Lambda}{R}_{NTC}(T)$ is the normalized NTC resistance to its nominal value. The normalized resistor value on most NTC thermistor datasheets is based on the value at 25°C.

Once the NTC thermistor resistor is determined, the series resistor can be derived by:

$$R_s = \frac{1.20V}{60\mu A} - R_{NTC}(T_1) = 20k\Omega - R_{NTC\_T_1} \quad \text{(EQ. 12)}$$

Once R_{NTCTo} and R_s is designed, the actual NTC resistance at T_2 and the actual T_2 temperature can be found in:

$$R_{NTC\_T2} = 2.78k\Omega + R_{NTC\_T_1} \quad \text{(EQ. 13)}$$

$$T_{2\_actual} = \frac{1}{\frac{1}{b}\ln(\frac{R_{NTC\_T_2}}{R_{NTCTo}}) + 1/(273+T_o)} - 273 \quad \text{(EQ. 14)}$$

One example of using Equations 10, 11 and 12 to design a thermal throttling circuit with the temperature hysteresis 100°C to 105°C is illustrated as follows. Since T_1 = 105°C and T_2 = 100°C, if we use a Panasonic NTC with b = 4700, Equation 9 gives the required NTC nominal resistance as

$$R_{NTC\_To} = 431k\Omega$$

The NTC thermistor datasheet gives the resistance ratio as 0.03956 at 100°C and 0.03322 at 105°C. The b value of 4700k in Panasonic datasheet only covers up to 85°C; therefore, using Equation 11 is more accurate for 100°C design and the required NTC nominal resistance at 25°C is 438kΩ. The closest NTC resistor value from manufacturers is 470kΩ. So Equation 12 gives the series resistance as follows:

$$R_s = 20k\Omega - R_{NTC\_105C} = 20k\Omega - 15.61k\Omega = 4.39k\Omega$$

The closest standard value is 4.42kΩ. Furthermore, Equation 13 gives the NTC resistance at T_2:

$$R_{NTC\_T2} = 2.78k\Omega + R_{NTC\_T_1} = 18.39k\Omega$$

The NTC branch is designed to have a 470k NTC and a 4.42k resistor in series. The part number of the NTC thermistor is ERTJ0EV474J. It is a 0402 package. The NTC thermistor should be placed in the spot that gives the best indication of the temperature of the voltage regulator. The actual temperature hysteretic window is approximately 105°C to 100°C.

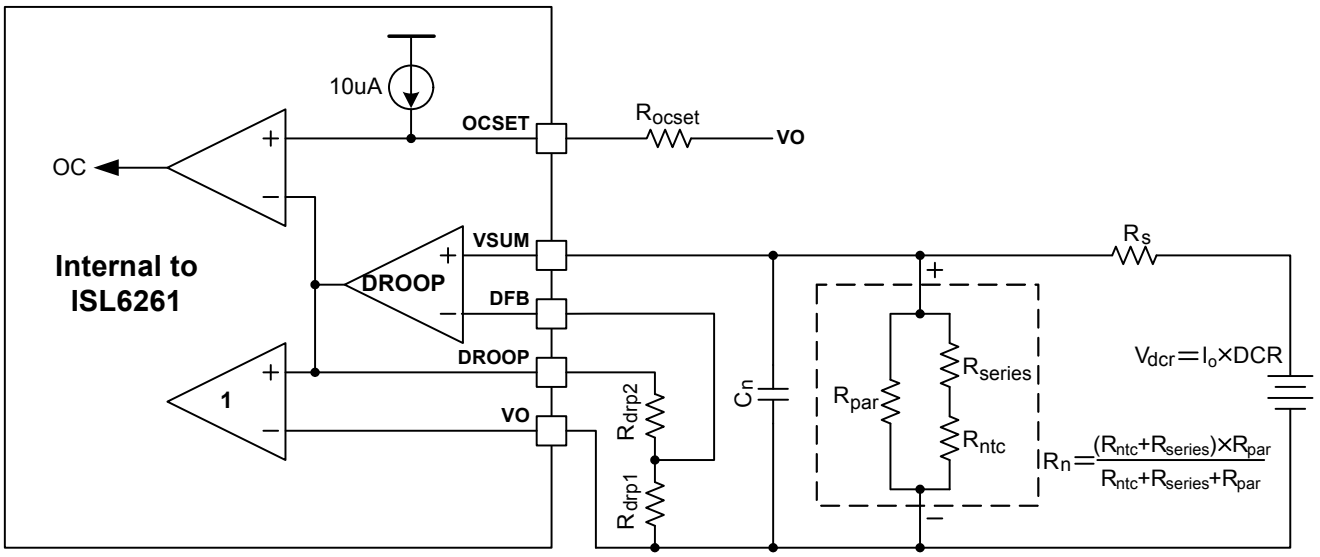


FIGURE 9. EQUIVALENT MODEL FOR DROOP CIRCUIT USING DCR SENSING

Static Mode of Operation - Static Droop Using DCR Sensing

The ISL6261 has an internal differential amplifier to accurately regulate the voltage at the processor die.

For DCR sensing, the process to compensate the DCR resistance variation takes several iterative steps. Figure 2 shows the DCR sensing method. Figure 9 shows the simplified model of the droop circuitry. The inductor DC current generates a DC voltage drop on the inductor DCR. Equation 15 gives this relationship.

$$V_{DCR} = I_o \times DCR \quad \text{(EQ. 15)}$$

An R-C network senses the voltage across the inductor to get the inductor current information. R_n represents the NTC network consisting of R_{ntc}, R_{series} and R_{par}. The choice of R_s will be discussed in the next section.

The first step in droop load line compensation is to choose R_n and R_s such that the correct droop voltage appears even at light loads between the VSUM and VO nodes. As a rule of thumb, the voltage drop across the R_n network, V_n, is set to be 0.5-0.8 times V_{DCR}. This gain, defined as G1, provides a fairly reasonable amount of light load signal from which to derive the droop voltage.

The NTC network resistor value is dependent on the temperature and is given by:

$$R_n(T) = \frac{(R_{series} + R_{ntc}) \cdot R_{par}}{R_{series} + R_{ntc} + R_{par}} \quad \text{(EQ. 16)}$$

G1, the gain of V_n to V_{DCR}, is also dependent on the temperature of the NTC thermistor:

$$G_1(T) \overset{\Delta}{=} \frac{R_n(T)}{R_n(T) + R_s} \quad \text{(EQ. 17)}$$

The inductor DCR is a function of the temperature and is approximately given by

$$DCR(T) = DCR_{25C} \cdot (1 + 0.00393 * (T - 25)) \quad \text{(EQ. 18)}$$

in which 0.00393 is the temperature coefficient of the copper. The droop amplifier output voltage divided by the total load current is given by:

$$R_{droop} = G_1(T) \cdot DCR(T) \cdot k_{droopamp} \quad \text{(EQ. 19)}$$

R_{droop} is the actual load line slope. To make R_{droop} independent of the inductor temperature, it is desired to have:

$$G_1(T) \cdot (1 + 0.00393 * (T - 25)) \cong G_{1target} \quad \text{(EQ. 20)}$$

where $G_{1target}$ is the desired ratio of V_n/V_{DCR}. Therefore, the temperature characteristics G_1 is described by:

$$G_1(T) = \frac{G_{1target}}{(1 + 0.00393 * (T - 25)} \quad \text{(EQ. 21)}$$

For different G1 and NTC thermistor preference, Intersil provides a design spreadsheet to generate the proper value of R_{ntc}, R_{series}, R_{par}.

R_{drp1} (R_{11} in Figure 2) and R_{drp2} (R_{12} in Figure 2) sets the droop amplifier gain, according to Equation 22:

$$k_{droopamp} = 1 + \frac{R_{drp2}}{R_{drp1}} \quad \text{(EQ. 22)}$$

After determining R_s and R_n networks, use Equation 23 to calculate the droop resistances R_{drp1} and R_{drp2}.

$$R_{drp2} = \left(\frac{R_{droop}}{DCR \cdot G1(25^o C)} - 1\right) \cdot R_{drp1} \quad \text{(EQ. 23)}$$

R_{droop} is 2.1mV/A per Intel® IMVP-6® specification.

The effectiveness of the R_n network is sensitive to the coupling coefficient between the NTC thermistor and the inductor. The NTC thermistor should be placed in close proximity of the inductor.

To verify whether the NTC network successfully compensates the DCR change over temperature, one can apply full load current, and wait for the thermal steady state, and see how much the output voltage deviates from the initial voltage reading. Good thermal compensation can limit the drift to less than 2mV. If the output voltage decreases when the temperature increases, that ratio between the NTC thermistor value and the rest of the resistor divider network has to be increased. Following the evaluation board value and layout of NTC placement will minimize the engineering time.

The current sensing traces should be routed directly to the inductor pads for accurate DCR voltage drop measurement. However, due to layout imperfection, the calculated R_{drp2} may still need slight adjustment to achieve optimum load line slope. It is recommended to adjust R_{drp2} after the system has achieved thermal equilibrium at full load. For example, if the max current is 20A, one should apply 20A load current and look for 42mV output voltage droop. If the voltage droop is 40mV, the new value of R_{dpr2} is calculated by:

$$R_{drp\ 2\_new} = \frac{42\,mV}{40\,mV}(R_{drp\ 1} + R_{drp\ 2}) - R_{drp\ 1} \quad \text{(EQ. 24)}$$

For the best accuracy, the effective resistance on the DFB and VSUM pins should be identical so that the bias current of the droop amplifier does not cause an offset voltage. The effective resistance on the VSUM pin is the parallel of R_s and R_n, and the effective resistance on the DFB pin is the parallel of R_{drp1} and R_{drp2}.

Dynamic Mode of Operation – Droop Capacitor Design in DCR Sensing

Figure 10 shows the desired waveforms during load transient response. V_{core} needs to be as square as possible at I_{core} change. The V_{core} response is determined by several factors, namely the choice of output inductor and output capacitor, the compensator design, and the droop capacitor design.

The droop capacitor refers to C_n in Figure 9. If C_n is designed correctly, its voltage will be a high-bandwidth analog voltage of the inductor current. If C_n is not designed correctly, its voltage will be distorted from the actual waveform of the inductor current and worsen the transient response. Figure 11 shows the transient response when C_n is too small. V_{core} may sag excessively upon load application to create a system failure. Figure 12 shows the transient response when C_n is too large. V_{core} is sluggish in drooping to its final value. There will be excessive overshoot if a load occurs during this time, which may potentially hurt the CPU reliability.

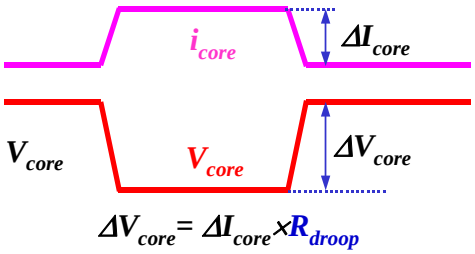


FIGURE 10. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

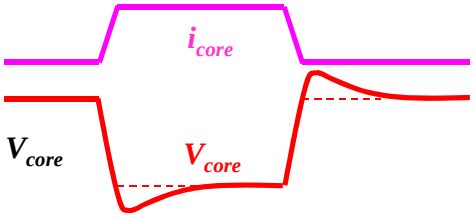


FIGURE 11. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO SMALL

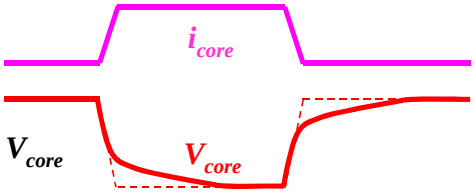


FIGURE 12. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO LARGE

The current sensing network consists of R_n, R_s and C_n. The effective resistance is the parallel of R_n and R_s. The RC time constant of the current sensing network needs to match the L/DCR time constant of the inductor to get correct representation of the inductor current waveform. Equation 25 shows this equation:

$$\frac{L}{DCR} = \left(\frac{R_n \times R_s}{R_n + R_s}\right) \times C_n \quad \text{(EQ. 25)}$$

Solving for Cn yields

$$C_n = \frac{\frac{L}{DCR}}{\frac{R_n \times R_s}{R_n + R_s}} \quad \text{(EQ. 26)}$$

For example: L = 0.45µH, DCR = 1.1mΩ, R_s = 7.68kΩ, and R_n = 3.4kΩ

$$C_n = \frac{\frac{0.45\mu H}{0.0011}}{parallel(7.68k, 3.4k)} = 174nF \quad \text{(EQ. 27)}$$

Since the inductance and the DCR typically have 20% and 7% tolerance respectively, the L/DCR time constant of each individual inductor may not perfectly match the RC time constant of the current sensing network. In mass production, this effect will make the transient response vary a little bit from board to board. Compared with potential long-term damage on CPU reliability, an immediate system failure is worse. So it is desirable to avoid the waveforms shown in Figure 11. It is recommended to choose the minimum C_n value based on the maximum inductance so only the scenarios of Figures 10 and 12 may happen. It should be noted that, after calculation, fine-tuning of C_n value may still be needed to account for board parasitics. C_n also needs to be a high-grade cap like X7R with low tolerance. Another good option is the NPO/COG (class-I) capacitor, featuring only 5% tolerance and very good thermal characteristics. But the NPO/COG caps are only available in small capacitance values. In order to use such capacitors, the resistors and thermistors surrounding the droop voltage sensing and droop amplifier need to be scaled up 10X to reduce the capacitance by 10X. Attention needs to be paid in balancing the impedance of droop amplifier.

Dynamic Mode of Operation - Compensation Parameters

The voltage regulator is equivalent to a voltage source equal to VID in series with the output impedance. The output impedance needs to be 2.1mΩ in order to achieve the 2.1mV/A load line. It is highly recommended to design the compensation such that the regulator output impedance is 2.1mΩ. A type-III compensator is recommended to achieve the best performance. Intersil provides a spreadsheet to design the compensator parameters. Figure 13 shows an example of the spreadsheet. After the user inputs the parameters in the blue font, the spreadsheet will calculate the recommended compensator parameters (in the pink font), and show the loop gain curves and the regulator output impedance curve. The loop gain curves need to be stable for regulator stability, and the impedance curve needs to be equal to or smaller than 2.1mΩ in the entire frequency range to achieve good transient response.

The user can choose the actual resistor and capacitor values based on the recommendation and input them in the spreadsheet, then see the actual loop gain curves and the regulator output impedance curve.

Caution needs to be used in choosing the input resistor to the FB pin. Excessively high resistance will cause an error to the output voltage regulation due to the bias current flowing in the FB pin. It is recommended to keep this resistor below 3k.

Droop using Discrete Resistor Sensing - Static/Dynamic Mode of Operation

Figure 3 shows a detailed schematic using discrete resistor sensing of the inductor current. Figure 14 shows the equivalent circuit. Since the current sensing resistor voltage represents the actual inductor current information, R_s and C_n simply provide noise filtering. The most significant noise comes from the ESL of the current sensing resistor. A low low ESL sensing resistor is strongly recommended. The recommended R_s is 100Ω and the recommended C_n is 220pF. Since the current sensing resistance does not appreciably change with temperature, the NTC network is not needed for thermal compensation.

Droop is designed the same way as the DCR sensing approach. The voltage on the current sensing resistor is given by the following equation:

$$V_{rsen} = R_{sen} \cdot I_o \quad \text{(EQ. 28)}$$

Equation 21shows the droop amplifier gain. So the actual droop is given by

$$R_{droop} = R_{sen} \cdot \left(1 + \frac{R_{drp2}}{R_{drp1}}\right) \quad \text{(EQ. 29)}$$

Solving for R_{drp2} yields:

$$R_{drp2} = R_{drp1} \cdot \left(\frac{R_{droop}}{R_{sen}} - 1\right) \quad \text{(EQ. 30)}$$

For example: R_{droop} = 2.1mΩ. If R_{sen} = 1m and R_{drp1} = 1k, easy calculation gives that R_{drp2} is 1.1k.

The current sensing traces should be routed directly to the current sensing resistor pads for accurate measurement. However, due to layout imperfections, the calculated R_{drp2} may still need slight adjustment to achieve optimum load line slope. It is recommended to adjust R_{drp2} after the system has achieved thermal equilibrium at full load.

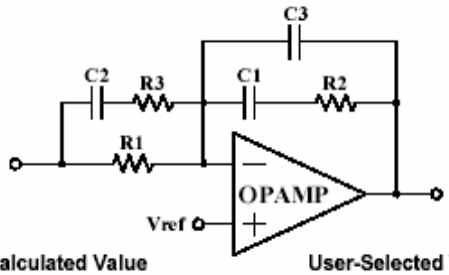
Operation Parameters

Controller Part Number:	ISL6261	
Phase Number:	1	
Vin:	12	volts
Vo:	1.2	volts
Full Load Current:	20	Amps
Estimated Full-Load Efficiency:	88	%
Number of Output Bulk Capacitors:	4	
Capacitance of Each Output Bulk Capacitor:	330	uF
ESR of Each Output Bulk Capacitor:	6	mΩ
Number of Output Ceramic Capacitors:	32	
Capacitance of Each Output Ceramic Capacitor:	22	uF
ESR of Each Output Ceramic Capacitor:	2	mΩ
Switching Frequency:	300	kHz
Inductance Per Phase:	0.45	uH
CPU Socket Resistance:	0.6	mΩ
Desired Load-Line Slope	2.1	mΩ

Read the instructions if you want to change these settings !

Kp2:	0.245
Kwi:	1.3

Compensator Component Parameters



	Calculated Value		User-Selected Value	
R1	2.200	kΩ	2.21	kΩ
R2	460.247	kΩ	464	kΩ
R3	5.472	kΩ	5.49	kΩ
C1	144.911	pF	150	pF
C2	395.742	pF	390	pF
C3	45.736	pF	47	pF

Use The User-Selected Value (Y/N)?

N

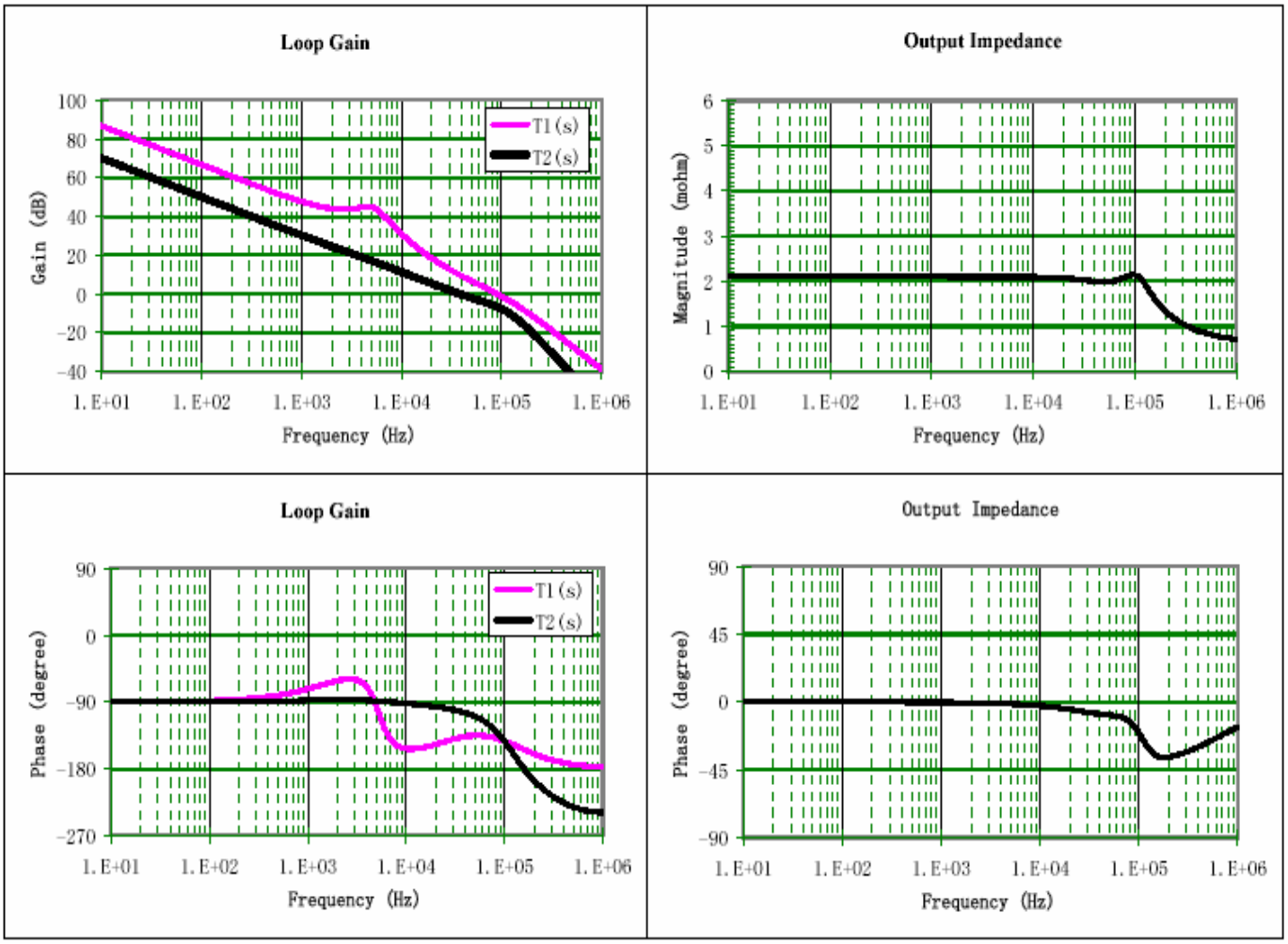


FIGURE 13. AN EXAMPLE OF ISL6261 COMPENSATION SPREADSHEET

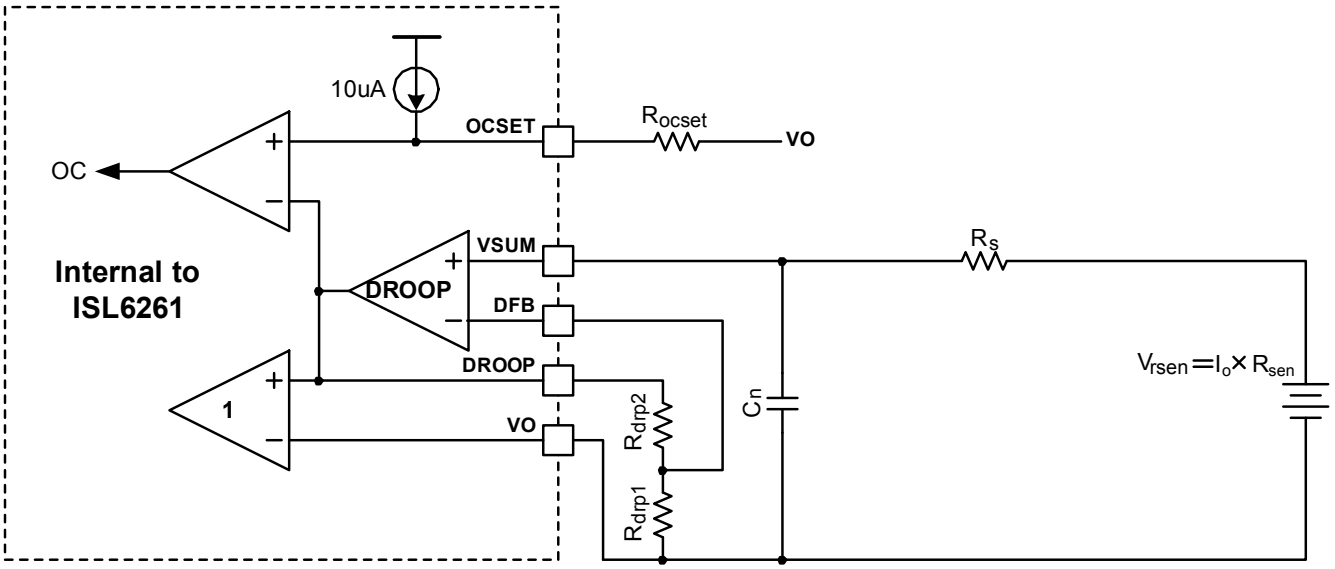


FIGURE 14. EQUIVALENT MODEL FOR DROOP CIRCUIT USING DISCRETE RESISTOR SENSING

Typical Performance (Data Taken on ISL6261 Eval1 Rev. C Evaluation Board)

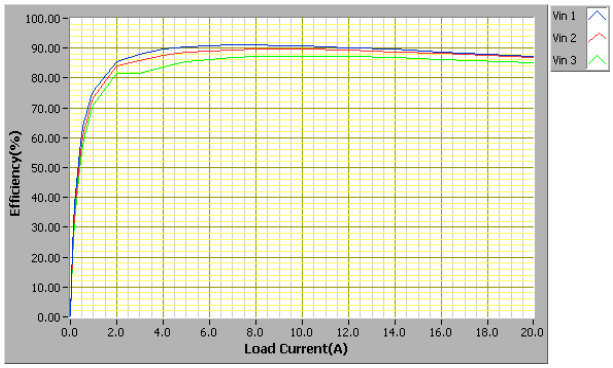


FIGURE 15. CCM EFFICIENCY, VID = 1.1V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

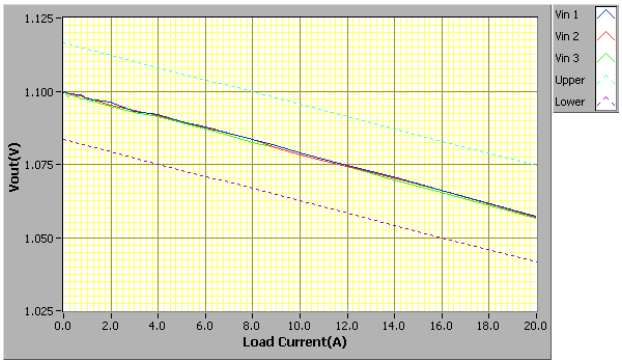


FIGURE 16. CCM LOAD LINE AND THE SPEC, VID = 1.1V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

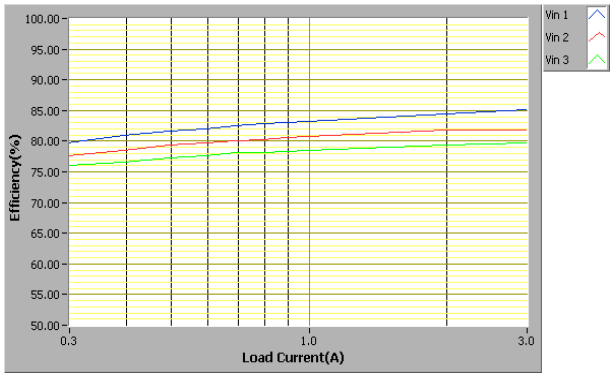


FIGURE 17. DEM EFFICIENCY, VID = 0.7625V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

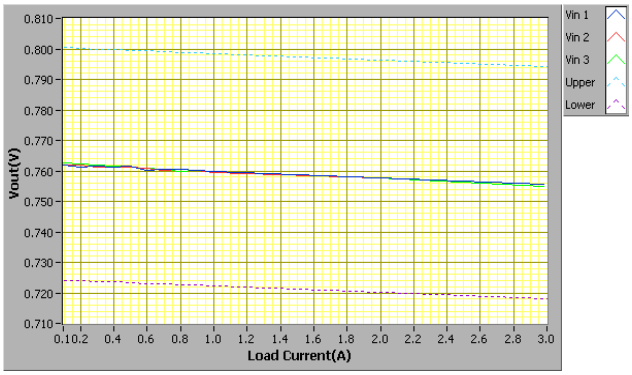


FIGURE 18. DEM LOAD LINE AND THE SPEC, VID = 0.7625V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

Typical Performance (Data Taken on ISL6261 Eval1 Rev. C Evaluation Board) **(Continued)**

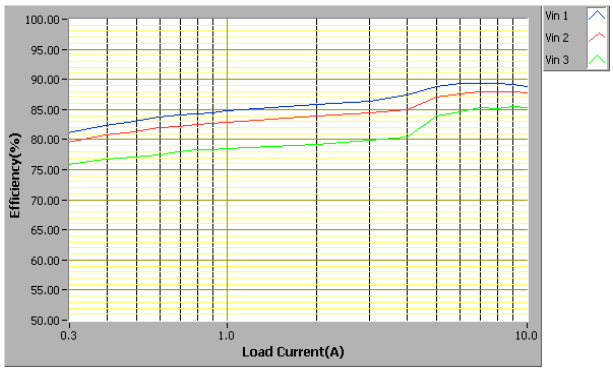


FIGURE 19. ENHANCED DEM EFFICIENCY, VID = 0.7625V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

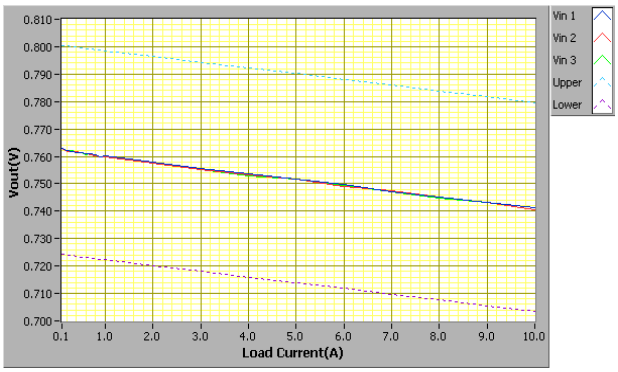


FIGURE 20. ENHANCED DEM LOAD LINE, VID = 0.7625V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

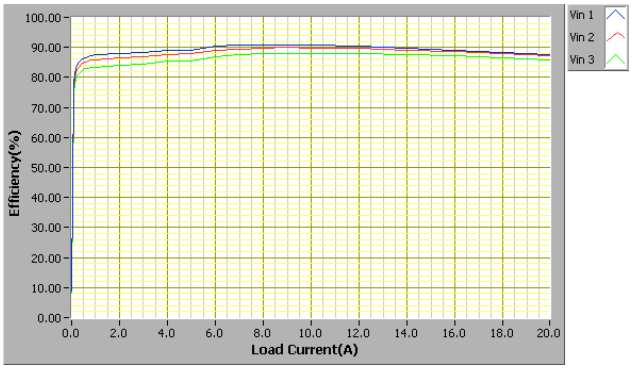


FIGURE 21. ENHANCED DEM EFFICIENCY, VID = 1.1V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

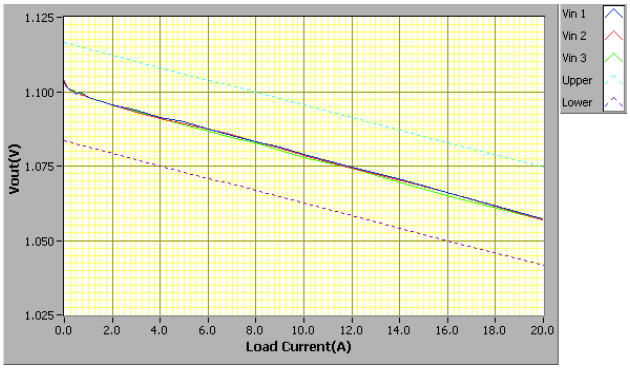


FIGURE 22. ENHANCED DEM LOAD LINE, VID = 1.1V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

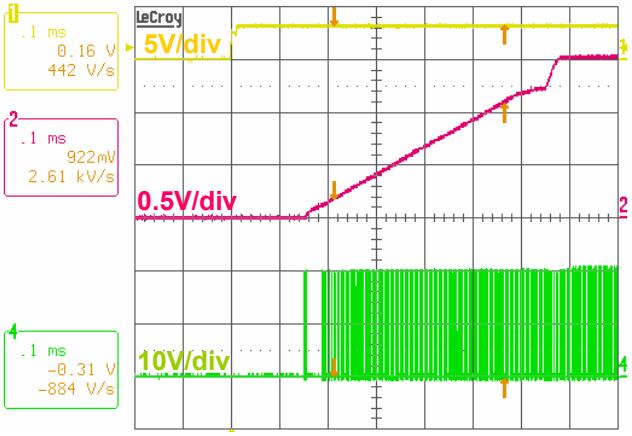


FIGURE 23. SOFT-START, V_{IN} = 19V, Io = 0A, VID = 1.5V, Ch1: VR_ON, Ch2: Vo, Ch4: PHASE

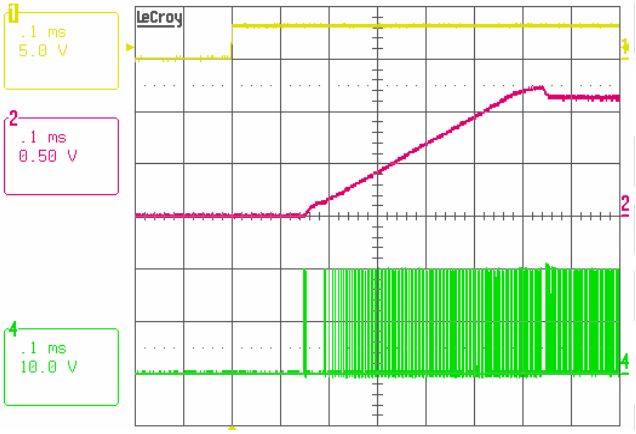


FIGURE 24. SOFT-START, V_{IN} = 19V, Io = 0A, VID = 1.1V, Ch1: VR_ON, Ch2: Vo, Ch4: PHASE

Typical Performance (Data Taken on ISL6261 Eval1 Rev. C Evaluation Board) **(Continued)**

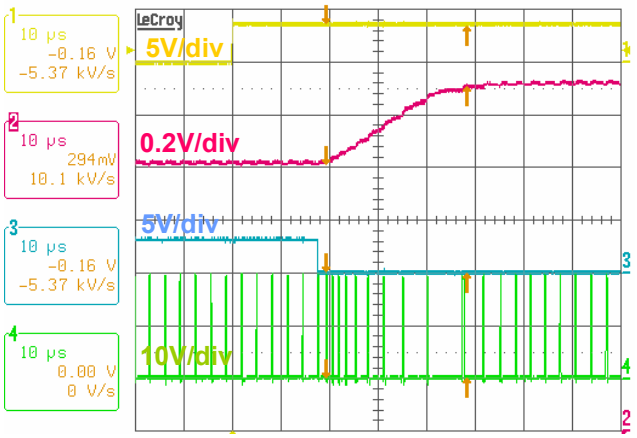


FIGURE 25. V_{BOOT} TO VID, V_{IN} = 19V, Io = 2A, VID = 1.5V, Ch1: PGD_IN, Ch2: Vo, Ch3: CLK_EN#, Ch4: PHASE

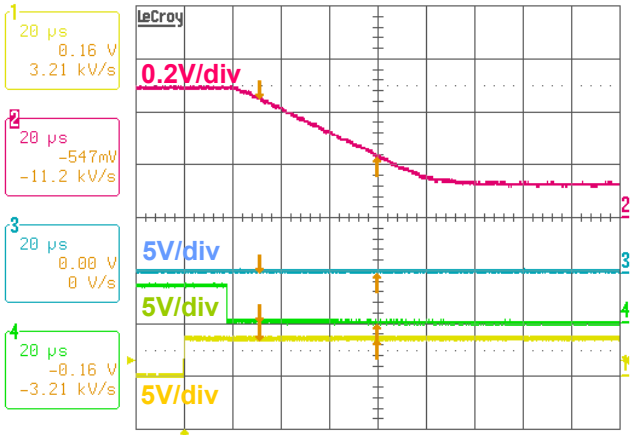


FIGURE 26. V_{BOOT} TO VID, V_{IN} = 19V, Io = 2A, VID = 0.7625V, Ch1: PGD_IN, Ch2: Vo, Ch3: PGOOD, Ch4: CLK_EN

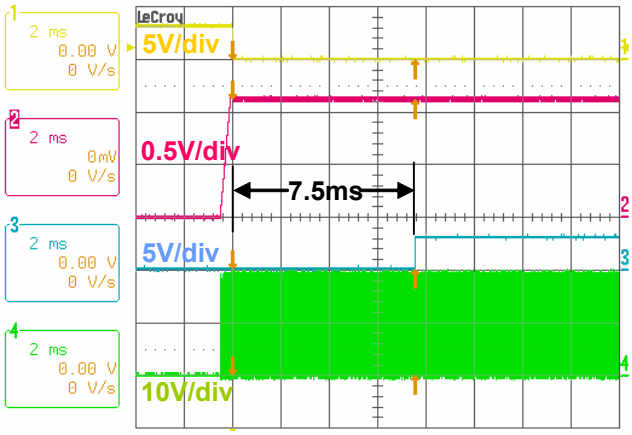


FIGURE 27. CLK_EN AND PGOOD ASSERTION DELAY, V_{IN}=19V, Io=2A, VID=1.1V, Ch1: CLK_EN#, Ch2: Vo, Ch3: PGOOD, Ch4: PHASE

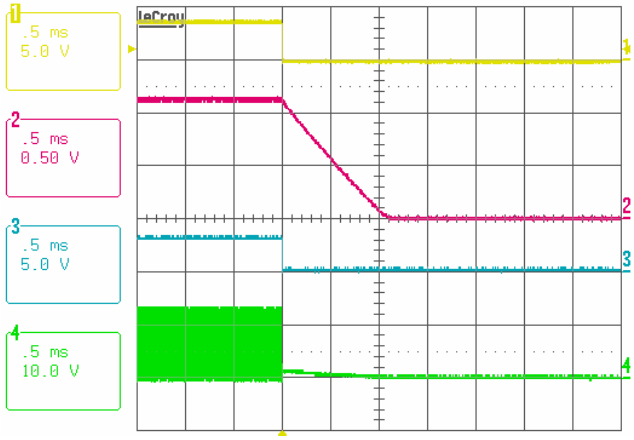


FIGURE 28. SHUT DOWN, V_{IN} = 19V, Io = 0.5A, VID = 1.5V, Ch1: VR_ON, Ch2: Vo, Ch3: PGOOD, Ch4: PHASE

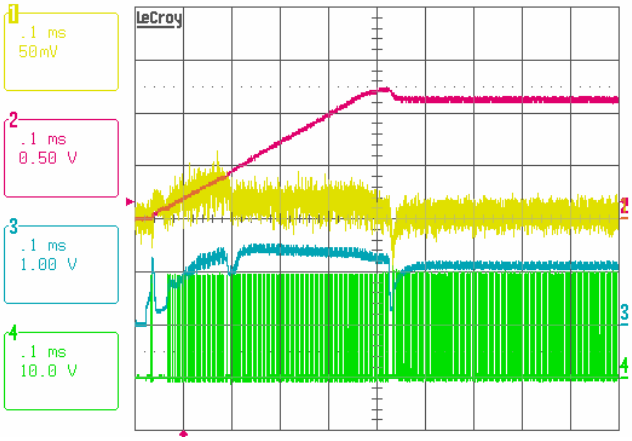


FIGURE 29. SOFT START INRUSH CURRENT, V_{IN} = 19V, Io = 0.5A, VID = 1.1V, Ch1: DROOP-VO (2.1mV = 1A), Ch2: Vo, Ch3: Vcomp, Ch4: PHASE

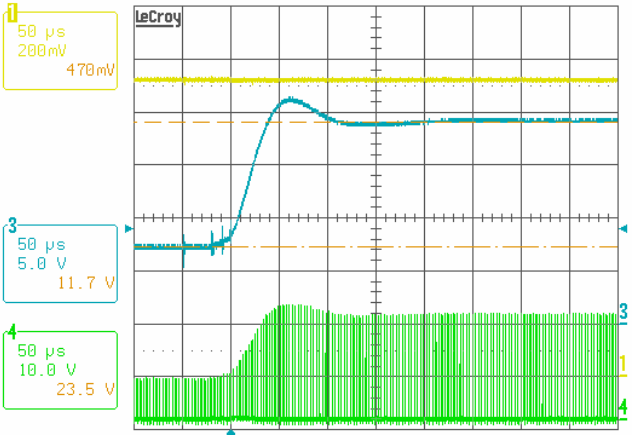


FIGURE 30. V_{IN} TRANSIENT TEST, V_{IN} = 8→19V, Io = 2A, VID = 1.1V, Ch1: Vo, Ch3: V_{IN}, Ch4: PHASE

Typical Performance (Data Taken on ISL6261 Eval1 Rev. C Evaluation Board) **(Continued)**

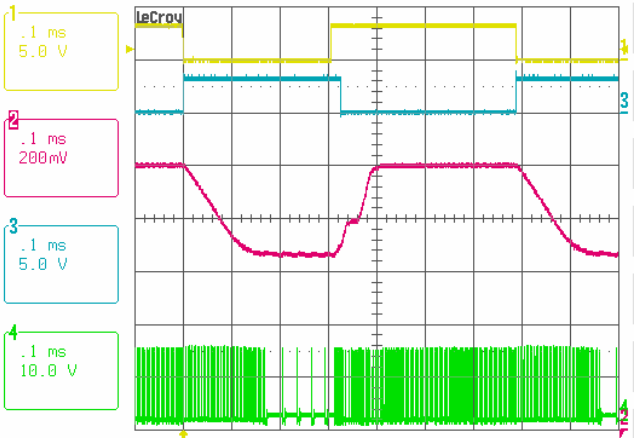


FIGURE 31. C4 ENTRY/EXIT, V_{IN} = 12.6V, Io = 0.7A, HFM VID = 1.1V, LFM VID = 0.9V, C4 VID = 0.7625V, FDE = DPRSLPVR, Ch1: DPRSTP#, Ch2: Vo, Ch3: DPRSLPVR/FDE, Ch4: PHASE

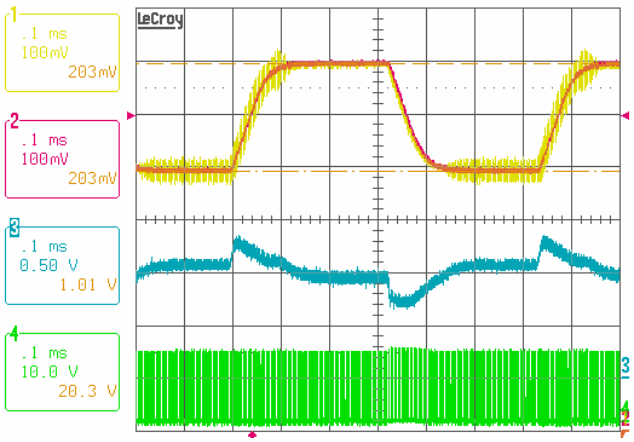


FIGURE 32. VID TOGGLING, V_{IN} = 12.6V, Io= 0.7A, HFM VID = 1.1V, LFM VID = 0.9V, Ch1: SOFT, Ch2: Vo, Ch3: Vcomp, Ch4: PHASE

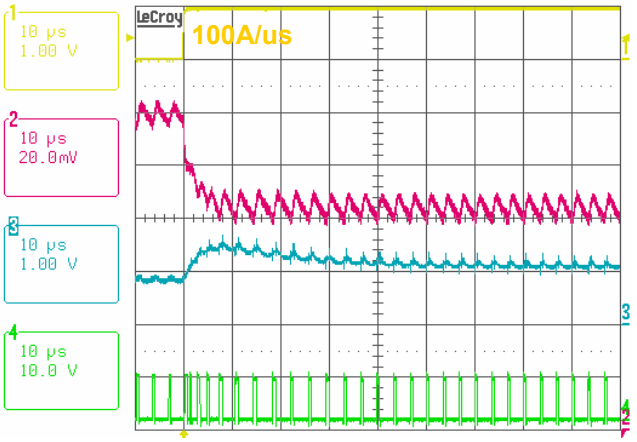


FIGURE 33. LOAD STEP UP RESPONSE IN CCM, V_{IN} = 8V, Io = 2A→20A at 100A/us, VID = 1.1V, Ch1: Io, Ch2: Vo, Ch3: Vcomp, Ch4: PHASE

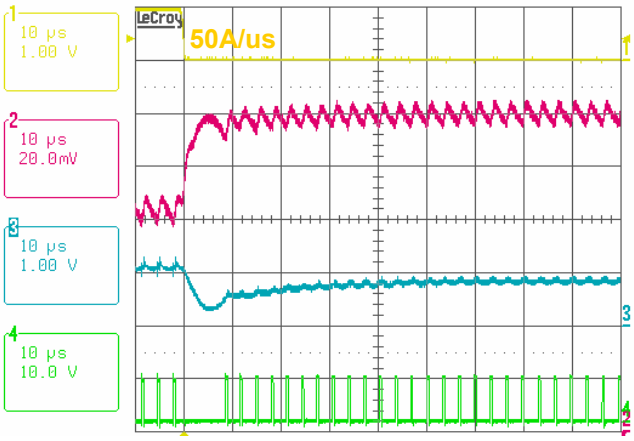


FIGURE 34. LOAD STEP DOWN RESPONSE IN CCM V_{IN} = 8V, Io = 20A→2A at 100A/us, VID = 1.1V, Ch1: Io, Ch2: Vo, Ch3: Vcomp, Ch4: PHASE

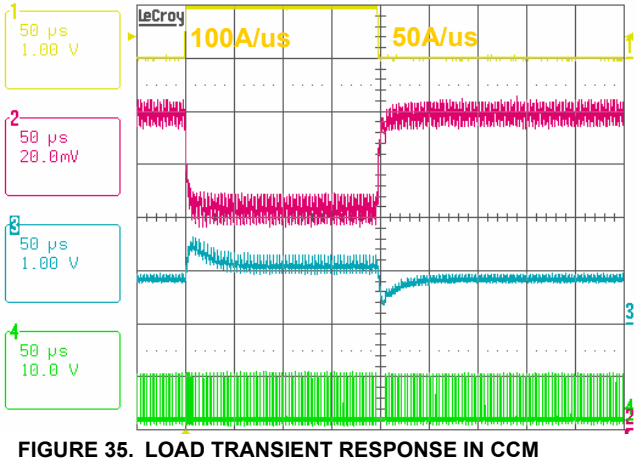


FIGURE 35. LOAD TRANSIENT RESPONSE IN CCM V_{IN} = 8V, Io = 2A←→20A, VID = 1.1V, Ch1: Io, Ch2: Vo, Ch3: Vcomp, Ch4: PHASE

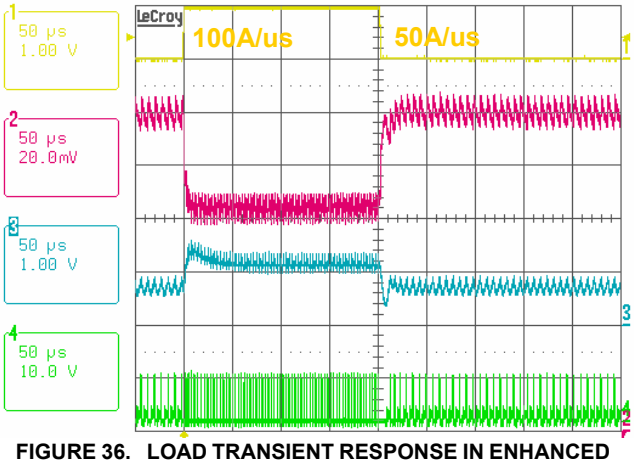


FIGURE 36. LOAD TRANSIENT RESPONSE IN ENHANCED DEM, V_{IN} = 8V, Io = 2A←→20A, VID = 1.1V, Ch1: Io, Ch2: Vo, Ch3: Vcomp, Ch4: PHASE

Typical Performance (Data Taken on ISL6261 Eval1 Rev. C Evaluation Board) **(Continued)**

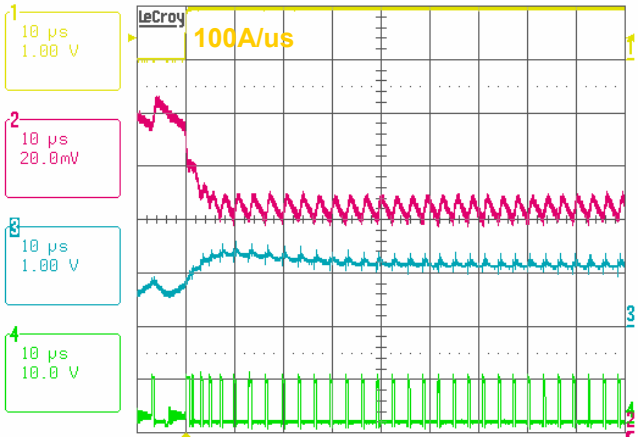


FIGURE 37. LOAD TRANSIENT RESPONSE IN ENHANCED DEM, V_{IN} = 8V, Io = 2A←→20A, VID = 1.1V, Ch1: Io, Ch2: Vo, Ch3: Vcomp, Ch4: PHASE

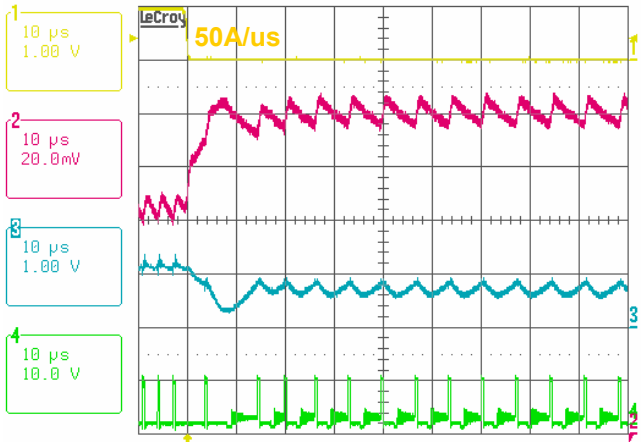


FIGURE 38. LOAD TRANSIENT RESPONSE IN ENHANCED DEM, V_{IN} = 8V, Io = 2A←→20A, VID = 1.1V, Ch1: Io, Ch2: Vo, Ch3: Vcomp, Ch4: PHASE

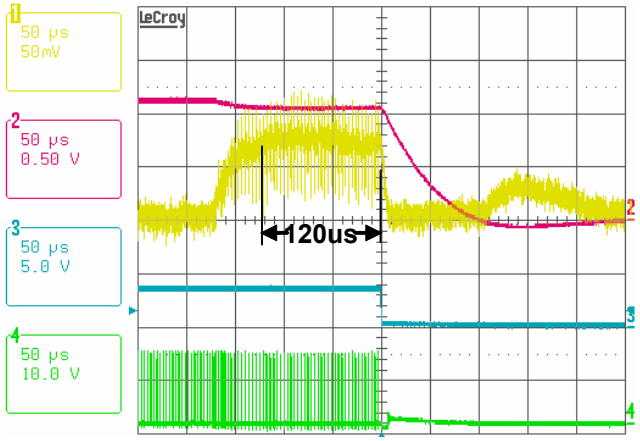


FIGURE 39. OVERCURRENT PROTECTION, V_{IN} = 12.6V, Io = 0A→28A, VID = 1.1V, Ch1: DROOP-VO (2.1mV = 1A), Ch2: Vo, Ch3: PGOOD, Ch4: PHASE

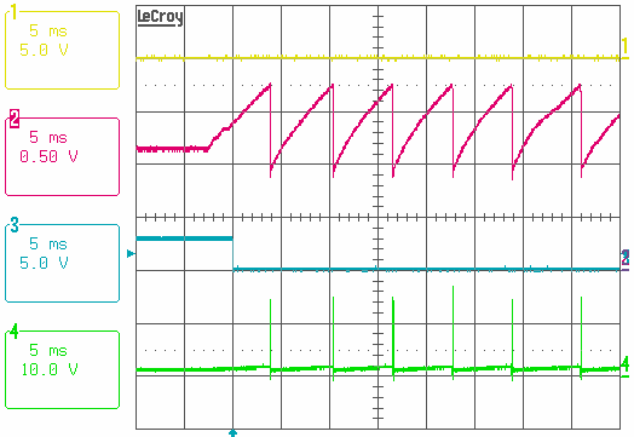
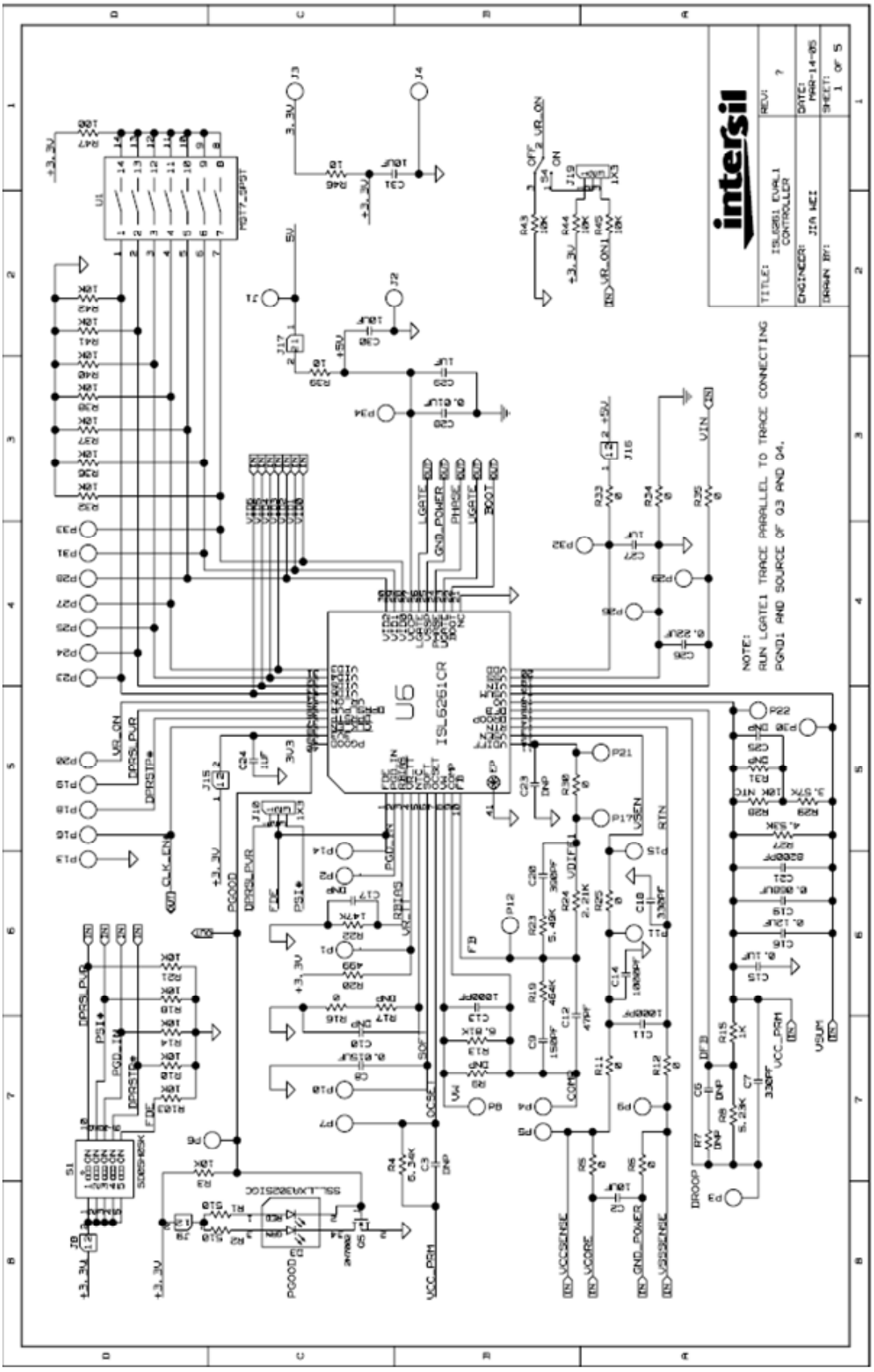
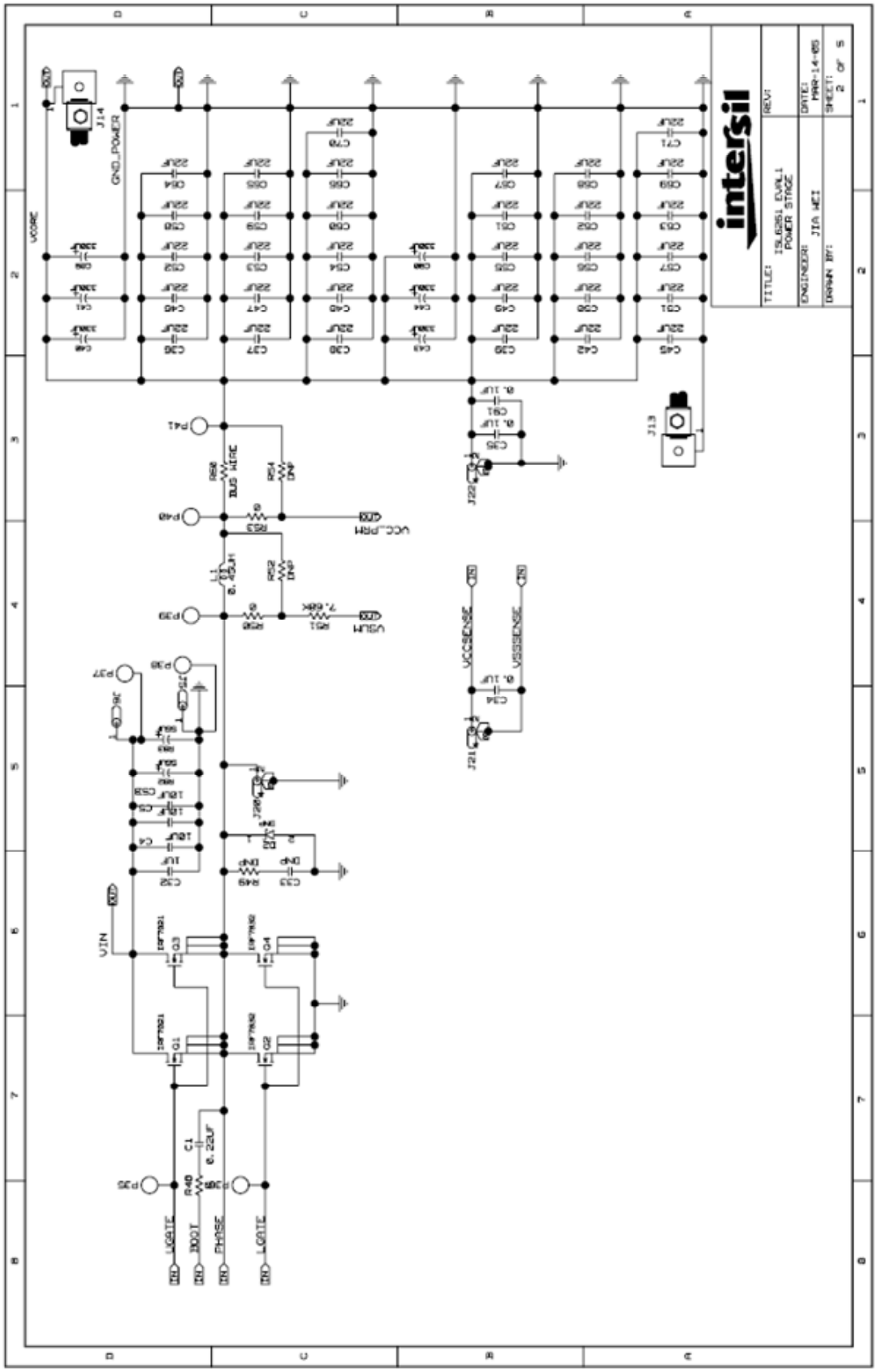


FIGURE 40. OVERVOLTAGE (>1.7V) PROTECTION, V_{IN} = 12.6V, Io = 2A, VID = 1.1V, Ch2: Vo, Ch3: PGOOD, Ch4: PHASE

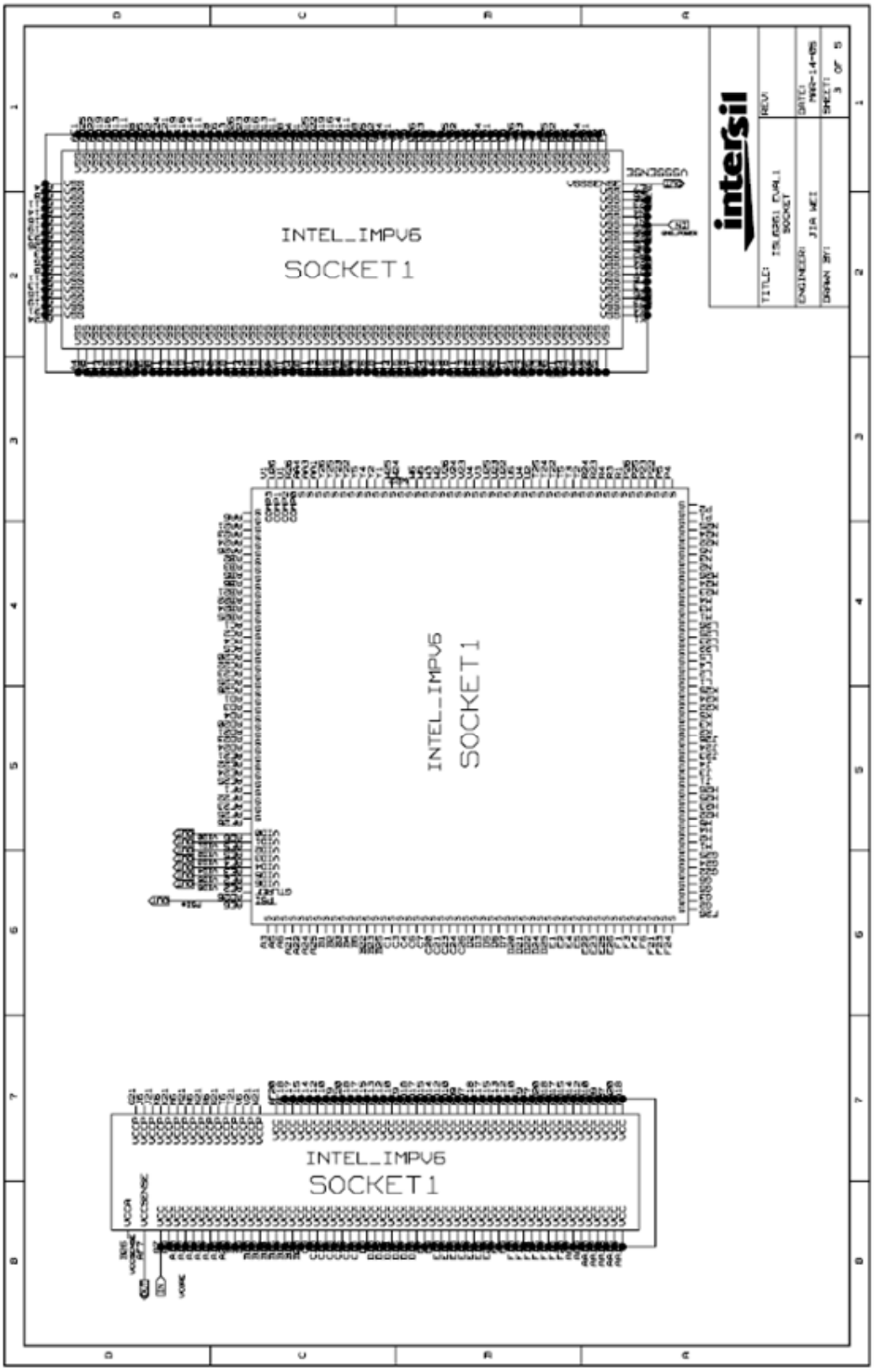
ISL6261 Eval1 Rev. C Evaluation Board Schematic



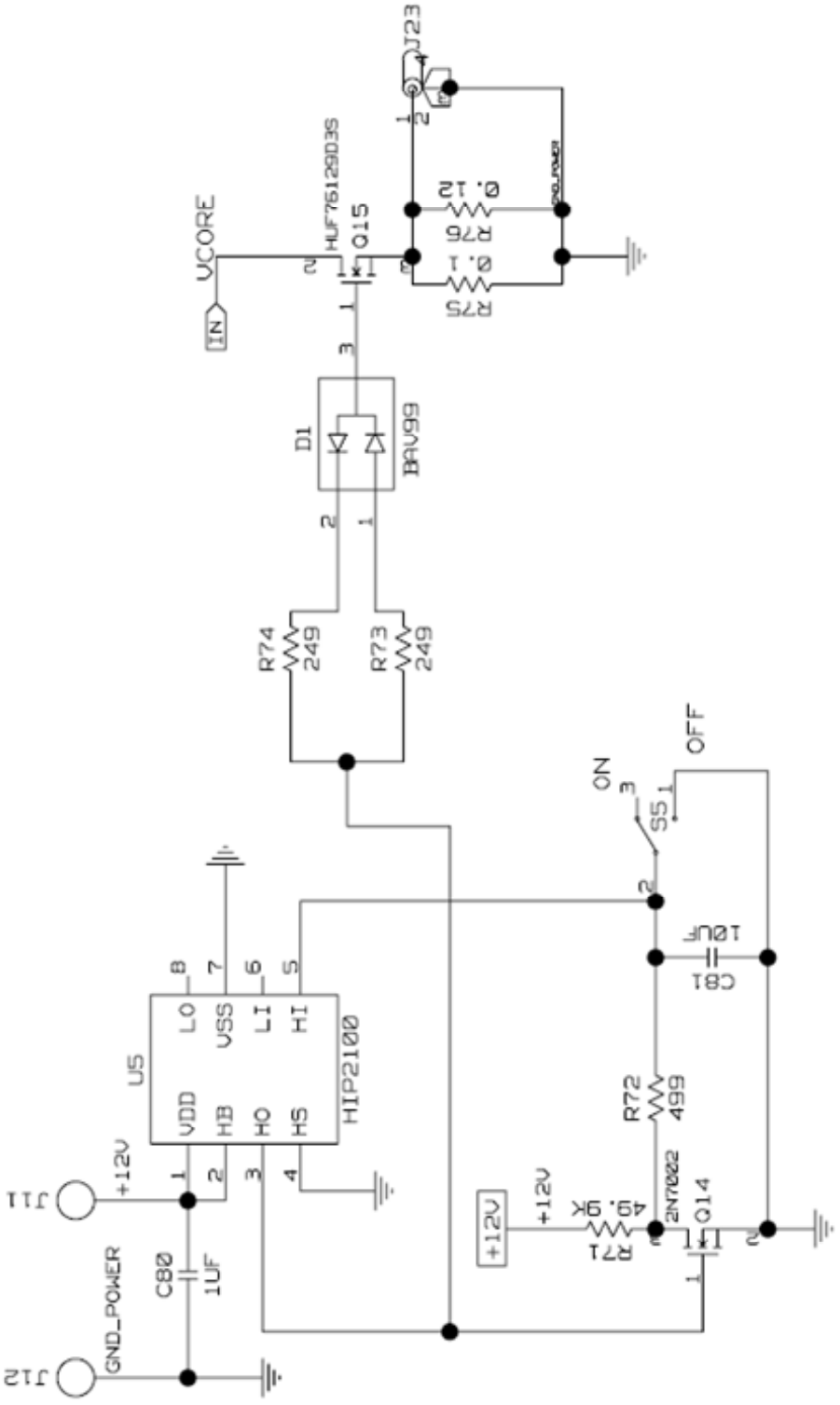
ISL6261 Eval1 Rev. C Evaluation Board Schematic (Continued)



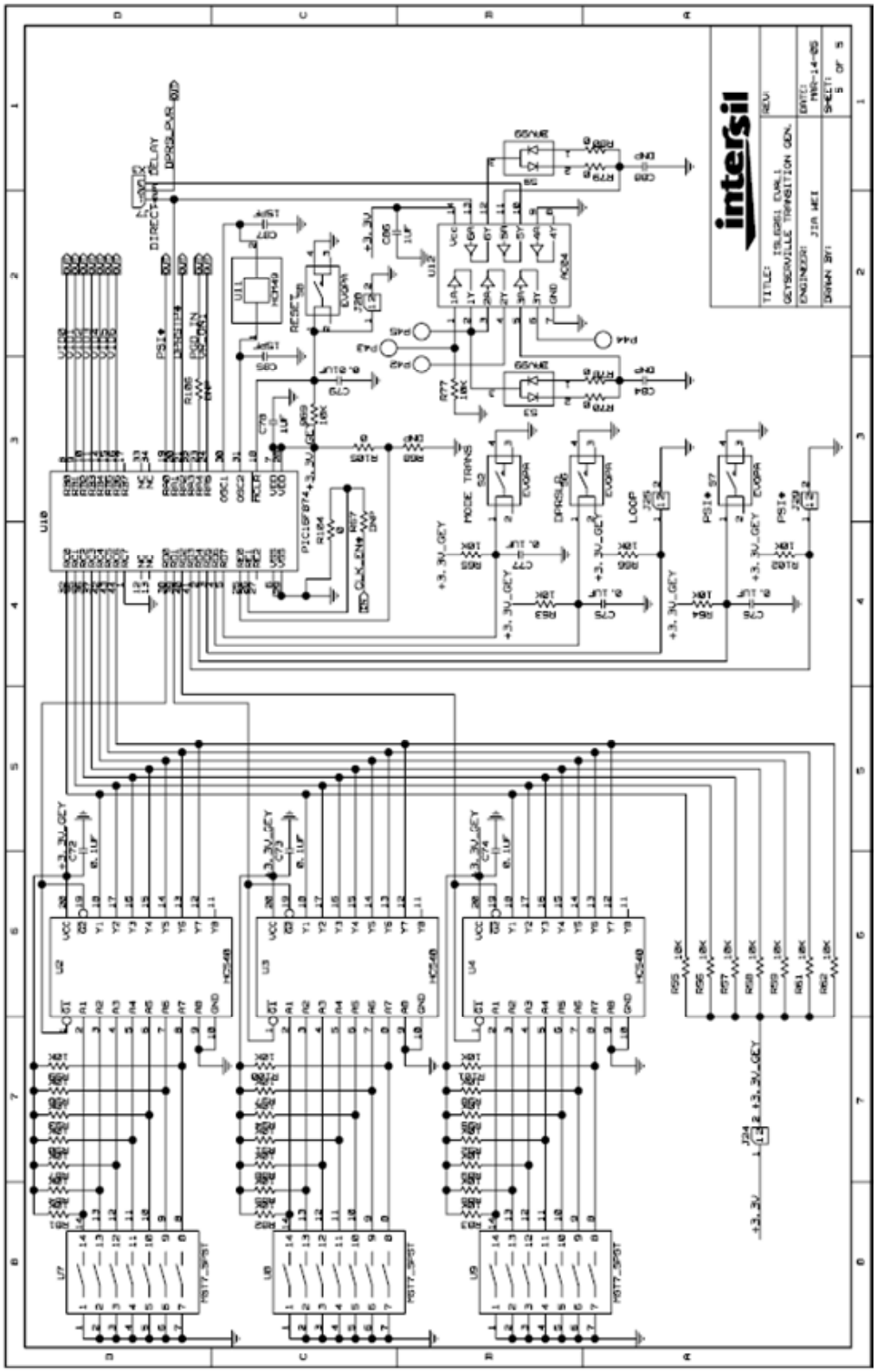
ISL6261 Eval1 Rev. C Evaluation Board Schematic (Continued)



ISL6261 Eval1 Rev. C Evaluation Board Schematic (Continued)



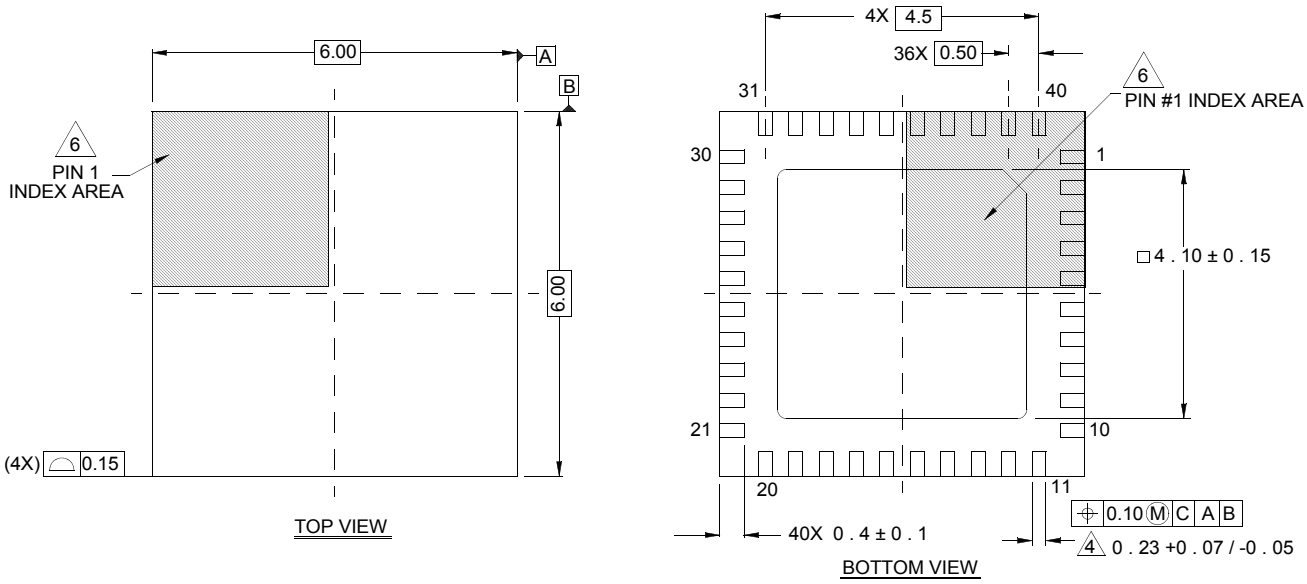
ISL6261 Eval1 Rev. C Evaluation Board Schematic (Continued)

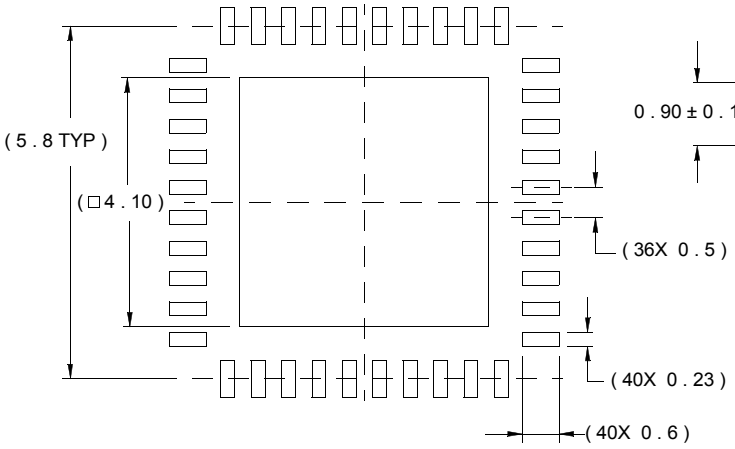


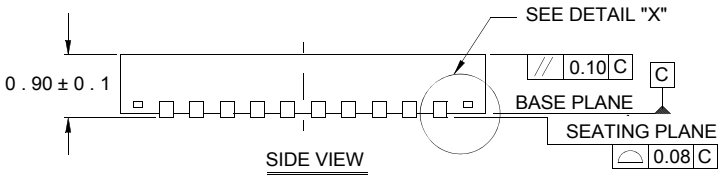
Package Outline Drawing

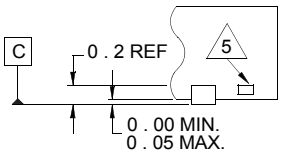
L40.6x6

40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 9/06









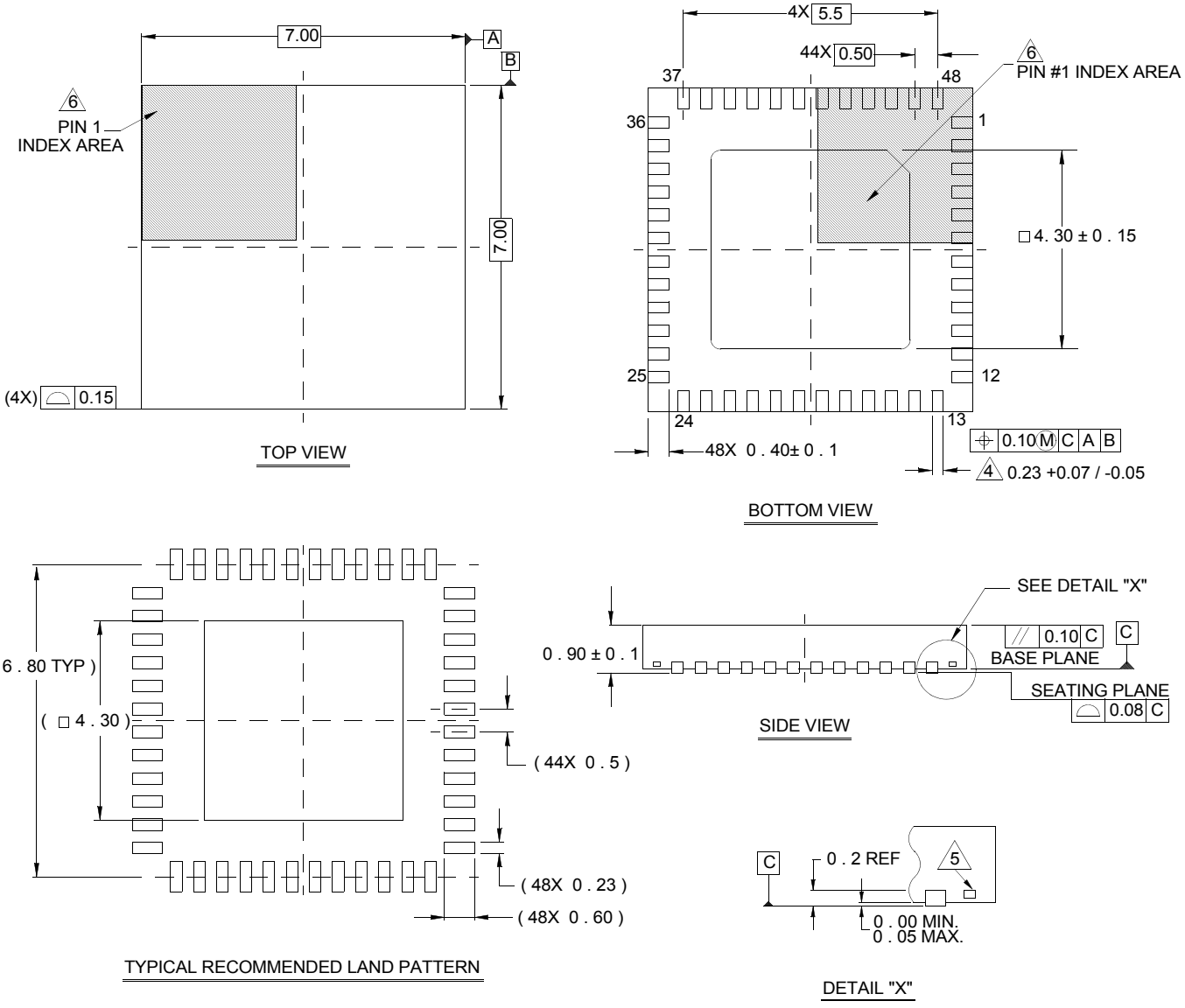
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between .015mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

Package Outline Drawing

L48.7x7

48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 3, 9/06



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between .015mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.