ISL59444

1GHz, 4x1 Multiplexing Amplifier with Synchronous Controls

FN7451
Rev 3.00
August 16, 2012

The ISL59444 is a single-output 4:1 MUX-amp. The MUX-amp has a fixed gain of 1 and a 1GHz bandwidth. The ISL59444 is ideal for professional video switching, HDTV, computer display routing, and other high performance applications.

The device contains logic inputs for channel selection (S0, S1), latch control signals ($\overline{LE1}$, $\overline{LE2}$), and a three-state output control (HIZ) for individual selection of MUX amps that share a common video output line. All logic inputs have pull-downs to ground and may be left floating.

TABLE 1. TRUTH TABLE

$\overline{LE1}/\overline{LE2}$	HIZ	S1	S0	OUT
0	0	0	0	IN0
0	0	0	1	IN1
0	0	1	0	IN2
0	0	1	1	IN3
X	1	X	X	HiZ

Features

- 1GHz (-3dB) Bandwidth (V_{OUT} = 200mV_{P-P})
- 220MHz (-3dB) Bandwidth (V_{OUT} = 2V_{P-P})
- Slew Rate (R_L = 500Ω, V_{OUT} = 4V) 1515V/µs
- Slew Rate (R_L = 500Ω, V_{OUT} = 5V) 1155V/µs
- High Speed Three-State Output (HIZ)
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- HDTV/DTV Analog Inputs
- Video Projectors
- Computer Monitors
- Set-top Boxes
- Security Video
- Broadcast Video Equipment
- RGB Video Distribution Systems
- RF Switching and Routing

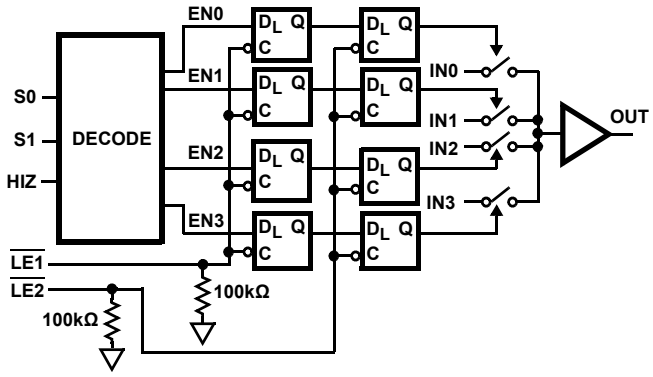


FIGURE 1. FUNCTIONAL DIAGRAM

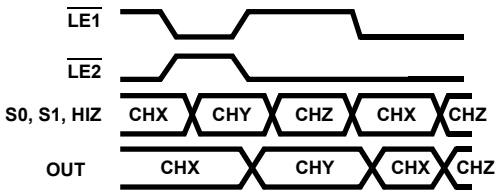
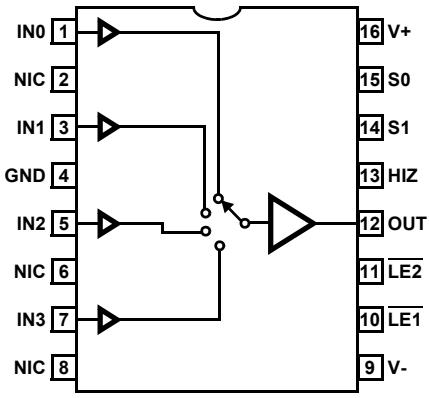


FIGURE 2. TIMING DIAGRAM

Pin Configuration

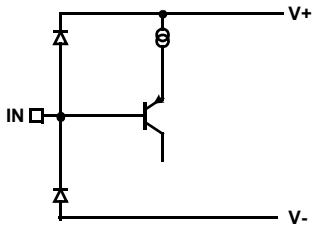
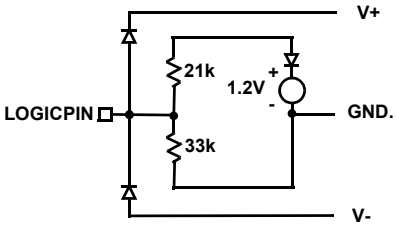
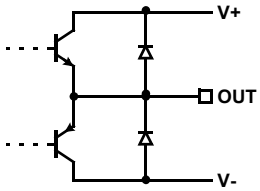
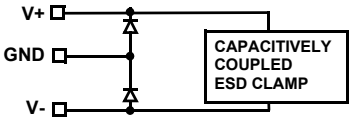
ISL59444 (16 LD SO)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	IN0	Circuit 1	Input for channel 0
2, 6, 8	NIC		Not Internally Connected; it is recommended this pin be tied to ground to minimize crosstalk.
3	IN1	Circuit 1	Input for channel 1
4	GND	Circuit 4	Ground pin
5	IN2	Circuit 1	Input for channel 2
7	IN3	Circuit 1	Input for channel 3
9	V-	Circuit 4	Negative Power Supply
10	$\overline{LE1}$	Circuit 2	Synchronized channel switching: When $\overline{LE1}$ is low, the master control latch loads the next switching address. The Mux Amp is configured for this address when $\overline{LE2}$ goes low. Synchronized operation results when $\overline{LE2}$ is the inverse of $\overline{LE1}$. Channel selection is asynchronous (changes with any control signal change) if both $\overline{LE1}$ and $\overline{LE2}$ are both low.
11	$\overline{LE2}$	Circuit 2	Synchronized channel switching: When $\overline{LE2}$ is low, the newly selected channel, stored in the master latch via $\overline{LE1}$ is selected. Synchronized operation results when $\overline{LE2}$ is the inverse of $\overline{LE1}$. Channel selection is asynchronous (changes with any control signal change) if both $\overline{LE1}$ and $\overline{LE2}$ are both low.
12	OUT	Circuit 3	Output
13	HIZ	Circuit 2	Output disable (active high); there are internal pull-down resistors, so the device will be active with no connection; “HI” puts the output in high impedance state.
14	S1	Circuit 2	Channel selection pin MSB (binary logic code)

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
15	S0	Circuit 2	Channel selection pin LSB (binary logic code)
16	V+	Circuit 4	Positive power supply
 CIRCUIT 1			 CIRCUIT 2
 CIRCUIT 3			 CIRCUIT 4

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TAPE & REEL	PACKAGE (Note 4)	PKG. DWG. #
ISL59444IBZ	59444IBZ	-	16 Ld SO (Pb-free)	MDP0027
ISL59444IBZ-T13	59444IBZ	7”	16 Ld SO (Pb-free)	MDP0027
ISL59444IBZ-T7	59444IBZ	13”	16 Ld SO (Pb-free)	MDP0027

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL59444. For more information on MSL please see tech brief TB363.
4. S016 (0.150”)

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V+ to V-) 11V
Input Voltage . . . . . V- -0.5V, V+ +0.5V
Supply Turn-on Slew Rate 1V/µs
Digital and Analog Input Current (Note 5) 50mA
Output Current (Continuous) 50mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 3kV
Machine Model 300V

Thermal Information

Storage Temperature Range . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . -40°C to +125°C
Power Dissipation . . . . . See Figures 21 and 22
θ_{JA} . . . . . See Figures 21 and 22

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

5. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, R_L = 500Ω to GND, V_{HIZ} = 0.8V, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
GENERAL						
I_S	Supply Current (V_{OUT} = 0V)	No load, V_{HIZ} = 0.8V	14.5	18	20	mA
		No load, V_{HIZ} = 2.0V	12.5	16	18	mA
V_{OUT}	Positive and Negative Output Swing	V_{IN} = ±3.5V, R_L = 500Ω	±3.2	±3.44		V
I_{OUT}	Output Current	R_L = 10Ω to GND	±80	±120	±180	mA
V_{OS}	Output Offset Voltage		-2	9	20	mV
Ib	Input Bias Current	V_{IN} = 0V	-5	-2.5	-1	µA
R_{out}	Output Resistance	HIZ = logic high, (DC), A_V = 1		1.4		MW
		HIZ = logic low, (DC), A_V = 1		0.2		Ω
R_{IN}	Input Resistance	V_{IN} = ±3.5V		10		MΩ
C_{IN}	Input Capacitance			1.1		pF
A_{CL} or A_V	Voltage Gain	V_{IN} = ±1.5V, R_L = 500Ω	0.999	1.001	1.003	V/V
I_{TRI}	Output Current in Three-state	V_{OUT} = 0V	-35	6	+35	µA
LOGIC						
V_H	Input High Voltage (Logic Inputs)		2			V
V_L	Input Low Voltage (Logic Inputs)				0.8	V
I_{IH}	Input High Current (Logic Inputs)		50		150	µA
I_{IL}	Input Low Current (Logic Inputs)		-10		5	µA
$t_{\overline{LE}}$	$\overline{LE1}$, $\overline{LE2}$ Minimum Pulse Width		-	4	-	ns
AC GENERAL						
-3dB BW	-3dB Bandwidth	V_{OUT} = 200mV_{P-P}, C_L = 1.6pF		1.0		GHz
		V_{OUT} = 2V_{P-P}, C_L = 23.6pF, R_S = 25Ω		230		MHz
0.1dB BW	0.1dB Bandwidth	V_{OUT} = 200mV_{P-P}, C_L = 1.6pF		80		MHz
		V_{OUT} = 2V_{P-P}, C_L = 23.6pF, R_S = 25Ω		50		MHz
dG	Differential Gain Error	NTSC-7, R_L = 150		0.01		%

Electrical Specifications

V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, R_L = 500Ω to GND, V_{HIZ} = 0.8V, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
dP	Differential Phase Error	NTSC-7, R_L = 150		0.02		°
+SR	Slew Rate	25% to 75%, V_{OUT} = 5V, R_L = 500Ω, C_L = 23.6pF, R_S = 25Ω		1515		V/µs
-SR	Slew Rate	25% to 75%, V_{OUT} = 5V, R_L = 500Ω, C_L = 23.6pF, R_S = 25Ω		1155		V/µs
PSRR	Power Supply Rejection Ratio	DC, PSRR V+ and V- combined V± = ±4.5V to ±5.5V	-50	-57		dB
ISO	Channel Isolation	f = 10MHz, Ch-Ch X-Talk and Off Isolation, C_L = 1.6pF		75		dB
SWITCHING CHARACTERISTICS						
V_{GLITCH}	Channel-to-Channel Switching Glitch	V_{IN} = 0V, C_L = 23.6pF, R_S = 25Ω		38		mV_{P-P}
	HIZ Switching Glitch	V_{IN} = 0V, C_L = 23.6pF, R_S = 25Ω		175		mV_{P-P}
t_{SW-L-H}	Channel Switching Time Low to High	1.2V logic threshold to 10% movement of analog output		32		ns
t_{SW-H-L}	Channel Switching Time High to Low	1.2V logic threshold to 10% movement of analog output		29		ns
TRANSIENT RESPONSE						
tr, tf	Rise and Fall Time, 10% to 90%	V_{OUT} = 200mV_{P-P}, C_L = 1.6pF		0.68		ns
		V_{OUT} = 2V_{P-P}, C_L = 23.6pF, R_S = 25Ω		1.4		ns
t_S	0.1% Settling Time	V_{OUT} = 2V_{P-P}, C_L = 23.6pF, R_S = 25Ω		6.8		ns
t_{PLH}	Propagation Delay - Low to High, 10% to 10%	V_{OUT} = 200mV_{P-P}, C_L = 1.6pF		0.5		ns
		V_{OUT} = 2V_{P-P}, C_L = 23.6pF, R_S = 25Ω		0.85		ns
t_{PHL}	Propagation Delay- High to Low, 10% to 10%	V_{OUT} = 200mV_{P-P}, C_L = 1.6pF		0.54		ns
		V_{OUT} = 2V_{P-P}, C_L = 23.6pF, R_S = 25Ω		0.88		ns
O_S	Overshoot	V_{OUT} = 200mV_{P-P}, C_L = 1.6pF		8.3		%
		V_{OUT} = 2V_{P-P}, C_L = 23.6pF, R_S = 25Ω		15.7		%

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = +25°C$, unless otherwise specified.

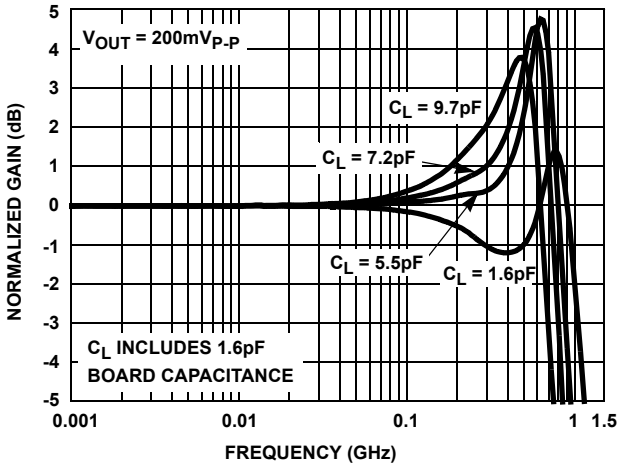


FIGURE 3. SMALL SIGNAL GAIN vs FREQUENCY vs C_L

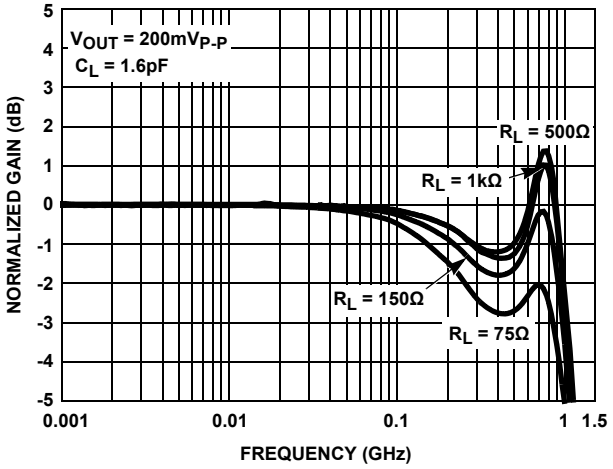


FIGURE 4. SMALL SIGNAL GAIN vs FREQUENCY vs R_L

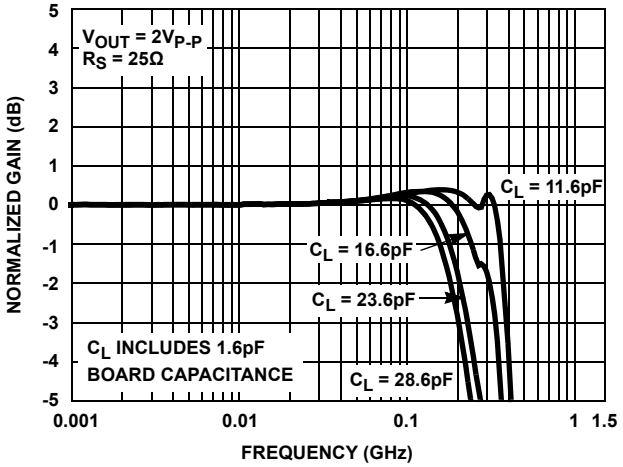


FIGURE 5. LARGE SIGNAL GAIN vs FREQUENCY vs C_L

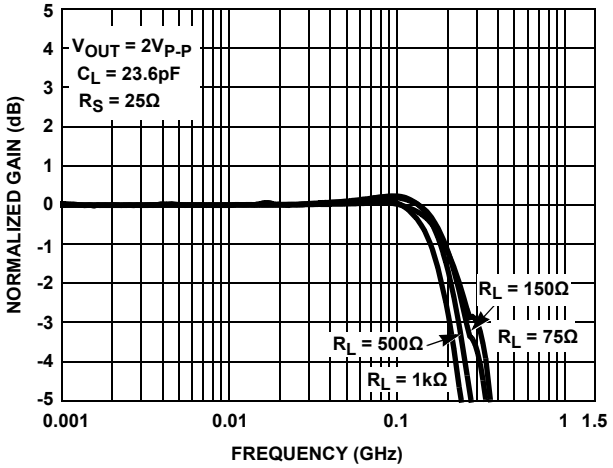


FIGURE 6. LARGE SIGNAL GAIN vs FREQUENCY vs R_L

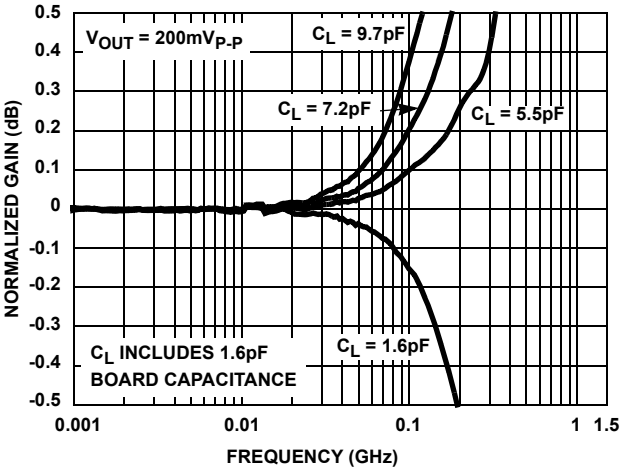


FIGURE 7. SMALL SIGNAL 0.1dB GAIN vs FREQUENCY vs C_L

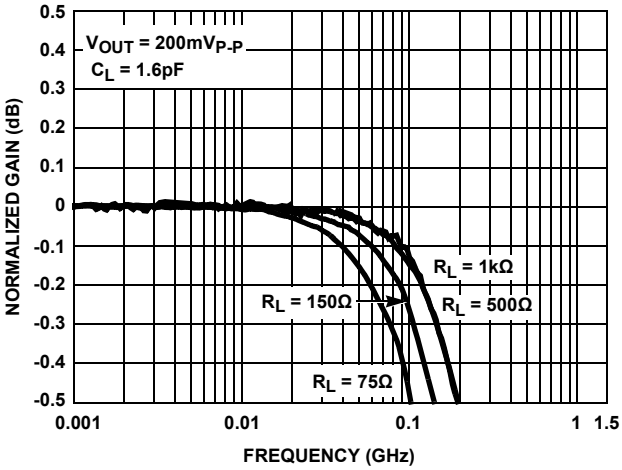


FIGURE 8. SMALL SIGNAL 0.1dB GAIN vs FREQUENCY vs R_L

Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = +25°C$, unless otherwise specified. **(Continued)**

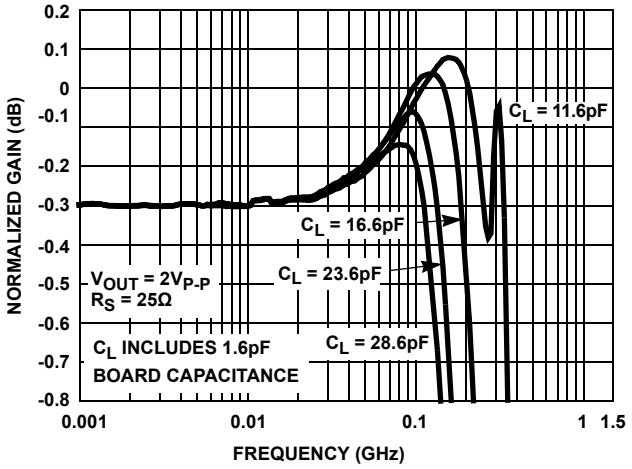


FIGURE 9. LARGE SIGNAL 0.1dB GAIN vs FREQUENCY vs C_L

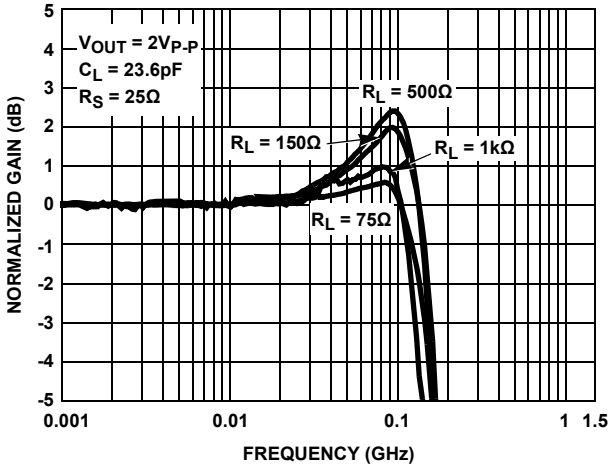


FIGURE 10. LARGE SIGNAL 0.1dB GAIN vs FREQUENCY vs R_L

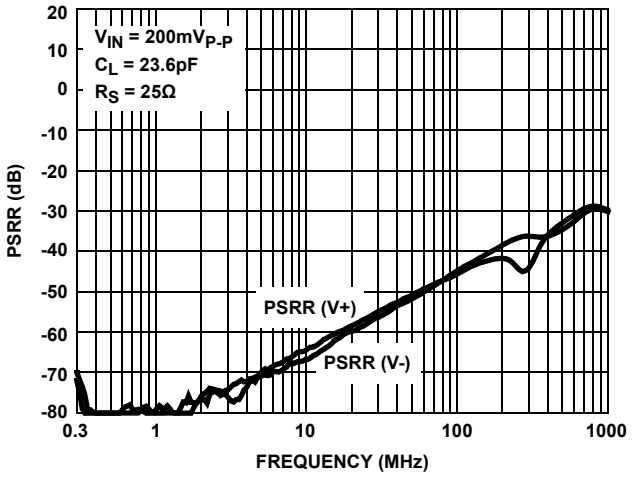


FIGURE 11. PSRR CHANNELS

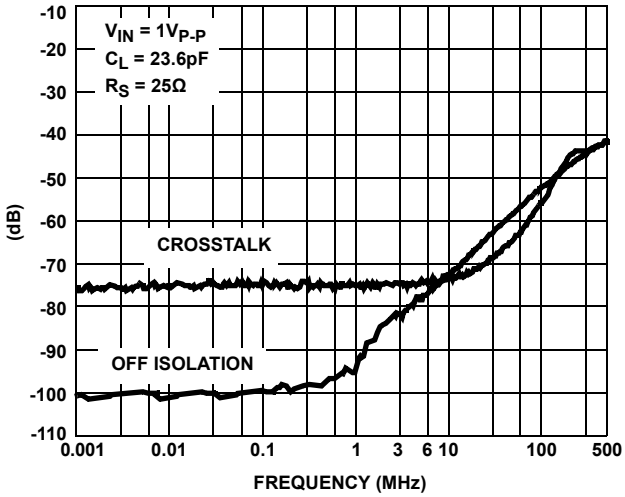


FIGURE 12. CROSSTALK AND OFF ISOLATION

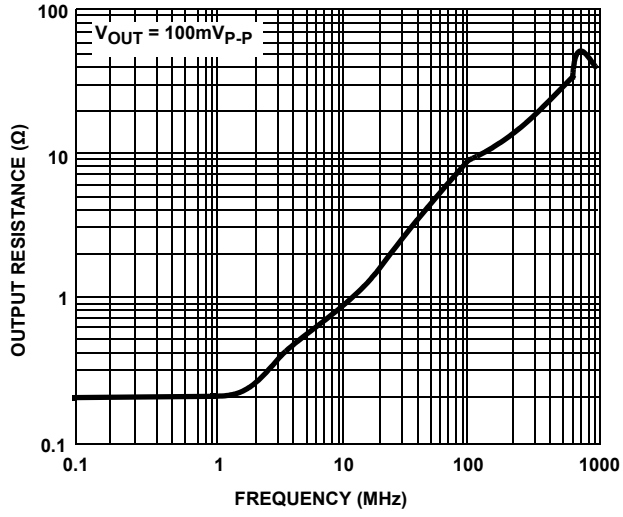


FIGURE 13. R_{OUT} vs FREQUENCY

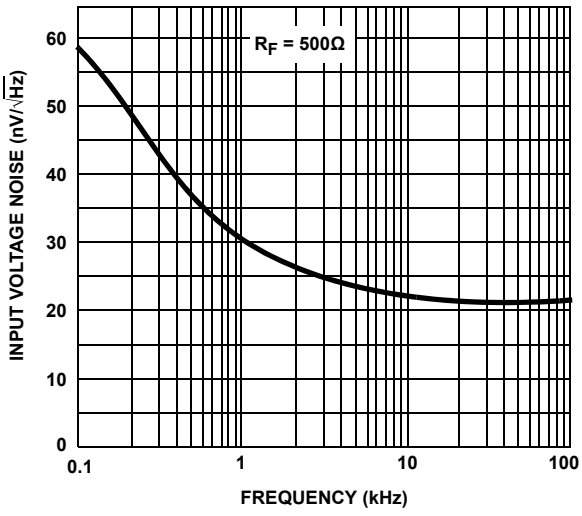


FIGURE 14. INPUT NOISE vs FREQUENCY

Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = +25°C$, unless otherwise specified. **(Continued)**

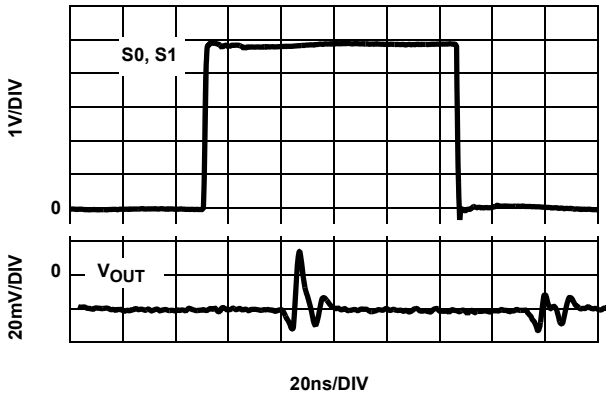


FIGURE 15. CHANNEL TO CHANNEL SWITCHING GLITCH V_{IN} = 0V, R_S = 25, C_L = 23.6pF

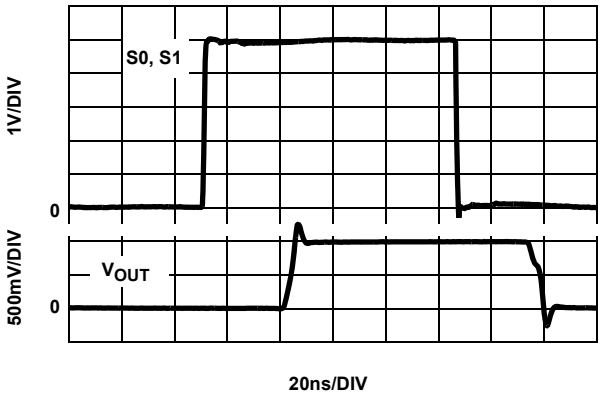


FIGURE 16. CHANNEL TO CHANNEL TRANSIENT RESPONSE V_{IN} = 1V, R_S = 25, C_L = 23.6pF

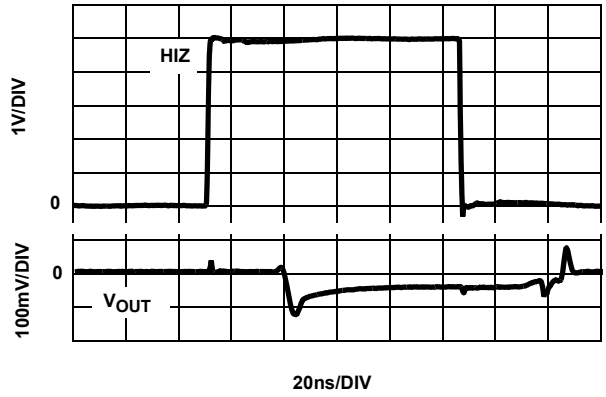


FIGURE 17. HIZ SWITCHING GLITCH V_{IN} = 0V, R_S = 25, C_L = 23.6pF

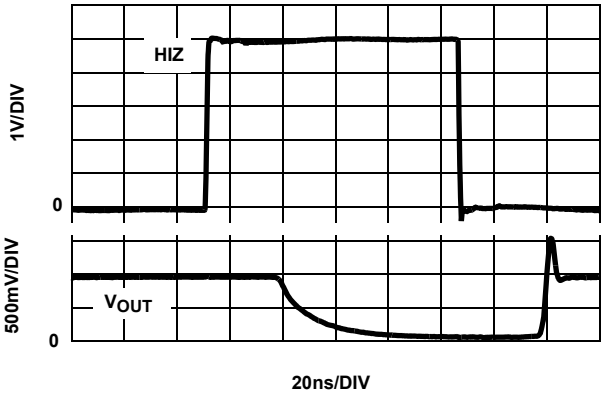


FIGURE 18. HIZ TRANSIENT RESPONSE V_{IN} = 1V, R_S = 25, C_L = 23.6pF

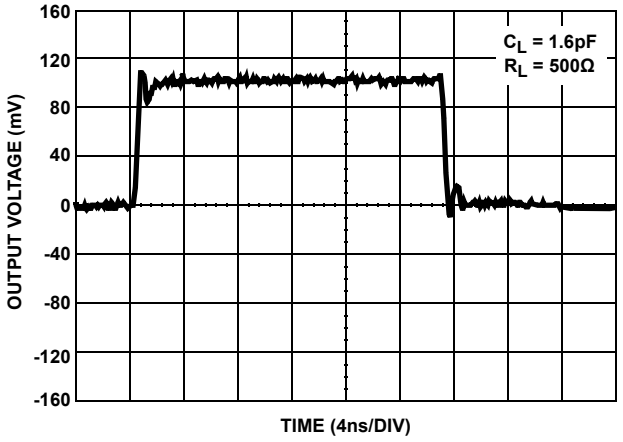


FIGURE 19. SMALL SIGNAL TRANSIENT RESPONSE

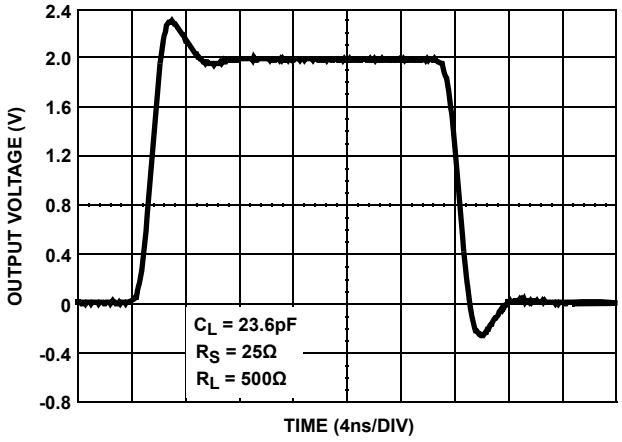


FIGURE 20. LARGE SIGNAL TRANSIENT RESPONSE

Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = +25°C$, unless otherwise specified. **(Continued)**

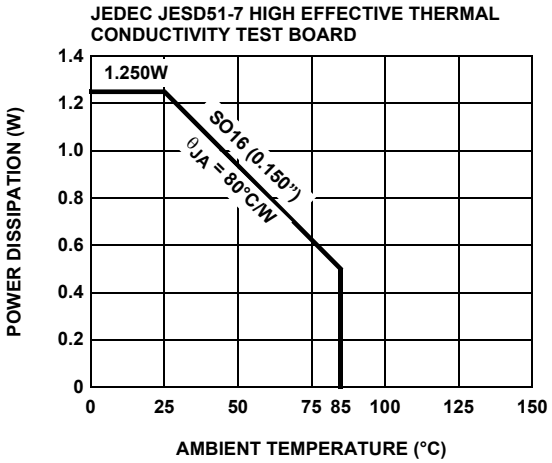


FIGURE 21. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

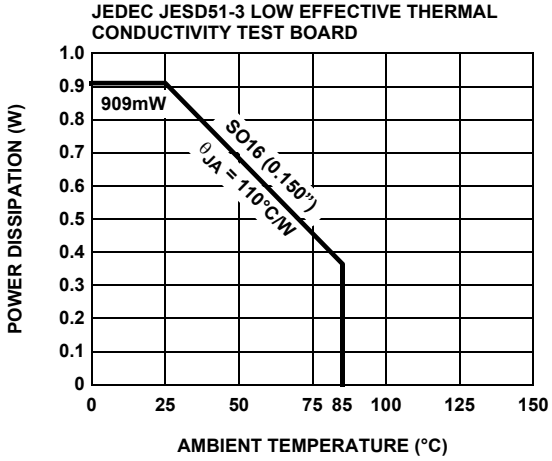


FIGURE 22. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

AC Test Circuits

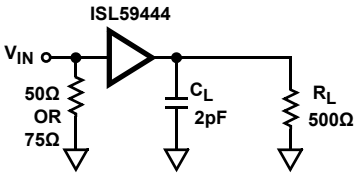


FIGURE 23A. TEST CIRCUIT WITH OPTIMAL OUTPUT LOAD

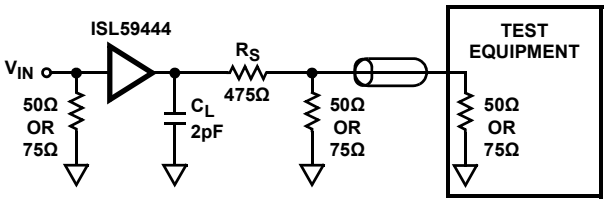


FIGURE 23B. TEST CIRCUIT FOR MEASURING WITH A 50Ω OR 75Ω INPUT TERMINATED EQUIPMENT

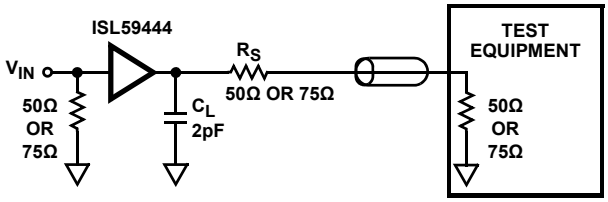


FIGURE 23C. BACKLOADED TEST CIRCUIT FOR VIDEO CABLE APPLICATION. BANDWIDTH AND LINEARITY FOR R_L LESS THAN 500Ω WILL BE DEGRADED.

Figure 23A illustrates the optimum output load for testing AC performance. Figure 23B illustrates the optimum output load when connecting to input terminated equipment. Figure 23C illustrates back loaded test circuit for video cable.

Application Circuits

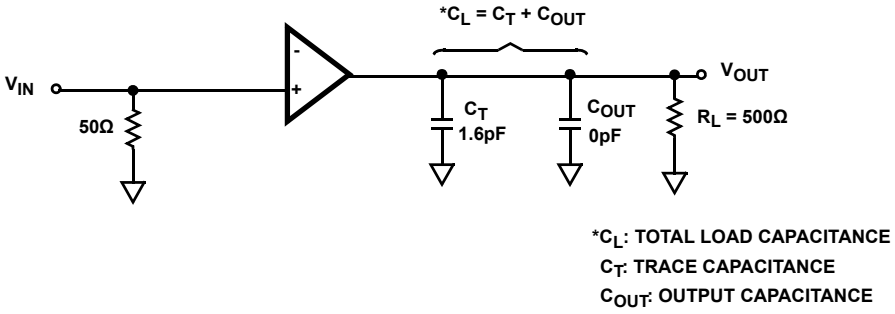


FIGURE 24A. SMALL SIGNAL 200mV_{P-P} APPLICATION CIRCUIT

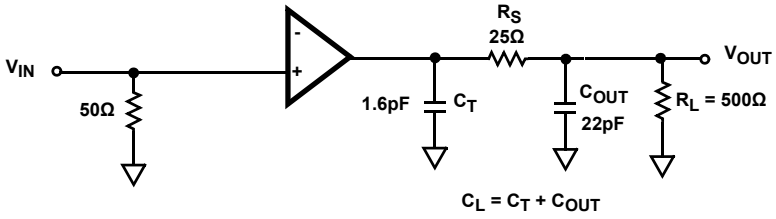


FIGURE 24B. LARGE SIGNAL 1V_{P-P} APPLICATION CIRCUIT

Application Information

General

The ISL59444 is a 4:1 mux that is ideal as a matrix element in high performance switchers and routers. The ISL59444 is optimized to drive a 2pF in parallel with a 500Ω load. The capacitance can be split between the PCB capacitance an and external load capacitance. Their low input capacitance and high input resistance provide excellent 50Ω or 75Ω terminations.

Capacitance at the Output

The output amplifier is optimized for capacitance to ground (C_L) directly on the output pin. Increased capacitance causes higher peaking with an increase in bandwidth. The optimum range for most applications is ~1.0pF to ~6pF. The optimum value can be achieved through a combination of PC board trace capacitance (C_T) and an external capacitor (C_{OUT}). A good method to maintain control over the output pin capacitance is to minimize the trace length (C_T) to the next component, and include a discrete surface mount capacitor (C_{OUT}) directly at the output pin.

For large signal applications where overshoot is important the circuit in Figure 24B should be used. The series resistor (R_S) and capacitor (C_L) form a low pass network that limits system bandwidth and reduces overshoot. The component values shown result in a typical pulse response shown in Figure 20.

Ground Connections

For the best isolation and crosstalk rejection, the GND pin and NIC pins must connect to the GND plane. The NIC pins are placed on both sides of the input pins. These pins are not internally connected to the die. It is recommended this pin be tied to ground to minimize crosstalk.

Control Signals

S0, S1, HIZ - These pins are, TTL/CMOS compatible control inputs. The S0, S1 pins select which one of the inputs connect to the output. The HIZ pin is used to three-state the output amplifiers. For control signal rise and fall times less than 10ns the use of termination resistors close to the part will minimize transients coupled to the output.

HIZ State

An internal pull-down resistor connected to the HIZ pin ensures the device will be active with no connection to the HIZ pin. The HIZ state is established within approximately 30ns by placing a logic high (>2V) on the HIZ pin. If the HIZ state is selected, the output is a high impedance 1.4MΩ. Use this state to control the logic when more than one mux shares a common output.

In the HIZ state the output is three-stated, and maintains its high Z even in the presence of high slew rates. The supply current during this state is basically the same as the active state.

Latch State

The latched control signals allow for synchronized channel switching. When $\overline{LE1}$ is low the master control latch loads the next switching address (S0, S1), while the closed (assuming $\overline{LE2}$ is the inverse of $\overline{LE1}$) slave control latch maintains the current state. $\overline{LE2}$ switching low closes the master latch (with previous assumption), loads the now open slave latch, and switches the crosspoint to the newly selected channel. Channel selection is asynchronous (changes with any control signal change) if both $\overline{LE1}$ and $\overline{LE2}$ are low.

Power-Up Considerations

The ESD protection circuits use internal diodes from all pins the V+ and V- supplies. In addition, a dv/dt triggered clamp is connected between the V+ and V- pins, as shown in the Equivalent Circuits 1 through 4 section of the “Pin Descriptions” on page 2. The dv/dt triggered clamp imposes a maximum supply turn-on slew rate of 1V/µs. Damaging currents can flow for power supply rates-of-rise in excess of 1V/µs, such as during hot plugging. Under these conditions, additional methods should be employed to ensure the rate of rise is not exceeded.

Consideration must be given to the order in which power is applied to the V+ and V- pins, as well as analog and logic input pins. Schottky diodes (Motorola MBR0550T or equivalent) connected from V+ to ground and V- to ground (Figure 25) will shunt damaging currents away from the internal V+ and V- ESD diodes in the event that the V+ supply is applied to the device before the V- supply.

If positive voltages are applied to the logic or analog video input pins before V+ is applied, current will flow through the internal ESD diodes to the V+ pin. The presence of large decoupling capacitors and the loading effect of other circuits connected to V+, can result in damaging currents through the ESD diodes and other active circuits within the device. Therefore, adequate current limiting on the digital and analog inputs is needed to prevent damage during the time the voltages on these inputs are more positive than V+.

Limiting the Output Current

No output short circuit current limit exists on these parts. All applications need to limit the output current to less than 50mA. Adequate thermal heat sinking of the parts is also required.

PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- The use of low inductance components such as chip resistors and chip capacitors is strongly recommended.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners, use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces greater than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. High frequency performance may be degraded for traces greater than one inch, unless strip lines are used.
- Match channel-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize use of AC de-coupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e., no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- Use proper value and location of termination resistors. Termination resistors should be as close to the device as possible.
- When testing use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- Minimum of 2 power supply de-coupling capacitors are recommended (1000pF, 0.01µF) as close to the devices as possible. Avoid vias between the cap and the device because vias add unwanted inductance. Larger caps can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.
- The NIC pins are placed on both sides of the input pins. These pins are not internally connected to the die. It is recommended these pins be tied to ground to minimize crosstalk.

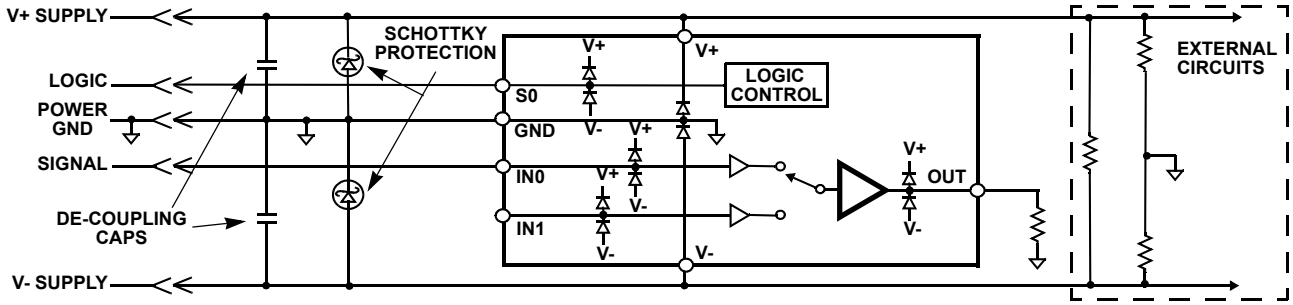
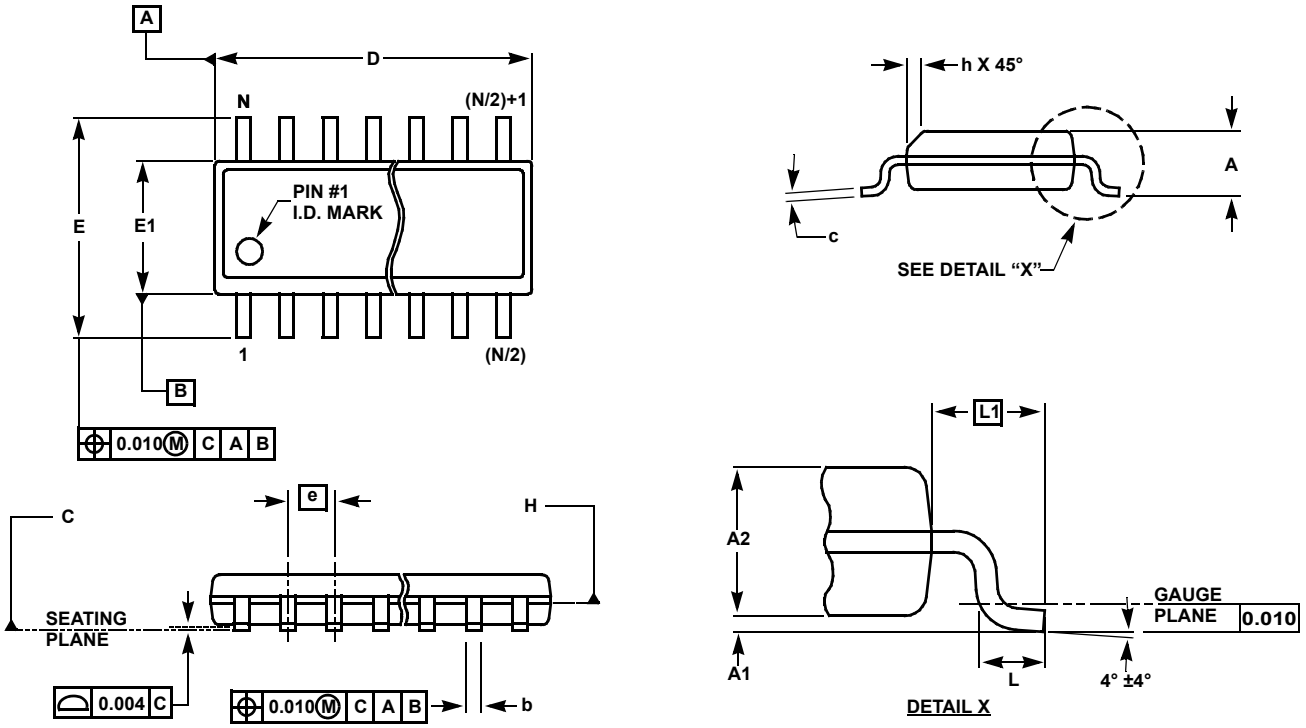


FIGURE 25. SCHOTTKY PROTECTION CIRCUIT

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994