IS31SE5118

8-CH PROGRAMMABLE CAPACITIVE TOUCH SENSOR

December 2021

GENERAL DESCRIPTION

IS31SE5118 is an ultra-low power, 8-channel capacitive touch controller. The controller allows sleep mode and uses auto detection for wakeup. It also provides a shield output to increase moisture immunity. The built-in hardware monitor and calibration for the environment is to prevent false triggers.

A host MCU is required to communicate with IS31SE5118. An on-chip I²C slave controller with 400kHz capability serves as the communication port for the host MCU. An interrupt, INT, can be configured and it is generated when a touch trigger event occurs. Trigger condition can be configured by setting the interrupt register.

IS31SE5118 is available in TSSOP-16 package. It operates from 2.7V to 5.5V over the temperature range from -40°C to +105°C.

FEATURES

- 8-channel capacitive touch controller with readable key value
- Touch threshold setting for individual key
- Optional multiple-key function
- Individual key calibration
- Interrupt output with auto-clear and repeating
- Auto sleep mode for extremely low power
- Keys wake up from sleep mode
- Buzzer/Melody Generator
- 400kHz fast-mode I²C interface
- Operating temperature between -40°C to +105°C
- TSSOP-16 ROHS compliant package

APPLICATIONS

- Touch keys for home appliances
- Touch keys for industrial control

TYPICAL APPLICATION CIRCUIT (TSSOP-16)

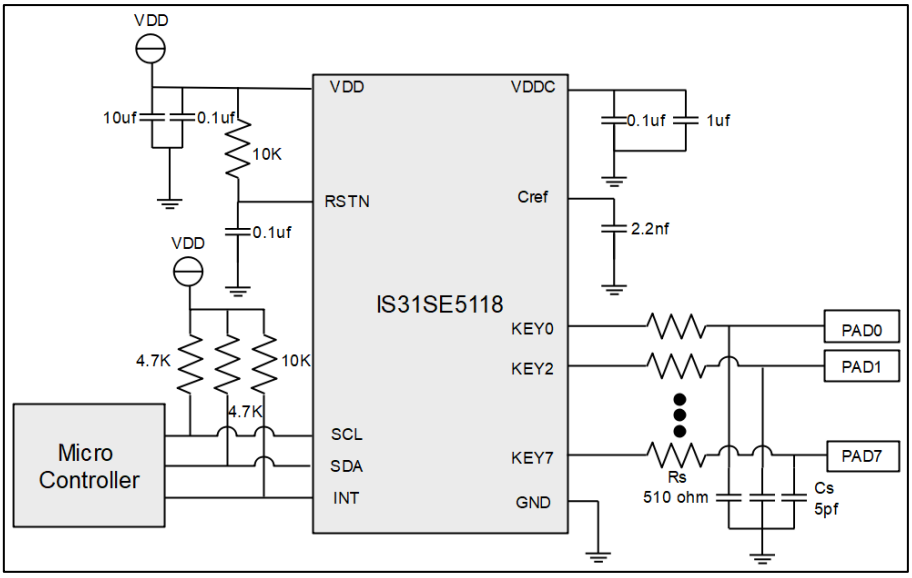


Figure 1: Typical Application Circuit (TSSOP-16)

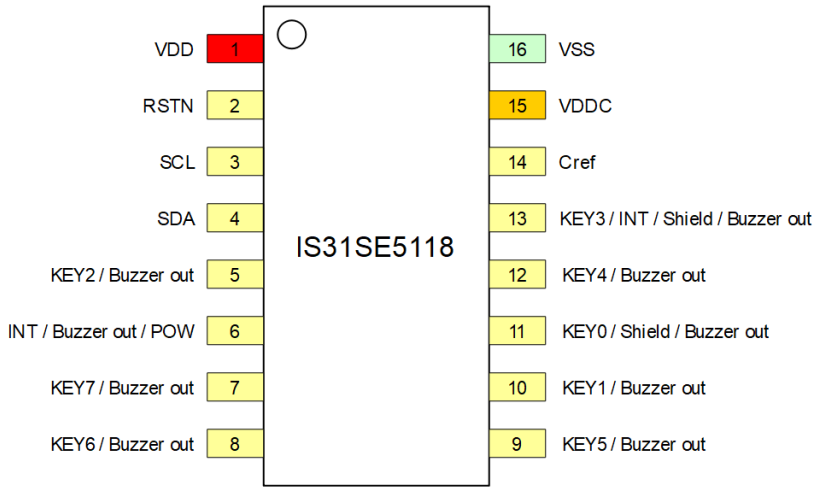
Note 1: SE5118 should be placed far away from the noise source for EMS.

Note 2: R_S and C_S should be placed as close to the chip as possible to reduce EMI.

Note 3: INT can be configured as POW pin for melody application.

Note 4: The capacitors connected to VDD and VDDC should be as close to chip as possible to reduce EMI.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
TSSOP-16	

PIN DESCRIPTION

No.	Pin	Description
1	VDD	Power supply
2	RSTN	Reset Low Active
3	SCL	I2C serial clock
4	SDA	I2C serial data
5	KEY2/Buzzer out	Multiple function pin. Can be configured to touch sense channel 2 or Buzzer output.
6	INT/Buzzer out/ POW	Multiple function pin. Can be configured to interrupt output (active low), Buzzer output or melody power control (POW).
7 – 10	KEY7/6/5/1/ Buzzer out	Multiple function pins. Can be configured to Input sensor channel (refer to the pin configuration) or Buzzer output.
11	KEY0/Shield/ Buzzer out	Multiple function pin. Can be configured to Input sense channel 0, Shield output or Buzzer output.
12	KEY4/Buzzer out	Multiple function pin. Can be configured to Input sense channel 4 or Buzzer output.
13	KEY3/INT/ Shield/ Buzzer out	Multiple function pin. Can be configured to Input sense channel 3, interrupt output (active low), Shield output or Buzzer output.
14	Cref	External reference Capacitor for touch sense
15	VDDC	Internal 1.5V power supply. Connect to external 1.0uF decoupling capacitor.
16	VSS	Ground

ORDERING INFORMATION

Industrial Range: -40°C to +105°C

Order Part No.	Package	QTY
IS31SE5118-ZNLS3-TR	TSSOP-16, Lead-free	2500/Reel

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +105°C
Junction Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}(TSSOP-16)	50.2°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 2.7V ~ 5.5V, unless otherwise noted. Typical values are T_A = 25°C, V_{CC} = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{CC} = 5.5V		50		μA
ΔC_S	Minimum detectable capacitance	C_S = 5pF (Note 4)		0.2		pF
Logic Electrical Characteristics						
V_{IL}	Logic "0" input voltage	V_{CC} = 2.7V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC} = 5.5V	1.4			V
I_{IL}	Logic "0" input current	V_{INPUT} = 0V (Note 4)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT} = V_{CC} (Note 4)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 4)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time				0.9	μs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals	(Note 5)		20+0.1C_b	300	ns
t_F	Fall time of both SDA and SCL signals	(Note 5)		20+0.1C_b	300	ns

Note 4: Guaranteed by design.

Note 5: C_b = total capacitance of one bus line in pF. I_{SINK} ≤ 6mA. t_R and t_F measured between 0.3 × V_{CC} and 0.7 × V_{CC}.

FUNCTION BLOCK DIAGRAM

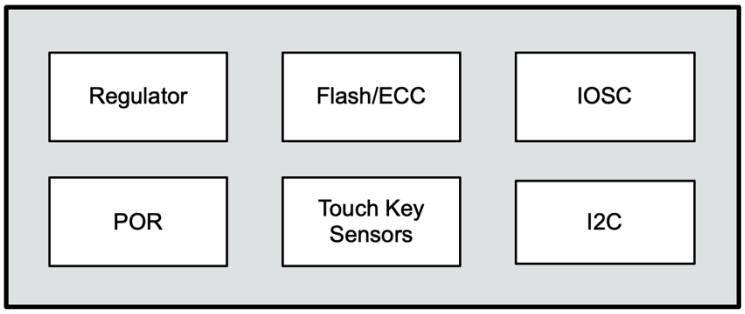


Figure 2: Functional Block Diagram

Basic introduction for touch sense data process flow

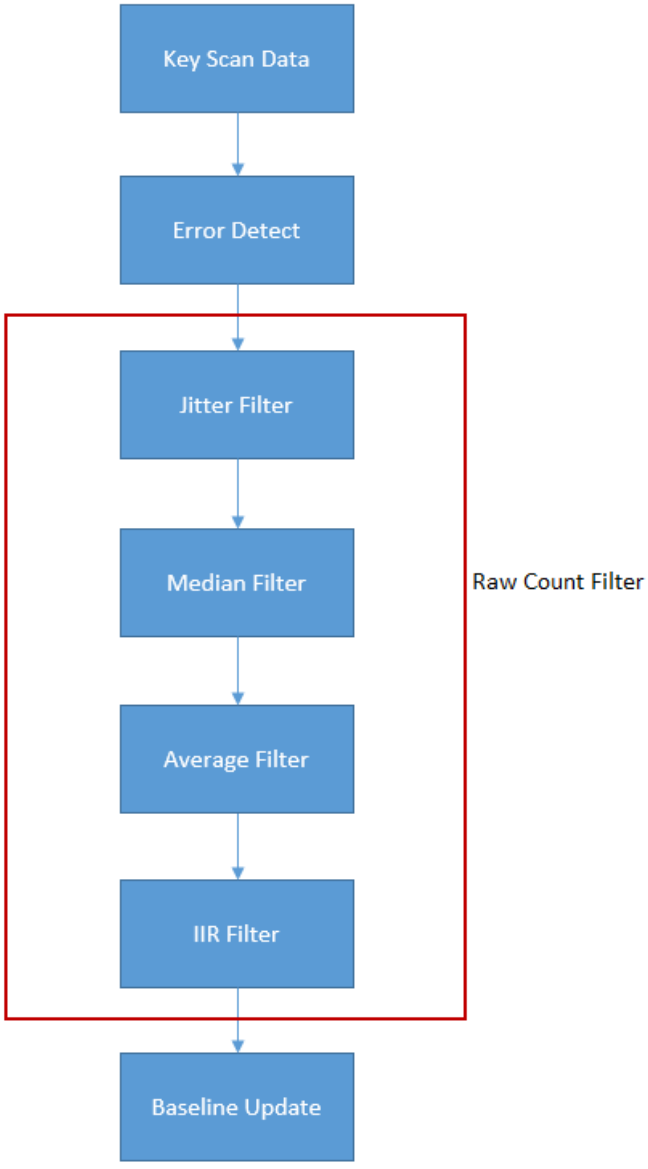


Figure 3: Touch Sense Data Process Flow

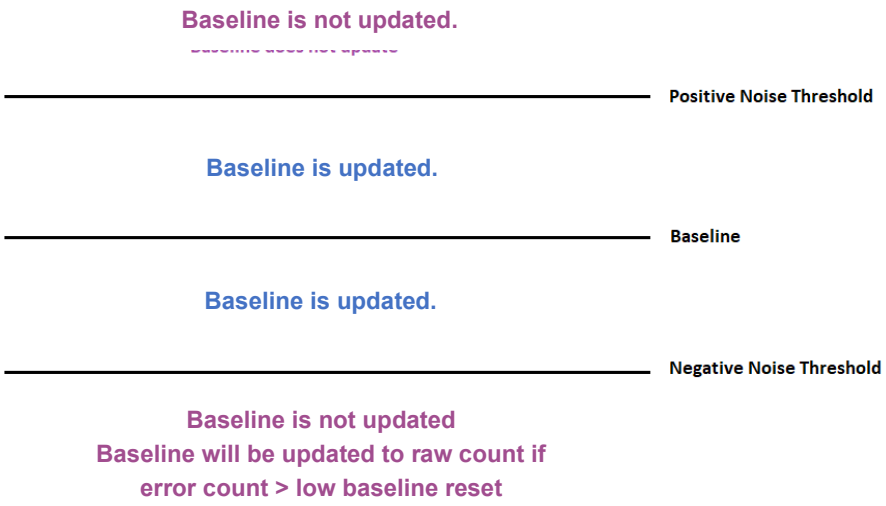


Figure 4: Baseline Process based on difference of baseline and raw count

Touch sense data identification

Ignore touch key scan if the signal exceeds the lock threshold.

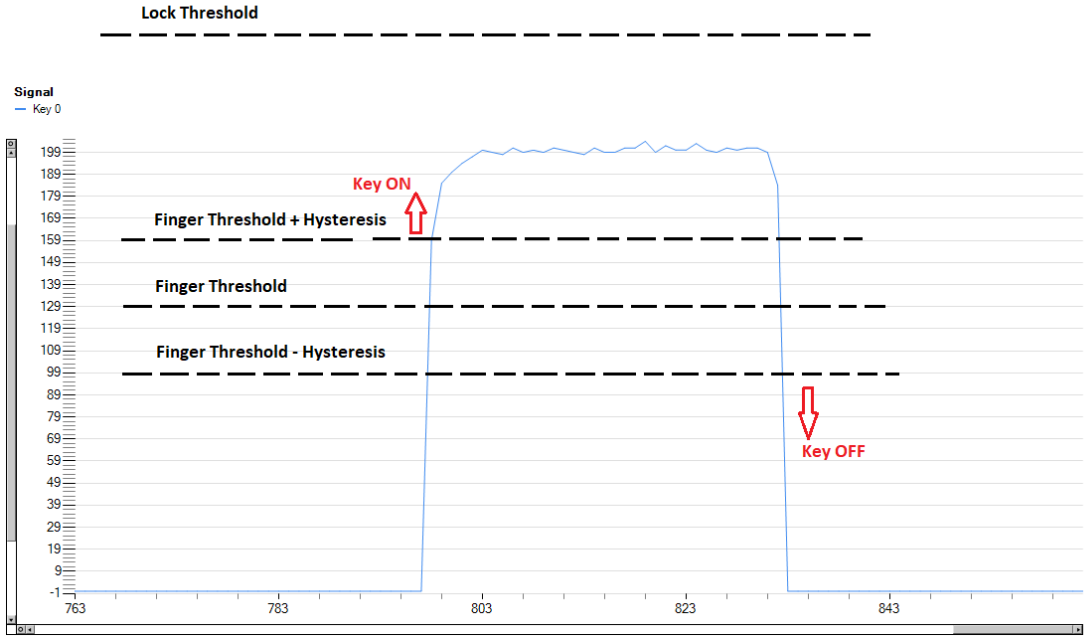


Figure 5: Touch Sense Data Identification

DETAILED DESCRIPTION

I2C INTERFACE

IS31SE5118 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. IS31SE5118 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 "0" for a write command and set A0 "1" for a read command.

The complete slave address is:

Bit	A7:A1	A0
Value	0111100	1/0

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. During communication, microcontroller is the master and IS31SE5118 is the slave.

The timing diagram for the I2C is shown in Figure 6. The SDA is latched on the stable high level of the SCL. When there is no bus activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next and most significant bit first. Each address bit must be ready while the SCL level is high.

After the last bit of the chip address is sent, the master checks for IS31SE5118's acknowledge. The master releases the SDA line high (through a pull-up resistor). and sends an SCL pulse. If IS31SE5118 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31SE5118, the register address byte is sent and most significant bit first. IS31SE5118 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, and most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, IS31SE5118 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

READING PORT REGISTERS

To read the device data, the bus master must first send the address of IS31SE5118 with the R/$\overline{W}$ bit set to "0", followed by the register address byte, which determines which register is accessed. After a restart, the bus master must send IS31SE5118 address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is sent from IS31SE5118 to the master (Figure 9).

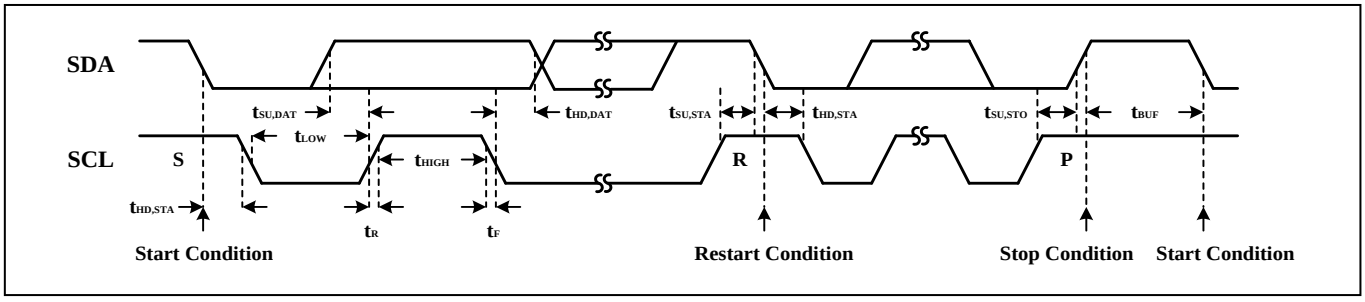


Figure 6: Interface Timing

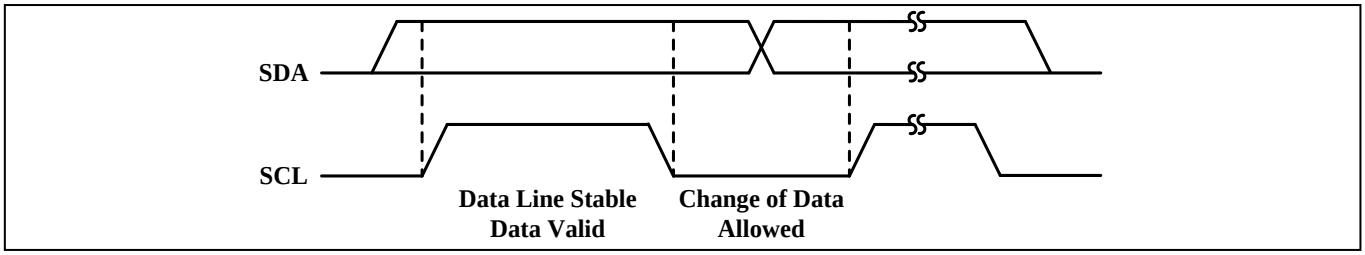


Figure 7: Bit Transfer

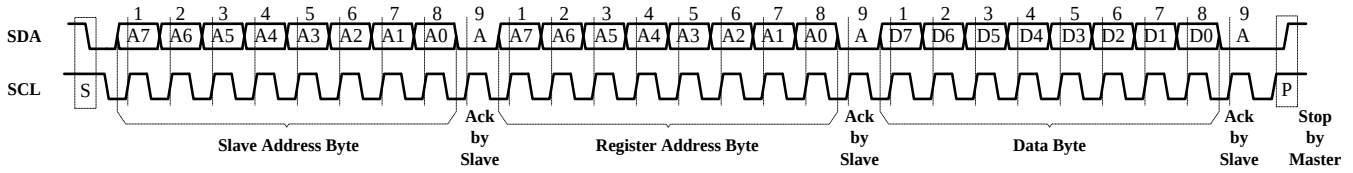


Figure 8: Writing to IS31SE5118

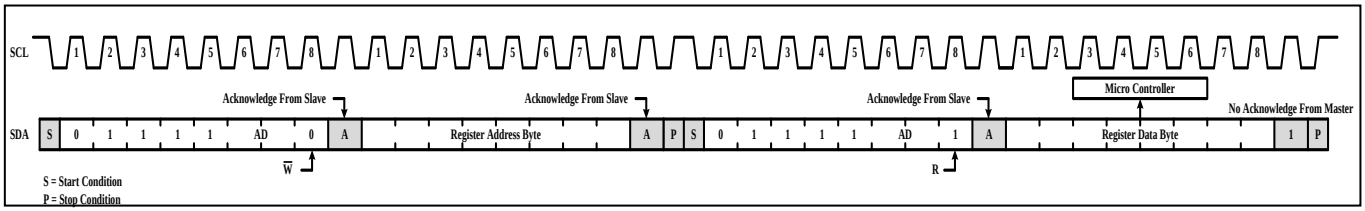


Figure 9: Reading from IS31SE5118

Note: Successive read or write protocol is supported.

REGISTER DEFINITION

Address	Name	Definition	R/W	Default
00h	Chip Part Number	Chip's part number	R	18h
01h-02h	Chip Version	Chip's version	R	-
03h	Firmware Version	Firmware version	R	40h
04h	Main Control	System reset, power saving and parameters management	W	00h
05h	-	Reserved	-	-
06h	Key Status	Key 0-Key 7 status bits	R	00h
07h	Buzzer W	Buzzer data or stop command	W	-
07h	Buzzer R	Available buzzer buffer size	R	0Ah
08h-0Fh	Key Signal	Key 0-Key 7 signal value	R	00h
10h-1Fh	Key Raw Count	Key 0-Key 7 raw count value	R	0000h
20h-2Fh	Key Baseline	Key 0-Key 7 baseline value	R	0000h
30h-37h	Key Finger Threshold	Key 0-Key 7 finger threshold setting	R/W	8Ch
38h-3Fh	Key Noise Threshold	Key 0-Key 7 noise threshold setting	R/W	46h
40h-47h	Key Negative Noise Threshold	Key 0-Key 7 negative noise threshold setting	R/W	46h
48h-4Fh	Key Low Baseline Reset	Key 0-Key 7 low baseline reset setting	R/W	1Eh
50h-57h	Key Hysteresis	Key 0-Key 7 hysteresis setting	R/W	12h
58h-5Fh	Key ON Debounce	Key 0-Key 7 de-bounce setting	R/W	02h
60h	Key Interrupt Enable	Key 0-Key 7 enable Interrupts associated with capacitive touch sensor inputs	R/W	00h
61h	Raw Count Filter	Raw count filter setting	R/W	00h
62h	Baseline IIR Ratio	Baseline IIR ratio setting	R/W	01h
63h	Lock Threshold High Byte	Lock threshold High Byte setting	R/W	03h
64h	Lock Threshold Low Byte	Lock threshold Low Byte setting	R/W	E8h
65h	Lock Scan Cycle	Lock scan cycle setting	R/W	08h

66h	Raw Count Difference Limit	Raw count difference limit setting	R/W	64h
67h	Multi Touch Key Configure	Multiple touch key function setting	R/W	01h
68h	Max Duration Time	Maximum duration time setting	R/W	1Ah
69h	Interrupt Configuration	Interrupt configuration	R/	0Ah
6Ah	Interrupt Repeat Time	Repeat cycle for pressing key interrupt setting	R/W	00h
6Bh	Key Pin Select	Select pins as Key0-Key7	R/W	00h
6Ch	Shield Pin Select	Select pin as shield	R/W	08h
6Dh-6Eh	INT Pin Select	Select pin as INT	R/W	0000h
6Fh	Buzzer Pin Select	Select pin as buzzer for Key0-Key7	R/W	04h
70h	Buzzer Pin Select	Select pin as buzzer for Pin 13	R/W	00h
71h	Buzzer Power Pin Select	Select pin as buzzer power for Key0-Key7	R/W	00h
72h	Buzzer Power Pin Select	Select pin as buzzer power for Pin 13	R/W	01h
73h	TKIII Control 1	Repeat sequence, discard starting edges, inserts an inter-sequence idle time, and low frequency noise filter	R/W	13h
74h	TKIII Control 2	Pseudo random sequence setting	R/W	20h
75h	TKIII Control 3	Multi frequency scan/cycle count setting	R/W	03h
76h	TKIII CCHG	Internal charge capacitance setting	R/W	60h
77h	TKIII PUD	Pull-up current/ pull-up resistors setting	R/W	00h
78h	System Clock Select	System clock setting	R/W	00h
79h	Spread Spectrum	Spread spectrum setting	R/W	0Ch
7Ah	Auto Sleep Mode	Auto enter sleep mode time setting	R/W	0Fh
7Bh	Sleep Mode Control	Sleep mode control setting	R/W	00h
7Ch	Wake Up Key Select	Select Key0~Key7 to exit sleep mode	R/W	00h
7Dh	Wake Up Threshold	Wake up threshold setting	R/W	08h
7Eh	TKIII Sleep Mode CCHG	Sleep mode internal charge capacitance setting	R/W	60h

7Fh	TKIII Sleep Mode PUD	Sleep mode pull-up current/ pull-up resistors setting	R/W	00h
80h-81h	Sleep Mode Raw Count	Sleep mode raw count value	R	0000h
82h-83h	Sleep Mode Baseline	Sleep mode baseline value	R	0000h
84h	Key Scan Once	I2C control key scan	R/W	00h
85h	Table Ready Mark	Mark for flash data ready	R	00h

00h Chip Part Number Register (RO)

Bit	D7:D0
Name	CPN[7:0]
Default	0001 1000

CPN Chip Part Number

Chip's part number 18h

01h Chip Version Register 1 (RO)

Bit	D7:D0
Name	CV1[7:0]
Default	-

CV1 Chip Version information 1

02h Chip Version Register 2 (RO)

Bit	D7:D0
Name	CV2[7:0]
Default	-

CV2 Chip Version information 2

CV1 & CV2 bytes contain chip revision. CV1 indicates mask set version. CV2 indicates minor version.

03h Firmware Version Register (RO)

Bit	D7:D0		
Name	FV1[2:0]	FV2[2:0]	FV3[1:0]
Default	010	000	00

FV Firmware Version

Default version is 2.0.0
FV1[2:0] Major version
FV2[2:0] Minor version
FV3[1:0] Patch version

04h Main Control Register (WO)

Bit	D7	D6	D5	D4	D3	D2:D0
Name	SR	RD	-	SP	SS	-
Default	0	0	0	0	0	000

SR System Reset

1 System reset

RD Reset All Parameters to Manufacturer Default Setting.

1 Reset all user defined parameters to manufacture default setting.

SP Sleep Mode

1 Sleep mode

SS Save User Defined Parameters

1 Save current parameters into flash.

05h Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Reserved

06h Key Status Register (RO)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

KSx Key0~Key7 Status

If the key is detected as pressed, the corresponding bit (KSx) will be set to “1”.

0 Not detected

1 Key is detected.

07h Buzzer Register (W)

Bit	D7:D0
Name	BW[7:0]
Default	-

BW Buzzer Register Write

Buzzer data or stop command

07h Buzzer Register (R)

Bit	D7:D0
Name	BR[7:0]
Default	0000 1010

BR Buzzer Register Read

It shows the available tone buffer size. SE5118 has 10 built-in note buffers.

08h~0Fh KEY0~KEY7 Signal Register (RO)

Bit	D7:D0
Name	KEYx_SIGNAL[7:0]
Default	0000 0000

KEYx_SIGNAL Key Signal Count

The difference between baseline and raw count.

The maximum value is 254. It will keep 254 if the value is over 254. Value 255 means noise existence.

10h, 12h …, 1Ch, 1Eh KEY0~KEY7 Raw Count High Byte Register (RO)

Bit	D7:D0
Name	KEYx_RAWCOUNT[15:8]
Default	0000 0000

11h, 13h …, 1Dh, 1Fh KEY0~KEY7 Raw Count Low Byte Register (RO)

Bit	D7:D0
Name	KEYx_RAWCOUNT[7:0]
Default	0000 0000

KEYx_RAWCOUNT

Raw count of each key, provides an indication of the magnitude of the sensor’s capacitance.

20h, 22h …, 2Ch, 2Eh KEY0~KEY7 Baseline High Byte Register (RO)

Bit	D7:D0
Name	KEYx_BASELINE[15:8]
Default	0000 0000

21h, 23h …, 2Dh, 2Fh KEY0~KEY7 Baseline Low Byte Register (RO)

Bit	D7:D0
Name	KEYx_BASELINE[7:0]
Default	0000 0000

KEYx_Baseline

Baseline of each key

30h~37h KEY0~KEY7 Finger Threshold Register (RW)

Bit	D7:D0
Name	KEYx_TH[7:0]
Default	1000 1100

KEYx_TH

Finger threshold of each key. It is used with hysteresis to determine the key state.

38h~3Fh KEY0~KEY7 Noise Threshold Register (RW)

Bit	D7:D0
Name	KEYx_NTH[7:0]
Default	0100 0110

KEYx_NTH

Noise threshold of each key

Baseline needs to be updated if the difference (baseline and raw count) is less than the noise threshold.

40h~47h KEY0~KEY7 Negative Noise Threshold Register (RW)

Bit	D7:D0
Name	KEYx_NNTH[7:0]
Default	0100 0110

KEYx_NNTH
Negative noise threshold of each key

48h~4Fh KEY0~KEY7 Low Baseline Reset Register (RW)

Bit	D7:D0
Name	RCx[7:0]
Default	0001 1110

RCx Reset Count
Low baseline reset count of each key. A reset count increases one if the absolute |raw count – baseline| > absolute |negative noise threshold|. Once the reset count exceeds the low baseline register value, the baseline is reset to the current raw count. The reset count will be reset to 0 if the absolute |raw count – baseline| <= absolute |negative noise threshold|.

50h~57h KEY0~KEY7 Hysteresis Register (RW)

Bit	D7:D0
Name	HYSTERESISx[7:0]
Default	0001 0010

HYSTERESISx
Hysteresis of each key

58h~5Fh KEY0~KEY7 On Debounce Register (RW)

Bit	D7:D0
Name	DEBOUNCEx[7:0]
Default	0000 0010

DEBOUNCEx
De-bounce number of each key. When the acquired number > de-bounce setting value, then the key is granted as on.

60h Key Interrupt Enable Register (RW)

Bit	D7:D0
Name	INTEN[7:0]
Default	0000 0000

The Interrupt Enable Register determines whether a key is detected and it causes the interrupt pin to be asserted.

INTEN	Key Interrupt Enable
0	Disable
1	Enable

The default value for Interrupt Enable Registers is interrupt disable. Setting INE bit of Interrupt Configuration Register (69h) to “1”, INT pin will generate interrupt signal.

61h Raw Count Filter Register (RW)

Bit	D7	D6	D5:D4	D3	D2:D1	D0
Name	MF	AF	IIR[1:0]	JF	JD[1:0]	-
Default	0	0	00	0	00	0

MF	Median Filter
0	Disable
1	Enable

AF	Average Filter
0	Disable
1	Enable

IIR	IIR Filter
00	Disable
01	1/2
10	1/4
11	1/8

JF	Jitter Filter
0	Disable
1	Enable

JD	Jitter Delta
00	1
01	2
10	4
11	8

62h Baseline IIR Ratio Register (RW)

Bit	D7:D0
Name	RATIO[7:0]

Default	0000 0001

RATIO

Range 1 ~ 255

63h Lock Threshold High Byte Register (RW)

Bit	D7:D0
Name	LT[15:8]
Default	0000 0011

64h Lock Threshold Low Byte Register (RW)

Bit	D7:D0
Name	LT[7:0]
Default	1110 1000

LT Lock Threshold

65h Lock Scan Cycle Register (RW)

Bit	D7:D0
Name	LSC[7:0]
Default	0000 1000

LSC Lock Scan Cycle

Ignore the key scan data for the setting Lock scan cycle if the |raw count – baseline| > Lock threshold.

66h Raw Count Difference Limit Register (RW)

Bit	D7:D0
Name	RCDL[7:0]
Default	0110 0100

RCDL Raw Count Difference Limit

Ignore the key scan data if the difference between previous raw count and current raw count exceeds the limit.

67h Multiple Touch Key Configure Register (RW)

Bit	D7:D2	D1:D0
Name	-	MTK[1:0]
Default	000000	01

MTK Multi Touch Key

01 Allow one key triggered at one time.

10 Allow two keys triggered at one time.

11 Allow three keys triggered at one time.

68h Max Duration Time Register (RW)

Bit	D7	D6	D5	D4	D3:D0
Name	-	-	-	MDEN	MDT[3:0]-
Default	0	0	0	1	1010

MDEN Maximum Duration Time Enable

0 Disable

1 Enable

MDT Maximum Duration Time

0000 0.5s

0001 1s

0010 2s

0011 3s

0100 4s

0101 5s

0110 6s

0111 7s

1000 8s

1001 9s

1010 10s

1011 11s

1100 12s

1101 13s

1110 14s

1111 15s

MDT bits set the pressed time. When key pressed duration exceeds the programmed time (MDT), device will be forced to calibrate the pressed key. Set MDEN to “1” will enable this function.

69h Interrupt Configuration Register (RW)

Bit	D7	D6:D4	D3	D2:D0
Name	INE	-	ACEN	ACT[2:0]
Default	0	000	1	010

INE Interrupt Function Enable

0 Disable

1 Enable

ACEN Auto-Clear Interrupt Enable

0 Disable

1 Enable

ACT Auto-Clear Interrupt Time

000	10ms
001	20ms
010	30ms
011	40ms
100	50ms
101	100ms
110	150ms
111	200ms

When ACEN=0, the INT will keep low until device 06h register is read or the key is released. When ACEN=1, the INT will be released after ACT setting time is expired even 06h register is not read or key is still pressed.

6Ah Interrupt Repeat Time Register (RW)

Bit	D7:D4	D3:D0
Name	-	INTRT[3:0]
Default	0000	0000

INTRT	**Interrupt Repeat Time**
0000	disable
0001	50ms
0010	100ms
0011	150ms
0100	200ms
0101	250ms
0110	300ms
0111	350ms
1000	400ms
1001	450ms
1010	500ms
1011	600ms
1100	700ms
1101	800ms
1110	900ms
1111	1s

After INTRT is set, second interrupt will be generated after the interrupt repeat time is expired If there is a key keeping pressed.

6Bh Key Pin Select Register (RW)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

KS	**Key Pin Selection Setting**
0	Disable
1	Enable

6Ch Shield Pin Select Register (RW)

Bit	D7:D0
Name	SHDE[7:0]
Default	0000 1000

SHDE	Shield Enable (only for bit0 and bit3)
0	Disable shield driver
1	Enable shield driver

6Dh INT Pin Select Register 1 (RW)

Bit	D7:D0
Name	IPS1[7:0]
Default	0000 0000

6Eh INT Pin Select Register 2 (RW)

Bit	D0
Name	IPS2[0]
Default	0

IPS1/2 INT Pin Select 1/2

IPS1[7:0] maps to KEY[7:0]. Write 1 will enable the related Key as an INT pin.

IPS2[0] maps to Pin 13. Write 1 will enable Pin13 as an INT pin.

6Fh Buzzer Pin Select Register 1 (RW)

Bit	D7:D0
Name	BPS1[7:0]
Default	0000 0100

70h Buzzer Pin Select Register 2 (RW)

Bit	D0
Name	BPS2[0]
Default	0

BPS1/2 Buzzer output Select 1/2

BPS1[7:0] maps to KEY[7:0]. Write 1 will enable the related Key as a Buzzer output pin.

BPS2[0] maps to Pin 13. Write 1 will enable Pin 13 as a Buzzer output pin.

71h Buzzer Power Pin Select Register 1 (RW)

Bit	D7:D0
Name	EBP1[7:0]
Default	0000 0000

72h Buzzer Power Pin Select Register 2 (RW)

Bit	D0
Name	EBP2[0]
Default	1

EBP1/2 Buzzer Power Select 1/2

EBP1[7:0] maps to KEY[7:0]. Write 1 will enable the related Key as a Buzzer Power pin.

EBP2[0] maps to Pin 13. Write 1 will enable Pin 13 as a Buzzer Power pin.

73h TKIII Control Register 1 (RW)

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	RPT	INI	ASTDLY	
Default	00	01	00	11

RPT Repeat Sequence Count

00 No repeat
01 Repeat 4 times
10 Repeat 8 times
11 Repeat 16 times

INI Initial Setting Delay

INI[1-0] defines the number of TKCLK period for initial settling of pin Cref. The delay is (INI[1-0] + 1) *4*TKCLK.

ASTDLY Auto Mode Start Delay

ASTDLY[1-0] inserts an inter-sequence idle time of (ASTDLY[1-0] +1) * 256 TKCLK at each sequence start. This delay allows the stabilization time from normal mode to sleep mode.

LFNF Low Frequency Noise Filter Setting

00 disable LFNE

If the scan count with noise injection detect is larger than (LFNF[1-0] * 8), the scan result is ignored.

74h TKIII Control Register 2 (RW)

Bit	D3	D2:D1	D0
Name	-	-	-
Default	0	00	0

Bit	D7	D6	D5	D4
Name	-	-	PRS	-
Default	0	0	1	0

PRS Pseudo Random Sequence

0 Disable PRS
1 Enable PRS

75h TKIII Control Register 3 (RW)

Bit	D7:D4	D3	D2:D0
Name	-	MFEN	CCNT[2:0]
Default	0000	0	011

MFEN Multi Frequency Scan

0 Disable MF
1 Enable MF

CCNT Cycle Count of Each Conversion Sequence

000 1024
001 2048
010 4096
011 8192
100 12288
101 16384
110 32768
111 65536

76h TKIII CCHG Register (RW)

Bit	D7:D5	D4:D0
Name	CCHG[2:0]	-
Default	011	00000

CCHG Internal Reference Capacitance Select

000 10pF
001 20pF
010 30pF
011 40pF
100 50pF
101 60pF

110	70pF
111	80pF

77h TKIII PUD Register (RW)

Bit	D3:D0		
Name	PUD[3:0]		
Default	0000		
Bit	D7	D6	D5:D4
Name	PUDIEN	PUDREN	-
Default	0	0	00

TK3PUD is to configure a constant DC pull-up/pull-down on pin Cref to allow high capacitance touch-key detection. A DC pull-up/pull-down can compensate the equivalent resistance which is caused by a high capacitance key. Connecting a constant current source or resistor can thus maintain touch key detection sensitivity. In general, we will try to maintain the raw count around half of CCNT for the case without key touched.

For DC current, PUD[3:0] enables 8uA/4uA/2uA/1uA current source. For Resistor, PUD[3-0] enables 5K/10K/20K/40K resistor.

PUDIEN Pull-up/Pull-down DC Current Enable

PUDREN Pull-up/Pull-down DC Resistor Enable

PUD	**Pull up DC Current**
1000	Enable 8uA current source.
0100	Enable 4uA current source.
0010	Enable 2uA current source.
0001	Enable 1uA current source.

PUD	**Pull up Resistor**
1000	Enable 5K resistor source.
0100	Enable 10K resistor source.
0010	Enable 20K resistor source.
0001	Enable 40K resistor source.

78h System Clock Select Register (RW)

Bit	D7:D4	D3	D2:D0
Name	-	CLKS	OSCD[2:0]
Default	0000	0	000

CLKS	**Clock Stretching (For I2C)**
0	Disable stretching
1	Enable stretching

OSCD	**Oscillator Division**
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

79h Spread Spectrum Register (RW)

Bit	D7:D2		
Name	SSR[3:0]	SSA[1:0]	-
Default	0000	11	-

SS Spread Spectrum Setting

With spread spectrum technique, electromagnetic energy produced over a particular bandwidth is spread in the frequency domain, and that can reduce EMI. Two parameters are listed as follows:

SSR[3:0] Defines the spread spectrum sweep rate. If the SSR[3:0] =0, then spread spectrum is disabled.

SSA[1:0] Defines how to adjust the spread spectrum frequency bandwidth. The frequency is adjusted by adding SSA [1:0] range to the actual internal OSC control register.

SSA[1:0]=11 +/- 32
SSA[1:0]=10 +/- 16
SSA[1:0]=01 +/- 8
SSA[1:0]=00 +/- 4

7Ah Auto Sleep Mode Register (RW)

Bit	D3:D0		
Name	AST[3:0]-		
Default	1111		
Bit	D7	D6	D5:D4
Name	ASEN	-	BLMA[1:0]
Default	0	0	00

ASEN	**Auto-SLEEP Enable**
0	Disable

1 Enable

BLMA Baseline moving average

Hardware baseline can be generated by slow moving average setting.

00 32 average
01 64 average
10 128 average
11 256 average

AST Auto Sleep Time

0000 0.5s
0001 1s
0010 1.5s
0011 2s
0100 2.5s
0101 3s
0110 3.5s
0111 4s
1000 4.5s
1001 5s
1010 6s
1011 7s
1100 8s
1101 9s
1110 10s

7Bh Sleep Mode Control Register (RW)

Bit	D3:D2		D1:D0	
Name	T2[1:0]		T1[1:0]	
Default	00		00	
Bit	D7	D6	D5	D4
Name	-	PW	-	SC
Default	0	0	0	0

PW Proximity Wakeup

Disable: wake up>>scan key once>>go to sleep again

Enable: wake up>> generates INT signal (optional) >>go to sleep after Auto Sleep Time is expired if no key is detected

0 Disable
1 Enable

SC Sleep Calibration

0 Disable
1 Enable

T2 Wake Up Period with Key Disable

Device will be woken up according to the T2 setting by polling the status of Key.

00 50ms
01 100ms
10 200ms
11 300ms

T1 Wake Up Period with Key Enable

Device will be woken up according to the T1 setting to maintain the baseline to prevent the change of environment from stopping Key waking up device.

00 2s
01 4s
10 8s
11 16s

7Ch Wake Up Key Select Register (RW)

Bit	D7:D0
Name	WK[7:0]
Default	0000 0000

WK Wakeup Key Select Setting

0 Disable
1 Enable

7Dh Wake Up Threshold Register (RW)

Bit	D7:D0
Name	WTH[7:0]
Default	0000 1000

Wake up threshold range from 0 to 255

7Eh TKIII Sleep Mode CCHG Register (RW)

Bit	D7:D5	D4:D0
Name	CCHG[2:0]	-
Default	011	00000

CCHG Internal Reference Capacitance Select

000 10pF
001 20pF

010	30pF
011	40pF
100	50pF
101	60pF
110	70pF
111	80pF

7Fh TKIII Sleep Mode PUD Register (RW)

Bit	D3:D0		
Name	PUD[3:0]		
Default	0000		
Bit	D7	D6	D5:D4
Name	PUDIEN	PUDREN	-
Default	0	0	00

TK3 PUD is to configure a constant DC pull-up/pull-down on pin Cref to allow high capacitance touch-key detection. A DC pull-up/pull-down can compensate the equivalent resistance caused by a high capacitance key. Connecting a switching current source or resistor can thus maintain touch key detection sensitivity.

For DC current, PUD[3:0] can enable 8uA/4uA/2uA/1uA current source. For Resistor, PUD[3-0] can enable 5K/10K/20K/40K resistor.

PUDIEN Pull-up/Pull-down DC Current Enable
PUDREN Pull-up/Pull-down DC Resistor Enable

PUD	**Pull up DC Current**
1000	Enable 8uA current source.
0100	Enable 4uA current source.
0010	Enable 2uA current source.
0001	Enable 1uA current source.

PUD	**Pull up Resistor**
1000	Enable 5K resistor source.
0100	Enable 10K resistor source.
0010	Enable 20K resistor source.
0001	Enable 40K resistor source.

80h Sleep Mode Raw Count Register 1 (RO)

Bit	D7:D0
Name	SLRC[15:8]
Default	0000 0000

81h Sleep Mode Raw Count Register 2 (RO)

Bit	D7:D0
Name	SLRC[7:0]
Default	0000 0000

SLRC Sleep Mode Raw Count
Read only. Value for reference

82h Sleep Mode Baseline Register 1 (RO)

Bit	D7:D0
Name	SLB[15:8]
Default	0000 0000

83h Sleep Mode Baseline Register 2 (RO)

Bit	D7:D0
Name	SLB[7:0]
Default	0000 0000

SLB Sleep Mode Baseline
Read only. Value for reference

84h Key Scan Once Register (RW)

Bit	D7:D2	D1	D0
Name	-	TR	EN
Default	000000	0	0

TR

Write	1	Trigger one scan
Read	1	Busy
Read	0	Data ready

EN	**Enable Key Scan Once**
0	Continuous scan of all enabled keys
1	Scan all enabled keys once

85h Table Ready Mark Register (RO)

Bit	D7:D0
Name	MARK[7:0]
Default	0000 0000

MARK
It is used for firmware control touch key table.
Ready/Fail status

00	ready
Others	not ready

BUZZER / MELODY APPLICATION

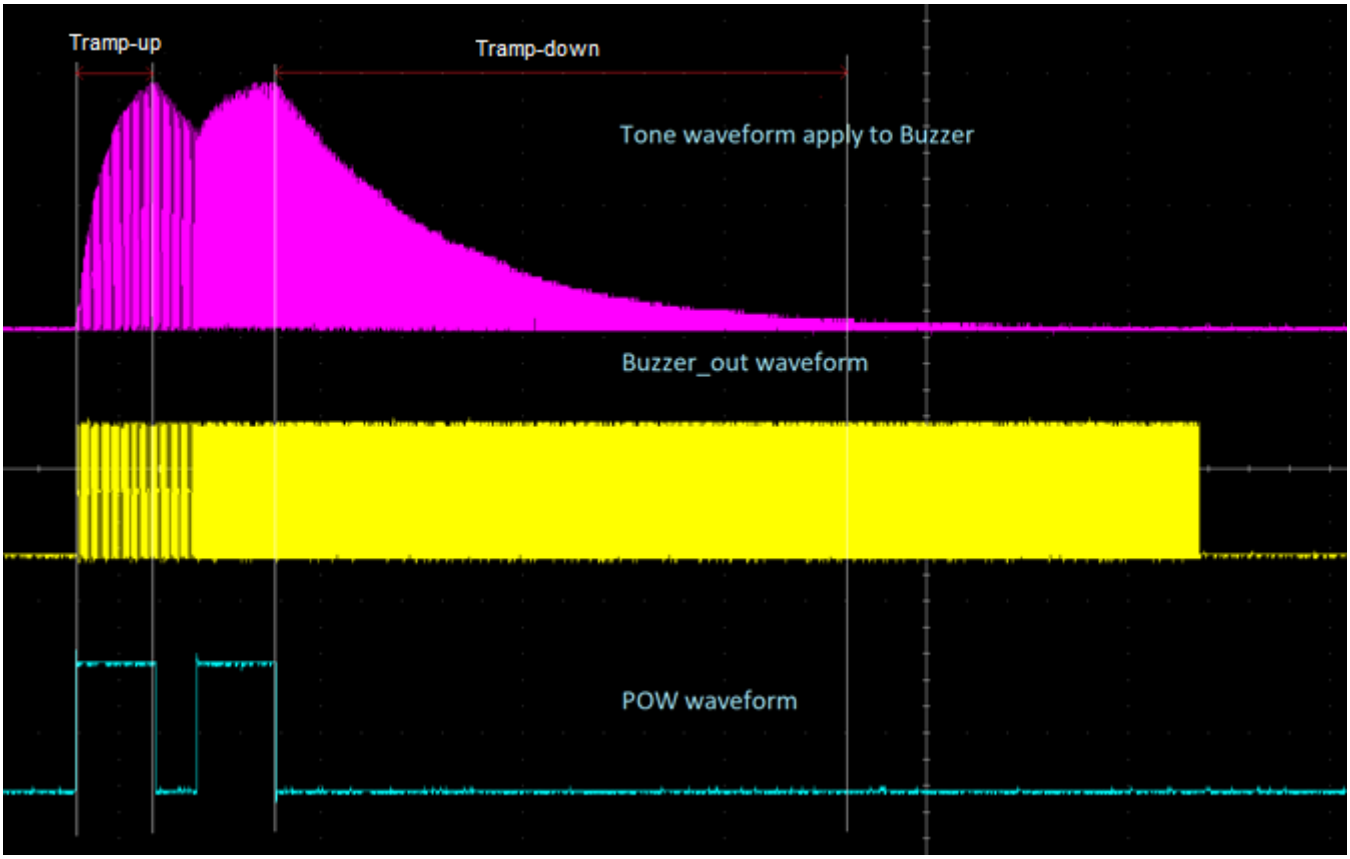


Figure 10: Buzzer/Melody Waveform

Note:

$T_{ramp-up}$: 100R as below figure 11 decides the signal ramp up rate.

$T_{ramp-down}$: The signal ramps down because POW is low and 47uF capacitor as below figure 11 decides the ramp down rate.

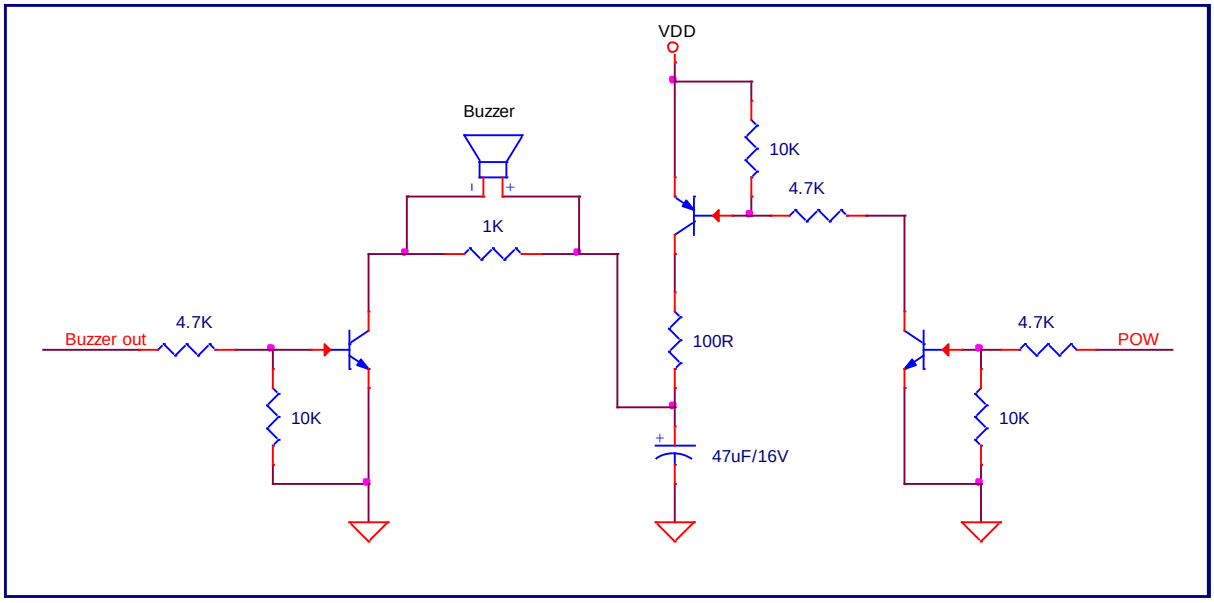
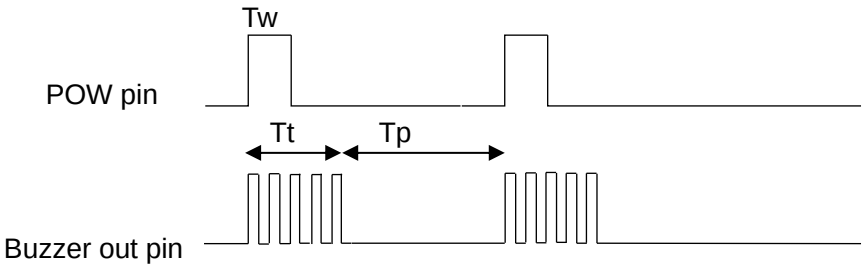


Figure 11: Typical Application Circuit for Melody

07h Buzzer Register (W)

Bit	D7:D0
Name	BW
Default	-

1st byte	2nd byte	3rd byte	4th byte
Scale ID	Tt	Tw	Tp



Tt, Tw and Tp range from 0 to 255 @ 4ms step

A Tone played duration is defined as Tt + Tp.

The support scale is from 3A to 8G#.

Frequencies for equal-tempered scale, A**4** = 440 Hz
"Middle C" is C4

	3	freq	divisor	freq error	4	freq	divisor	freq error	5	freq	divisor	freq error
C					3	261.6	1911	0.01%	15	523.3	956	-0.05%
C#					4	277.2	1804	-0.01%	16	554.4	902	-0.01%
D					5	293.7	1703	-0.02%	17	587.3	851	0.04%
D#					6	311.1	1607	0.00%	18	622.3	804	-0.06%
E					7	329.6	1517	-0.01%	19	659.3	758	0.06%
F					8	349.2	1432	-0.02%	20	698.5	716	-0.02%
F#					9	370.0	1351	0.03%	21	740.0	676	-0.05%
G					10	392.0	1276	-0.04%	22	784.0	638	-0.04%
G#					11	415.3	1204	-0.01%	23	830.6	602	-0.01%
A	0	220.0	2273	-0.01%	12	440.0	1136	0.03%	24	880.0	568	0.03%
A#	1	233.1	2145	0.01%	13	466.2	1073	-0.04%	25	932.3	536	0.05%
B	2	246.9	2025	-0.01%	14	493.9	1012	0.04%	26	987.8	506	0.04%

	6	freq	divisor	freq error	7	freq	divisor	freq error	8	freq	divisor	freq error
C	27	1046.5	478	-0.05%	39	2093.0	239	-0.05%	51	4186.0	119	0.37%
C#	28	1108.7	451	-0.01%	40	2217.5	225	0.21%	52	4434.9	113	-0.23%

D	29	1174.7	426	-0.08%	41	2349.3	213	-0.08%	53	4698.6	106	0.39%
D#	30	1244.5	402	-0.06%	42	2489.0	201	-0.06%	54	4978.0	100	0.44%
E	31	1318.5	379	0.06%	43	2637.0	190	-0.21%	55	5274.0	95	-0.21%
F	32	1396.9	358	-0.02%	44	2793.8	179	-0.02%	56	5587.7	89	0.54%
F#	33	1480.0	338	-0.05%	45	2960.0	169	-0.05%	57	5919.9	84	0.55%
G	34	1568.0	319	-0.04%	46	3136.0	159	0.28%	58	6271.9	80	-0.35%
G#	35	1661.2	301	-0.01%	47	3322.4	150	0.33%	59	6644.9	75	0.33%
A	36	1760.0	284	0.03%	48	3520.0	142	0.03%				
A#	37	1864.7	268	0.05%	49	3729.3	134	0.05%				
B	38	1975.5	253	0.04%	50	3951.1	127	-0.36%				

Scale ID(Sid): 0 is 3A, 1 is 3A#, 2 is 3B ….

07h Buzzer Register (W)

Bit	D7:D0
Name	BW
Default	0000 0000

Write melody data, stop melody play and clear the FIFO

07h Buzzer Register (R)

Bit	D7:D0
Name	BR
Default	0000 1010

BR Buzzer Register Read. It shows the available tone buffer size. SE5118 has 10 built-in note buffers.

I2C command format - Each node is composed of 4 byte data and the incomplete note will be ignored. The incoming note data will be ignored when the FIFO is full.

0x78, 0x07, (Sid, Tt, Tw, Tp), (Sid, Tt, Tw, Tp), ….
0x78, 0x07, 0xFF stops the melody play and clear the FIFO.

0x78, 0x07 Set the register number 0xF0.
0x79 Read FIFO's remaining length.

TYPICAL APPLICATION INFORMATION

GENERAL DESCRIPTION

The IS31SE5118 is an ultra-low power, fully integrated 8-channel solution for capacitive touch-buttons applications. The chip allows electrodes to project sense fields through any dielectric material such as glass or plastic.

SENSITIVITY ADJUSTING

Sensitivity can be adjusted by the external capacitor or internal register.

Higher capacitor value will yield out lower detect sensitivity. Lower capacitor value will yield out higher detect sensitivity.

INTERRUPT

Touch key detection event will trigger INT pin. The INT pin will be driven to low when the selected channel is pressed.

CLASSIFICATION REFLOW PROFILE

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time between 25°C to peak temperature	8 minutes max.

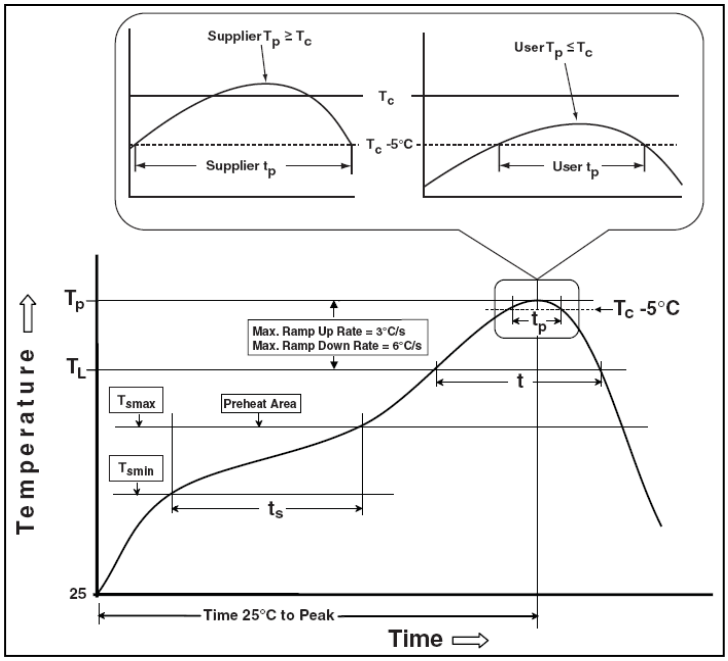
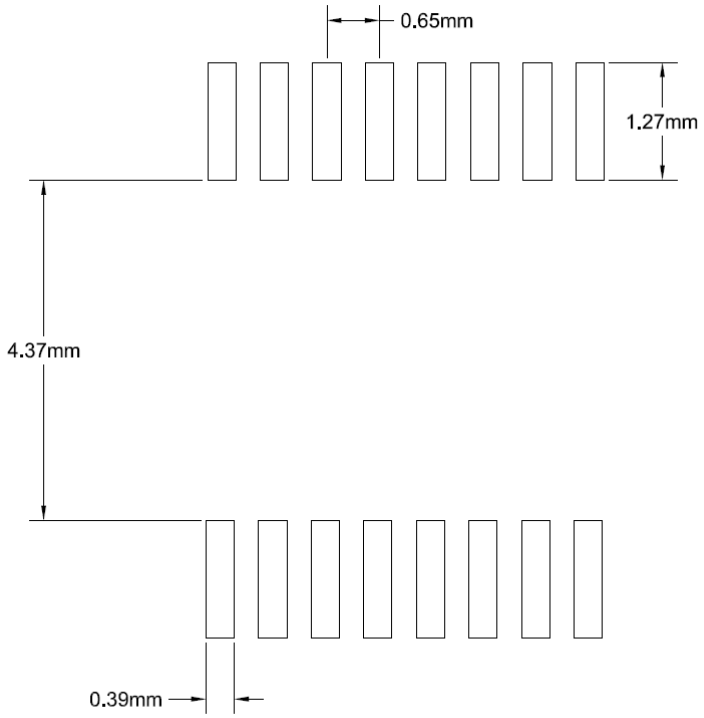


Figure 12: Classification Profile

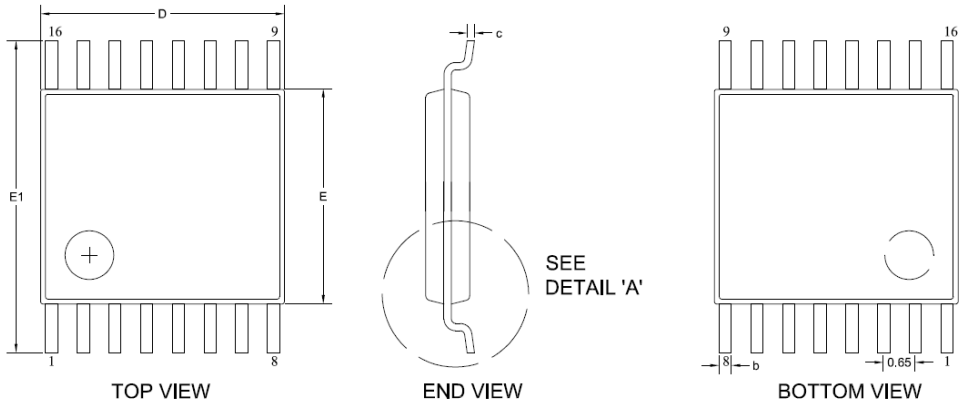
PACKAGE INFORMATION

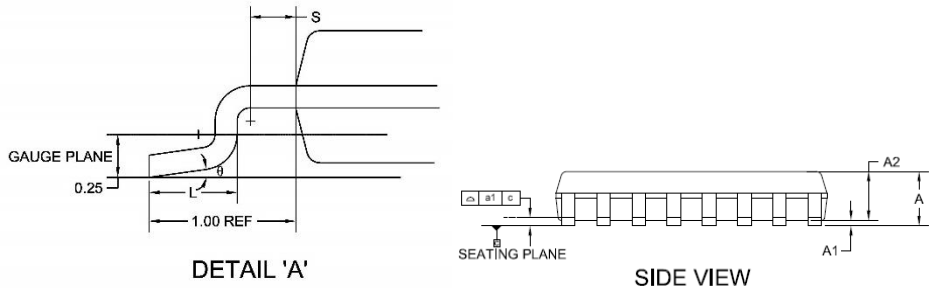
TSSOP-16

RECOMMENDED LAND PATTERN



POD





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1. 20
A1	0.05	—	0. 15
A2	0. 80	1.00	1. 05
D	4. 90	5.00	5. 10
E	4. 30	4. 40	4. 50
E1	6. 40BSC		
L	0. 45	0. 60	0. 75
b	0. 19	—	0. 30
S	0. 20		
c	0. 09	—	0. 20
θ	0°		8°
a1	0. 10		

NOTES:

1. CONTROLLING DIMENSION: MM
2. REFERENCE DOCUMENT: JEDEC MO-153

REVISION HISTORY

Revision	Detailed Information	Date
B	1. Update register default values 2. Add detailed descriptions for touch key sense registers and functions 3. Add ROHS compliant claim	2021.12.30
A	Formal Release	2021.06.08