



IQS7222A DATASHEET

12 Channel Mutual/ Self-capacitive, Inductive force and Hall sensing controller with I²C communications interface, configurable GPIOs and low power options

1 Device Overview

The IQS7222A ProxFusion® IC is a sensor fusion device for applications that require multiple sensing capabilities from a single sensor IC. The sensor is fully I²C compatible and on-chip calculations enable multiple application options. Various UIs from gestures to power mode switching allows the IC to respond effectively in the intended application with ultra-low power consumption.

1.1 Main Features

- > Highly flexible ProxFusion® device
- > 9 (QFN) / 8 (WLCSP) external sensor pad connections
- > Configure up to 12 Channels using the external connections or internal sensorⁱ
- > External sensor options:
 - Up to 8 self capacitive buttons
 - Up to 4 self capacitive wear detection pairs (with physical reference)
 - Up to 10 projected capacitive touch/proximity sensors
 - Up to 4 inductive sensor elements (metal detection/force sensing)
- > Internal sensor options:
 - Hall Switch
- > Built-in basic functions:
 - Automatic tuning
 - Noise filtering
 - Active environment tracking with reference sensor
 - Debounce & Hysteresis
 - Dual direction trigger indication
- > Built-in Signal processing options:
 - Slider output
 - Up to 4 elements per slider
 - Up to 2 sliders simultaneously
 - Slider gesture outputs
- > Design simplicity
 - PC Software for debugging and obtaining optimal settings and performance
 - One-time programmable settings for custom power-on IC configuration
 - Auto-run from programmed settings for simplified integration
- > Automated system power modes for optimal response vs consumption
- > I²C communication interface with IRQ/RDY (up to fast plus -1MHz)
- > Event and streaming modes
- > Customizable user interface due to programmable memory
- > Supply Voltage 1.8V(-5%) to 3.5V
- > Package options
 - WLCSP18 (1.62 x 1.62 x 0.5 mm) - interleaved 0.4mm x 0.6mm ball pitch
 - QFN20 (3 x 3 x 0.5 mm) - 0.4mm pitch



ⁱWLCSP18 package has 1 less external pad connection and the maximum amount of buttons that can be configured are less than QFN20 package



1.2 Applications

- > SAR Compliance in Mobile devices
- > Low power Wake-up Buttons / Proximity
- > Appliance user interface (Slider & Buttons)
- > TWS earphones (touch, slider, wear, force and dock detection)
- > Waterproof Buttons (Inductive)
- > Wear Detection
- > HALL-effect Dock Detection

1.3 Block Diagram

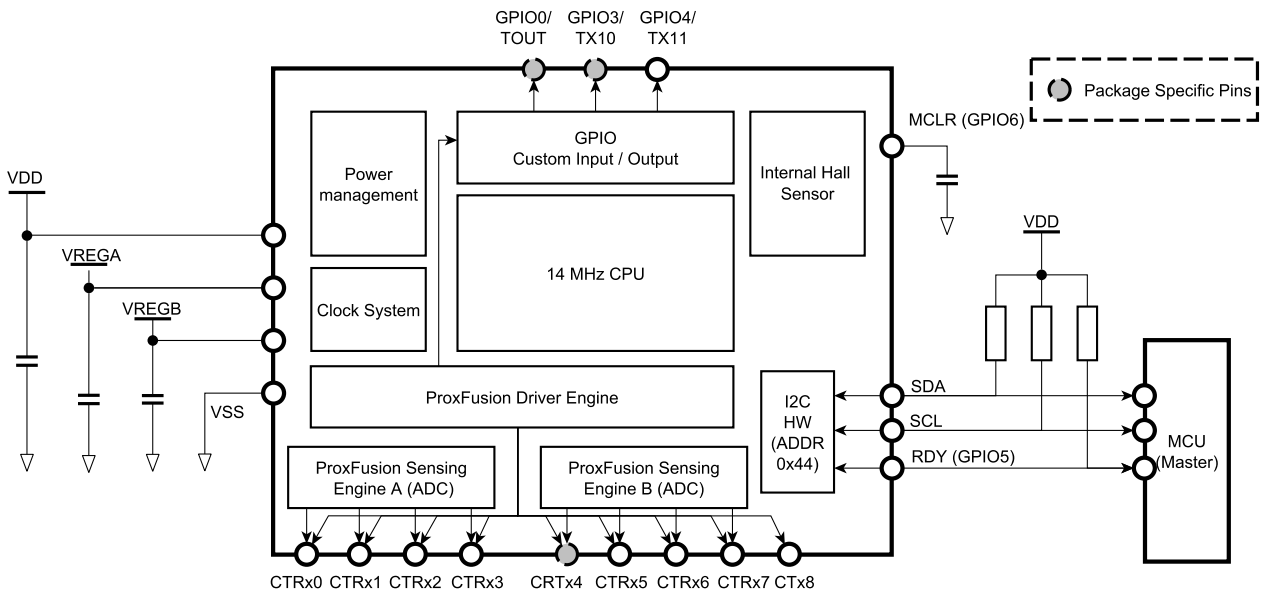


Figure 1.1: Functional Block Diagramⁱⁱ

ⁱⁱWLCSP18 packages do not have a CRX4 and combines GPIO0 and GPIO3



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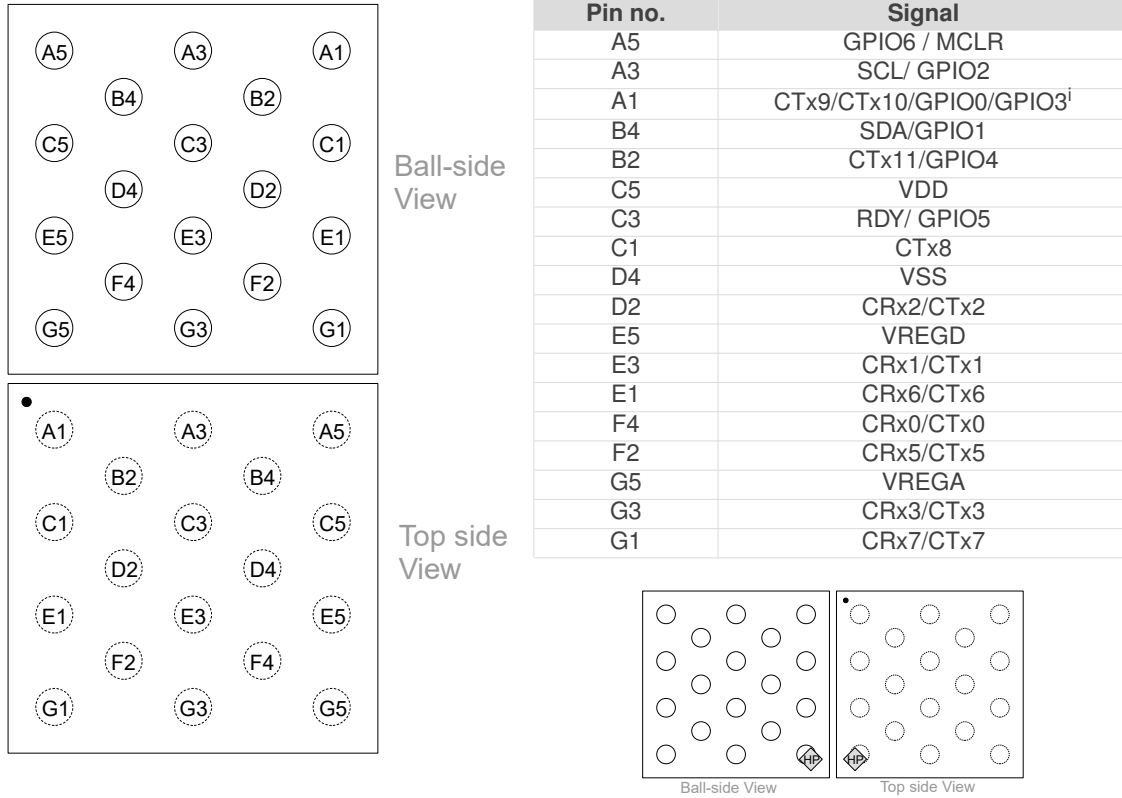
Memory Map Descriptions



2 Hardware Connection

2.1 WLCSP18 Pin Diagrams

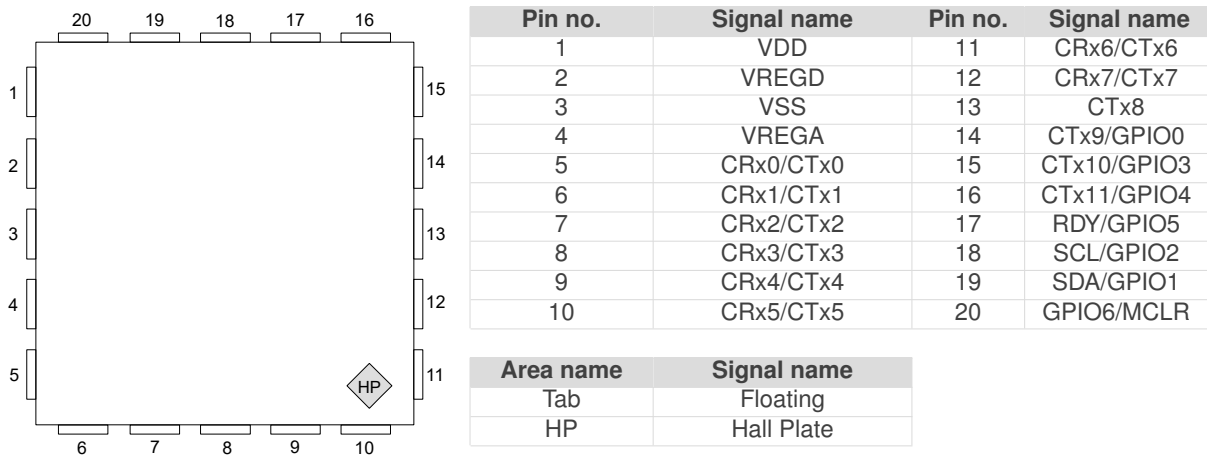
Table 2.1: 18-pin WLCSP18 Package (Bottom/Ball-side View)



Area Name	Signal Name
HP	Hall Plate

2.2 QFN20 Pin Diagram

Table 2.2: 20-pin QFN Package (Top View)



ⁱPlease note that CTx9 and CTx10 are connected together in the WLCSP18 package



2.3 Pin Attributes

Table 2.3: Pin Attributes

Pin no.		Signal name	Signal type ⁱⁱ	Buffer type	Power source
WLCSP18	QFN20				
C5	1	VDD	Power	Power	N/A
E5	2	VREGD	Power	Power	N/A
D4	3	VSS	Power	Power	N/A
G5	4	VREGA	Power	Power	N/A
F4	5	CRx0/CTx0	Analog		VREGA
E3	6	CRx1/CTx1	Analog		VREGA
D2	7	CRx2/CTx2	Analog		VREGA
G3	8	CRx3/CTx3	Analog		VREGA
-	9	CRx4/CTx4	Analog		VREGA
F2	10	CRx5/CTx5	Analog		VREGA
E1	11	CRx6/CTx6	Analog		VREGA
G1	12	CRx7/CTx7	Analog		VREGA
C1	13	CTx8	Analog		VREGA
A1	14	GPIO0/CTx9	Digital/Prox		VDD/VREGA
B4	19	SDA/GPIO1	Digital		VDD
A3	18	SCL/GPIO2	Digital		VDD
A1	15	GPIO3/CTx10	Digital/Prox		VDD/VREGA
B2	16	GPIO4/CTx11	Digital/Prox		VDD/VREGA
C3	17	RDY/GPIO5	Digital/Prox		VDD
A5	20	MCLR/GPIO6	Digital		VDD

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal name	Pin no.		Pin type	Description	
		WLCSP18	QFN20			
ProxFusion®	CRx0/CTx0	F4	5	IO	ProxFusion® channel	
	CRx1/CTx1	E3	6	IO		
	CRx2/CTx2	D2	7	IO		
	CRx3/CTx3	G3	8	IO		
	CRx4/CTx4	-	9	IO		
	CRx5/CTx5	F2	10	IO		
	CRx6/CTx6	E1	11	IO		
	CRx7/CTx7	G1	12	IO		
	CTx8	C1	13	IO		
	CTx9/ GPIO0	A1	14	IO		CTx9 pad
	CTx10/GPIO3	A1	15	IO		CTx10 pad
	CTx11/GPIO4	B2	16	IO		CTx11 pad
GPIO	MCLR/ GPIO6	A5	20	IO	Input filter disabled for external clock input. Active pulldown, 200k resistor to VDD, Pulled low during POR, and MCLR function enabled by default. VPP input for OTP	
I ² C	SDA/GPIO1	B4	19	IO	I ² C Data	
	SCL/GPIO2	A3	18	IO	I ² C clock	
Power	VDD	C5	1	P	Power supply input voltage	
	VREGD	E5	2	P	Internal regulated supply output for digital domain	
	VSS	D4	3	P	Analog/Digital Ground	
	VREGA	G5	4	P	Internal regulated supply output for analog domain	

ⁱⁱSignal Types: I = Input, O = Output, I/O = Input or Output



2.5 Reference Schematic

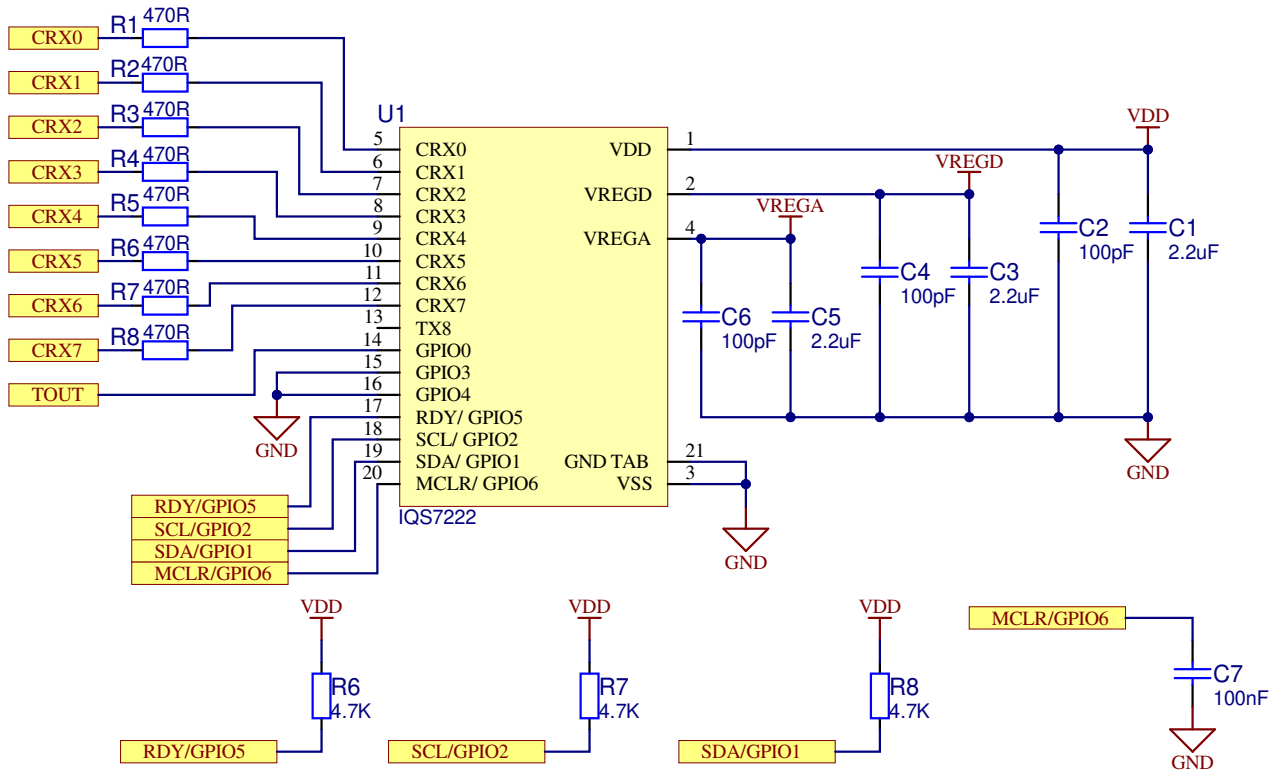


Figure 2.1: 8 Button Self Capacitance Reference Schematic

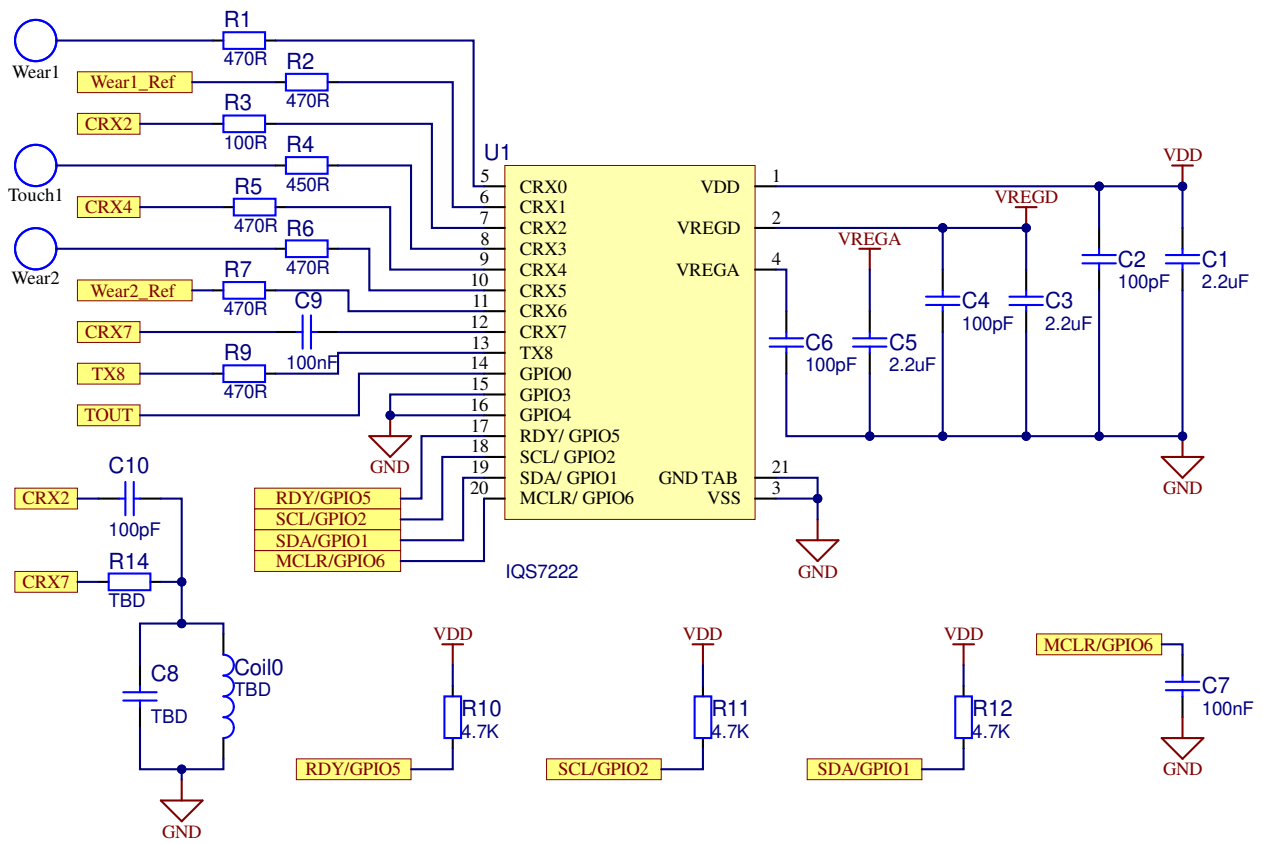


Figure 2.2: Wear, Reference and Inductive Sensing Reference Schematic

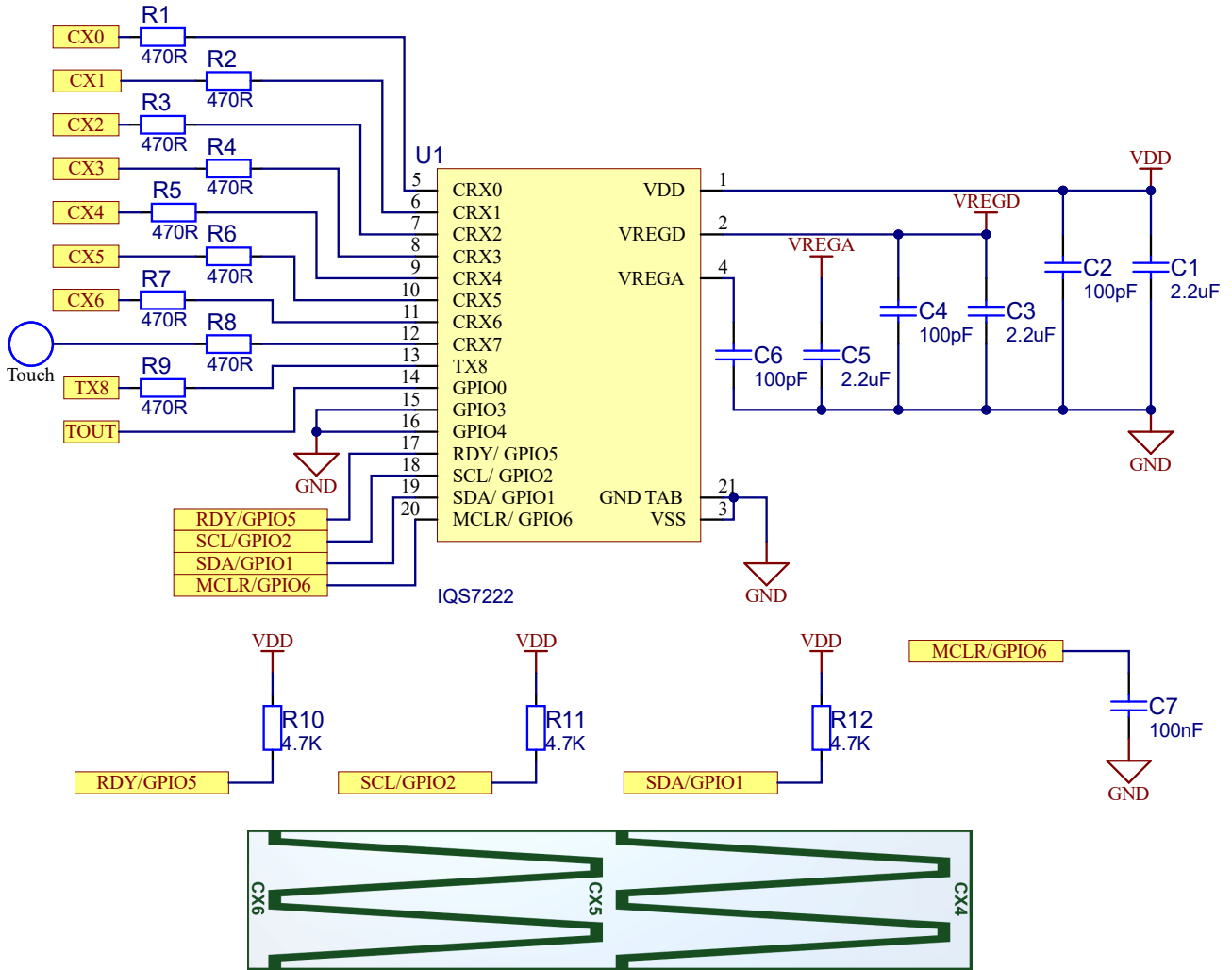


Figure 2.3: 3 Channel Slider with Touch Sensor Reference Schematic



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.5	V
Voltage applied to any ProxFusion® pin	-0.3	VREG	V
Voltage applied to any other pin (referenced to VSS)	-0.3	VDD + 0.3 (3.5V max)	V
Storage temperature, T _{stg}	-40	85	°C

3.2 ESD Rating

Table 3.2: ESD Rating

	Value	Unit
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁱ	± 4000 V

3.3 Recommended Operating Conditions

Table 3.3: Recommended Operating Conditions

Recommended operating conditions		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: F _{OSC} = 14MHz F _{OSC} = 18MHz	1.71 2.2		3.5 3.5	V
VREGA	Internal regulated supply output for analog domain: F _{OSC} = 14MHz F _{OSC} = 18MHz		1.53 1.75		V
VREGD	Internal regulated supply output for digital domain: F _{OSC} = 14MHz F _{OSC} = 18MHz		1.59 1.8		V
VSS	Supply voltage applied at VSS pin		0		V
T _A	Operating free-air temperature	-40	25	85	°C
C _{VDD}	Recommended capacitor at VDD	1	2	10	μF
C _{VREGA}	Recommended external buffer capacitor at VREG, ESR ≤ 200mΩ	1	2	10	μF
C _{VREGD}	Recommended external buffer capacitor at VREG, ESR ≤ 200mΩ	1	2	10	μF
C _{X_SELF-VSS}	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (self-capacitance mode)	1	-	400 ⁱⁱ	pF
C _{m_CTX-CRX}	Capacitance between Receiving and Transmitting electrodes on all ProxFusion® blocks (mutual-cap mode)	0.2	-	9 ⁱⁱ	pF
C _{p_CRX-VSS-1M}	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (mutual-capacitance mode @ f _{xfer} =1MHz)			100 ⁱⁱ	pF
C _{p_CRX-VSS-4M}	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (mutual-capacitance mode @ f _{xfer} =4MHz sensing)			25 ⁱⁱ	pF
$\frac{C_{p_{CRX-VSS}}}{C_{m_{CTX-CRX}}}$	Capacitance ratio for optimal SNR in mutual capacitance mode ⁱⁱⁱ	10		20	n/a
RC _{X_CRX/CTX}	Series (in-line) resistance of all mutual capacitance pins (Tx & Rx pins) in mutual capacitance mode	0 ^{iv}	0.47	10 ^v	kΩ
RC _{X_SELF}	Series (in-line) resistance of all self capacitance pins in self capacitance mode	0 ^{iv}	0.47	10 ^v	kΩ



3.4 Hall Effect Sensing Characteristics

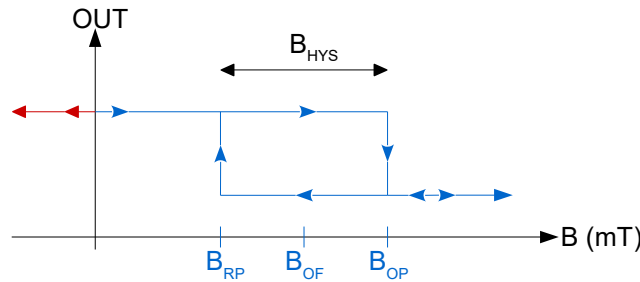


Figure 3.1: Magnet Trigger Level Description (Active Low Output)

Table 3.4: Example Power-on Magnet Detection Options

Hall Sensor Setup	Output Type	B _{RP} (mT)	B _{OP} (mT)	B _{HYS} (mT)	B _{RP} and B _{OP} Accuracy (mT) -10 °C to 80 °C
Threshold example 1	Direct	2.1	3	0.9	27%
Adjustable Threshold	I ² C/Direct	0 - 100% of B _{OP} (default 95%)	Software register	0 - 100% of B _{OP} (default 5%)	TBD

3.5 Current Consumption

Power mode	Active channels	Report rate (Sampling rate) [ms]	Current [μA]	
			3.3V	1.8V
NP	Defaults (10 channels self-capacitance & Hall)	16	732	729
	TWS: Wear, slider, inductive resonant without bias, Hall	16	750	749
LP	Defaults (10 channels self-capacitance & Hall)	60	126	126
	TWS: Wear, slider, inductive resonant without bias, Hall	60	122	121
ULP	Distributed (2 self-capacitance auto-prox channels), default setup	150	5.7	5.6
	Distributed (2 self-capacitance auto-prox channels), TWS setup	150	5.6	5.4
	Distributed (2 self-capacitance auto-prox channels), default setup	200	4.5	4.3
	Distributed (2 self-capacitance auto-prox channels), TWS setup	200	4.4	4.12

ⁱJEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

ⁱⁱRC_x = 0 Ω

ⁱⁱⁱPlease note that the the maximum values for C_p and C_m are subject to this ratio

^{iv}Nominal series resistance of 470Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection

^vSeries resistance limit is a function of f_{xfer} and the circuit time constant, RC. R_{max} × C_{max} = $\frac{1}{(6 \times f_{xfer})}$ where "C" is the pin capacitance to V_{ss}.

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Typ	Max	Unit
V_{VDD}	Power-up/down level (Reset trigger) - slope >100V/s	1.040	1.353	1.568	V
V_{VREG}	Power-up/down level (Reset trigger) - slope >100V/s	0.945	1.122	1.304	V

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)VDD_HI}$	MCLR Input high level voltage	VDD = 3.3V	VSS-0.3	-	1.05	V
$V_{IL(MCLR)VDD_LOW}$	MCLR Input low level voltage	VDD = 1.7V	VSS-0.3	-	0.75	V
$V_{IH(MCLR)VDD_HI}$	MCLR Input high level voltage	VDD = 3.3V	2.25	-	VDD_HI+0.3	V
$V_{IH(MCLR)VDD_LOW}$	MCLR Input high level voltage	VDD = 1.7V	1.05	-	VDD_LOW+0.3	V
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width - no trigger	VDD = 3.3V	-	-	15	ns
$t_{PULSE(MCLR)}$	MCLR input pulse width - no trigger	VDD = 1.7V	-	-	10	ns
$t_{TRIG(MCLR)}$	MCLR input pulse width - ensure trigger	VDD = 3.3V, VDD = 1.7V	250	-	-	ns

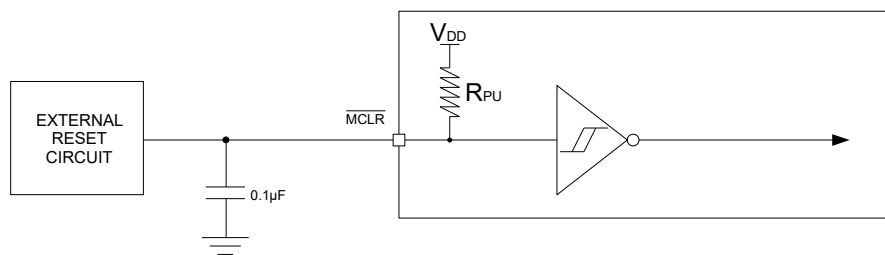


Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
f_{xfer}	Charge transfer frequency (derived from f_{SYS})	42	500-1500	5000	kHz
f_{OSC}	Master CLK frequency tolerance 14MHz	13.23	14	14.77	MHz
f_{OSC}	Master CLK frequency tolerance 18MHz	17.1	18	19.54	MHz



4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
V _{OL}	GPIO1 & GPIO2 Output low voltage	I _{sink} = 20mA		0.3	V
V _{OL}	GPIO0,3,4,5 Output low voltage	I _{sink} = 10mA		0.15	V
V _{OH}	Output high voltage	I _{source} = 20mA	VDD - 0.2		V
V _{IL}	Input low voltage		VDD * 0.3		V
V _{IH}	Input high voltage			VDD * 0.7	V
C _{b_max}	GPIO1 & GPIO2 maximum bus capacitance			550	pF

4.5 I²C Characteristics

Table 4.5: I²C Characteristics

Parameter	Test Conditions	VDD	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	1.8V, 3.3V			1000	kHz
t _{HD,STA}	Hold time (repeated) START	1.8V, 3.3V	0.26			μs
t _{SU,STA}	Setup time for a repeated START	1.8V, 3.3V	0.26			μs
t _{HD,DAT}	Data hold time	1.8V, 3.3V	0			ns
t _{SU,DAT}	Data setup time	1.8V, 3.3V	50			ns
t _{SU,STO}	Setup time for STOP	1.8V, 3.3V	0.26			μs
t _{SP}	Pulse duration of spikes suppressed by input filter	1.8V, 3.3V	50			ns

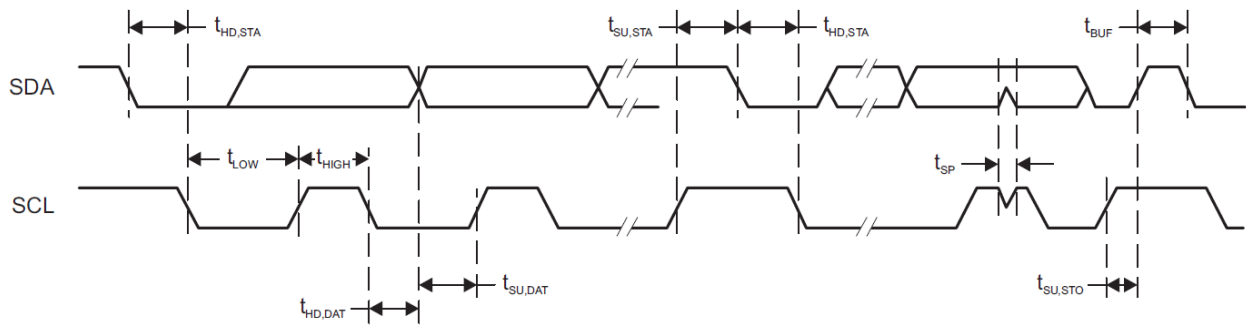


Figure 4.2: I²C Mode Timing Diagram



5 ProxFusion® Module

The IQS7222A contains dual ProxFusion® modules that uses patented technology to measure and process the sensor data. Two modules ensure a rapid response from multi-channel implementations. The multiple touch, proximity and weighted average (slider) outputs are the primary output from the sensor.

5.1 Channel Options

Self-capacitance, Mutual capacitance, Reference tracking, Inductive designs and Hall effect sensing are possible with the IQS7222A.

- > Sensor pad design overview: AZD008
- > Mutual capacitance (also known as Projected capacitance) button layout guide: AZD036
- > Inductive design layout guide: AZD115
- > Hall effect Switch UI Sensing: Section 5.1.1

5.1.1 Hall Effect Switch UI

Hall effect sensing is an internal sensing option that requires no external sensor design.

The Hall effect switch UI measures the magnetic field induced on the hall plate of the IC and is, by default, activated when both Hall-effect channels (channel 10 and channel 11) are active. The UI uses two channels to determine the magnetic field induced on the Hall plate. Using two channels ensures that the ATI (refer to section 5.5) can still be used in the presence of the magnet. An inverted channel allows the capability of calculating a reference value which will always be the same regardless of the presence of a magnet. Enabling the UI will enable the IC to display the effects of the magnet by reading the data in the Hall UI flags and output registers.

The Hall effect switch UI is used for detection of the presence of a single magnet.

There are two channel outputs and each channel controls different parameters of the Hall effect. Please note that parameters not listed under the relevant channel's setting, below, must be left as default.

Channel 10 output is the signal output, calculated using:

$$\text{Channel 10}_{\text{output}} = \frac{\text{Counts} - \text{Counts}_{\text{inv}}}{2}$$

Settings from Channel 10 used for Hall effect switch UI:

- > Touch Threshold
- > Prox Threshold
- > Touch Hysteresis
- > Enter debounce
- > Exit debounce

Channel 11 output is the LTA and signal without the output on Channel10, calculated using:

$$\text{Channel 11}_{\text{output}} = \frac{\text{Counts} + \text{Counts}_{\text{inv}}}{2}$$

Channel 11 allows ATI to be performed without changing the count value on Channel 10.



Settings from Channel 11 used for Hall effect switch UI:

- > ATI Mode
- > ATI Band
- > ATI Compensation
- > ATI Compensation Divider
- > ATI Coarse Fractional Divider
- > ATI Coarse Fractional Multiplier
- > ATI Fine Fractional Divider

Settings that should be the same on channel 10 and channel 11 are:

- > Frequency fraction
- > Frequency period
- > Ground inactive Rx's
- > Vref 0v5 Enable
- > Cs cap size
- > ATI Base
- > ATI Target

5.2 Low Power Options

The IQS7222A offers 3 power modes:

- > Normal power mode (NP)
 - Flexible key scan rate
- > Lower power mode (LP)
 - Flexible key scan rate
 - Typically set to a slower rate than NP
- > Ultra-low power mode (ULP)
 - Optimized firmware setup
 - Intended for rapid wake-up on a single channel (e.g. distributed proximity event), enabling immediate button response for an approaching user
 - Other sensor channels are typically sampled at a slower rate in order to optimize power consumption

5.3 Count Value

The sensing measurement returns a *count value* for each channel. Count values are inversely proportional to capacitance/inductance, and all outputs are derived from this.

5.3.1 Max Count

Each channel is limited to having a count value smaller than the configurable limit (*Maximum counts*). If the ATI setting or hardware causes measured count values higher than this, the conversion will be stopped, and the max value will be read for that relevant count value.

5.4 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value. The reference value/LTA of a sensor is slowly updated to track changes in the environment and is not updated during user interaction.



5.4.1 Reseed

Since the *Reference* for a channel is critical for the device to operate correctly, there could be known events or situations which would call for a manual reseed. A reseed takes the latest measured counts, and seeds the *reference/LTA* with this value, therefore updating the value to the latest environment. A reseed command can be given by setting the corresponding bit (Register 0xD0, bit3).

5.5 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in the new ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode capacitances and inductance, without modification to external components. The ATI settings allow tuning of various parameters. For a detailed description of ATI, please see contact Azoteq.

5.6 Automatic Re-ATI

5.6.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. This could cause the wrong ATI Compensation to be configured, since the user affects the capacitance of the sensor. A Re-ATI would correct this. It is recommended to always have this enabled. When a Re-ATI is performed on the IQS7222A, a status bit will set momentarily to indicate that this has occurred.

5.6.2 Conditions for Re-ATI to activate

A Re-ATI is performed when the reference of a channel drifts outside of the acceptable range around the ATI Target. The boundaries where Re-ATI occurs for the channels are adjustable in registers listed in Table A.16.

$$\text{Re-ATI Boundary}_{\text{default}} = \text{ATI target} \pm \left(\frac{1}{16} \text{ATI Target}\right)$$

For example, assume that the ATI target is configured to 800 and that the and the default boundary value is $1/16 * 800 = 50$. If Re-ATI is enabled, the ATI algorithm will be repeated under the following conditions:

$$\text{Reference} > 850 \text{ or } \text{Reference} < 750$$

The ATI algorithm executes in a short time, so goes unnoticed by the user.

5.6.3 ATI Error

After the ATI algorithm is performed, a check is done to see if there was any error with the algorithm. An ATI error is reported if one of the following is true for any channel after the ATI has completed:

- > ATI Compensation = 0 (min value)
- > ATI Compensation \geq 1023 (max value)
- > Count is already outside the Re-ATI range upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set (*ATI Error*). The flag status is only updated again when a new ATI algorithm is performed.



Re-ATI will not be repeated immediately if an ATI Error occurs. A configurable time (*ATI error timeout*) will pass where the Re-ATI is momentarily suppressed. This is to prevent the Re-ATI repeating indefinitely. An ATI error should however not occur under normal circumstances.



6 Sensing Modes

6.1 Mode Timeout

In order to optimize power consumption and performance, power modes are "stepped" by default in order to move to power efficient modes when no interaction has been detected for a certain (configurable) time known as the "mode timeout".

6.2 Count Filter

6.2.1 IIR Filter

The IIR filter applied to the digitized raw input offers various damping options as defined in Table A.23 and Table A.24

$$\text{Damping factor} = \text{Beta}/256$$



7 Hardware Settings

Settings specific to hardware and the ProxFusion® Module charge transfer characteristics can be changed.

Below, some are described, the other hardware parameters are not discussed as they should only be adjusted under guidance of Azoteq support engineers.

7.1 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) can be configured using the product GUI, and the relative parameters (Charge Transfer frequency) will be provided. For high resistance sensors, it might be needed to decrease f_{xfer} .

7.2 Reset

7.2.1 Reset Indication

After a reset, the Reset bit will be set by the system to indicate the reset event occurred. This bit will clear when the master sets the Ack Reset, if it becomes set again, the master will know a reset has occurred, and can react appropriately.

7.2.2 Software Reset

The IQS7222A can be reset by means of an I²C command (Soft Reset).



8 Additional Features

8.1 Setup Defaults

The supplied GUI can be utilised to configure the optimal settings. The design specific settings are exported and can be written to the device by the master after every power-on reset.

8.2 Automated Start-up

The device is programmed with the application firmware, bundled with settings specifically configured for the current hardware as described in Section 8.1. After power-up the device will automatically use the settings and perform the configuration/setup accordingly.

8.3 RF Immunity

The IQS7222A has immunity to high power RF noise. To improve the RF immunity, extra decoupling capacitors are suggested on V_{REG} and V_{DD} .

Place a 100pF in parallel with the 2.2 μ F ceramic on V_{REG} . Place a 2.2 μ F ceramic on V_{DD} . All decoupling capacitors should be placed as close as possible to the V_{DD} and V_{REG} pads.

If needed, series resistors can be added to Rx electrodes to reduce RF coupling into the sending pads. Normally these are in the range of 470 Ω -1k Ω . PCB ground planes also improve noise immunity.



9 I²C Interface

9.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of an RDY (ready interrupt) line. The communications interface of the IQS7222A supports the following:

- > *Fast-mode-plus* standard I²C up to 1MHz.
- > Streaming data as well as event mode.
- > The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS7222A implements 8-bit addressing with 2 bytes at each address with the exception of extended addresses, which implement 16-bit addressing with 2 bytes at each address. Two consecutive read/writes are required in this memory map structure. The two bytes at each address will be referred to as "byte 0" (least significant byte) and "byte 1" (most significant byte).

9.2 I²C Address

The default 7-bit device address is 0x44 ('01000100'). The full address byte will thus be 0x89 (read) or 0x88 (write).

Other address options exist on special request. Please contact Azoteq.

9.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

9.4 Memory Map Addressing

9.4.1 8-bit Address

Most of the memory map implements an 8-bit addressing scheme for the required user data. Extended memory map addresses implement 16-bit addressing scheme.

9.5 Data

The data is 16-bit words, meaning that each address obtains 2 bytes of data. For example, address 0x10 will provide two bytes, then the next two bytes read will be from address 0x11.

The 16-bit data is sent in little endian byte order (least significant byte first).

9.6 I²C Timeout

If the communication window is not serviced within the *I²C timeout* period (in milliseconds), the session is ended (RDY goes HIGH), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive, however the corresponding data was missed/lost, and this should be avoided. The I²C timeout period is set to 20ms.



9.7 Terminate Communication

A standard I²C STOP ends the current communication window.

If the stop bit disable (bit 0 register 0xDC) is cleared, the device will not respond to a standard I²C STOP. The communication window must be terminated using the end communications command (0xFF).

9.8 RDY/IRQ

The communication has an open-drain active-LOW RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and obtain the data accordingly. It is also useful to allow the master MCU to enter low-power/sleep allowing wake-up from the touch device when user presence is detected.

9.9 Event Mode Communication

The device can be set up to bypass the communication window when no activity is sensed (Event Mode). This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurred. The communication will resume (RDY will indicate available data) if an enabled event occurs. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

9.9.1 Events

Numerous events can be individually enabled to trigger communication, bit definitions can be found in Table A.2 and Table A.3:

- > Power mode change
- > Proximity or touch event
- > ATI error
- > ATI active
- > ATI Event
- > Current power mode

9.9.2 Force Communication / Polling

The master can initiate communication even while RDY is HIGH (inactive). The IQS7222A will clock stretch until an appropriate time to complete the I²C transaction. The master firmware will not be affected (if clock stretching is correctly handled).

For optimal program flow, it is suggested that RDY is used to sync on new data. The forced/polling method is only recommended if the master must perform I²C and *Event Mode* is active



10 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions

Address	Data (16bit)	Notes
0x00 - 0x09	Version details	See Table A.1
0x10	System Status	See Table A.2
0x11	Events	See Table A.3
0x12	Proximity event States	See Table A.4
0x13	Touch event States	See Table A.5
0x14	Slider 0 Output	16-bit value
0x15	Slider 1 Output	
0x16	Slider 0 Status	See Table A.6
0x17	Slider 1 Status	
Channel Counts		
0x20	Channel 0 Counts	16-bit value
0x21	Channel 1 Counts	
0x22	Channel 2 Counts	
0x23	Channel 3 Counts	
0x24	Channel 4 Counts	
0x25	Channel 5 Counts	
0x26	Channel 6 Counts	
0x27	Channel 7 Counts	
0x28	Channel 8 Counts	
0x29	Channel 9 Counts	
0x2A	Channel 10 Counts	
0x2B	Channel 11 Counts	
Channel LTA		
0x30	Channel 0 LTA	16-bit value
0x31	Channel 1 LTA	
0x32	Channel 2 LTA	
0x33	Channel 3 LTA	
0x34	Channel 4 LTA	
0x35	Channel 5 LTA	
0x36	Channel 6 LTA	
0x37	Channel 7 LTA	
0x38	Channel 8 LTA	
0x39	Channel 9 LTA	
0x3A	Channel 10 LTA	
0x3B	Channel 11 LTA	
Cycle Setup		
0x8000		See Table A.7
0x8001	Cycle Setup 0	See Table A.8
0x8002		See Table A.9
0x8100		See Table A.7
0x8101	Cycle Setup 1	See Table A.8
0x8102		See Table A.9
0x8200		See Table A.7
0x8201	Cycle Setup 2	See Table A.8
0x8202		See Table A.9
0x8300		See Table A.7
0x8301	Cycle Setup 3	See Table A.8
0x8302		See Table A.9
0x8400		See Table A.7
0x8401	Cycle Setup 4	See Table A.8
0x8402		See Table A.9
0x8500		See Table A.7
0x8501	Cycle Setup 5	See Table A.8
0x8502		See Table A.9
0x8600		See Table A.7
0x8601	Cycle Setup 6	See Table A.8



0x8602		See Table A.9
0x8700	Global Cycle Setup	See Table A.10
0x8701	Coarse and Fine Multiplier Preloads	See Table A.11
0x8702	Compensation Preload	See Table A.12
Button Setup - Thresholds, Hysteresis and Debounce		
0x9000		See Table A.13
0x9001	Button Setup 0	See Table A.14
0x9002		See Table A.15
0x9100		See Table A.13
0x9101	Button Setup 1	See Table A.14
0x9102		See Table A.15
0x9200		See Table A.13
0x9201	Button Setup 2	See Table A.14
0x9202		See Table A.15
0x9300		See Table A.13
0x9301	Button Setup 3	See Table A.14
0x9302		See Table A.15
0x9400		See Table A.13
0x9401	Button Setup 4	See Table A.14
0x9402		See Table A.15
0x9500		See Table A.13
0x9501	Button Setup 5	See Table A.14
0x9502		See Table A.15
0x9600		See Table A.13
0x9601	Button Setup 6	See Table A.14
0x9602		See Table A.15
0x9700		See Table A.13
0x9701	Button Setup 7	See Table A.14
0x9702		See Table A.15
0x9800		See Table A.13
0x9801	Button Setup 8	See Table A.14
0x9802		See Table A.15
0x9900		See Table A.13
0x9901	Button Setup 9	See Table A.14
0x9902		See Table A.15
0x9A00		See Table A.13
0x9A01	Button Setup 10	See Table A.14
0x9A02		See Table A.15
0x9B00		See Table A.13
0x9B01	Button Setup 11	See Table A.14
0x9B02		See Table A.15
Channel Setup- ATI Parameters, Reference Channel and Rx Select		
Channel 0		
0xA000	CRX Select and General Channel Setup	See Table A.16
0xA001	ATI Base and Target	See Table A.18
0xA002	Fine and Coarse Multipliers	See Table A.19
0xA003	ATI Compensation	See Table A.20
0xA004	Reference Channel Settings 0	See Table A.21
0xA005	Reference Channel Settings 1	See Table A.22
Channel 1		
0xA100	CRX Select and General Channel Setup	See Table A.16
0xA101	ATI Base and Target	See Table A.18
0xA102	Fine and Coarse Multipliers	See Table A.19
0xA103	ATI Compensation	See Table A.20
0xA104	Reference Channel Settings 0	See Table A.21
0xA105	Reference Channel Settings 1	See Table A.22
Channel 2		
0xA200	CRX Select and General Channel Setup	See Table A.16
0xA201	ATI Base and Target	See Table A.18
0xA202	Fine and Coarse Multipliers	See Table A.19
0xA203	ATI Compensation	See Table A.20



0xA204	Reference Channel Settings 0	See Table A.21
0xA205	Reference Channel Settings 1	See Table A.22
Channel 3		
0xA300	CRX Select and General Channel Setup	See Table A.16
0xA301	ATI Base and Target	See Table A.18
0xA302	Fine and Coarse Multipliers	See Table A.19
0xA303	ATI Compensation	See Table A.20
0xA304	Reference Channel Settings 0	See Table A.21
0xA305	Reference Channel Settings 1	See Table A.22
Channel 4		
0xA400	CRX Select and General Channel Setup	See Table A.16
0xA401	ATI Base and Target	See Table A.18
0xA402	Fine and Coarse Multipliers	See Table A.19
0xA403	ATI Compensation	See Table A.20
0xA404	Reference Channel Settings 0	See Table A.21
0xA405	Reference Channel Settings 1	See Table A.22
Channel 5		
0xA500	CRX Select and General Channel Setup	See Table A.17
0xA501	ATI Base and Target	See Table A.18
0xA502	Fine and Coarse Multipliers	See Table A.19
0xA503	ATI Compensation	See Table A.20
0xA504	Reference Channel Settings 0	See Table A.21
0xA505	Reference Channel Settings 1	See Table A.22
Channel 6		
0xA600	CRX Select and General Channel Setup	See Table A.17
0xA601	ATI Base and Target	See Table A.18
0xA602	Fine and Coarse Multipliers	See Table A.19
0xA603	ATI Compensation	See Table A.20
0xA604	Reference Channel Settings 0	See Table A.21
0xA605	Reference Channel Settings 1	See Table A.22
Channel 7		
0xA700	CRX Select and General Channel Setup	See Table A.17
0xA701	ATI Base and Target	See Table A.18
0xA703	Fine and Coarse Multipliers	See Table A.19
0xA704	ATI Compensation	See Table A.20
0xA704	Reference Channel Settings 0	See Table A.21
0xA705	Reference Channel Settings 1	See Table A.22
Channel 8		
0xA800	CRX Select and General Channel Setup	See Table A.17
0xA801	ATI Base and Target	See Table A.18
0xA802	Fine and Coarse Multipliers	See Table A.19
0xA803	ATI Compensation	See Table A.20
0xA804	Reference Channel Settings 0	See Table A.21
0xA805	Reference Channel Settings 1	See Table A.22
Channel 9		
0xA900	CRX Select and General Channel Setup	See Table A.17
0xA901	ATI Base and Target	See Table A.18
0xA902	Fine and Coarse Multipliers	See Table A.19
0xA903	ATI Compensation	See Table A.20
0xA904	Reference Channel Settings 0	See Table A.21
0xA905	Reference Channel Settings 1	See Table A.22
Hall Switch Channel		
0xAA00	CRX Select and General Channel Setup	See Table A.17
0xAA01	ATI Base and Target	See Table A.18
0xAA02	Fine and Coarse Multipliers	See Table A.19
0xAA03	ATI Compensation	See Table A.20
0xAA04	Reserved	Value = 0x0000
0xAA05	Reserved	Value = 0x0000
Hall effect Control Channel		
0xAB00	CRX Select and General Channel Setup	See Table A.17



0xAB01	ATI Base and Target	See Table A.18
0xAB02	Fine and Coarse Multipliers	See Table A.19
0xAB03	ATI Compensation	See Table A.20
0xAB04	Reserved	Value = 0x0000
0xAB05	Reserved	Value = 0x0000
Filter Betas		
0xAC00	Filter Beta	See Table A.23
0xAC01	Fast Filter Beta	See Table A.24
Slider 0 Setup		
0xB000	Slider 0 General Setup	See Table A.25
0xB001	Calibration and Bottom Speed	See Table A.26
0xB002	Top Speed/Resolution	See table A.27
0xB003	Enable Mask	See Table A.28
0xB004	Enable Status Link	See Table A.29
0xB005	Delta Link 0	See Table A.30
0xB006	Delta Link 1	See Table A.30
0xB007	Delta Link 2	See Table A.30
0xB008	Delta Link 3	See Table A.30
0xB009	Gesture Setup 0	See Table A.31
0xB00A	Gesture Setup 1	See Table A.32
Slider 1 Setup		
0xB100	Slider 1 General Setup	See Table A.25
0xB101	Calibration and Bottom Speed	See Table A.26
0xB102	Top Speed/Resolution	See table A.27
0xB103	Enable Mask	See Table A.28
0xB104	Enable Status Link	See Table A.29
0xB105	Delta Link 0	See Table A.30
0xB106	Delta Link 1	See Table A.30
0xB107	Delta Link 2	See Table A.30
0xB108	Delta Link 3	See Table A.30
0xB109	Gesture Setup 0	See Table A.31
0xB10A	Gesture Setup 1	See Table A.32
GPIO0 Settings		
0xC000	GPIO0 Enable and Configuration Settings	See Table A.33
0xC001	GPIO0 Mask	See Table A.34
0xC002	GPIO0 Enable Status Link	See Table A.29
PMU and System Settings		
0xD0	Control settings	See Table A.35
0xD1	ATI Error Timeout	16-bit value (s)
0xD2	ATI Report Rate	16-bit value (ms)
0xD3	Normal Power Mode Timeout	16-bit value (ms)
0xD4	Normal Power Mode Report Rate	16-bit value (ms)
0xD5	Low Power Mode Timeout	16-bit value (ms)
0xD6	Low Power Mode Report Rate	16-bit value (ms)
0xD7	Normal Power Update rate in Ultra-low Power Mode	16-bit value (ms)
0xD8	Ultra-low Power Mode Report Rate	16-bit value (ms) Range: 0 - 3276
0xD9	ULP Entry Mask	See Table A.36
0xDA	Event Enable	See Table A.37
0xDB	Hall Offset and Bias Current	See Table A.38
0xDC	I ² C Communication	See Table A.39



11 Applications, Implementation and Layout

11.1 Layout Fundamentals

NOTE

Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 2.2- μ F plus a 100-pF low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters).

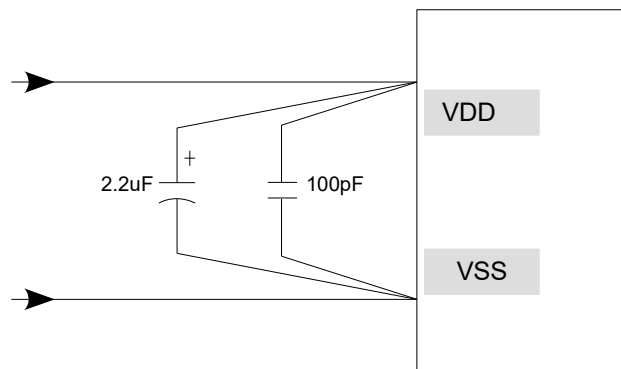


Figure 11.1: Recommended Power Supply Decoupling

11.1.2 Transient Signal Management

During power up, power down, and device operation, VDD must not exceed the absolute maximum ratings. Exceeding the specified limits may cause malfunction of the device.

11.1.3 ProxFusion[®] Peripheral

This section provides a brief introduction to the ProxFusion[®] technology with examples of PCB layout and performance from a design kit. Please contact Azoteq for more details on design variables not covered here.

11.1.4 VREG

The VREG pin requires a 2.2- μ F capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the microcontroller. The figure below shows an example layout where the capacitor is placed close to the IC.

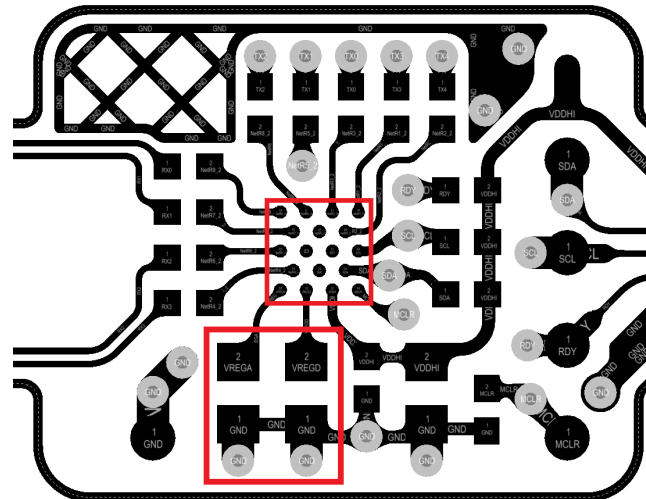


Figure 11.2: VREG Capacitor Placement Close to IC

11.1.5 ESD Protection

Typically, the laminate overlay provides several kilovolts of breakdown isolation to protect the circuit from ESD strikes. More ESD protection can be added with a series resistor placed on each channel used. A value of $470\ \Omega$ is recommended.

11.1.6 Self-capacitance Electrode Design

Self-capacitance electrodes are characterized by having only one sensing pin from the IC that both excites and measures the capacitance. The capacitance being measured is between the electrode and circuit ground, so any capacitance local to the PCB or outside of the PCB (a touch event) influences the measurement.

For PCB layout design it is important to minimize local parasitic capacitances while shielding (with circuit GND) the self-capacitance traces against mechanical changes, induced noise and temperature effects of the board material. Minimize the local parasitic capacitances in order to maximize the effect of external capacitances (proximity and touch effects). To minimize parasitic effects on the PCB, the ground pour on the bottom layer is hatched and there is no pour directly below the electrode: 1.27mm spacing between the electrode and ground fill.

11.1.7 ATI (Auto Tuning Implementation)

The ATI process adjusts three values (Coarse multiplier, Fine multiplier, Compensation) using two parameters per plate (ATI base and ATI target). The ATI process is used to ensure that the sensor's sensitivity is not severely affected by external influences (Temperature, voltage supply change, etc.). For a detailed description of ATI, please contact Azoteq.



12 Ordering Information

12.1 Ordering Code

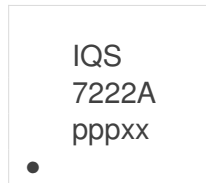
IQS7222A zzz ppb

IC NAME	IQS7222A	=	IQS7222A	
POWER-ON CONFIGURATION	zzz	=	001	I ² C with initialize settings requirement
PACKAGE TYPE	pp	=	CS	WLCSP-18 package
		=	QN	QFN-20 package
BULK PACKAGING	b	=	R	WLCSP-18 Reel (3000pcs/reel) QFN-20 Reel (2000pcs/reel)

Figure 12.1: Order Code Description

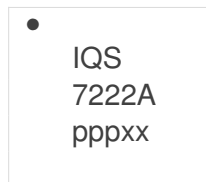
12.2 Top Marking

12.2.1 WLCSP18 Package



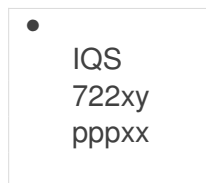
Product Name
ppp = product code
xx = batchcode

12.2.2 QFN20 Package Marking Option 1



Product Name
ppp = product code
xx = batchcode

12.2.3 QFN20 Package Marking Option 2



Product Name
ppp = product code
xx = batchcode



13 Package Specification

13.1 Package Outline Description - WLCSP18

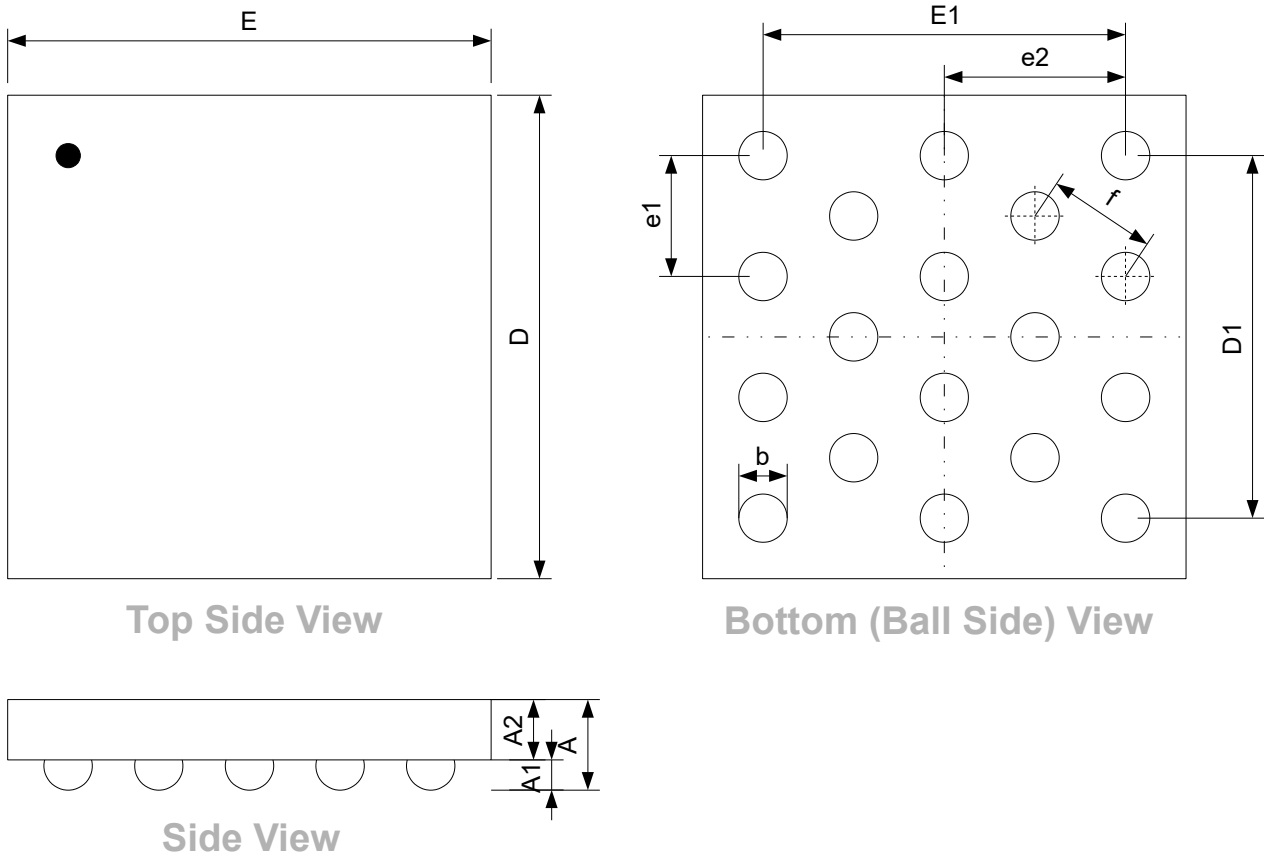


Figure 13.1: WLCSP (1.62x1.62) - 18 Package Outline Visual Description

Table 13.1: WLCSP (1.62x1.62) - 18 Package Outline Visual Description

Dimension	[mm]	Dimension	[mm]
A	0.525±0.05	E	1.620±0.015
A1	0.2±0.02	E1	1.2
A2	0.3±0.025	e1	0.4
b	0.260±0.039	e2	0.6
D	1.620±0.015	f	0.36
D1	1.2		



13.2 Package Outline Description - QFN20

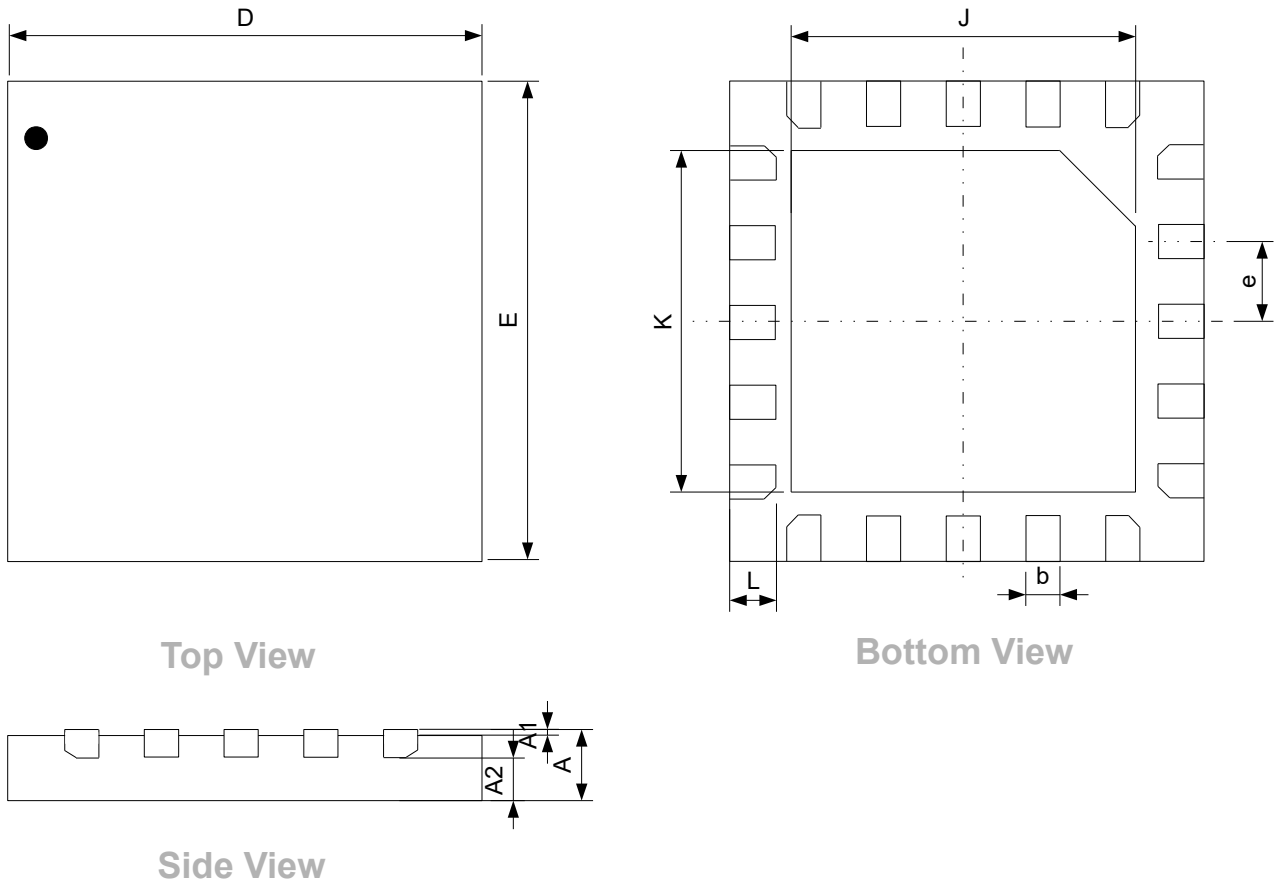


Figure 13.2: QFN (3x3)-20 Package Outline Visual Description

Table 13.2: QFN (3x3)-20 Package Outline Visual Description

Dimension	[mm]	Dimension	[mm]
A	0.5±0.1	E	3
A1	0.035±0.05	e	0.4
A2	0.3	J	1.7±0.1
A3	0.203	K	1.7±0.1
b	0.2±0.05	L	0.4±0.05
D	3		

13.3 Tape and Reel Specifications

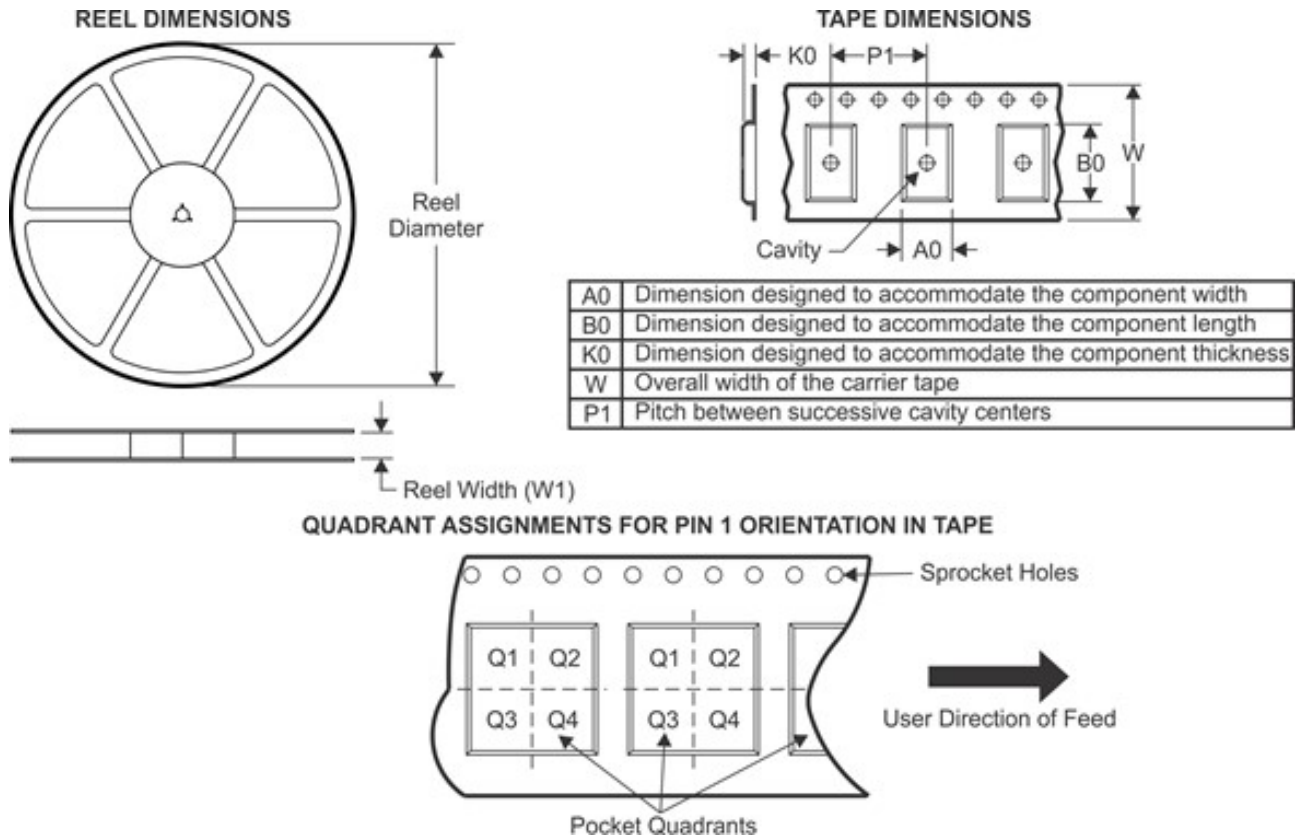


Figure 13.3: Tape and Reel Specification

Table 13.3: Tape and reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2
WLCSP18	18	179	8.4	1.78	1.78	0.69	4	8	Q1

13.4 Moisture Sensitivity Levels

Package	MSL
QFN20	1
WLCSP18	1

13.5 Reflow Specifications

Contact Azoteq



A Memory Map Descriptions

Table A.1: Version Information

Register: 0x00 - 0x09		Category	Name	Value
0x00		Application Version Info	Product Number	840
0x01			Major Version	1
0x02			Minor Version	0
0x03			Reserved	Reserved
0x04			Reserved	Reserved
0x05 - 0x09		Reserved		

Table A.2: System Status

Register: 0x10															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Global Halt	NP up-date	Power mode	Reset	Res	ATI Error	ATI Active	

- > **Bit 7: Global Halt**
 - 0: Global Halt not active
 - 1: Global Halt active
- > **Bit 6: NP Update**
 - 0: No Normal Power Update occurred
 - 1: Normal Power update occurred
- > **Bit 4-5: Power Mode**
 - 00: Normal power mode
 - 01: Low power mode
 - 10: Ultra-low power mode
- > **Bit 3: Device Reset**
 - 0: No reset occurred
 - 1: Reset occurred
- > **Bit 1: ATI Error**
 - 0: No ATI error occurred
 - 1: ATI error occurred
- > **Bit 0: ATI Active**
 - 0: ATI not active
 - 1: ATI active

Table A.3: Events

Register: 0x11															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power Event	ATI Event	Reserved										Touch Event	Prox Event

- > **Bit 13: Power Event**
 - 0: No Power Event occurred
 - 1: Power Event occurred
- > **Bit 12: ATI Event**
 - 0: No ATI Event occurred
 - 1: ATI Event occurred
- > **Bit 1: Touch Event**
 - 0: No Touch Event occurred
 - 1: Touch Event occurred
- > **Bit 0: Proximity Event**
 - 0: No Proximity Event occurred
 - 1: Proximity Event occurred

Table A.4: Proximity Event States

Register: 0x12															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- > **Bit 0-10: Channel Proximity Event**



- 0: No Proximity event occurred on channel
- 1: Proximity event occurred on channel

Table A.5: Touch Event States

Register: 0x13															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

> Bit 0-10: **Channel Touch Event**

- 0: No touch event occurred on channel
- 1: Touch event occurred on channel

Table A.6: Slider Event States

Register: 0x16, 0x17															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
			Reserved					Busy	Event	Neg	Reserved	Flick	Swipe	Tap	

> Bit 7: **Busy**

- 0: Slider not busy
- 1: Slider busy

> Bit 6: **Event**

- 0: No slider event occurred
- 1: Slider event occurred

> Bit 5: **Negative**

- 0: Gesture event occurred in positive direction
- 1: Gesture event occurred in negative direction

> Bit 2: **Flick**

- 0: No flick event occurred
- 1: Flick event occurred

> Bit 1: **Swipe**

- 0: No swipe event occurred
- 1: Swipe event occurred

> Bit 0: **Tap**

- 0: No tap event occurred
- 1: Tap event occurred

Table A.7: Cycle Setup 0

Register: 0x8000, 0x8100, 0x8200, 0x8300, 0x8400, 0x8500, 0x8600															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Conversion Frequency Period								Conversion Frequency Fraction							

> Bit 8-15: **Conversion Period**

- $\frac{128}{\text{FrequencyFraction}} - 2$
- Range: 0 - 127

> Bit 0-7: **Frequency Fraction**

- $256 * \frac{f_{\text{conv}}}{f_{\text{clk}}}$
- Range: 0 - 255

> Note: if Frequency fraction is fixed at 127, the following values of the conversion period will result in the corresponding charge transfer frequencies:

- 1: 2MHz
- 5: 1MHz
- 12: 500kHz
- 17: 350kHz
- 26: 250kHz
- 53: 125kHz

Table A.8: Cycle Setup 1

Register: 0x8001, 0x8101, 0x8201, 0x8301, 0x8401, 0x8501, 0x8601															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTX8	CTX7	CTX6	CTX5	CTX4	CTX3	CTX2	CTX1	CTX0	Inactive Rx - GND	Dead time enabled	FOSC TX Freq	Vbias enable	PXS Mode		



- > Bit 15: **Tx8**
 - 0: Tx8 disabled
 - 1: Tx8 enabled
- > Bit 14: **Tx7**
 - 0: Tx7 disabled
 - 1: Tx7 enabled
- > Bit 13: **Tx6**
 - 0: Tx6 disabled
 - 1: Tx6 enabled
- > Bit 12: **Tx5**
 - 0: Tx5 disabled
 - 1: Tx5 enabled
- > Bit 11: **Tx4**
 - 0: Tx4 disabled
 - 1: Tx4 enabled
- > Bit 10: **Tx3**
 - 0: Tx3 disabled
 - 1: Tx3 enabled
- > Bit 9: **Tx2**
 - 0: Tx2 disabled
 - 1: Tx2 enabled
- > Bit 8: **Tx1**
 - 0: Tx1 disabled
 - 1: Tx1 enabled
- > Bit 7: **Tx0**
 - 0: Tx0 disabled
 - 1: Tx0 enabled
- > Bit 6: **Inactive Rx GND**
 - 0: Inactive Rx floating
 - 1: Inactive Rx Grounded
- > Bit 5: **Dead Time Enabled**
 - 0: Deadtime disabled
 - 1: Deadtime enabled
- > Bit 4: **TX FOSC Frequency**
 - 0: Disabled
 - 1: Enabled
- > Bit 3: **Vbias Enabled**
 - 0: Vbias disabled
 - 1: Vbias enabled
- > Bit 0-2: **PXS Mode**
 - 000: None
 - 001: Self-capacitive
 - 010: Projected capacitance
 - 011: Mutual inductance

Table A.9: Cycle Setup 2

Register:	0x8002, 0x8102, 0x8202, 0x8302, 0x8402, 0x8502, 0x8602														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved					Current Reference Enable	Current Reference Output		Current Reference Level				Current Reference Trim			

- > Bit 10: **Current Reference Enable**
 - 0: Disable current reference
 - 1: Enable current reference
- > Bit 8-9: **Current Reference Output**
 - 00; Disabled
 - 10: Self-inductance to pads
- > Bit 4-7: **Current Reference Level**
 - 4 bit value to scale current output
 - Higher values will result in a higher output current
- > Bit 0-3: **Current Reference Trim**



- 4 bit value to adjust current supply output
- Higher values will result in a higher output current

Table A.10: Global Cycle Setup

Register:		0x8700													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RF Filter EN	Maximum counts			Reserved				1	1	00		Auto Mode		Reserved	

> **Bit 15: RF Filter Enable**

- 0: RF Filter disabled
- 1: RF Filter enabled

> **Bit 13-14: Maximum counts**

- 00: 1023
- 01: 2047
- 10: 4095
- 11: 16384

> **Bit 2-3: Auto Mode**

- Number of conversions created before each interrupt is generated
- 00: 4
- 01: 8
- 10: 16
- 11: 32

Table A.11: Coarse and Fine Multipliers Preload

Register:		0x8701													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Multiplier Preload					Reserved			Coarse Multiplier Preload					

> **Bit 0-4: Coarse Multiplier Preload**

- 5-bit coarse multiplier preload value

> **Bit 9-13: Fine Multiplier Preload**

- 5-bit fine multiplier preload value

Table A.12: ATI Compensation Preload

Register:		0x8702													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						ATI Compensation Preload									

> **Bit 0-9: ATI Compensation Preload**

- 10-bit preload value

Table A.13: Button Setup 0

Register:		0x9000, 0x9100, 0x9200, 0x9300, 0x9400, 0x9500, 0x9600, 0x9700, 0x9800, 0x9900, 0x9A00, 0x9B00													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Exit				Enter				Proximity Threshold							

> **Bit 12-15: Exit Debounce Value**

- 0000: Debounce disabled
- 4-bit value

> **Bit 8-11: Enter Debounce Value**

- 0000: Debounce disabled
- 4-bit value

> **Bit 0-7: Proximity Threshold**

- 8-bit value

Table A.14: Button Setup 1

Register:		0x9001, 0x9101, 0x9201, 0x9301, 0x9401, 0x9501, 0x9601, 0x9701, 0x9801, 0x9901, 0x9A01, 0x9B01													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Hysteresis							Touch Threshold								

> **Bit 8-15: Touch Hysteresis**



- Touch hysteresis value determines the release threshold. Release threshold can be determined as follows:
 - $\frac{LTA}{256} * \text{Threshold bit value} - \frac{LTA}{216} * \text{Hysteresis bit value}$
- > **Bit 0-7: Touch Threshold**
 - $\frac{LTA}{256} * 8\text{bit value}$

Table A.15: Button Setup 2

Register:	0x9002, 0x9101, 0x9202, 0x9302, 0x9402, 0x9502, 0x9602, 0x9702, 0x9802, 0x9902														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Event Timeout										Prox Event Timeout					

- > **Bit 8-15: Touch Event Timeout**
 - 8-bit value * 500ms
 - 0: Never timeout (recommended for use with follower and reference channels and required for ULP entry channels retaining an active state in ULP)
- > **Bit 0-7: Proximity Event Timeout**
 - 8-bit value * 500ms
 - 0: Never timeout (recommended for use with follower and reference channels)

Table A.16: CRX Select and General Channel Setup(CH0-CH4)

Register:	0xA000, 0xA100, 0xA200, 0xA300, 0xA400														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mode	ATI Band	Global halt	Invert	Dual	Enabled	CRX3	CRX2	CRX1	CRX0	Cs 80pF	0v5 Rev	Proj Bias Select			

- > **Bit 14-15: Mode**
 - 00: Independent
 - 01: Reference
 - 10: Follower
- > **Bit 12-13: ATI band**
 - 00: 1/16 * Target
 - 01: 1/8 * Target
 - 10: 1/4 * Target
 - 11: 1/2 * Target
- > **Bit 11: Global halt**
 - 0: Halt disabled
 - 1: Halt enabled
- > **Bit 10: Invert Direction**
 - 0: Invert direction disabled
 - 1: Invert direction enabled
- > **Bit 9: Bi-directional**
 - 0: Bi-directional sensing disabled
 - 1: Bi-directional sensing enabled
- > **Bit 8: Channel Enabled**
 - 0: Channel disabled
 - 1: Channel enabled
- > **Bit 7: CRx3**
 - 0: CRx3 disabled
 - 1: CRx3 enabled
- > **Bit 6: CRx2**
 - 0: CRx2 disabled
 - 1: CRx2 enabled
- > **Bit 5: CRx1**
 - 0: CRx1 disabled
 - 1: CRx1 enabled
- > **Bit 4: CRx0**
 - 0: CRx0 disabled
 - 1: CRx0 enabled
- > **Bit 3: Cs 80pF**
 - 0: 40pF
 - 1: 80pF
- > **Bit 2: Vbias enabled**
 - 0: Vbias disabled
 - 1: Vbias enabled



> Bit 0-1: **Projected Bias Select**

- 00: 2μA
- 01: 5μA
- 10: 7μA
- 11: 10μA

Table A.17: CRX Select and General Channel Setup(CH5-CH9)

Register: 0xA500, 0xA600, 0xA700, 0xA800, 0xA900, 0xAA00, 0xAB00															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mode	ATI Band		Global halt	Invert	Dual	Enabled	CRX7	CRX6	CRX5	CRX4	Cs 80pF	0v5 Rev	Proj Bias Select		

> Bit 14-15: **Mode**

- 00: Independent
- 01: Reference
- 10: Follower

> Bit 12-13: **ATI band**

- 00: 1/16 * Target
- 01: 1/8 * Target
- 10: 1/4 * Target
- 11: 1/2 * Target

> Bit 11: **Global halt**

- If enabled, the LTA on the channel will halt when any other channel with global halt enabled, is in a proximity/-touch state. The function is aimed at slider applications
- 0: Halt disabled
- 1: Halt enabled

> Bit 10: **Invert Direction**

- If this bit is enabled, the direction in which a touch will be triggered, is inverted. Bit must be enabled for mutual capacitive mode
- 0: Invert direction disabled
- 1: Invert direction enabled

> Bit 9: **Bi-directional**

- 0: Bi-directional sensing disabled
- 1: Bi-directional sensing enabled

> Bit 8: **Channel Enabled**

- 0: Channel disabled
- 1: Channel enabled

> Bit 7: **CRx7**

- 0: CRx7 disabled
- 1: CRx7 enabled

> Bit 6: **CRx6**

- 0: CRx6 disabled
- 1: CRx6 enabled

> Bit 5: **CRx5**

- 0: CRx5 disabled
- 1: CRx5 enabled

> Bit 4: **CRx4**

- 0: CRx4 disabled
- 1: CRx4 enabled

> Bit 3: **Cs 80pF**

- 0: 40pF
- 1: 80pF

> Bit 2: **Vbias enabled**

- 0: Vbias disabled
- 1: Vbias enabled

> Bit 0-1: **Projected Bias Select**

- 00: 2μA
- 01: 5μA
- 10: 7μA
- 11: 10μA



Table A.18: ATI Base and Target

Register: 0xA001, 0xA101, 0xA201, 0xA301, 0xA401, 0xA501, 0xA601, 0xA701, 0xA801, 0xA901, 0xAA01, 0xAB01															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI Target						ATI Base					ATI Mode				

- > Bit 8-15: **ATI Target**
 - 8-bit value * 8
- > Bit 3-7: **ATI Base**
 - 5-bit value * 16
- > Bit 0-2: **ATI Mode**
 - 000: ATI Disabled
 - 001: Compensation only
 - 010: ATI from compensation divider
 - 011: ATI from fine fractional divider
 - 100: ATI from coarse fractional divider
 - 101: Full ATI

Table A.19: Fine and Coarse Multipliers

Register: 0xA002, 0xA102, 0xA202, 0xA302, 0xA402, 0xA502, 0xA602, 0xA702, 0xA802, 0xA902, 0xAA02, 0xAB02															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Fractional Divider					Coarse Fractional Multiplier					Coarse Fractional Divider			

- > Bit 9-13: **Fine Fractional Divider**
 - 5-bit value
- > Bit 5-8: **Coarse Fractional Multiplier**
 - 4-bit value
- > Bit 0-4: **Coarse Fractional Divider**
 - 5-bit value

Table A.20: ATI Compensation

Register: 0xA003, 0xA103, 0xA203, 0xA303, 0xA403, 0xA503, 0xA603, 0xA703, 0xA803, 0xA903, 0xAA03, 0xAB03															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Compensation Divider					Res		Compensation Selection								

- > Bit 11-15: **Compensation Divider**
 - 5-bit value
- > Bit 0-9: **Compensation Selection**
 - 10-bit value

Table A.21: Reference Channel Settings 0

Register: 0xA004, 0xA104, 0xA204, 0xA304, 0xA404, 0xA504, 0xA604, 0xA704, 0xA804, 0xA904															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Follower Mask Link Ptr/ Reference Sensor Ptr															

- > Please note that the register value is used for either Follower Mask Link Ptr or Reference Sensor Ptr based on the mode selected in table A.16 / A.17, bit 14-15
- > Bit 0-15: **Follower Mask Link Ptr** - Mode = Reference
 - 0x6E6 (decimal = 1766): Proximity
 - 0x6E8 (decimal = 1768): Touch
- > Bit 0-15: **Reference Sensor Ptr** - Mode = Follower
 - 0x000 (decimal = 0): None
 - 0x418 (decimal = 1048): Channel 0
 - 0x442 (decimal = 1090): Channel 1
 - 0x46C (decimal = 1132): Channel 2
 - 0x496 (decimal = 1174): Channel 3
 - 0x4C0 (decimal = 1216): Channel 4
 - 0x4EA (decimal = 1258): Channel 5
 - 0x514 (decimal = 1300): Channel 6
 - 0x53E (decimal = 1342): Channel 7
 - 0x568 (decimal = 1384): Channel 8
 - 0x592 (decimal = 1426): Channel 9



Table A.22: Reference Channel Settings 1

Register:	0xA005, 0xA105, 0xA205, 0xA305, 0xA405, 0xA505, 0xA605, 0xA705, 0xA805, 0xA905														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Follower Mask/ Reference Sensor Weight															

- > Please note that the register value is used for either Follower Mask or Reference Weight based on the mode selected in table A.16 / A.17, bit 14-15
- > Bit 0-15: **Follower Mask** (used to enable current sensor as a reference channel for the selected channel) - Mode = Reference
 - 0: Disabled
 - 1: Channel enabled as reference for Channel 0
 - 2: Channel enabled as reference for Channel 1 enabled
 - 4: Channel enabled as reference for Channel 2 enabled
 - 8: Channel enabled as reference for Channel 3 enabled
 - 16: Channel enabled as reference for Channel 4 enabled
 - 32: Channel enabled as reference for Channel 5 enabled
 - 64: Channel enabled as reference for Channel 6 enabled
 - 128: Channel enabled as reference for Channel 7 enabled
 - 256: Channel enabled as reference for Channel 8 enabled
 - 512: Channel enabled as reference for Channel 9 enabled
- > Bit 0-15: **Reference Weight** - Mode = Follower
 - 16-bit decimal value/256

Table A.23: Filter Betas

Register:	0xAC00														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LTA Low Power Beta				LTA Normal Power Beta				Counts Low Power Beta				Counts Normal Power Beta			

- > Bit 12-15: **LTA Low Power Beta Filter Value**
 - 4-bit value
- > Bit 8-11: **LTA Normal Power Beta Filter Value**
 - 4-bit value
- > Bit 4-7: **Counts Low Power Beta Filter Value**
 - 4-bit value
- > Bit 0-3: **Counts Normal Power Beta Filter Value**
 - 4-bit value

Table A.24: Fast Filter Betas

Register:	0xAC01														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
				Reserved				LTA Low Power Fast Beta				LTA Normal Power Fast Beta			

- > Bit 4-7: **LTA Low Power Fast Beta Filter Value**
 - 4-bit value
- > Bit 0-3: **LTA Normal Power Fast Beta Filter Value**
 - 4-bit value

Table A.25: Slider Setup 0

Register:	0xB000, 0xB100																
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
Lower Calibration									Static Filter	Slow/Static Beta				Total Channels			

- > Bit 8-15: **Lower Calibration**
 - 8-bit value
- > Bit 6: **Static Filter**
 - 0; Static filter disabled
 - 1: Static filter enabled
- > Bit 3-5: **Bottom/Static Beta**
 - 3-bit value
- > Bit 0-2: **Total Channels**
 - 0010: 2 Channels
 - 0011: 3 Channels



- 0100: 4 Channels
- Else: Disabled

Table A.26: Slider Setup 1

Register: 0xB001, 0xB101															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bottom Filter Speed								Upper Calibration							

- > **Bit 8-15: Bottom Filter Speed**
 - 8-bit value * 4 (pixels per conversion)
 - Filter value = Bottom/static Beta
- > **Bit 0-7: Upper Calibration**
 - 8-bit value

Table A.27: Resolution and Top Speed

Register: 0xB002, 0xB102															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Resolution								Top Speed							

- > **Bit 8-15: Resolution**
 - 8-bit value * 16 (pixels)
- > **Bit 0-7: Top Speed**
 - 8-bit value * 4 (pixels per conversion)
 - Filter value = 255 (no filtering)

Table A.28: Slider Enable Mask

Register: 0xB003, 0xB103															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- > Please note that all channels in use must be selected
- > **Bit 0-9: Channel Enable Mask**
 - 0: Disabled
 - 1: Channel 0 enabled for slider
 - 2: Channel 1 enabled for slider
 - 4: Channel 2 enabled for slider
 - 8: Channel 3 enabled for slider
 - 16: Channel 4 enabled for slider
 - 32: Channel 5 enabled for slider
 - 64: Channel 6 enabled for slider
 - 128: Channel 7 enabled for slider
 - 256: Channel 8 enabled as output
 - 512: Channel 9 enabled as output

Table A.29: Enable Status Link

Register: 0xB004, 0xB104, 0xC002															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Enable Status Link															

- > **Bit 0-15: Enable Status Link**
 - 0x6E6 (decimal = 1766): Output linked to channel prox
 - 0x6E8 (decimal = 1768): Output linked to channel touch

Table A.30: Delta Link

Register: 0xB005, 0xB006, 0xB007, 0xB008, 0xB105, 0xB106, 0xB107, 0xB108															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Delta Link															

- > **Bit 0-15: Delta Link** - Select element order per channel
- > Delta link number corresponds with slider element order
 - 0x000 (decimal = 0): Disabled



- 0x438 (decimal = 1080): Channel 0 enabled for element
- 0x462 (decimal = 1122): Channel 1 enabled for element
- 0x48C (decimal = 1164): Channel 2 enabled for element
- 0x4B6 (decimal = 1206): Channel 3 enabled for element
- 0x4E0 (decimal = 1248): Channel 4 enabled for element
- 0x50A (decimal = 1290): Channel 5 enabled for element
- 0x534 (decimal = 1332): Channel 6 enabled for element
- 0x55E (decimal = 1374): Channel 7 enabled for element
- 0x588 (decimal = 1416): Channel 8 enabled for element
- 0x5B2 (decimal = 1458): Channel 9 enabled for element

Table A.31: Gesture Setup 0

Register: 0xB009, 0xB19A															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Maximum Tap Time								Minimum Tap Time					Flick En	Swipe En	Tap En

- > **Bit 8-15: Maximum Tap Time**
 - 8-bit value * 4 (ms)
- > **Bit 3-7: Minimum Tap Time**
 - 5-bit value * 4 (ms)
- > **Bit 2: Flick Gesture Enable**
 - 0: Flick Disabled
 - 1: Flick Enabled
- > **Bit 1: Swipe Gesture Enable**
 - 0: Swipe Disabled
 - 1: Swipe Enabled
- > **Bit 0: Tap Gesture Enable**
 - 0: Tap Disabled
 - 1: Tap Enabled

Table A.32: Gesture Setup 1

Register: 0xB00A, 0xB10A															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Minimum Swipe Distance								Maximum Swipe Time							

- > **Bit 8-15: Minimum Swipe Distance**
 - 8-bit value * 16 (pixels)
- > **Bit 0-7: Maximum Swipe Time**
 - 8-bit value * 4 (ms)

Table A.33: GPIO0 Enable and Configuration Settings

Register: 0xC000															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved														Open Drain	Enable

- > **Bit 0: Enable**
 - 0: GPIO0 Output disabled
 - 1: GPIO0 Output Enabled
- > **Bit 1: Open Drain**
 - 0: Push pull active high logic
 - 1: Open Drain active low logic

Table A.34: GPIO0 Enable Mask

Register: 0xC001															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved					CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- > Please note that more than one channel can be selected as an output
- > **Bit 0-7: Channel Enable Mask**
 - 0: **Disabled**



- 1: Channel 0 enabled as output
- 2: Channel 1 enabled as output
- 4: Channel 2 enabled as output
- 8: Channel 3 enabled as output
- 16: Channel 4 enabled as output
- 32: Channel 5 enabled as output
- 64: Channel 6 enabled as output
- 128: Channel 7 enabled as output
- > **Bit 8-9: Channel Enable Mask**
 - 256: Channel 8 enabled as output
 - 512: Channel 9 enabled as output
 - 1024: Channel 10/Hall Switch enabled as output

Table A.35: Control Settings

Register: 0xD0															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved							Interface type		Power mode		Reseed	Re-ATI	Soft Reset	ACK Reset	

- > **Bit 6-7: Interface Selection**
 - 00: I²C streaming
 - 01: I²C event mode
 - 10: I²C Stream in touch
- > **Bit 4-5: Power Mode Selection**
 - 00: Normal power
 - 01: Low power
 - 10: Ultra-low Power
 - 11: Automatic power mode switching
- > **Bit 3: Execute Reseed Command**
 - 0: Do not reseed
 - 1: Reseed
- > **Bit 2: Execute ATI Command**
 - 0: Do not ATI
 - 1: ATI
- > **Bit 1: Soft Reset**
 - 0: Do not reset device
 - 1: Reset device
- > **Bit 0: Acknowledge Reset Command**
 - 0: Do not acknowledge reset
 - 1: Acknowledge reset

Table A.36: Channel ULP Entry Mask

Register: 0xD9															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved					CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- > Please note that all channels required to enter ULP with an active prox/touch state, must be unmasked
- > **Bit 0-9: Channel ULP Entry Mask**
 - 0: Disabled
 - 1: Channel 0 ULP entry masked
 - 2: Channel 1 ULP entry masked
 - 4: Channel 2 ULP entry masked
 - 8: Channel 3 ULP entry masked
 - 16: Channel 4 ULP entry masked
 - 32: Channel 5 ULP entry masked
 - 64: Channel 6 ULP entry masked
 - 128: Channel 7 ULP entry masked
 - 256: Channel 8 ULP entry masked
 - 512: Channel 9 ULP entry masked
 - 1024: Channel 10/Hall Switch ULP entry masked



Table A.37: Event Enable

Register: 0xD9															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power event	ATI event	Reserved									Touch event	Prox event	

- > **Bit 13: Power Event**
 - 0: Power event masked
 - 1: Power event enabled
- > **Bit 12: ATI Event**
 - 0: ATI event masked
 - 1: ATI event enabled
- > **Bit 1: Touch Event**
 - 0: Touch event masked
 - 1: Touch event enabled
- > **Bit 0: Proximity Event**
 - 0: Proximity event masked
 - 1: Proximity event enabled

Table A.38: Hall Bias an Offset Current

Register: 0xDB															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Hall Coarse Offset				Hall Fine Offset				Hall Bias				Boost Gain			

- > **Bit 12-15: Hall Coarse Offset**
 - Coarse offset current in 3 μ A steps.
 - Range -21 μ A to 21 μ A
- > **Bit 8-11: Hall Fine Offset**
 - 4 bit value * 200 (nA)
- > **Bit 1-7: Hall Bias Current**
 - 7 bit value
- > **Bit 0: Boost Gain**
 - 0: Boost gain disabled
 - 1: Boost gain enabled

Table A.39: I²C Communication

Register: 0xDC															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved												Stop re-ceived	Start re-ceived	RW check dis-abled	Stop bit dis-abled

- > **Bit 3: Stop Received Flag**
 - 0: No I²C stop received
 - 1: I²C stop received
- > **Bit 2: Start Received Flag**
 - 0: No I²C start received
 - 1: I²C start received
- > **Bit 1: RW Check Disabled**
 - 0: Write not allowed to read only registers
 - 1: Read and write allowed to read only registers
- > **Bit 0: Stop Bit Disabled**
 - 0: I²C communication window terminated by stop bit.
 - 1: I²C communication window not terminated by stop bit. Send 0xFF to slave address to terminate window




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