
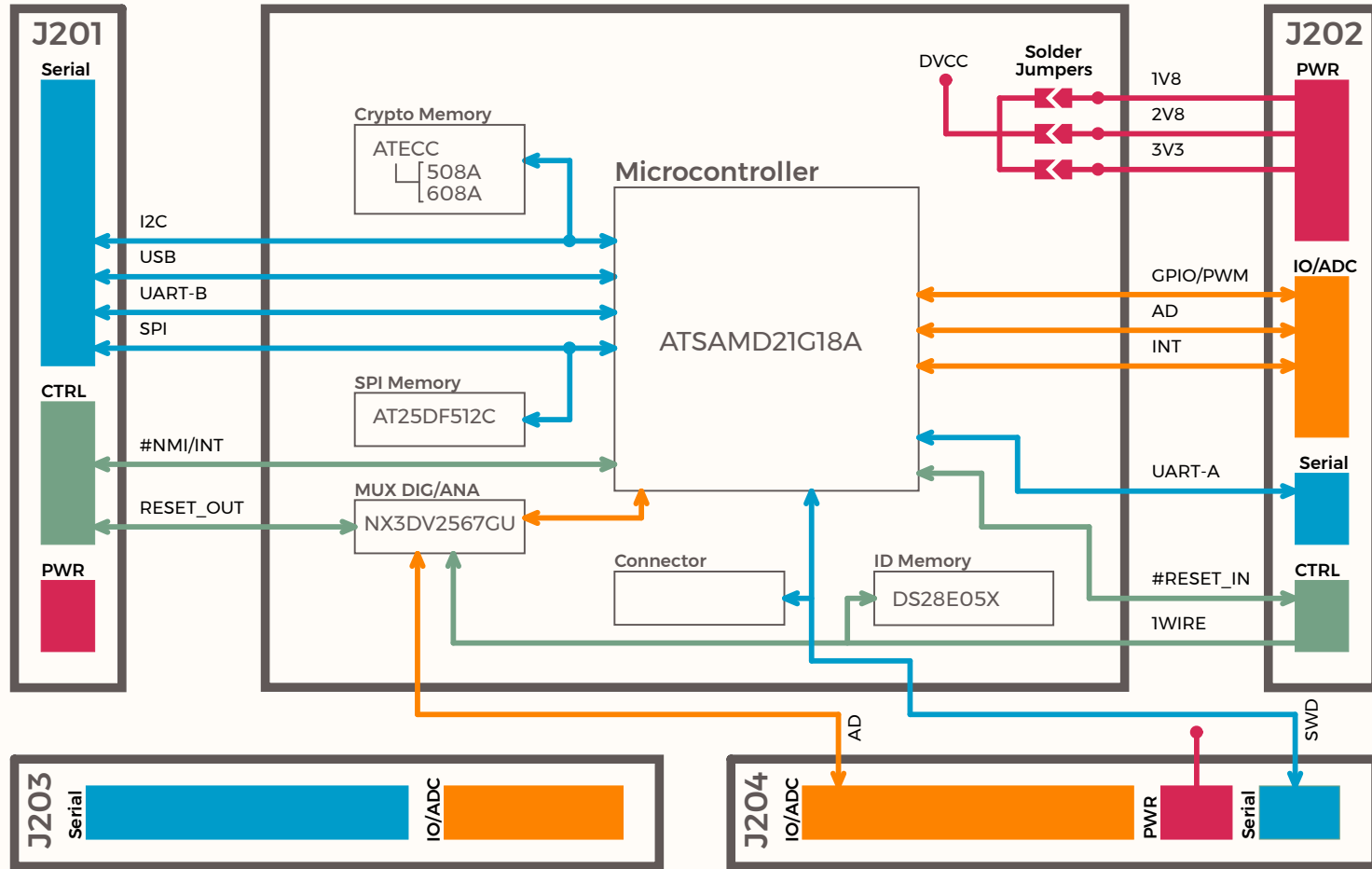


S200 Master - Duino Zero

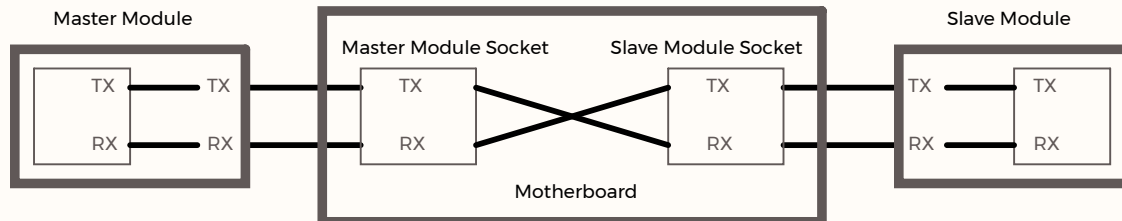
Page	Title
1	Index
2	Block Diagram
3	S200a Master - Plug
4	S200b Master - Plug
5	Power & Connections
6	MCU ATSAM21G18A
7	Memories
8	Production

Title: 01. Index.SchDoc		
Engineer: J.Park	Date: 08/02/2019	
Project: S200 Master - Duino Zero.PrjPcb		
Revision: v1.0	Sheet: 1 of 8	

S200 Master - Duino Zero



UART CONNECTIONS

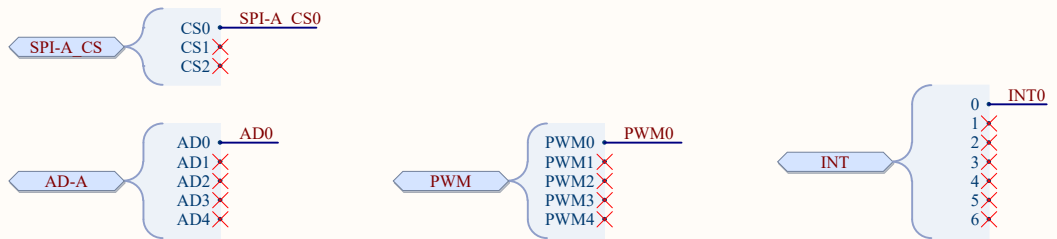
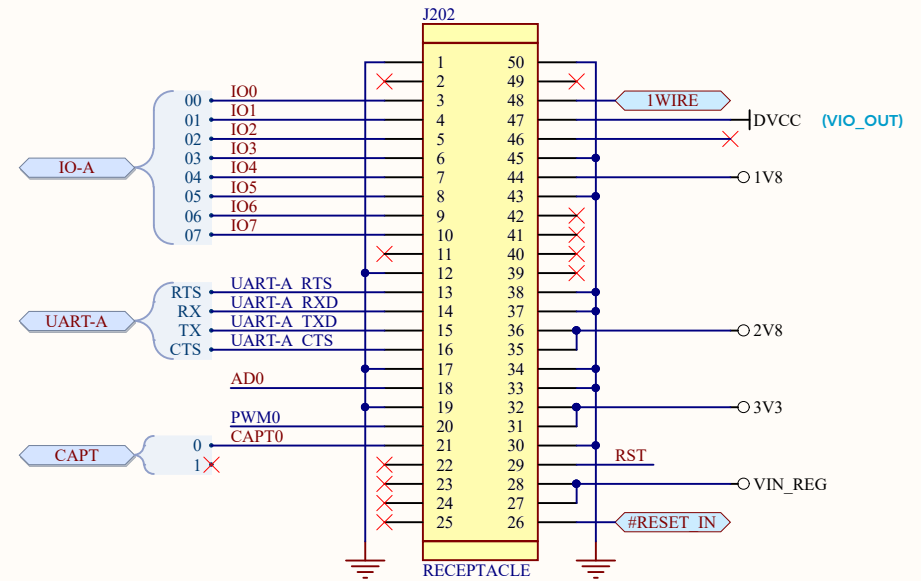
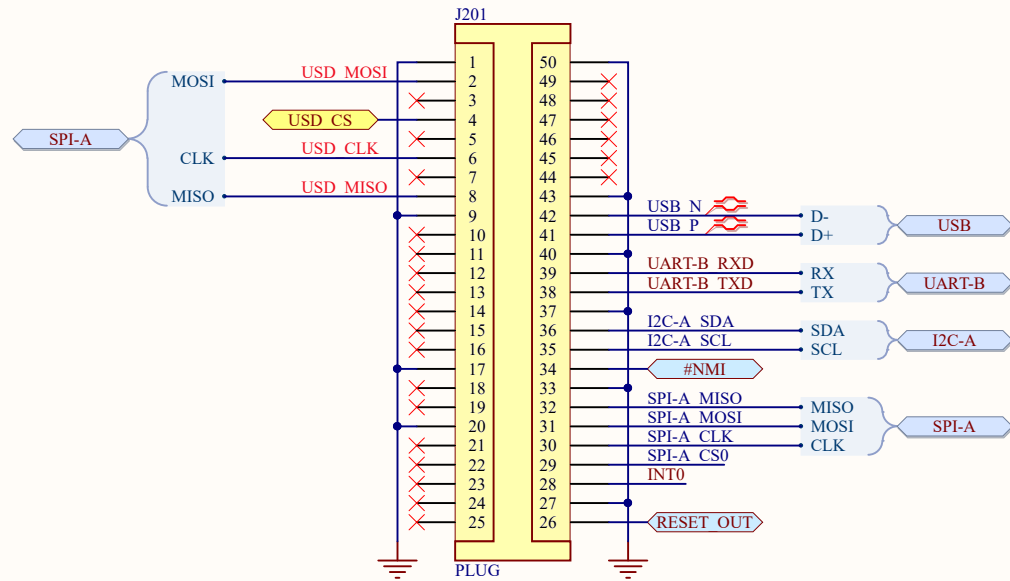


Title: 02. Block Diagram.SchDoc	
Engineer: J.Park	Date: 08/02/2019
Project: S200 Master - Duino Zero.PrjPcb	
Revision: v1.0	Sheet: 2 of 8



S200a MASTER - PLUG

Transparent TOP VIEW



DESIGN NOTE:

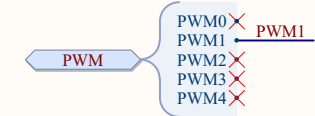
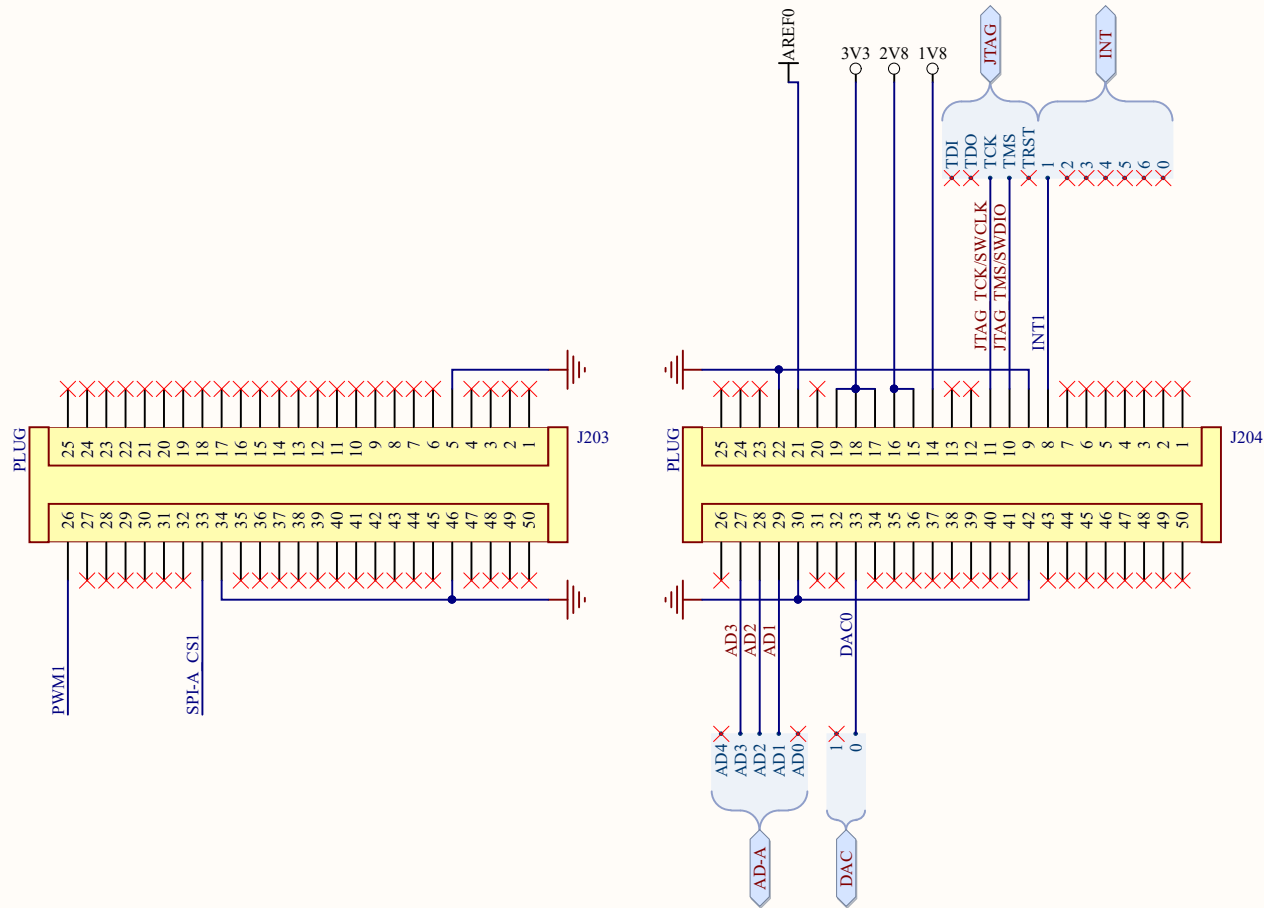
- I2C pull-up resistors are placed on the motherboard, not on the module.
- UART, CAN & SAI lines are crossed on the motherboard, not on the module.
- The text of the unused nets have been deleted.
- VIO_IN provides the voltage reference with which the Core operates.

Title: 03. S200a Master - Plug.SchDoc	
Engineer: J.Park	Date: 08/02/2019
Project: S200 Master - Duino Zero.PrjPcb	
Revision: v1.0	Sheet: 3 of 8



S200b MASTER - PLUG

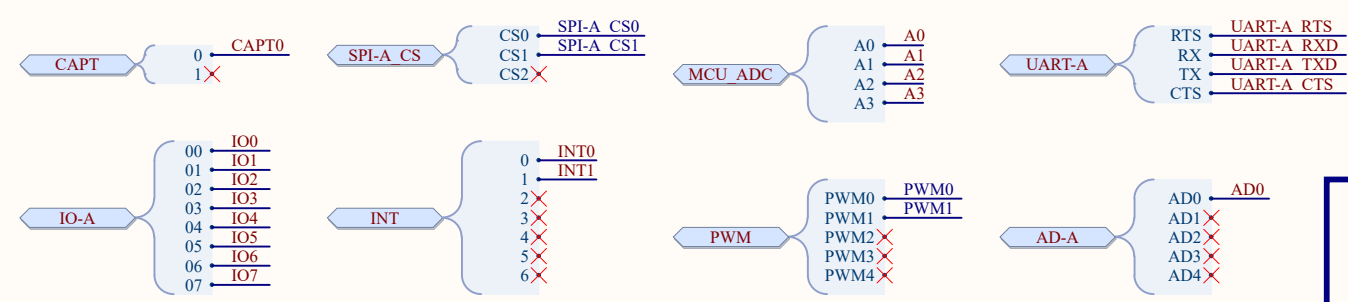
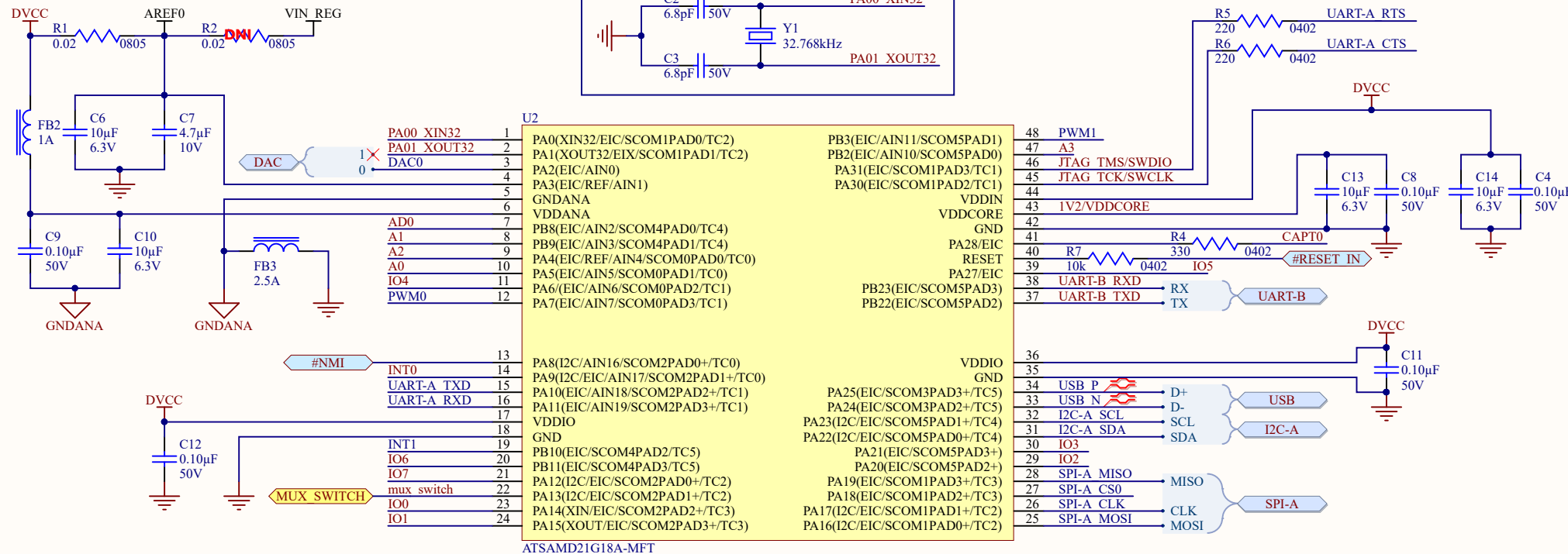
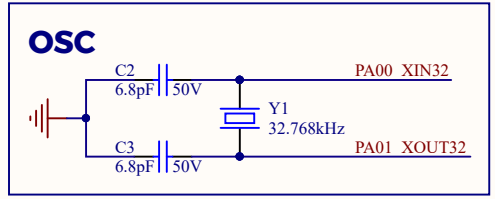
Transparent TOP VIEW



Title: 04. S200b Master - Plug.SchDoc	
Engineer: J.Park	Date: 08/02/2019
Project: S200 Master - Duino Zero.PrjPcb	
Revision: v1.0	Sheet: 4 of 8



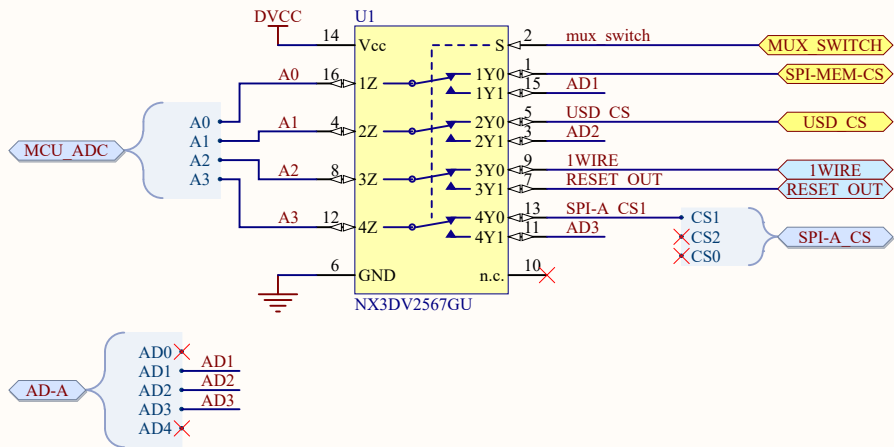
MCU ATSAMD21G18A



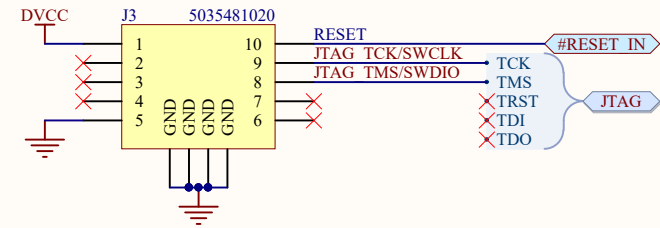
Title: 06. MCU ATSAMD21G18A.SchDoc	
Engineer: J.Park	Date: 08/02/2019
Project: S200 Master - Duino Zero.PrjPcb	
Revision: v1.0	Sheet: 5 of 8



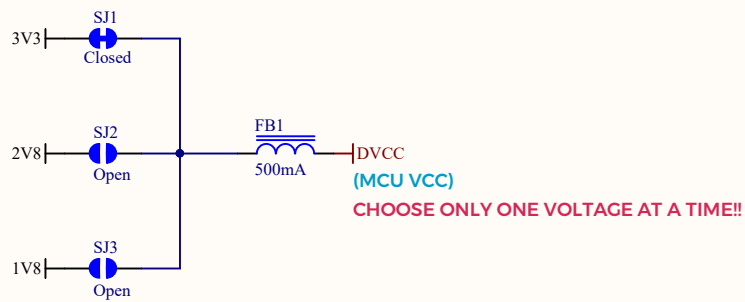
MUX DIG/ANA



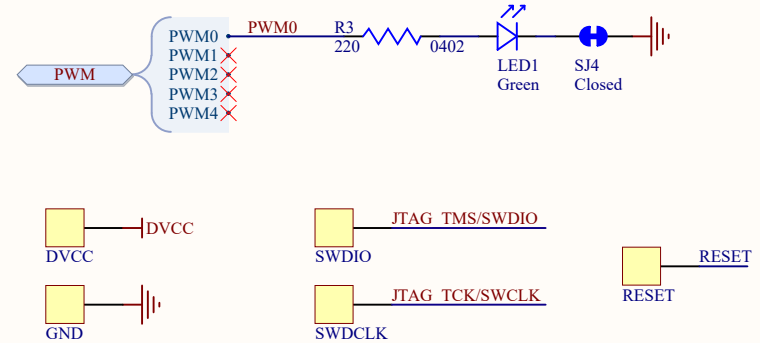
DEGUB CONNECTOR



POWER SUPPLY SELECTION



USER LED & TEST PADS



Title: 05. Power & Connections.SchDoc

Engineer: J.Park

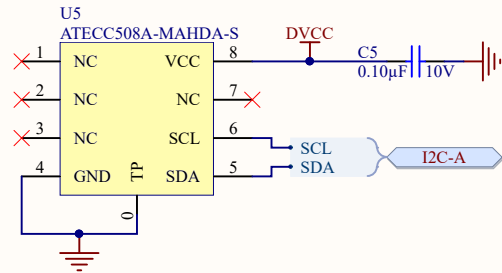
Date: 08/02/2019

Project: S200 Master - Duino Zero.PrjPcb

Revision: v1.0

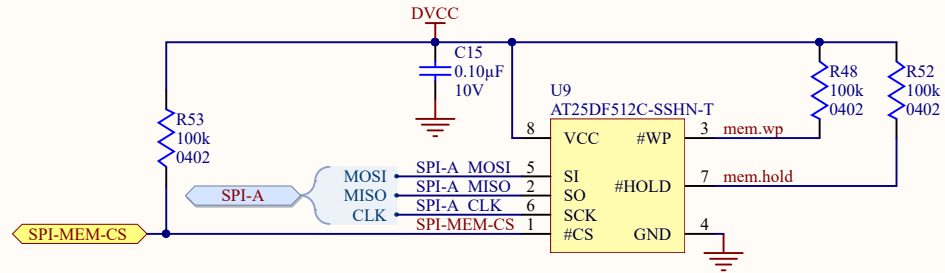
Sheet: 5 of 8

SECURITY



Supply IO levels from 1.8V to 5.5V

SPI MEMORY



Supply voltage range from 1.65V to 3.6V
Master Module is limited to 3.6V
because it's me Vmax supported by SPI memory

Title: 07. Memories.SchDoc	
Engineer: J.Park	Date: 08/02/2019
Project: S200 Master - Duino Zero.PrjPcb	
Revision: v1.0	Sheet: 6 of 8



1

2

3

4

A

A

PCB

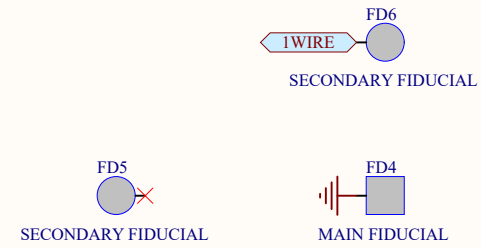
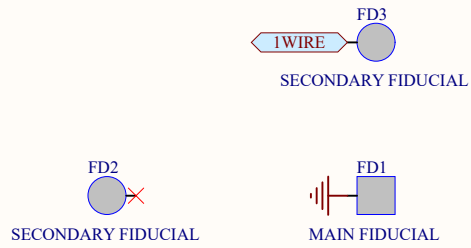
A PCB
 S200 Master
 Duino Zero
 RLRHMDUINOZERO101807

B

B

TOP LAYER FIDUCIALS

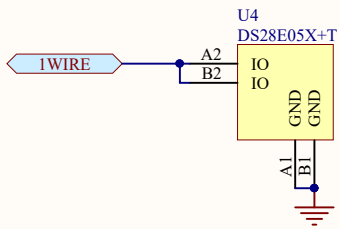
BOTTOM LAYER FIDUCIALS



C

C

ID EEPROM



D

D

Title: 08. Production.SchDoc	
Engineer: J.Park	Date: 08/02/2019
Project: S200 Master - Duino Zero.PrjPcb	
Revision: v1.0	Sheet: 7 of 8



1

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