Using The HI7188 Evaluation Kit

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Evaluation Kit Description

The HI7188 Evaluation Kit (evaluation board and evaluation software) can be used to evaluate the performance of the HI7188 16-bit Sigma Delta Analog-to-Digital Converter (ADC). The evaluation board includes a reference circuit, a crystal, an oscillator, and digital circuitry used to interface to a personal computer running the evaluation software. Also included are two single ended to differential converter circuits and two resistor ladder networks which can be used to provide inputs to the HI7188. In addition, the board provides means for the user to supply an external reference and an external clock.

HI7188 Description

The HI7188 is a Monolithic 8-Channel Sigma-Delta A/D Converter which operates from ±5V supplies and is intended for use in applications such as industrial weight scales, process controls, and process measurement systems. The block diagram shows that the device consists of an 8-channel multiplexer, Programmable Gain Instrumentation Amplifier (PGIA), Sigma-Delta modulator, digital filter, bidirectional serial port (compatible with many industry standard protocols), clock oscillator, a controller, and static RAMs used for calibration coefficients and conversion scan buffer.

The 8 to 1 multiplexer at the input, combined with the resetable modulator on the HI7188, allow for conversions of up to 8 channels of data with each channel being updated at a rate of 240 samples per second (with 60Hz line noise rejection enabled). After the signal has passed through the multiplexer it moves into the PGIA where it is gained up by a factor of 1 to 8 and then it passes to the sigma delta modulator. The data emerges from the modulator as a pulse train whose code density contains the analog signal information. The output of the modulator is fed into the digital integrating filter. Data out of the filter is available after 201 bits are received from the modulator. If the part is in line noise rejection mode, the integrator filter data is routed to one of eight averaging filters. The averaged data is then calibrated and stored in the data RAM.

If line noise rejection is disabled, the averaging filters are bypassed, calibration is performed on the data from the integrating filter, and the result is stored in the data RAM.

After all active channels are converted, the HI7188 generates an End-of-Scan interrupt, $\overline{EOS}$, that indicates all active channels have been updated and valid data is available to be read.

Converted data is read via the HI7188 serial I/O port which is compatible with most synchronous transfer formats including both the Motorola SPI and Intel 8051 series SSR protocols. Data is read from the HI7188 in “burst” mode. That is, the data for all active channels is read out of the HI7188 in a single read communication cycle.

Hardware Description

The HI7188 Evaluation Board provides the user with a very simple way of interfacing to, and evaluating the Intersil HI7188 16-channel sigma delta ADC. The board features two reference voltage generators, a crystal oscillator, and digital line drivers and receivers for interfacing to a PC running the evaluation software. The board consists of 4 layers with separate analog and digital ground planes for obtaining optimum noise performance.

Layout and Power Supplies

The HI7188 Evaluation Board consists of 4 layers laid out to optimize performance of the ADC. The figures at the end of this document include the various layers of the board and their layout, a list of the board components, and schematics. Users should feel free to copy this layout for use in their applications.

The power supplies are provided to the board via the edge connector located at the top of the board. It is recommended that twisted pair wires be used to connect the power supplies to the connector and that analog and digital grounds be tied together back at the power supplies. The separate supplies are necessary to keep the digital noise from coupling into the analog portions of the circuit. One of the internal layers of the board is the ground plane layer. This layer is roughly divided in half, with one half being digital ground and the other half being analog ground. The other internal layer is the power plane. It is divided into three sections; AV_{DD}, AV_{SS}, and DV_{DD}. Nominal values for the supplies are AV_{DD} = +5V, AV_{SS} = -5V, and DV_{DD} = +5V. In some cases (for instance, if there is a substantial offset between AGND and DGND) it may be necessary to tie the two grounds together on the board. Resistors R_2, R_4, and R_5 provide a means of connecting the two ground planes together via a low impedance.

A prototype area is provided on the left side of the board. This area has a small section of analog ground plane in the center and may be useful for input signal conditioning in front of the HI7188.

Reference Circuit

The reference inputs of the HI7188, V_{RHI} and V_{RLO}, provide a differential reference input capability. The reference inputs provide a high impedance dynamic load similar to the analog inputs. For proper circuit operation these pins must be driven by low impedance circuitry. Reference noise outside of the band of interest will be removed by the on-chip digital filter, but excessive reference noise inside the band of interest will degrade performance of the HI7188.

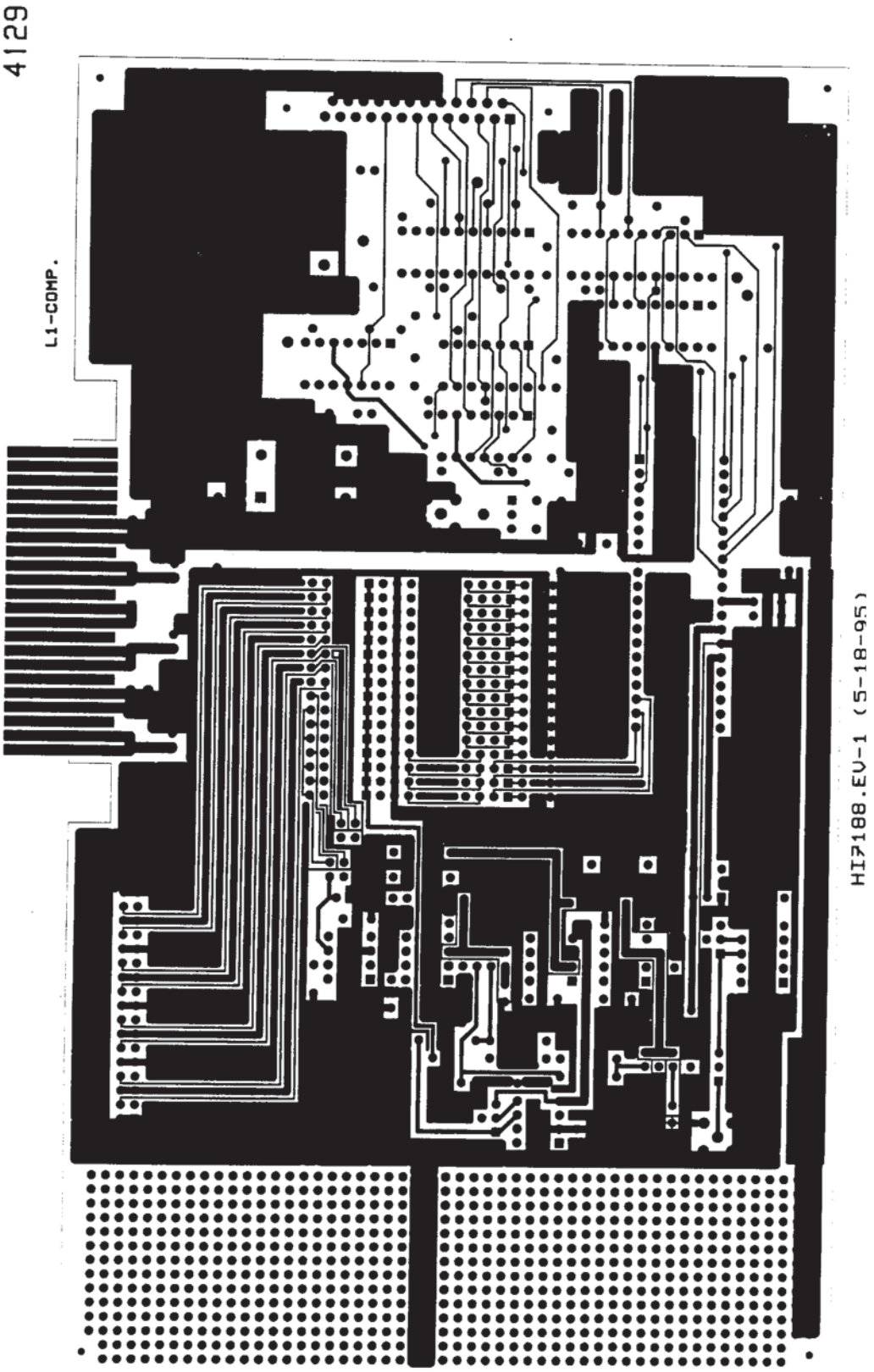

FIGURE 7. COMPONENT SIDE

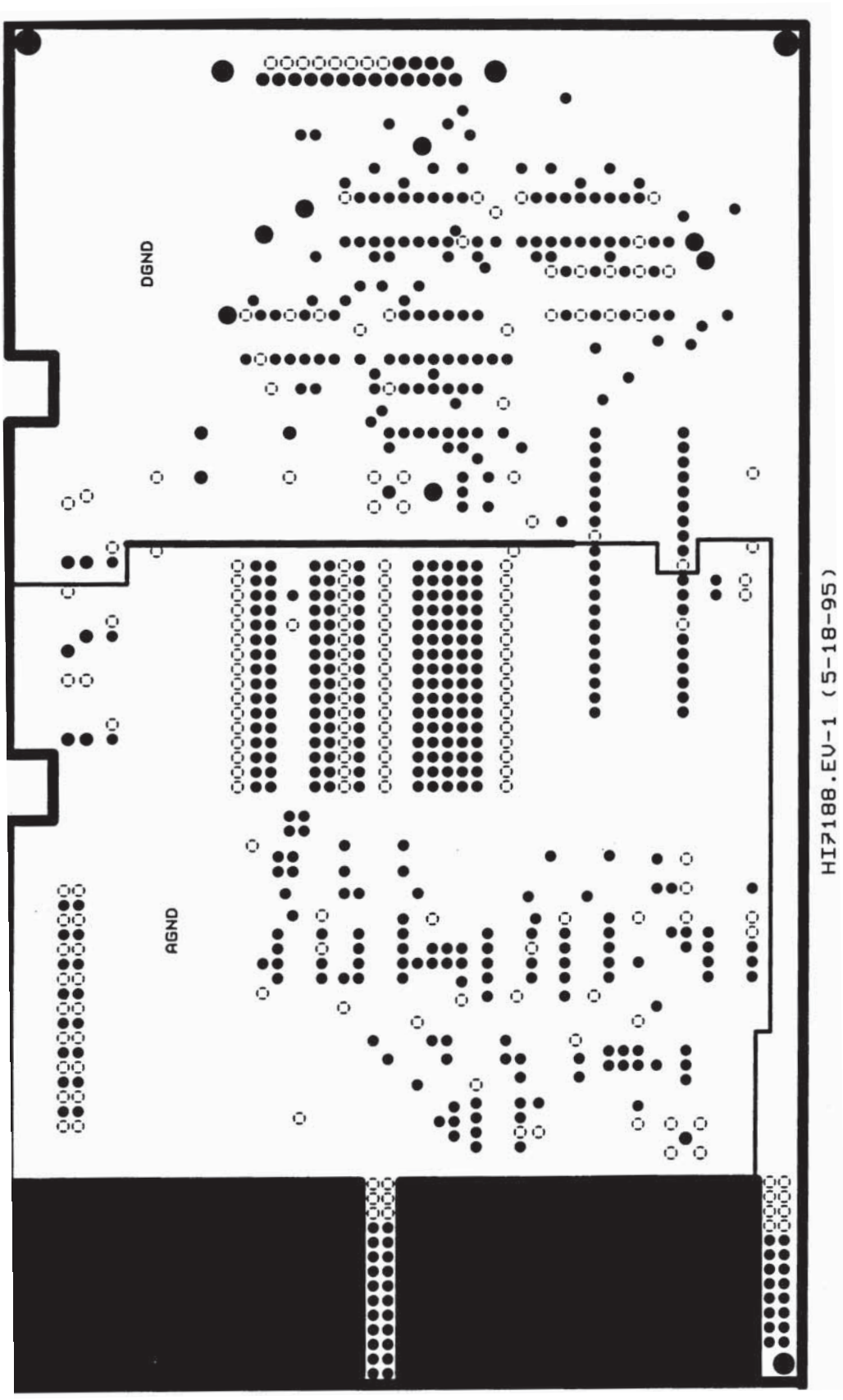

FIGURE 8. GROUND PLANES

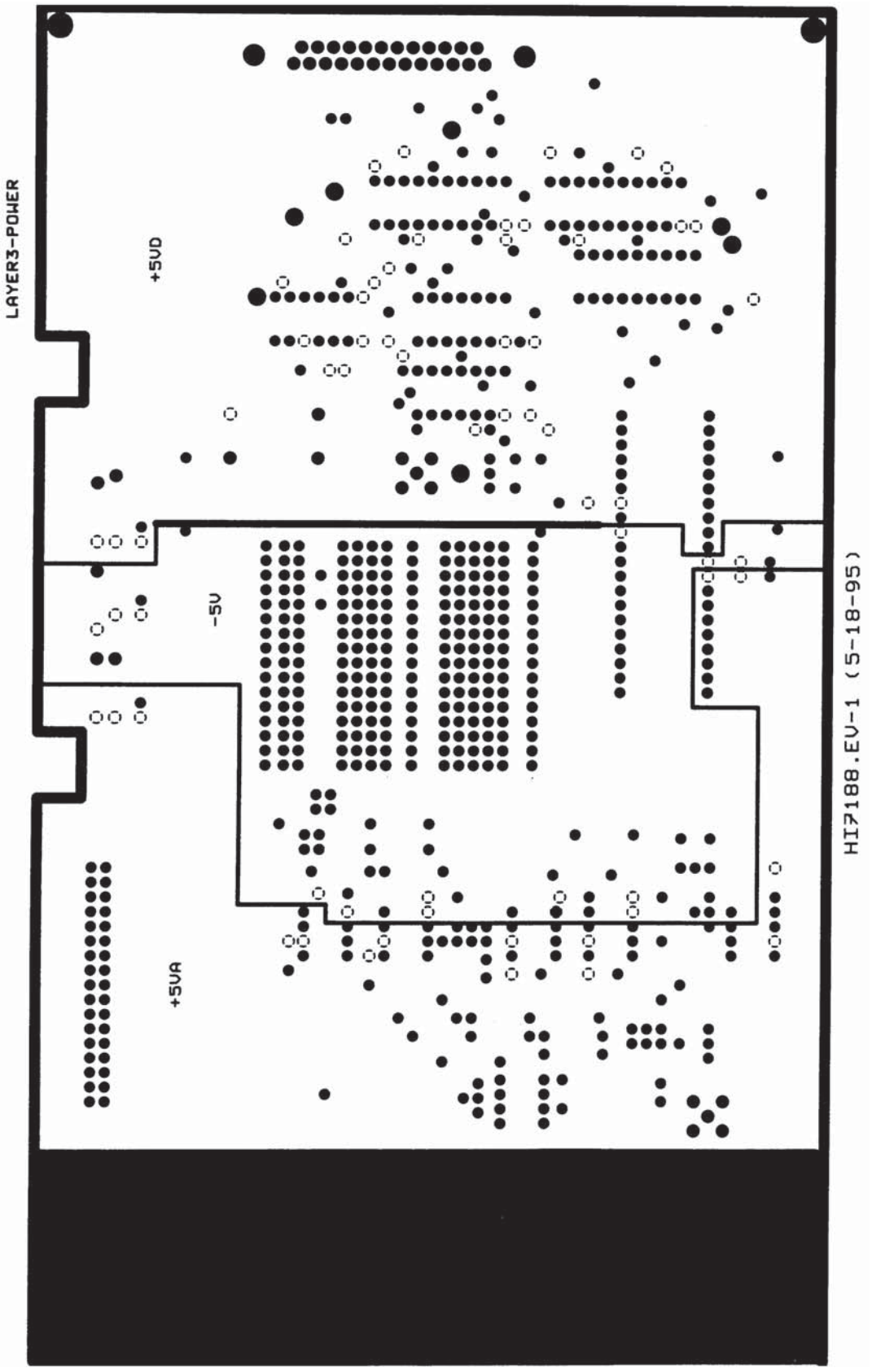

FIGURE 9. POWER PLANES

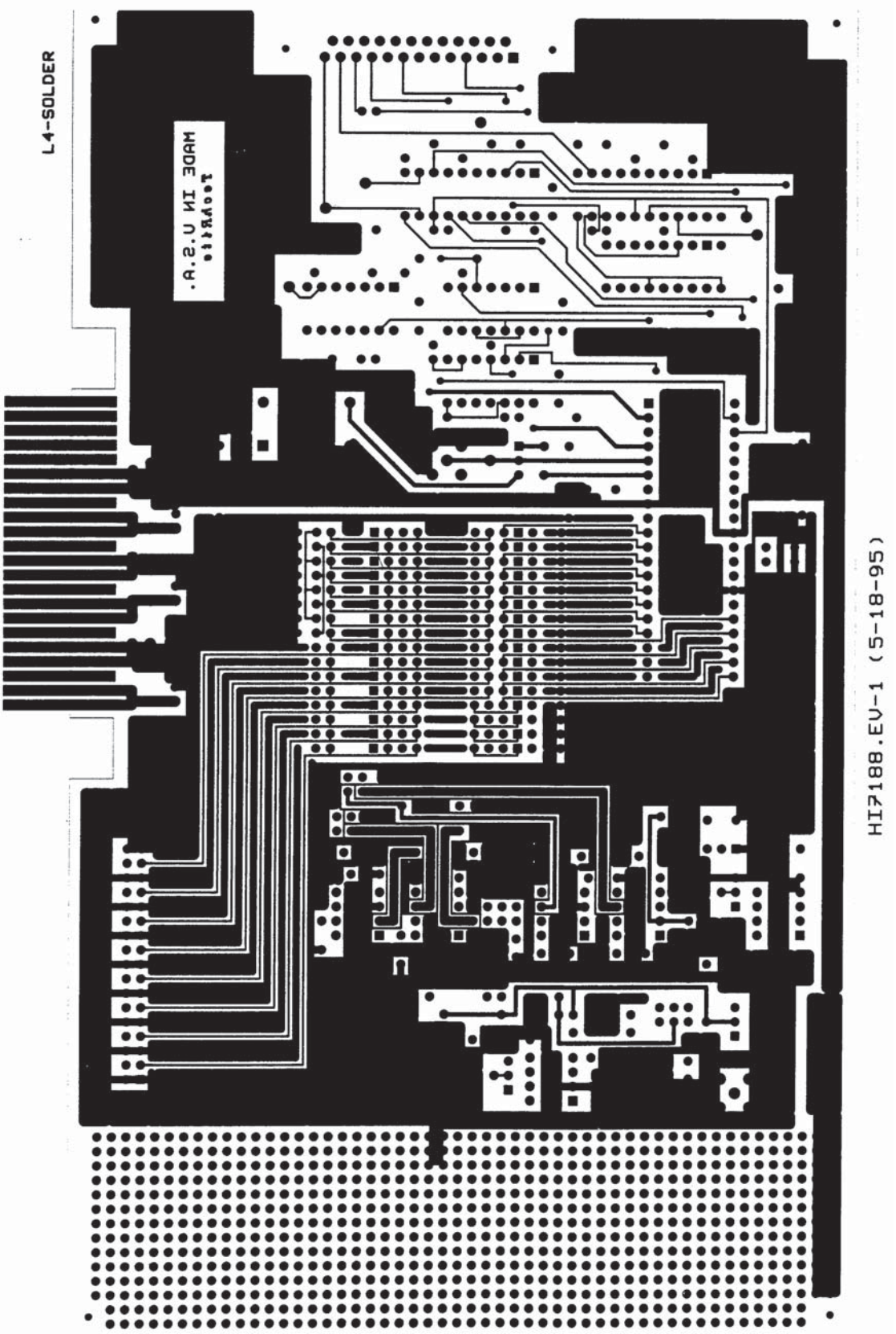

FIGURE 10. SOLDER SIDE