



User Guide

EVB-ATEK253N3-01

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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0		Initial Version	
1.1	06.07.2021	Plots Updated	5/5
1.2	08.01.2022	Format and Content Fixed	

INDEX

1 GENERAL INFORMATION 3

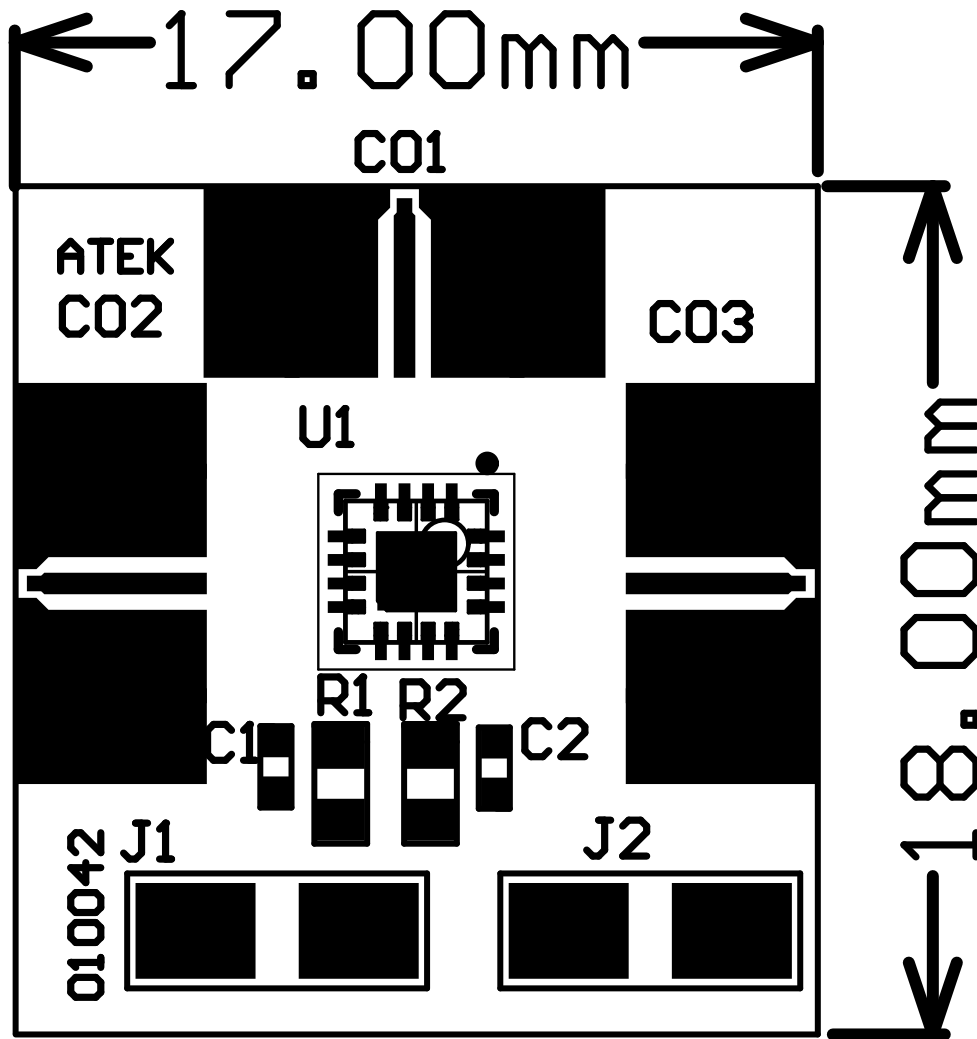
2 DESIGN INFORMATION..... 4

2.1 SCHEMATIC..... 4

2.2 BOM 4

3 TYPICAL PERFORMANCE PLOTS..... 5

1 GENERAL INFORMATION



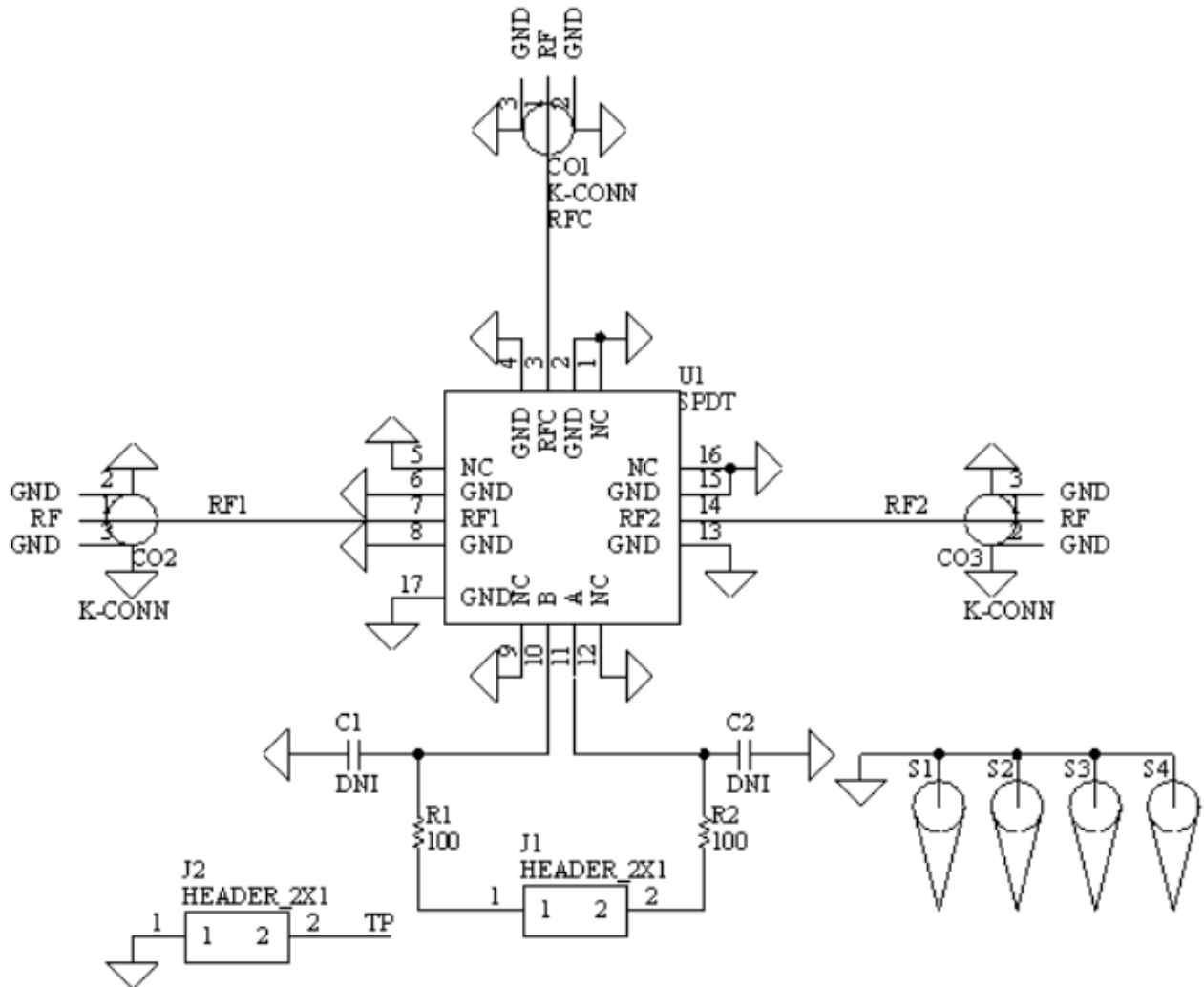
PIN Name	Definition	Comment
C01	RF IN	K Connector
C02, C03	RF OUT	K Connector
J1	Control Voltage	2.54mm Header
J2	N/A	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. Control Voltage is detailed in Datasheet.
3. The definition of up, down, right, and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



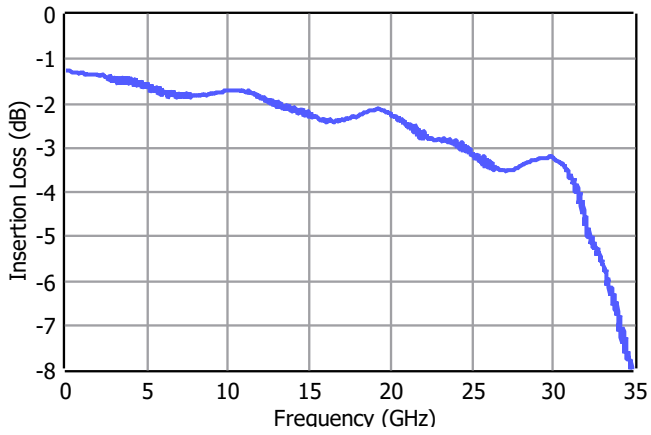
2.2 BOM

Designator	Footprint	Qty	Comment	PN
C1, C2	0402	2	DNP	
CO1, CO2, CO3	K Connector	3	K Connector	
J1, J2	2x1 Header	2	2x1 Header	
R1, R2	0603	2	OR	
U1	ATEKQ3316	1	SPDT	ATEK253N3

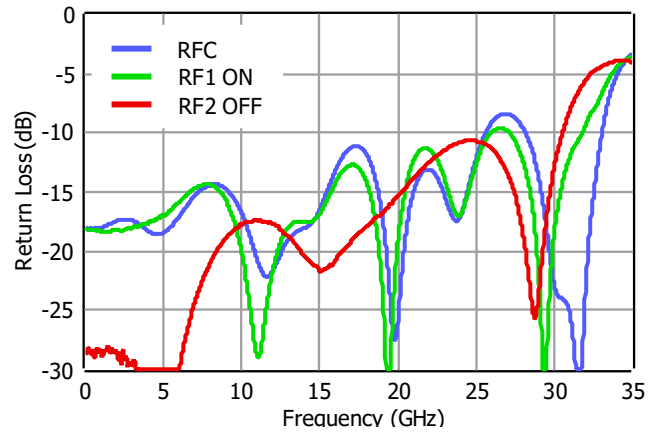
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified: $V_{CTRL} = 0/-5$ V, $T = 25$ C, CW. For details, please refer to the datasheet.

Insertion Loss



Return Loss



Isolation from RFC to RF2

