



Intel[®] Agilex[™] F-Series FPGA Development Kit User Guide



Online Version



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1. Overview

Intel® Agilex™ F-Series FPGA Development Kit is a complete design environment that includes both hardware and software you need to develop Intel Agilex FPGA designs. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Intel Agilex F-Series FPGA designs.

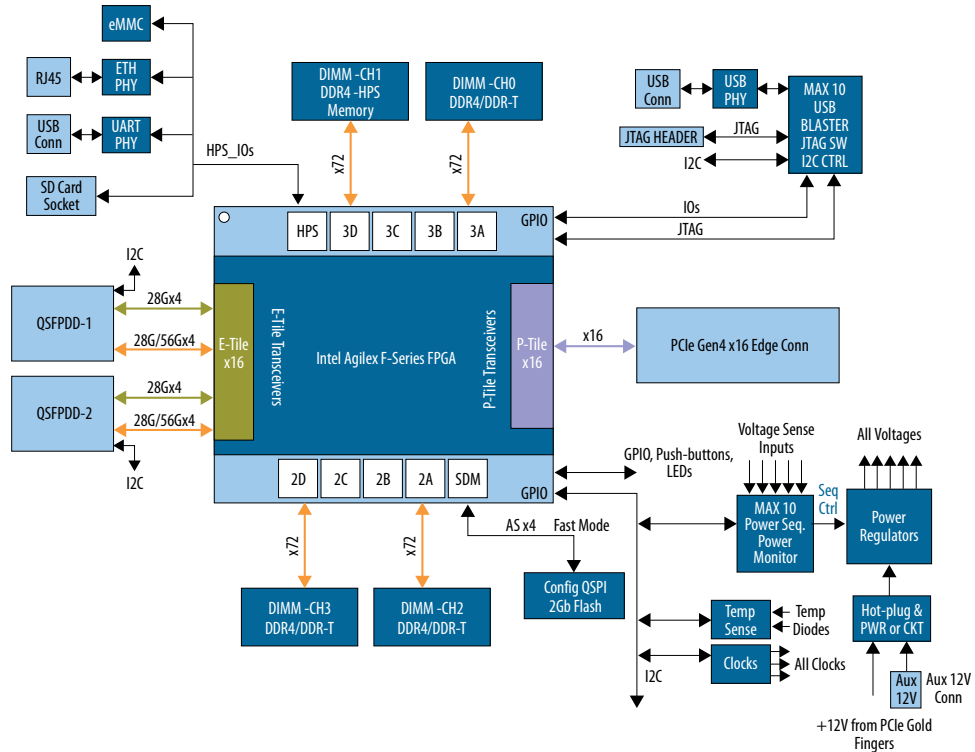
Table 1. Ordering Information

| Development Kit Version | Ordering Code | Device Part Number | Serial Number Identifier |
|---|-------------------|--------------------|--------------------------|
| Intel Agilex F-Series FPGA Development Kit (ES -3V) | DK-DEV-AGF014E3ES | AGFB014R24A2E3VR0 | Under 20000 |
| Intel Agilex F-Series FPGA Development Kit (ES -2V) | DK-DEV-AGF014E2ES | AGFB014R24A2E2VR0 | Above 20000 |
| Intel Agilex F-Series FPGA Development Kit (Production -2V) | DK-DEV-AGF014EA | AGFB014R24BE2V | Above 20220 |

Note: The -3V and -2V versions of the Intel Agilex F-Series FPGA Development Kits use different power solutions for VCC core. Refer to the power tree diagrams in [Power](#) on page 35 for additional information.

1.1. Block Diagram

Figure 1. Intel Agilex F-Series FPGA Development Kit Block Diagram



Feature Summary

- Intel Agilex F-Series FPGA, 1400 KLE, 2486- (R24A and R24B) packages
- 2x Standard QSPDD supports both optical and electrical cable interfaces connected to E-Tile transceivers
- PCIe x16 Gen 4 golden finger connected to P-Tile transceivers, supports x1/x4/x8/x16 modes
- 3x 288-Pin DDR4 DIMMs sockets to support 72 bits DDR4/DDR-T module in FPGA Fabric interface
- 1x 288-Pin DDR4 DIMM socket to support 72 bits DDR4 module for HPS memory interface
- 2 Gb QSPI Flash for active serial FPGA configuration (ASx4 mode)
- Programmable clock resource for XCVR, memory and FPGA fabric
- HPS interface supporting: ETH, UART, SD card socket, eMMC and Mictor connector

Note: Golden Software Reference Design for HPS (GSRD) is not currently available for this development kit.

1.2. Box Contents

Intel Agilex F-Series FPGA Development board, DDR4 DIMM module, USB2.0 Micro cable, Ethernet cable, 240W power adapter and NA/EU/JP/UK cords, ATX power convert cable - 24pin to 6pin.

Note: Only one DIMM module is provided with each development kit.

1.3. Operating Conditions

Table 2. Recommended Operating Conditions

| Operating Condition | Range |
|---|---------------|
| Ambient operating temperature range | 0 °C to 45 °C |
| ICC load current | 100 A |
| ICC load transient percentage | 200 A/μs |
| FPGA maximum power supported by active heatsink/fan | 150 W |

Handling Precautions

When handling the board, it is important to observe static discharge precautions.

Note: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Note: This development kit should not be operated in a vibration environment.

2. Getting Started

2.1. Software and Driver Installation

Intel Quartus® Prime design software is a multi-platform design environment that easily adapts to your specific needs in all phases of FPGA, CPLD and SoC designs. The Intel Quartus Prime software delivers the highest performance and productivity for Intel FPGAs, CPLDs, and SoCs. Intel Quartus Prime Pro Edition software is optimized to support the advanced features in next-generation FPGAs and SoCs with the Intel Agilex, Intel Stratix® 10, Intel Arria® 10 and Intel Cyclone® 10 GX device families.

Intel Agilex F-Series FPGA Development Kit includes on-board Intel FPGA Download Cable circuits for FPGA and system Intel MAX® 10 programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable driver on the host computer. Installation instructions for the Intel FPGA Download Cable driver for your operating system are available on the Intel website.

On the Intel website, navigate to the [Cable and Adapter Drivers Information](#) link to locate the table entry for your configuration and click the link to access the instructions.

The Intel SoC EDS is a comprehensive software tool suite for embedded software development on Intel SoC devices. It contains development tools, utility programs, run-time software, and application examples to expedite firmware and application software of SoC embedded systems.

Note: Please use Intel Quartus Prime 19.4 Pro Edition or later for this development kit test and debug.

For more information and steps to install the Intel SoC EDS Tool Suite refer to the links below.

Related Information

- [Quick-Start for Intel Quartus Prime Pro Edition Software](#)
- [Intel Quartus Prime Pro Edition User Guide: Getting Started](#)
- [Intel SoC FPGA Embedded Development Suite User Guide](#)
- [Intel Agilex FPGAs and SoCs Device Overview](#)
- [Intel Agilex Device Data Sheet](#)

2.2. Quick Start Guide

Refer to the *Intel Agilex F-Series FPGA Development Kit Quick Start Guide* to learn how the development kit works by default after power up.

2.3. Design Examples

Unzip the install package which includes board design files, documents and examples directories. The table below lists the file directory names and a description of their contents.

Table 3. Installed Development Kit Directory Structure

| Directory Name | Description of Directory Contents |
|--------------------|--|
| board_design_files | Contains schematics, layout, assembly and bill of material board design files. Use these files as a starting point for a new prototype board design |
| documents | Contains the development kit documentation - quick start guides and user guide |
| examples | Contains: <ul style="list-style-type: none"> • Board Test System: BTS GUI, Power GUI and Clock GUI • Golden Top project for pinout assignments management • Design Examples: Memory, XCVR, GPIO and PCIe Gen4 |
| power_max10 | Contains the instructions on how to program the power monitoring function in the Intel MAX 10 board controller (refer to Control on-board power regulator through Power GUI on page 12). |
| ubi_max10 | Contains the instructions on how to program UBII Intel MAX 10 |

3. Power Up the Development Kit

The instructions in this chapter explain how to setup the Intel Agilex F-Series FPGA Development Kit for specific use cases.

3.1. Default Settings

The Intel Agilex F-Series FPGA Development Kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the factory default switch settings table given below to return the board to its factory settings before proceeding forward.

Note: X refers to Don't Care in the table below.

Table 4. Factory Default Switch Settings

| Switch | Default Position | Function |
|-----------|------------------|--|
| SW1 [1:3] | OFF/ON/ON | Configuration mode setting bits By default, AS -> FAST mode |
| SW2 [1:4] | OFF/OFF/OFF/OFF | Select the resource of the System Intel MAX 10 JTAG from USB PHY Enable Si5341's outputs Power up Si52202 Enable UART interface |
| SW3 [1:4] | OFF/OFF/OFF/OFF | Enable all the I ² C level shifter. |
| SW4 [1:4] | OFF/ON/ON/OFF | Select on-board Intel FPGA Download Cable as JTAG master when external JTAG header is absent Bypass PWR Intel MAX 10 in JTAG chain; Bypass FPGA HPS in JTAG chain Enable FPGA in JTAG chain |
| SW5 | SW5.5 to SW5.6 | Power off the board |
| SW6 [1:4] | ON/OFF/OFF/OFF | PCIe x16 mode is selected |
| SW7.1 | ON | Select local clock as PCIe reference clock |

3.2. Power Up

Board runs as a standalone work bench

Use the provided 240 W power adapter to supply power through **J16**. After power adapter is plugged into **J16** and **SW5** is set to the ON position, one blue LED (**D8**) illuminates, indicating that the board powered up successfully.

Board runs in PCIe socket as an add-in card

Use the provided 240 W power adapter to supply power through **J16**. After the power adapter is plugged into **J16** and the board is plugged into the PCIe socket of server/PC, the board will power up when the server/PC is powered. One blue LED (**D8**) illuminates, indicating that the board powered up successfully.

3.3. Control on-board clock through Clock Controller GUI

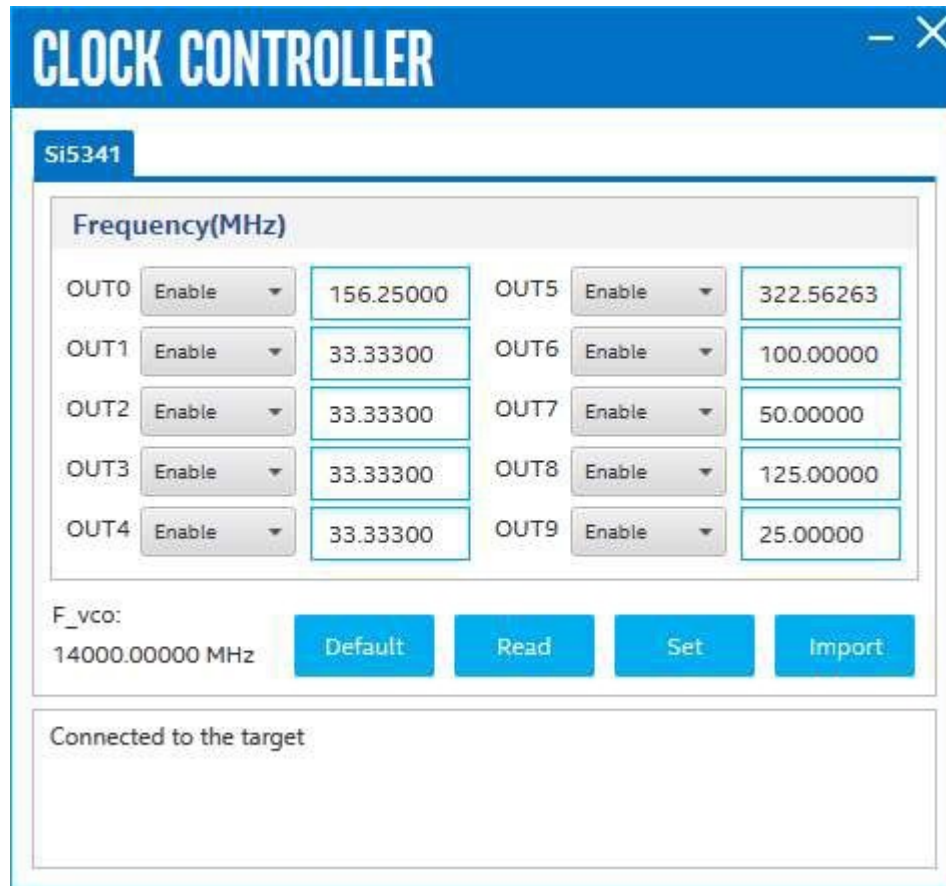
The Clock Controller application can change on-board Si5341 programmable PLLs to any customized frequency between 10 MHz and 750 MHz for differential output and 10 MHz to 350 MHz for LVCMOS single-ended output.

The Clock Controller application (ClockControl.exe) runs as a stand-alone application and resides in the <package_dir>\examples\board_test_system directory.

The Clock Controller communicates with the System Intel MAX 10 device through either USB port **J13** or 10 pin JTAG header **J14**. Then System Intel MAX 10 controls these programmable clock parts through a 2-wire I²C bus.

Note: You cannot run the stand-alone Clock Controller application when the BTS or Power Monitor GUI is running at the same time.

Figure 2. Clock Controller GUI



The following sections describe the Clock Controller buttons

Read

Reads the current frequency setting for the oscillator associated with the active tab.

Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Set

Sets the programmable oscillator frequency for the selected clock to the value in the CLKx output controls for the Si5338. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Intel recommends resetting the FPGA logic after changing frequencies.

Import

Si5341 has a two-time writable non-volatile memory (NVM). You can generate the register list from the ClockBuilder Pro tool and import it into Si5341 to update the settings of the NVM.

Related Information

[ClockBuilder Pro Software on Silicon Labs website](#)

3.4. Control on-board power regulator through Power GUI

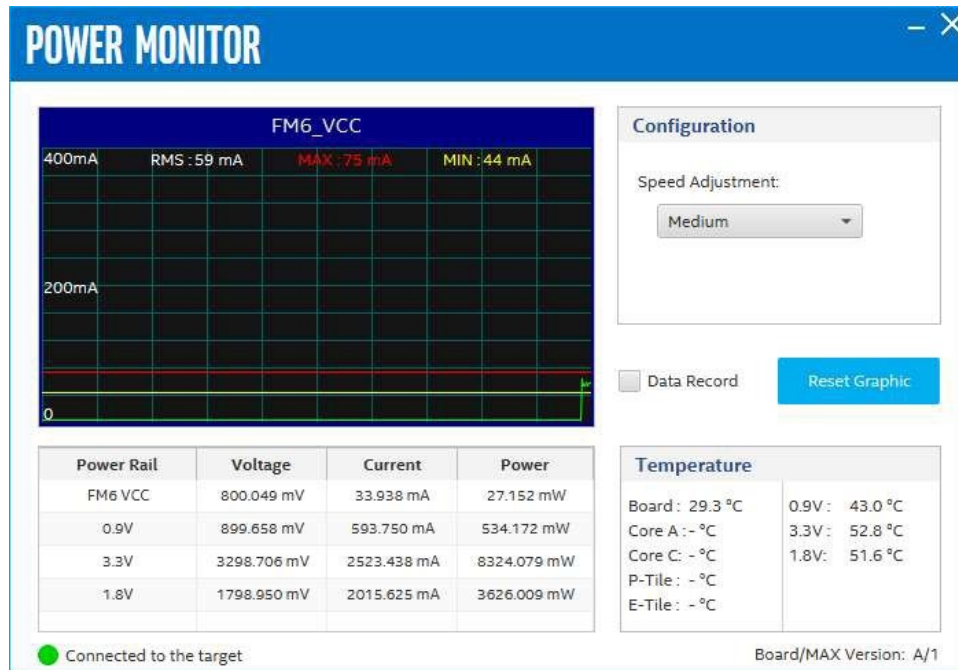
The Power Monitor application reports most power rails voltage, current, and power information on the board. It also collects temperature from FPGA die, power modules and diodes assembled on PCB.

Power GUI communicates with System Intel MAX 10 through either USB port **J13** or **J14**. System Intel MAX 10 monitors and controls power regulator, temperature/voltage/current sensing chips through a 2-wire serial bus.

The Power Monitor application (PowerMonitor.exe) runs as a stand-alone application and resides in the <package_dir>\examples\board_test_system directory.

Note: You cannot run the stand-alone Power Monitor application when the BTS or the Clock Controller GUI is running at the same time.

Figure 3. Power Monitor GUI



Temperature

Board: PCB surface temperature near U32

E-tile/P-tile/Core A/Core C: FPGA dies' internal TSD

0.9V/3.3V/1.8V: regulator U55/U71/U46.

4. Board Test System

The Intel Agilex F-Series FPGA Development Kit includes design examples and an application called the Board Test System (BTS) to test the functionality of this board.

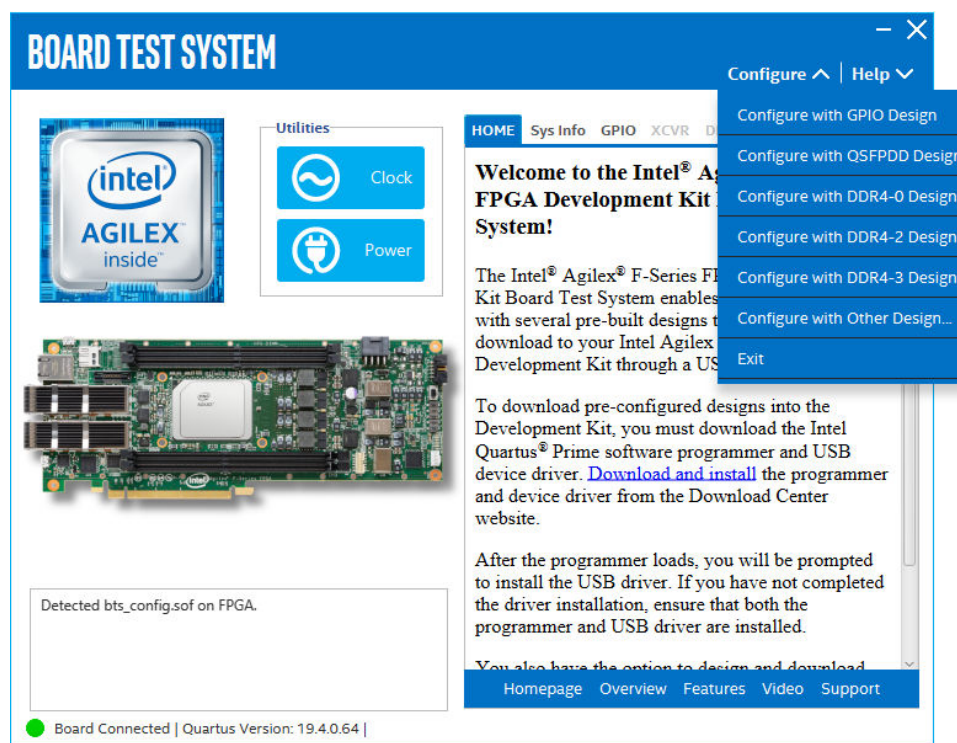
4.1. Test the functionality of the Development Kit

This section describes each control in the Board Test System (BTS).

4.1.1. The Configure Menu

Use the Configure Menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 4. The Configure Menu



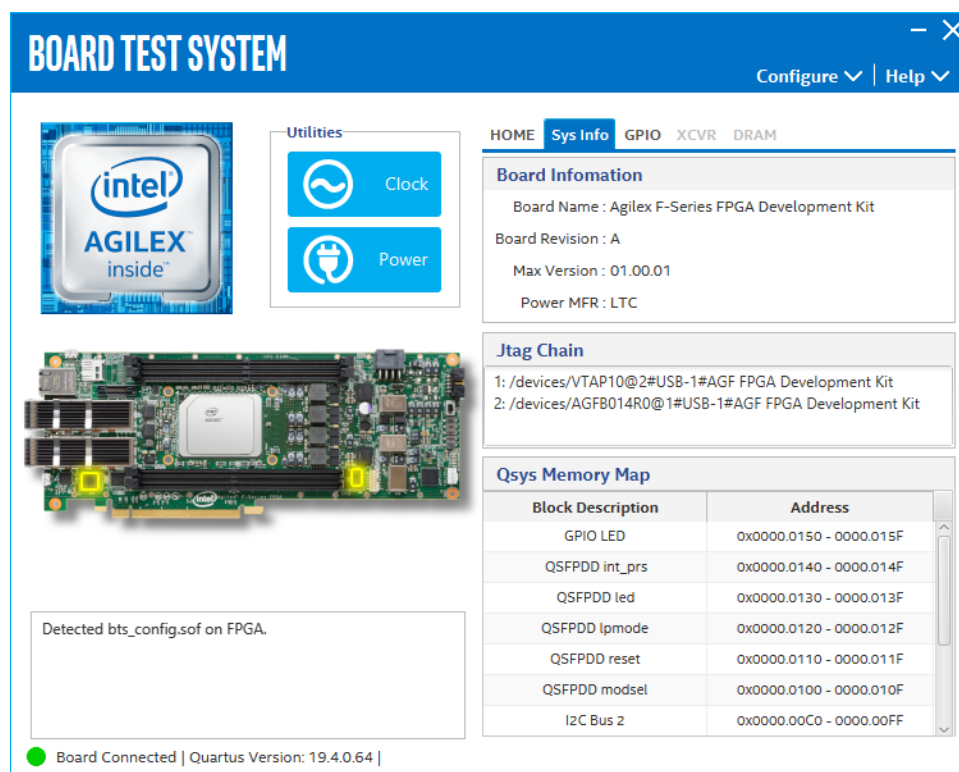
To configure the FPGA with a test system design, perform the following steps:

1. On the **Configure** Menu, click the **configure** command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (.sof) to the FPGA. The download process usually takes less than a minute.
3. When configuration finishes, the design begins running in the FPGA. The corresponding Graphical User Interface (GUI) application tabs that interface with the design are now enabled. If you use the Intel Quartus Prime Programmer for configuration, rather than the BTS GUI, you may need to restart the GUI.

4.1.2. The Sys Info Tab

The **Sys Info** tab shows information about the board's current configuration. The tab displays board information, JTAG Chain devices, Qsys Memory Map for **bts_config.sof** design and other details stored on the board.

Figure 5. The Sys Info Tab



The following sections describe the controls on the System Info tab.

Board Information

The Board Information control displays static information about your board.

- **Board Name:** Indicates the official name of the board given by the BTS.
- **Board Revision:** Indicates the revision of the board.
- **MAX version:** Indicates the version of the System Max
- **Power MFR:** Indicates the FPGA Power manufacture.

JTAG Chain

The JTAG chain control shows all the devices currently in the JTAG chain.

Note: System Intel MAX 10 (VTAP) is always on the JTAG chain, but change the settings of **SW4** to low or high to bypass or enable power Intel MAX 10, HPS and Intel Agilex FPGA. System Intel MAX 10 and FPGA should all be in the JTAG chain when configured and running the BTS GUI.

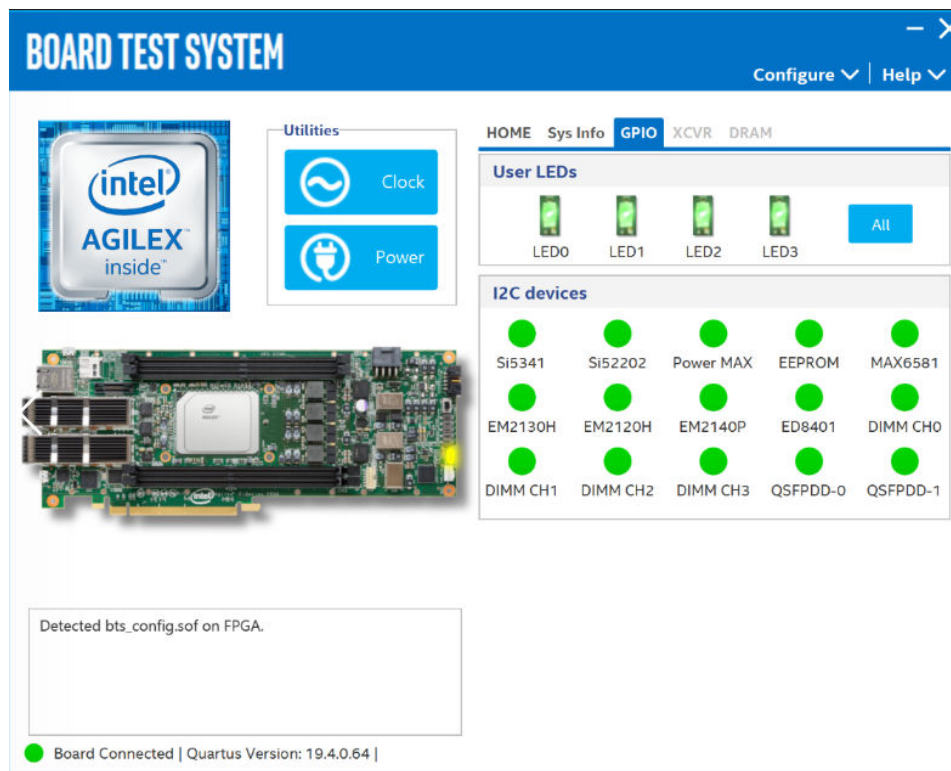
Qsys Memory Map

The Qsys memory map control shows the memory map of **bts_config.sof** design running on your board. This can be visible when **bts_config.sof** design is running on board.

4.1.3. The GPIO Tab

The **GPIO** Tab allows you to interact with all the general purpose user I/O components on your board. You can turn LEDs on or off and detect I2C target devices connection status.

Figure 6. The GPIO Tab



The following sections describe the controls on the GPIO tab.

I2C devices

The read-only I2C target devices control displays the connection status of devices which can be accessed by I²C bus. Unplug some devices to see the graphical display change.

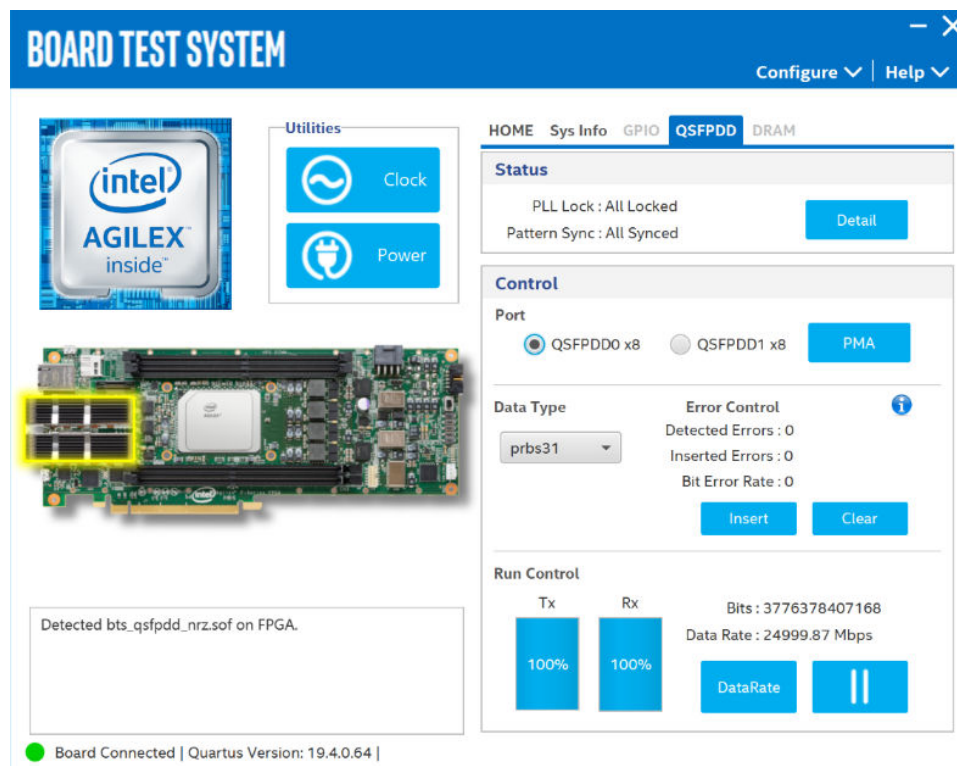
User LEDs

The User LEDs control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off.

4.1.4. The QSPFDD Tab

The **QSPFDD** Tab allows you to run transceivers QSPFDDx8 loopback tests on your board. You can run the test using either electrical loopback modules or optical fiber modules.

Figure 7. The QSPFDD Tab



The following sections describe controls in the QSPFDD tab.

Status

The Status control displays the following status information during the loopback test:

- **PLL lock:** Shows the PLL locked or unlocked state
- **Pattern Sync:** Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- **Detail:** Shows the PLL lock and pattern sync status.

Control

Use the following controls to select an interface to apply PMA settings, data type and error control:

- **QSFPDD0 x8**
- **QSFPDD1 x8**

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback:** Routes signals between the transmitter and the receiver.
- **VOD:** Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap:**
 - **Pre-tap 1:** Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
 - **Pre-tap 2:** Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
 - **Pre-tap 3:** Specifies the amount of pre-emphasis on the third pre-tap of the transmitter buffer.
 - **Post-tap 1:** Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.
- **Equalizer:** Specifies the RX tuning mode for receiver equalizer.

Figure 8. QSPFDD-PMA Setting

| Serial Loopback | | Pre-emphasis tap | | | | | |
|--------------------------|--------|------------------|-----------|-----------|-----------|------------|-----------|
| | | VOD | Pre-tap 1 | Pre-tap 2 | Pre-tap 3 | Post-tap 1 | Equalizer |
| <input type="checkbox"/> | All CH | 10 | 0 | 0 | 0 | 6 | Stop |
| <input type="checkbox"/> | CH0 | 10 | 0 | 0 | 0 | 6 | Stop |
| <input type="checkbox"/> | CH1 | 10 | 0 | 0 | 0 | 6 | Stop |
| <input type="checkbox"/> | CH2 | 10 | 0 | 0 | 0 | 6 | Stop |
| <input type="checkbox"/> | CH3 | 10 | 0 | 0 | 0 | 6 | Stop |
| <input type="checkbox"/> | CH4 | 10 | 0 | 0 | 0 | 6 | Stop |
| <input type="checkbox"/> | CH5 | 10 | 0 | 0 | 0 | 6 | Stop |
| <input type="checkbox"/> | CH6 | 10 | 0 | 0 | 0 | 6 | Stop |
| <input type="checkbox"/> | CH7 | 10 | 0 | 0 | 0 | 6 | Stop |

Data Type

The Data Type control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- **PRBS:** pseudo-random 7-bit sequences (default)
- **PRBS15:** pseudo-random 15-bit sequences
- **PRBS23:** pseudo-random 23-bit sequences
- **PRBS31:** pseudo-random 31-bit sequences

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the received bit stream.
- **Inserted Errors:** Displays the number of errors inserted into the transmit data stream.
- **Insert:** Insert a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- **Clear:** Resets the Detected Errors counter and Inserted Errors counter to zeros.

Run Control

- **TX and RX performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Start:** This control initiates the loopback tests.
- **Data Rate:** Displays the XCVR type and data rate of each channel.

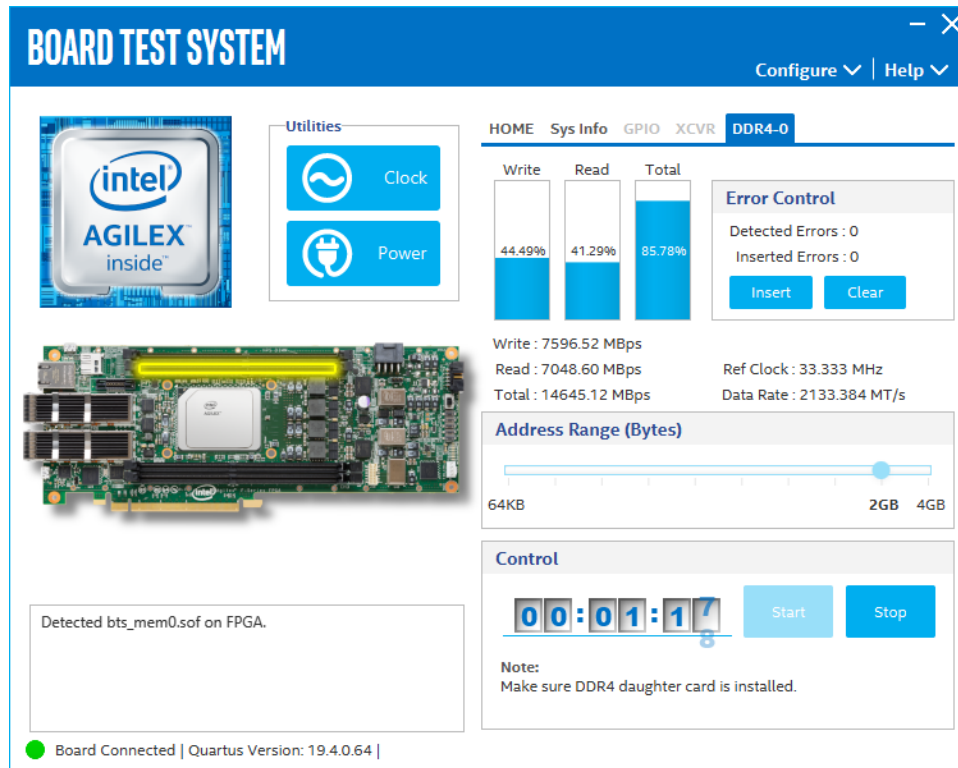
Figure 9. XCVR- Data Rate

| Channel | XCVR Type | Frequency |
|---------|-----------|---------------|
| 0 | GXE | 25000.06 Mbps |
| 1 | GXE | 25000.06 Mbps |
| 2 | GXE | 25000.06 Mbps |
| 3 | GXE | 25000.06 Mbps |
| 4 | GXE | 25000.06 Mbps |
| 5 | GXE | 25000.06 Mbps |
| 6 | GXE | 24999.94 Mbps |
| 7 | GXE | 25000.06 Mbps |

4.1.5. The DDR4-0 Tab

This tab allows you to read and write DDR4-0 memory on your board.

Figure 10. The DDR4-0 Tab



The following sections describe controls on this tab.

Start

Initiates DDR4 memory transaction performance analysis.

Stop

Terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write, Read and Total performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps), Read (MBps) and Total (MBps):** Show the number of bytes analyzed per second.
- **Data Bus:** 72 bits (8 bits ECC) wide, reference clock is 100 MHz and the frequency is 1066 MHz double data rate 2133 MT/s.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the hardware.
- **Inserted Errors:** Displays the number of errors inserted into the transaction stream.
- **Insert:** Inserts a one-word error into the transaction stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- **Clear:** Resets the detected error and inserted error counters to zeroes.

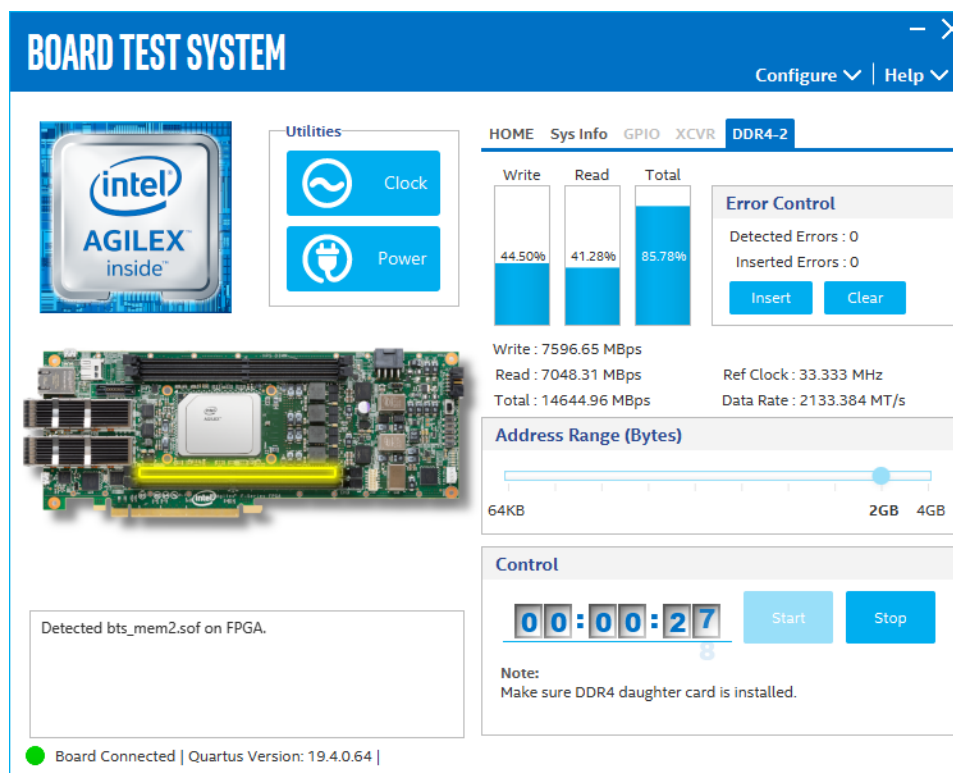
Number of Addresses to Read and Write

Determines the number of addresses to use in each iteration of reads and writes.

4.1.6. The DDR4-2 Tab

This tab allows you to read and write DDR4-2 memory on your board.

Figure 11. The DDR4-2 Tab



The following sections describe the controls on this tab.

Start

Initiates DDR4 memory transaction performance analysis.

Stop

Terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write, Read and Total performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps), Read (MBps) and Total (MBps):** Show the number of bytes analyzed per second.
- **Data Bus:** 72 bits (8 bits ECC) wide, reference clock is 100 MHz and the frequency is 1066 MHz double data rate 2133 MT/s.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the hardware.
- **Inserted Errors:** Displays the number of errors inserted into the transaction stream.
- **Insert:** Inserts a one-word error into the transaction stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- **Clear:** Resets the detected error and inserted error counters to zeroes.

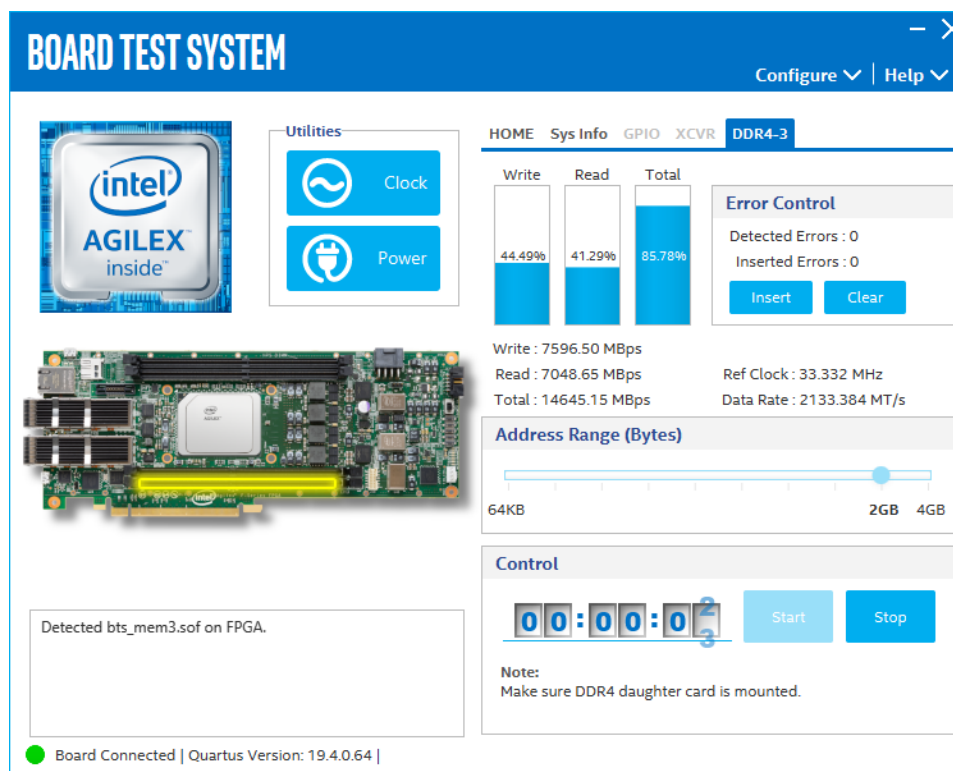
Number of Addresses to Read and Write

Determines the number of addresses to use in each iteration of reads and writes.

4.1.7. The DDR4-3 Tab

This tab allows you to read and write DDR4-3 memory on your board.

Figure 12. The DDR4-3 Tab



The following sections describe controls on the DDR4-3 tab.

Start

Initiates DDR4 memory transaction performance analysis.

Stop

Terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write, Read and Total performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps), Read (MBps) and Total (MBps):** Show the number of bytes analyzed per second.
- **Data Bus:** 72 bits (8 bits ECC) wide, reference clock is 100 MHz and the frequency is 1066 MHz double data rate 2133 MT/s.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the hardware.
- **Inserted Errors:** Displays the number of errors inserted into the transaction stream.
- **Insert:** Inserts a one-word error into the transaction stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- **Clear:** Resets the detected error and inserted error counters to zeroes.

Number of Addresses to Read and Write

Determines the number of addresses to use in each iteration of reads and writes.

4.2. BTS Test Areas

BTS checks for hardware fault before you can use the board. If one or more BTS test items fail, it implies either a wrong hardware setting or hardware fault on specific interface.

4.3. Identify Test Pass/Fail based on BTS GUI test status

DDR4 DIMMs

Plug the DDR4 DIMM module which is shipped alone with this development kit in **J1/J2/J3/J4**. BTS GUI only supports fabric memory interfaces namely DDR4 #0, #2 and #3

QSFPDD/QSFP28

Plug QSFPDD/QSFP28 loopback module in **J5/J6** before you configure QSFPDD NRZ example build through BTS GUI. The pseudo random bitstream (PRBS) traffic is running at 25 Gbps for NRZ build, but you can manually try it out PAM4 @50 Gbps with hard PRBS pattern with temporary PAM4 build in installer package.

5. Development Kits Hardware and Configuration

The Intel Agilex F-Series FPGA Development Kit only supports ASx4 configuration mode on the board. You need to change the hardware setting and/or re-program system images for the case.

The table below show which configuration mode it supports:

Table 5. Supported Configuration Mode

| SW1 [1:3] | MSEL [2:0] | Configuration Mode |
|------------|------------|----------------------------------|
| OFF/ON/ON | 001 | AS - Fast Mode (Default Setting) |
| OFF/OFF/ON | 011 | AS - Normal Mode |

5.1. Configure the FPGA and access HPS Debug Access Port by JTAG

JTAG access doesn't rely on **SW1** settings and system Intel MAX 10 image.

Plug the USB cable to **J13** or Intel FPGA Download Cable to **J14**.

Open Intel Quartus Prime programmer, system console to configure Intel Agilex FPGA SDM, system Intel MAX 10 and PCIe JTAG nodes.

Open Arm* Development Studio 5* (DS-5*) Intel SoC FPGA Edition to connect to and communicate with the HPS Debug Access Port (DAP) through the same JTAG interface.

Note: By default, HPS and FPGA SDM JTAG nodes are chained together internally. **SW4** bypass or enable both nodes at the same time.

If attestation and/or Black Key Provisioning (BKP) is enabled on the Intel Agilex device, you must use the updated SDM firmware and TCK guidelines (JTAG clock).

- You must update to the SDM firmware delivered with the Intel Quartus Prime Pro Edition version 21.3 and beyond.
- For the TCK pin, you must either leave the TCK pin unconnected, or connect the TCK pin to the VCCIO_SDM supply using a 10-kΩ pull-up resistor.

Note: The existing guidance in the *Intel Agilex Device Family Pin Connection Guidelines* to connect TCK to a 1-kΩ pull-down resistor is included for noise suppression. The change in guidance to a 10-kΩ pull-up resistor is not expected to affect the device functionally.

For more information about connecting the TCK pin, refer to the *Intel Agilex Device Family Pin Connection Guidelines*.

5.2. Configure the FPGA device by AS modes (Default Mode)

Default **SW1** setting and system Intel MAX 10 image support AS configuration mode. Power on and observe FPGA D13 Configuration LED behavior.

The Intel Agilex F-Series FPGA Development Kit also supports some HPS interfaces. You can demonstrate the following HPS functions on this board:

- 10/100/1000Mbps Ethernet PHY: U7_KSZ9031 and RJ45 connector J6
- USB UART for communication port: micro USB connector J10
- SD socket: J11
- eMMC on board: U16_MTFC8GAKAJCN-4M
- Mictor Connector for debug: J12

6. Custom Projects for the Development Kit

6.1. Add SmartVID settings in the QSF file

Intel Agilex FPGA assembled on this development kit enables SmartVID feature by default.

You must put the constraints listed below into your project QSF file to avoid Intel Quartus Prime from generating an error due to incomplete SmartVID settings.

Open your project QSF file and copy and paste constraint scripts listed below into the file. You must ensure that there are no other similar settings with different values.

```
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 47
set_global_assignment -name PWRMGT_SLAVE_DEVICE1_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE2_ADDRESS 00
set_global_assignment -name ACTIVE_SERIAL_CLOCK_AS_FREQ_100MHZ
set_global_assignment -name USE_PWRMGT_SCL SDM_IO14
set_global_assignment -name USE_PWRMGT_SDA SDM_IO11
set_global_assignment -name USE_CONF_DONE SDM_IO16
```

For Intel Agilex F-Series FPGA Development Kit (-3V version)

```
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE OTHER
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-12"
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE ON
```

For Intel Agilex F-Series FPGA Development Kit (-2V version)

```
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE ED8401
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-13"
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE OFF
```

6.2. Golden Top

You can use the Golden Top project as the starting point. It contains the constraints, pin locations, defines I/O standards, direction and general termination.

Note:

The Golden Top project is slightly different from the Intel Agilex F-Series Development Kit's -3V version to -2V version, please to refer to corresponding golden top project in installer package for more information.

7. Revision History

Table 6. Revision History of the Intel Agilex F-Series FPGA Development Kit User Guide

| Document Version | Changes |
|------------------|--|
| 2022.06.21 | Updated the <i>Configure the FPGA and access HPS Debug Access Port by JTAG</i> section to provide more details on the TCK guidelines if attestation or Black Key Provisioning is enabled. |
| 2022.02.21 | Updated the settings in the <i>For Intel Agilex F-Series FPGA Development Kit (-3V version)</i> subsection. |
| 2021.08.13 | <ul style="list-style-type: none"> Added Figure: <i>Power Tree Block Diagram (-2V Production Device)</i>. Updated Table: <i>Ordering Information</i> to include production device. Updated Table: <i>Power Sequence Groups</i> to include a note for VCCA_PLL power rail. Updated the description for <code>power_max10</code> directory in Table: <i>Installed Development Kit Directory Structure</i>. Updated the feature summary in the <i>Block Diagram</i> section. Updated the <i>Software and Driver Installation</i> section to include references to the <i>Intel Agilex FPGAs and SoCs Device Overview</i> and <i>Intel Agilex Device Data Sheet</i>. Updated the <i>A.1. Intel Agilex FPGA</i> section. Updated the <i>A.4. Memory Interfaces</i> section. |
| 2020.09.02 | Updated note in Box Contents on page 6 |
| 2020.07.09 | Board Test System (BTS) information added |
| 2020.05.15 | Engineering Silicon (ES) Release |
| 2020.02.11 | Initial Release |

A. Development Kit Components

A.1. Intel Agilex FPGA

Intel Agilex F-Series FPGA F2486A or F2486B

- Part Number:
 - AGFB014R24A2E3VR0 (-3V ES version)
 - AGFB014R24A2E2VR0 (-2V ES version)
 - AGFB014R24BE2V (-2V production version)
- F2486A or F2486B FBGA Package 55 mm x 42.5 mm
- 1473 KLEs
- 9200 18x19 Multipliers
- 36 Mb eSRAM
- 16 x 28 Gbps NRZ transceivers (E-tile)
- 16 x 17.4 Gbps NRZ transceivers (P-tile)
- 1x PCIe Gen4 x16 Hard IP blocks
- 1x 100G Ethernet MAC Hard IP blocks
- 768 GPIO

A.2. Configuration Support

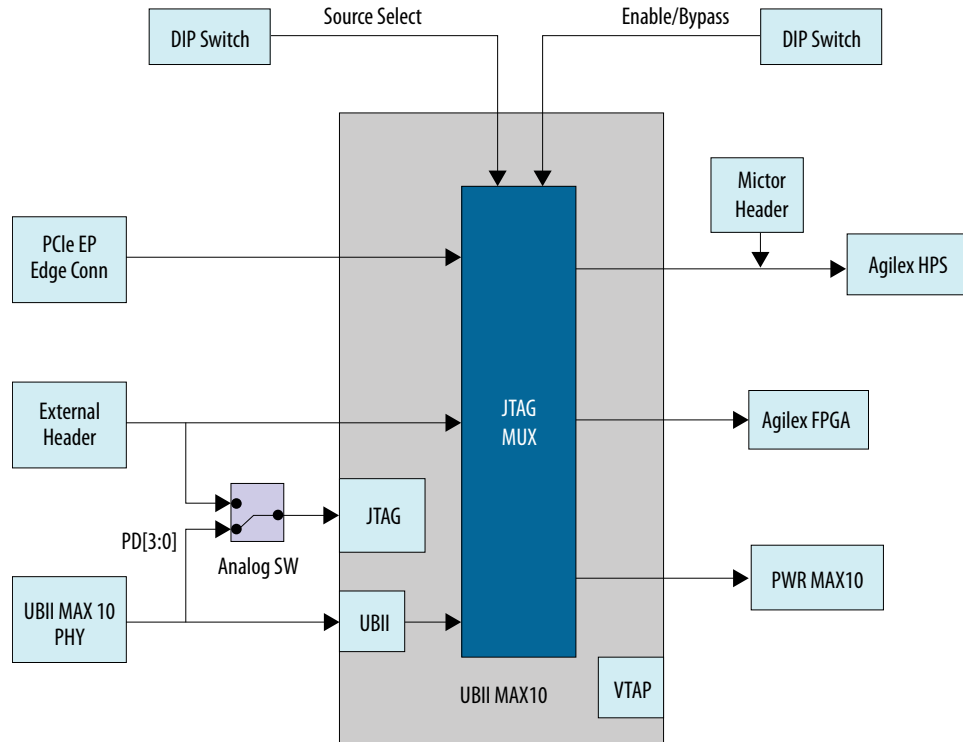
This development kit supports two configuration methods. A dip switch is used to select between JTAG only mode and ASx4 configuration mode by manipulating the MSEL pins.

1. ASx4 Mode. MT25QU02GCBB3E12-1SIT is a QSPI FLASH on board to support ASx4 configuration mode.
2. JTAG Mode.
 - a. JTAG via 10-pin header for connecting an Intel standard UB2/UB1 dongle. The header shall be a right angle shrouded type connector and it will be accessible through the PCIe bracket.
 - b. On-board Intel FPGA Download Cable

A.2.1. JTAG Chain and Header

The figure below shows the JTAG Chain connections. An option to bypass the Intel Agilex FPGA during board bring up is provided but not shown in the figure.

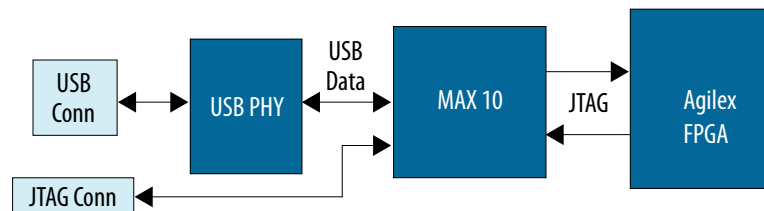
Figure 13. JTAG chain on the Development Kit



The JTAG chain allows programming of the Intel Agilex FPGA and the Intel MAX 10 CPLD devices using the external Intel FPGA Download Cable II dongle. The dongle can be used to program both the Intel Agilex FPGA and Intel MAX 10 CPLD via the external 2x5pin 0.1" programming header. This header uses a shrouded right angle connector and is designed to be accessible from the PCIe bracket side. This avoids having to remove the PC case to program the device when the board is installed in a closed system.

A.2.2. On-board Intel FPGA Download Cable II

Figure 14. Intel FPGA Download Cable II Block Diagram



The embedded Intel FPGA Download Cable II core for USB-based configuration of the Intel Agilex FPGA is implemented using a TYPE B USB connector, a CY7C68013A USB2 PHY device, and a Intel MAX 10 device. This allows for the configuration of the Intel Agilex FPGA using a USB cable directly connected to a PC running Intel Quartus Prime software without requiring the external Intel FPGA Download Cable II dongle.

This design converts USB data to interface with the Intel Agilex’s dedicated JTAG port. Four LEDs are provided to indicate Intel FPGA Download Cable II activity. Two of them monitor the JTAG data-in and data-out signals; the remaining two monitor System Console activity. The embedded Intel FPGA Download Cable is automatically disabled when an external Intel FPGA Download Cable II dongle is connected to the JTAG chain.

A.3. Clocks

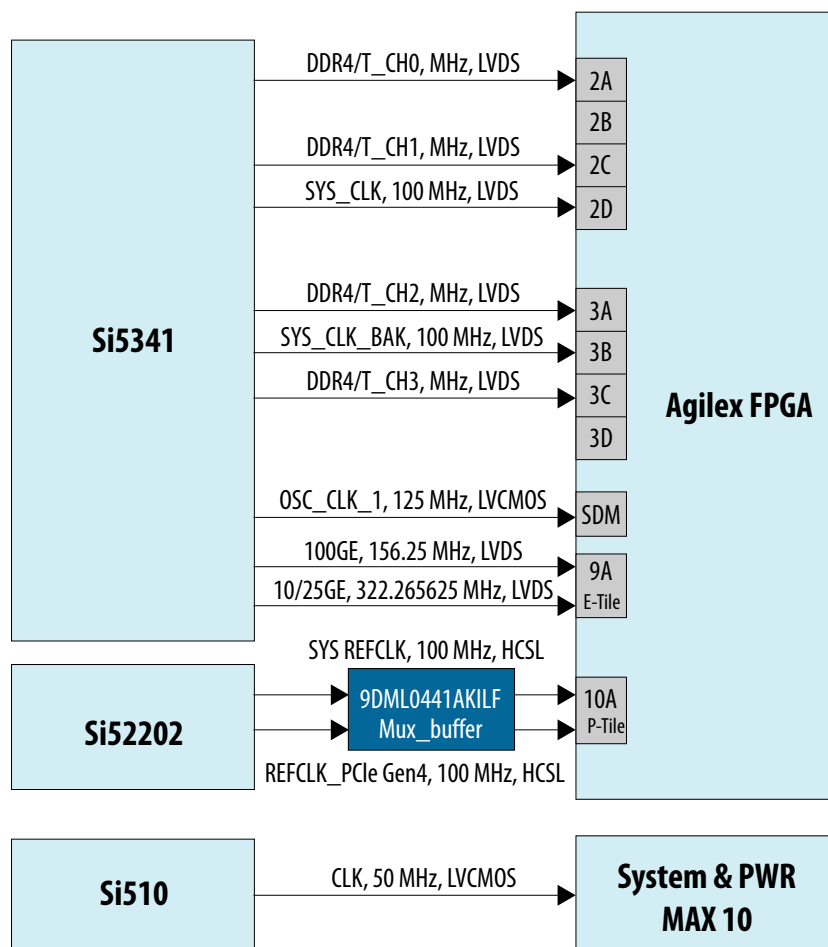
There are three clock devices in the Intel Agilex F-Series FPGA Development Kit: Si5341, Si52202 and Si510.

Si5341 provides most of clocks to the Intel Agilex FPGA including reference clocks for memory interfaces, QSFP-DD, and the FPGA SDM/fabric core.

Si52202 provides the dedicated reference clock as an local clock option of PCIe Gen4 by choosing in clock buffer 9DML0441AKILF. Another input of the clock buffer is from PCIe Golden Finger as a system clock of PCIe Gen4.

Si510 provides a 50 MHz clock to System Intel MAX 10 and Power Intel MAX 10.

Figure 15. Clocking in the Intel Agilex F-Series FPGA Development Kit



A.4. Memory Interfaces

The Intel Agilex F-Series FPGA Development Kit has four channels of 288 pin DDR4 DIMM 72-bit interfaces: DDR4 DIMM CH0, DDR4 DIMM CH1, DDR4 DIMM CH2 and DDR4 DIMM CH3.

DDR4 DIMM CH1 is designed for HPS dedicated applications. The other three memory channels are for FPGA general usage and support both DDR4 and DDR-T (Intel Optane™ PMem modules).

- DDR4 DIMM CH0 is located in FPGA Bank 3A and 3B. It supports both DDR4 and DDR-T modules.
- DDR4 DIMM CH1 is located in FPGA Bank 3C and 3D. It only supports DDR4 module.
- DDR4 DIMM CH2 is located in FPGA Bank 2A and 2B. It supports both DDR4 and DDR-T modules.
- DDR4 DIMM CH3 is located in FPGA Bank 2C and 2D. It supports both DDR4 and DDR-T modules.

A.5. Transceiver Interfaces

Two transceiver banks are present on the Intel Agilex F-Series FPGA Development Kit

- Bank 9A is used for two standard QSFP-DD optical modules (J5 and J6) and support up to 200 Gbps with hard IP for each QSFP-DD module
- Bank 10A is fully compliant with PCIe Gen4 x16 and are connected to the golden finger J7 in this PCIe add-in card

A.6. HPS Interface

The Intel Agilex FPGA Development Kit enables the HPS function and supports several HPS interfaces:

- RJ 45 supporting Ethernet 10/100/1000 Mbps by RGMII
- UART port by USB (Micro) connector
- Micro SD card socket
- Mictor Connector for HPS JTAG
- eMMC (8 GB x 8)

Note: Golden Software Reference Design for HPS (GSRD) is not currently available for this development kit.

A.7. General Input and Output

A.7.1. Switches

Table 7. SW1 Pin Connections

| SW1 Pin | Board Label | Function | Default Settings |
|---------|-------------|---------------------------------|------------------|
| SW1.1 | MSEL0 | Mode select 0 for configuration | OFF |
| SW1.2 | MSEL1 | Mode select 1 for configuration | ON |
| SW1.3 | MSEL2 | Mode select 2 for configuration | ON |

Table 8. SW2 Pin Connections

| SW2 Pin | Board Label | Function | Default Settings |
|---------|--------------------|--|------------------|
| SW2.1 | USB MAX JTAG SEL | ON = UBII MAX10 JTAG select External JTAG HEADER. OFF = UBII MAX10 JTAG select USB PHY. | OFF |
| SW2.2 | SI5341 Enable | ON = Disable SI5341's outputs OFF = Enable SI5341's outputs | OFF |
| SW2.3 | SI52202 Power Down | ON = Power down SI52202 OFF = Power up SI52202 | OFF |
| SW2.4 | UART Enable | ON = Disable UART OFF = Enable UART | OFF |

Table 9. SW3 Pin Connections

| SW3 Pin | Board Label | Function | Default Settings |
|---------|-------------------|---|------------------|
| SW3.1 | FPGA I2C Enable | ON = Isolate FPGA from main I2C chain. OFF = connect FPGA to main I2C chain. | OFF |
| SW3.2 | HPS I2C Enable | ON = Isolate HPS from main I2C chain. OFF = connect HPS to main I2C chain. | OFF |
| SW3.3 | Main PMBUS Enable | ON = Isolate power module of VCC_core from main I2Cchain. OFF= connect power module of VCC_core to main I2C chain. | OFF |
| SW3.4 | FPGAPMBUS Enable | ON = Isolate power module of VCC_core from SDMPMBUS. OFF= connect power module of VCC_core to SDM PMBUS. | OFF |

Table 10. SW4 Pin Connections

| SW4 Pin | Board Label | Function | Default Settings |
|---------|--------------------|--|------------------|
| SW4.1 | JTAG Input Source | ON = select PCIe edge as JTAG master when external JTAG is absent. OFF = select On-Board Intel FPGA Download Cable as JTAG master when external JTAG is absent. | OFF |
| SW4.2 | Power Max10 Bypass | ON = bypass Power Max10 in the JTAG chain. | ON |
| SW4.3 | Mictor Bypass | ON = bypass HPS in the JTAG chain. OFF = enable HPS in the JTAG chain. | ON |
| SW4.4 | FPGABypass | ON = bypass FPGA in the JTAG chain. OFF = enable FPGA in the JTAG chain. | OFF |

Table 11. SW5 Pin Connections

| SW5 Pin | Board Label | Function | Default Settings |
|----------------|-------------|---------------------|------------------|
| SW5.5 to SW5.4 | Power ON | Power ON the board | |
| SW5.5 to SW5.6 | Power OFF | Power OFF the board | Default |

Table 12. SW6 Pin Connections

| SW6 Pin | Board Label | Function | Default Settings |
|---------|---------------------|---------------------------------------|------------------|
| SW6.1 | PCIe EP Present x16 | ON = x16 select OFF = x16 deselect | ON |
| SW6.2 | PCIe EP Present x8 | ON = x8 select OFF = x8 deselect | OFF |
| SW6.3 | PCIe EP Present x4 | ON = x4 select OFF = x4 deselect | OFF |
| SW6.4 | PCIe EP Present x1 | ON = x1 select OFF = x1 deselect | OFF |

Table 13. SW7 Pin Connections

| SW7 Pin | Board Label | Function | Default Settings |
|---------|-------------|---|------------------|
| SW7.1 | SEL_A_B | ON = select SI52202 as clock source for PCIe Gen4 OFF = select PCIe edge as clock source for PCIe Gen4 | OFF |

A.7.2. Buttons

Table 14. Buttons on the Development Kit

| Board Reference | Type | Description |
|-----------------|---------------------------|--|
| S1 | HPS cold reset | Cold reset to HPS |
| S2 | CPU reset | Fabric core reset |
| S3 | PCIe reset | PCIe Hard IP reset |
| S4 | HPS warm reset | Warm reset to HPS |
| S5 | System Intel MAX 10 reset | On-board Intel FPGA Download Cable Reset |

A.7.3. LEDs

Table 15. LEDs on the Development Kit

| Board Reference | Schematic Signal Name | Intel Agilex FPGA Pin Number | I/O Standard |
|-----------------|-----------------------|------------------------------|--------------|
| D7 | FPGA_3V3_LED0 | C30 | 1.2V LVCMOS |
| D9 | FPGA_3V3_LED1 | A30 | 1.2V LVCMOS |
| D10 | FPGA_3V3_LED2 | D31 | 1.2V LVCMOS |
| D12 | FPGA_3V3_LED3 | B31 | 1.2V LVCMOS |
| D13 | FPGA_CONF_DONE | CA60 | 1.8V LVCMOS |
| D14 | FPGA_CVP_CONF_DONE | CA58 | 1.8V LVCMOS |
| D8 | PWR_LED_DR | B12(Max10_U30) | 3.3V LVCMOS |
| D11 | OVERTEMPn | K11(Max10_U30) | 3.3V LVCMOS |
| D21 | QSFDD0_LED0 | H19 | 1.2V LVCMOS |
| D22 (Bi-color) | QSFDD0_LED1 | F19 | 1.2V LVCMOS |
| | QSFDD0_LED2 | J20 | 1.2V LVCMOS |
| D23 | QSFDD1_LED0 | G20 | 1.2V LVCMOS |
| D24 (Bi-color) | QSFDD1_LED1 | H21 | 1.2V LVCMOS |
| | QSFDD1_LED2 | F21 | 1.2V LVCMOS |

A.8. Power

The power to the Intel Agilex F-Series FPGA Development Kit is provided from the PCIe slot (up to 75 W) and a secondary Auxiliary 2x4 PCIe power connector capable of an additional 150 W. The development kit does not power up until both the +12 V rails from the PCIe slot and the secondary auxiliary PCIe power connector are detected.

The development kit can also operate as a stand-alone bench top board for laboratory evaluation when an external 12 V power supply is connected to its 2x4 PCIe power connector. In this mode, the external supply will supply the total 240 W power for both the VCC core and other power rails on the board. An on-board slide switch is used to start the power for stand-alone mode.

Figure 17. Power Tree Block Diagram (-3V ES Version)

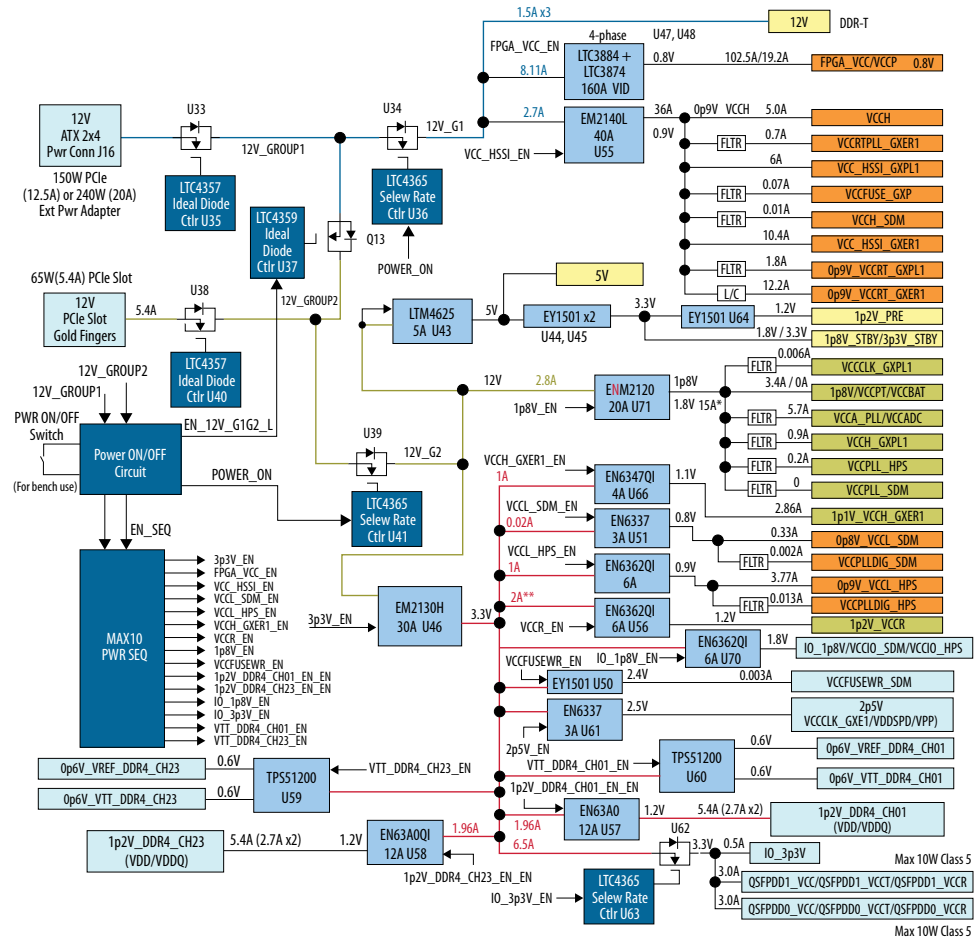


Table 16. Power Sequence Groups

| Group Number | Voltage Rails |
|--------------|--|
| Group1 | VCC, VCCP, VCCL_HPS, VCCL_SDM, VCCH, VCC_HSSI_GXER, VCC_HSSI_GXPL, VCCH, VCCRT_GXER, VCCRT_GXPL |
| Group2 | VCCPT, VCCBAT, VCCH_GXER, VCCH_GXPL, VCCA_PLL ⁽¹⁾ , VCCPLL_SDM, VCCADC, VCCPLL_HPS, VCCCLK_GXER |
| Group3 | VCCIO, VCCIO_SDM, VCCIO_HPS, VCCFUSEWR_SDM |

A.8.2. Power Measurement

Power measurement is provided for your evaluation to help correlate actual power versus EPE tool. Voltage measurements will be provided for eight FPGA power rails by using an 8-channel ADC embedded in Power Intel MAX 10. Current measurements used by the internal measurement on power modules which are digital power module and support PMBUS access.

The current for the four groups of power rails can be read through Power Monitor GUI. The power rails have the current monitor as below:

- VCC and VCCP
- VCCH, VCC_HSSI, VCCRT_GXER, and VCCRT_GXPL
- VCCPT, VCCH_GXPL, and VCCA_PLL
- 3.3V

A.8.3. Temperature Monitor

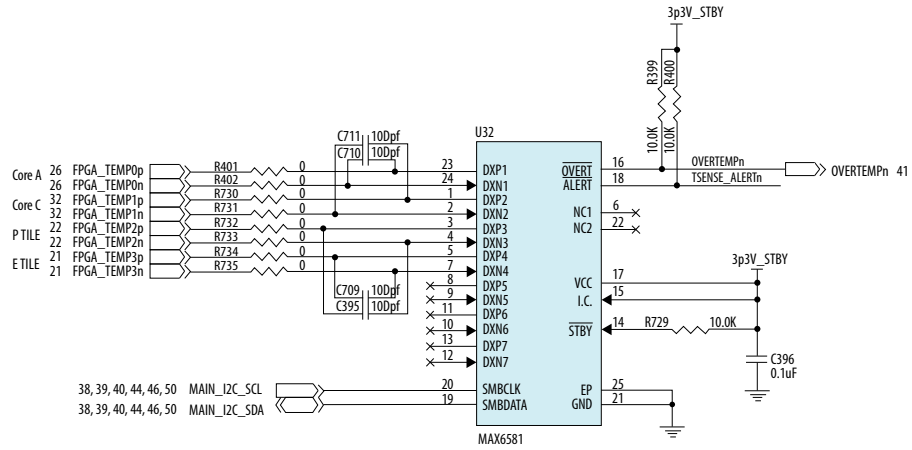
An 8-channel temperature sensor device, MAX6581, monitors the temperature of the Intel Agilex FPGA including fabric core and transceivers. Temperature monitoring of the board ambient is also done by MAX6581 with its embedded temperature sensor diode.

The MAX6581 connects to the Intel MAX 10 System Controller by a 2-wire I²C interface. Additionally, the `OVERTEMPn` and `ALERTn` signals from the MAX6581 are also routed to the Power Intel MAX 10 CPLD to allow it to immediately sense a temperature fault condition if the board gets too hot.

An over temperature warning LED (Red-colored) is connected to the Intel MAX 10 device so software can indicate a visual over temperature warning. This LED indicates the temperature fault condition and that the fan should be running. The fan will be controlled by the `OVERTEMP_OUT` signal from the Intel MAX 10 and can be controlled by software. Temperature fault set points can be programmed into the MAX6581 by the I²C bus through the System Intel MAX 10.

(1) VCCA_PLL is in Group 2 for ES device and Group 3 for production device.

Figure 19. MAX6581 Temperature Sensor Circuit



B. Additional Information

B.1. Safety and Regulatory Information



ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

B.1.1. Safety Warnings



Power Supply Hazardous Voltage

AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

| | | |
|---|-------------------------------|--|
| | WARNING | |
| | RISK OF ELECTRIC SHOCK | |
| <p>Connect only to a properly earth grounded outlet. Apparaten skall anslutas till jordat uttag när den ansluts till ett nätverk.</p> | | |

System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product will be attached is also connected to properly wired and grounded receptacles.

| | | |
|--|-------------------------------|--|
| | WARNING | |
| | RISK OF ELECTRIC SHOCK | |
| <p>Do not attempt to modify or use the supplied AC power cord if it is not the exact type and rating required.</p> | | |

Power Cord Requirements

The connector that plugs into the wall outlet must be a grounding-type male plug designed for use in your region. It must have marks showing certification by an agency in your region. The connector that plugs into the AC receptacle on the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord and do not use it with adapters.



Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

B.1.2. Safety Cautions

| | | |
|---|------------------------------|--|
| | CAUTION | |
| | Hot Surfaces and Sharp Edges | |
| Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp pins and edges on some boards. Contact should be avoided. | | |

Caution: Hot Surfaces and Sharp Edges. Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp edges on some boards. Contact should be avoided.

Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.



Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, the user is required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.



Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

B.2. Compliance Information

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

