TEXAS INSTRUMENTS

DAC7654
Evaluation Module

User's Guide

April 2004

Data Acquisition

SLAU130

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the supply voltage range of −5.25 V to 5.25 V and −15 V to 15 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 100°C. The EVM is designed to operate properly with certain components above 100°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Read This First

About This Manual

This user's guide describes the DAC7654 evaluation module. It covers the operating procedures and characteristics of the EVM board along with the device that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 – EVM Overview
- ❏ Chapter 2 – PCB Design and Performance
- ❏ Chapter 3 – EVM Operation

Information about Cautions and Warnings

This manual may contains cautions and warnings.

This is an example of a CAUTION statement.

A CAUTION statement describes a situation that could potentially damage this EVM board or your software or equipment.

This is an example of a WARNING statement.

A WARNING statement describes a situation that could potentially cause HARM to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477 – 8924 or the Product Information Center (PIC) at (972) 644 – 5580. When ordering, identify this manual by its title and literature number. Updated documents can also be obtained through our Web site at *www.ti.com.*

Data Sheets:	**Literature Number:**
DAC7654	SBAS263
OPA627	SBOS165

If you need Assistance

If you have questions about this or other Texas Instruments Data Converter evaluation modules, please feel free to e−mail the Data Converter Application Team at dataconvapps@list.ti.com. Please include in the subject heading the product you have questions or concerns with.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Trademark

Contents

Figures

Tables

Chapter 1

EVM Overview

This chapter provides an overview of the DAC7654 evaluation module (EVM) and instructions on setting up and using the EVM.

Topic **Page**

1.1 Features

This EVM features the DAC7654 digital-to-analog converters (DAC). It provides a quick and easy way to evaluate the functionality and performance of the high-resolution serial input quad DAC. The EVM provides the serial interface header to easily attach to any host microprocessor or TI DSP base system for communication.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The dc power supply for the digital section (V_{DD}) of this EVM is dedicated to 5 V via the J3−1 terminal or J6−10 terminal and is referenced to ground through the J3−2 and J6−5 terminals. The power for IOV_{DD} can be selected between 3.3 V and 5 V via the W23 jumper. If the 5 V is selected for IOV_{DD}, it is basically the same power as V_{DD}. The 3.3 V comes from J3−3 or J6−9 terminals and referenced to J3−2 and J6−5, respectively.

The dc power supply requirements for the analog section of this EVM are as follows: the V_{CC} and V_{SS} are typically ±15 V but can range from ±4.5 V minimum to ±18 V maximum and connect through J1−3 and J1−1, respectively, or through J6−1 and J6−2 terminals. The 5 VA connects through J6−3 and the −5 VA connects through J6−4. All of the analog power supplies are referenced to analog ground through J1−2 and J6−6 terminals.

The device under test (U1) analog power supply can be provided by ±5 VA (via J6−3 and J6−4). The V_{CC} supply source provides the positive rail of the external output operational amplifier, U2. The negative rail of U2 can be selected between V_{SS} and AGND via the W5 jumper. The external operational amplifier is installed as an option to provide output signal conditioning or for other output configurations.

CAUTION
To avoid potential damage to the EVM board, make sure the correct cables are connected to their respective terminals as labelled on the EVM board.
Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

1.2.2 Reference Voltage

The precision voltage reference up to ±2.5 V is internally generated by the DAC7654. This provides the DAC7654 voltage output range.

1.3 EVM Basic Functions

This EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC7654 DAC. Functional evaluation of the installed DAC device can be accomplished with the use of any microprocessor, TMS320™ DSP family or some sort of a waveform generator.

The headers J2 and P2 are connectors provided to allow the control signals and data required to interface a host processor or waveform generator with the DAC7654 EVM using a custom-built cable.

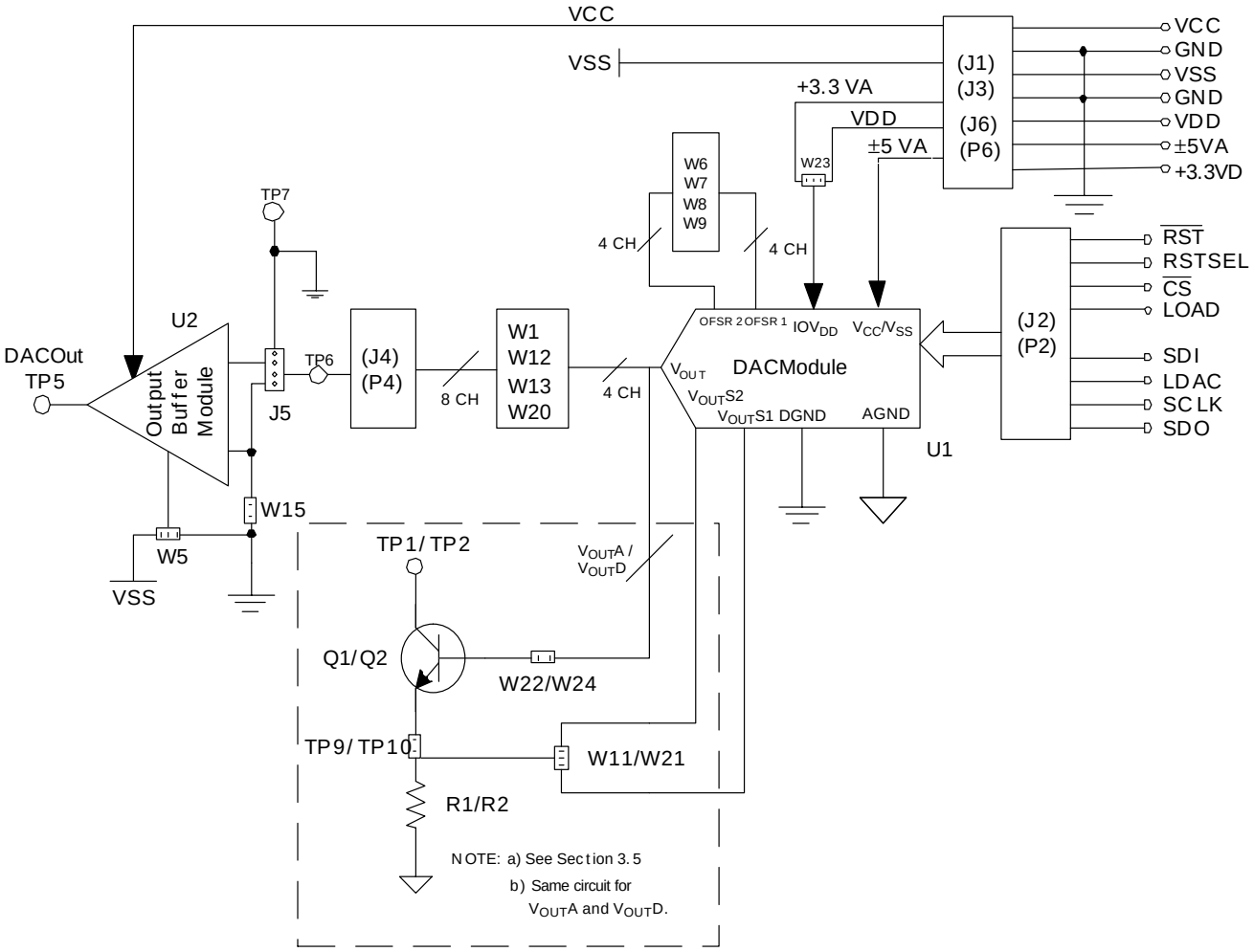
A specific adapter interface card is available for most of TI's DSP Starter Kit (DSK), and the card model depends on the type of the TI DSP Starter Kit to be used. To acquire the correct adapter interface card, be sure to specify the DSP that is used. This EVM can connect to and interface with an MSP430 based platform (HPA449) that uses the MSP430F449 microprocessor. For more details or information regarding the adapter interface card or the HPA449 platform, call Texas Instruments. or send email to dataconvapps@list.ti.com.

The DAC outputs are monitored through the selected pins of the J4 header connector. The outputs of U1 can be switched from their respective jumpers W2, W3, W4, and W10 for stacking purposes. Stacking allows a total of eight DAC channels if two DAC7654 EVMs are stacked.

In addition, the option of selecting one DAC output (from J4−2, 4, 6, and 8 only) to be connected to the output operational amplifier, U2, is also possible by using a jumper across the selected pins of J4. The output operational amplifier, U2, is configurable through J5, W5, and W15 for any desired waveform characteristic.

A block diagram of the DAC7654 EVM is shown in Figure 1−1.

Figure 1−1. DAC7654 EVM Block Diagram



Chapter 2

PCB Design and Performance

This chapter discusses the layout design of the PCB, describing the physical and mechanical characteristics of the EVM. It shows the resulting performance of the EVM, which can be compared to the device specification listed in the data sheet. The list of components used on the module is included in the bill of materials (BOM).

Topic **Page**

2.1 PCB Layout

The DAC7654 EVM is designed to demonstrate the performance quality of the installed DAC device under test, as specified in the data sheet. Careful analysis of the EVM's physical restrictions and factors that contributes to the EVM's performance degradation is the key to a successful design implementation. The attributes that contributes to the poor performance of the EVM can be avoided during the schematic design phase by properly selecting the correct components and correctly designing the circuit. The circuit should include adequate bypassing, identifying and managing the analog and digital signals, and knowing or understanding the components mechanical attributes.

The obscure part of the design lies particularly in the layout process. The main concern is primarily with the placement of components and the proper routing of signals. The bypass capacitors must be placed as close as possible to the pins, and the analog and digital signals should be properly separated from each other. The power and ground plane is important and should be carefully considered in the layout process. A solid plane is ideally preferred but sometimes impractical; so, when solid planes are not possible, a split plane does the job. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling the noise and other effects that otherwise contributes to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces but use the largest trace width possible in the design. These design practices discussed are seen in the following figures.

The DAC7654 EVM board is constructed on a four-layer printed-circuit board using a copper-clad FR−4 laminate material. The printed-circuit board has a dimension of 43,1800 mm (1.7000 inch) X 82,5500 mm (3.2000 inch), and the board thickness is 1,5748 mm (0.0620 inch). Figure 2−1 through Figure 2−7 show the individual artwork layers.

Figure 2−1. Top Silkscreen

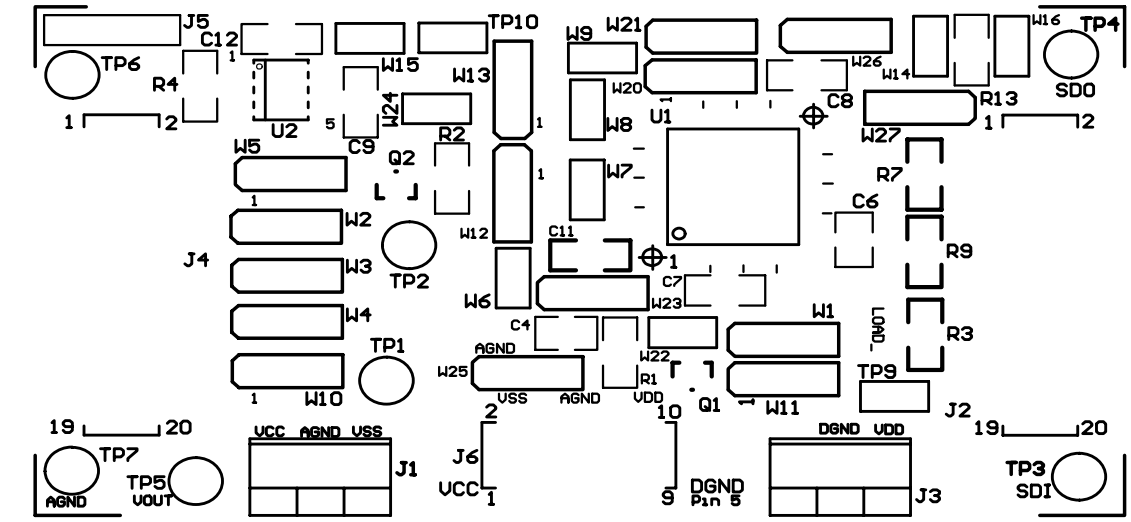


Figure 2−2. Layer 1 (Top Signal Plane)

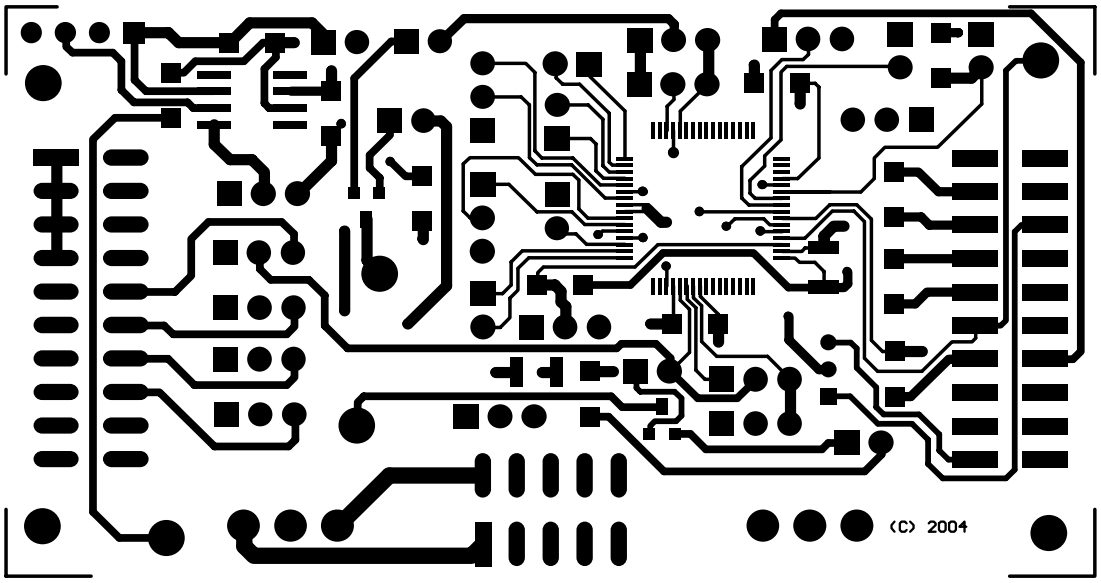


Figure 2−3. Layer 2 (Ground Plane)

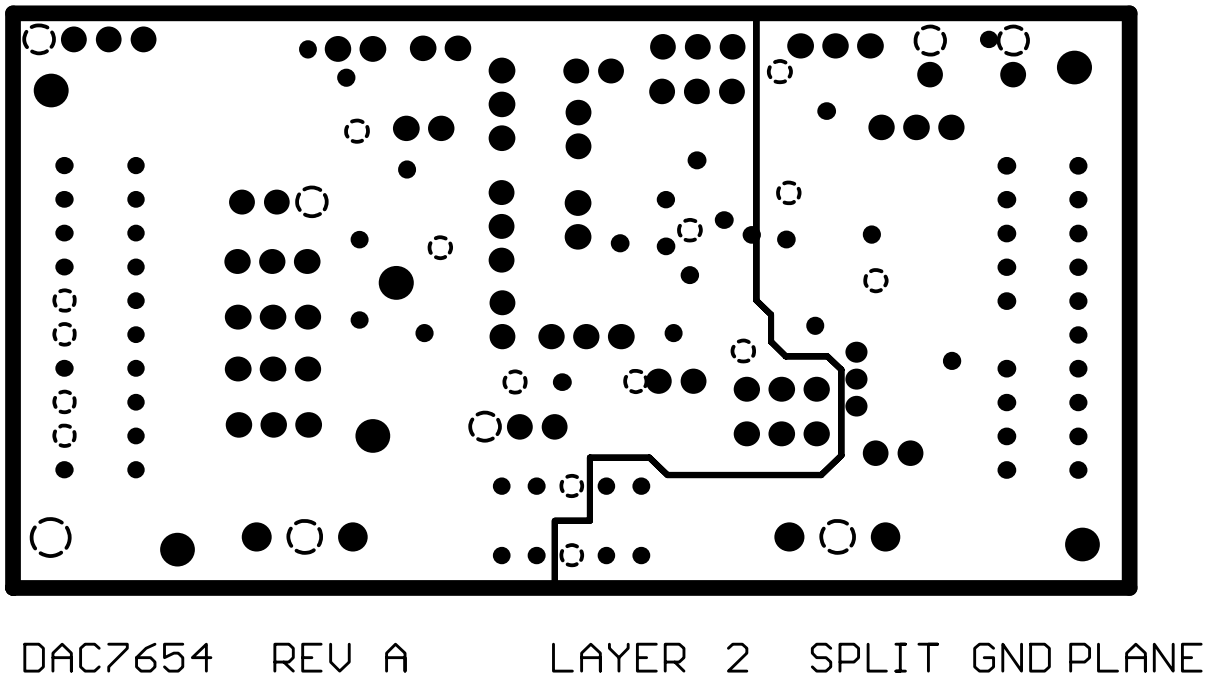


Figure 2−4. Layer 3 (Power Plane)

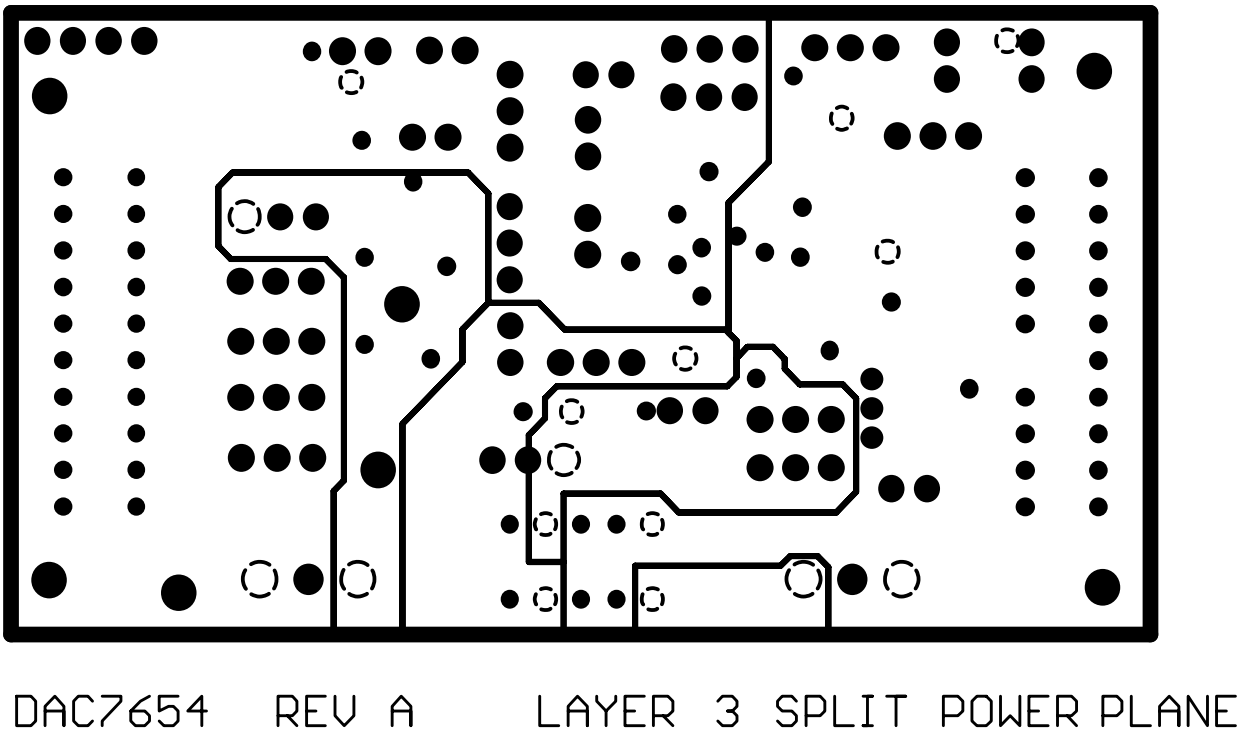


Figure 2−5. Layer 4 (Bottom Signal Plane)

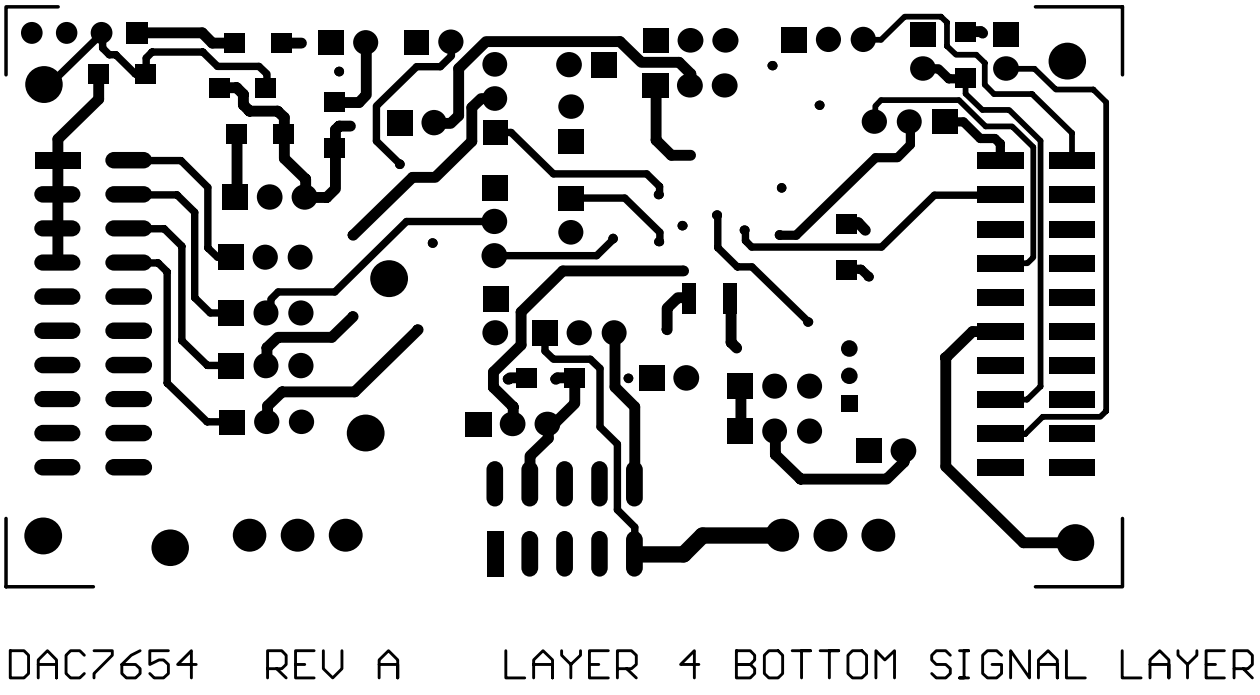


Figure 2−6. Bottom Silkscreen

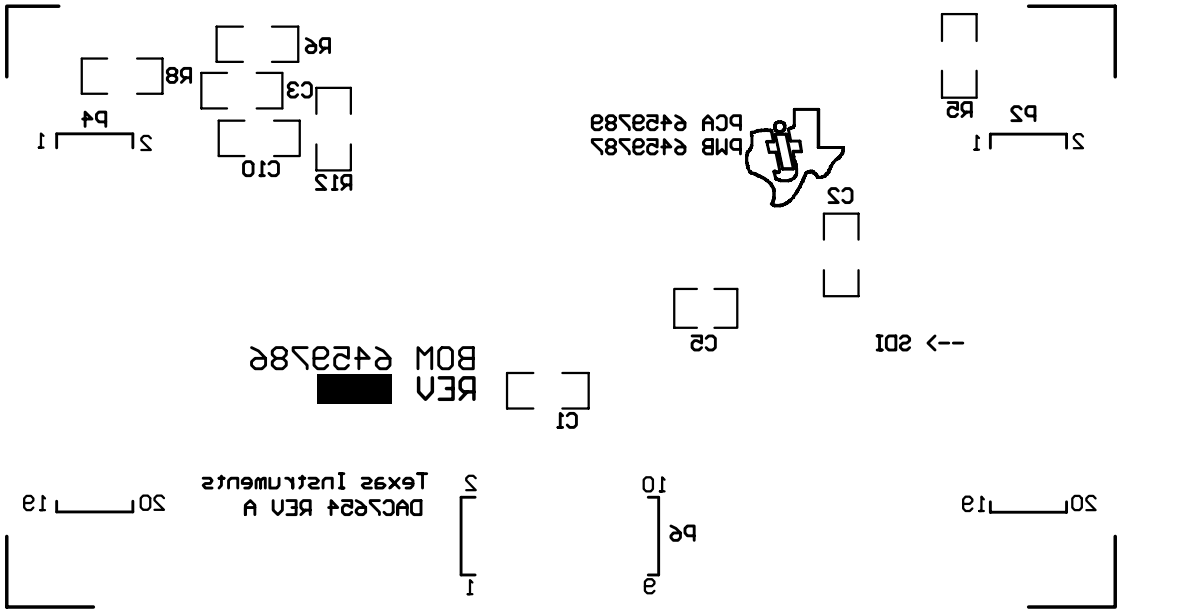
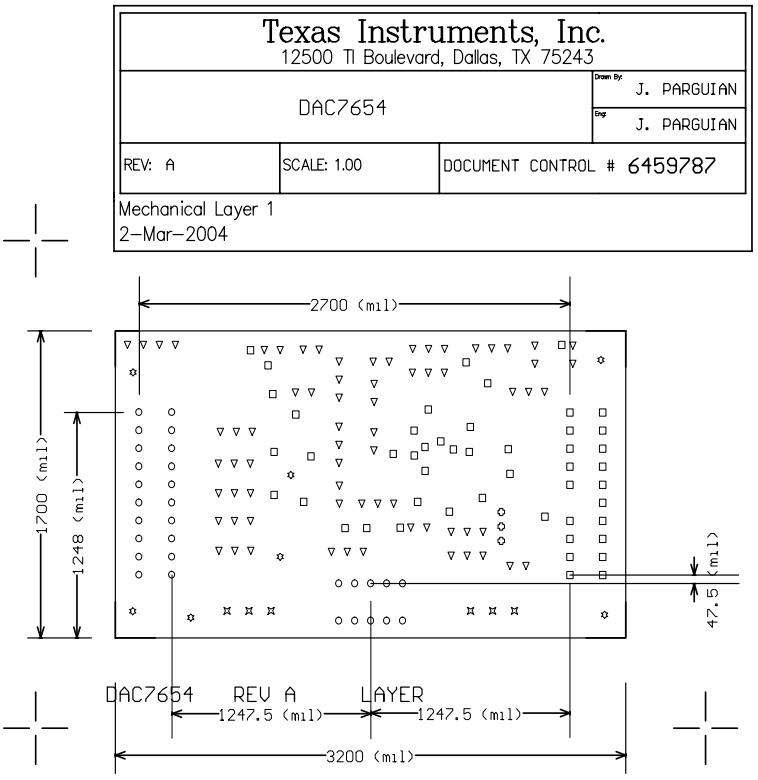


Figure 2−7. Drill Drawing



Notes:

1. PWB TO BE FABRICATED TO MEET OR EXCEED IPC−6012, CLASS 3 STANDARDS AND WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 3 - CURRENT REVISIONS
2. BOARD MATERIAL AND CONSTRUCTION TO BE UL APPROVED AND MARKED ON THE FINISHED BOARD.
3. LAMINATE MATERIAL: COPPER−CLAD FR−4
4. COPPER WEIGHT: 1oz FINISHED
5. FINISHED THICKNESS: .062 +/− .010
6. MIN PLATING THICKNESS IN THROUGH HOLES: .001"
7. SMOBC / HASL
8. LPI SOLDERMASK BOTH SIDES USING APPROPRIATE LAYER ARTWORK: COLOR = GREEN
9. LPI SILKSCREEN AS REQUIRED: COLOR − WHITE
10. VENDER INFORMATION TO BE INCORPORATED ON BACK SIDE WHENEVER POSSIBLE
11. MINIMUM COPPER CONDUCTOR WIDTH IS: 10 MILS MINIMUM CONDUCTOR SPACING IS: 8 MILS
12. NUMBER OF FINISHED LAYERS: 4

○	30	13mil	0.3302mm	PTH
□	49	15mil	0.381mm	PTH
◇	3	25mil	0.635mm	PTH
▽	71	37mil	0.9398mm	PTH
⌑	6	47.244mil	1.2mm	PTH
✡	7	62mil	1.5748mm	PTH
	166	Total		

2.2 EVM Performance

The EVM performance test is performed using a high density DAC bench test board, an Agilent 3458A digital multimeter, and a PC running the LABVIEW software. The EVM board is tested for all codes of the device under test (DUT) and is allowed to settle for 1 ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL results.

The parameters and results of the DAC7654 EVM characterization test are shown in Figure 2−8 to Figure 2−12.

Figure 2−8. DAC7654 EVM Test Parameters and Results in Bipolar Configuration

Figure 2−9. INL and DNL Characterization Graph of DAC7654 Channel A

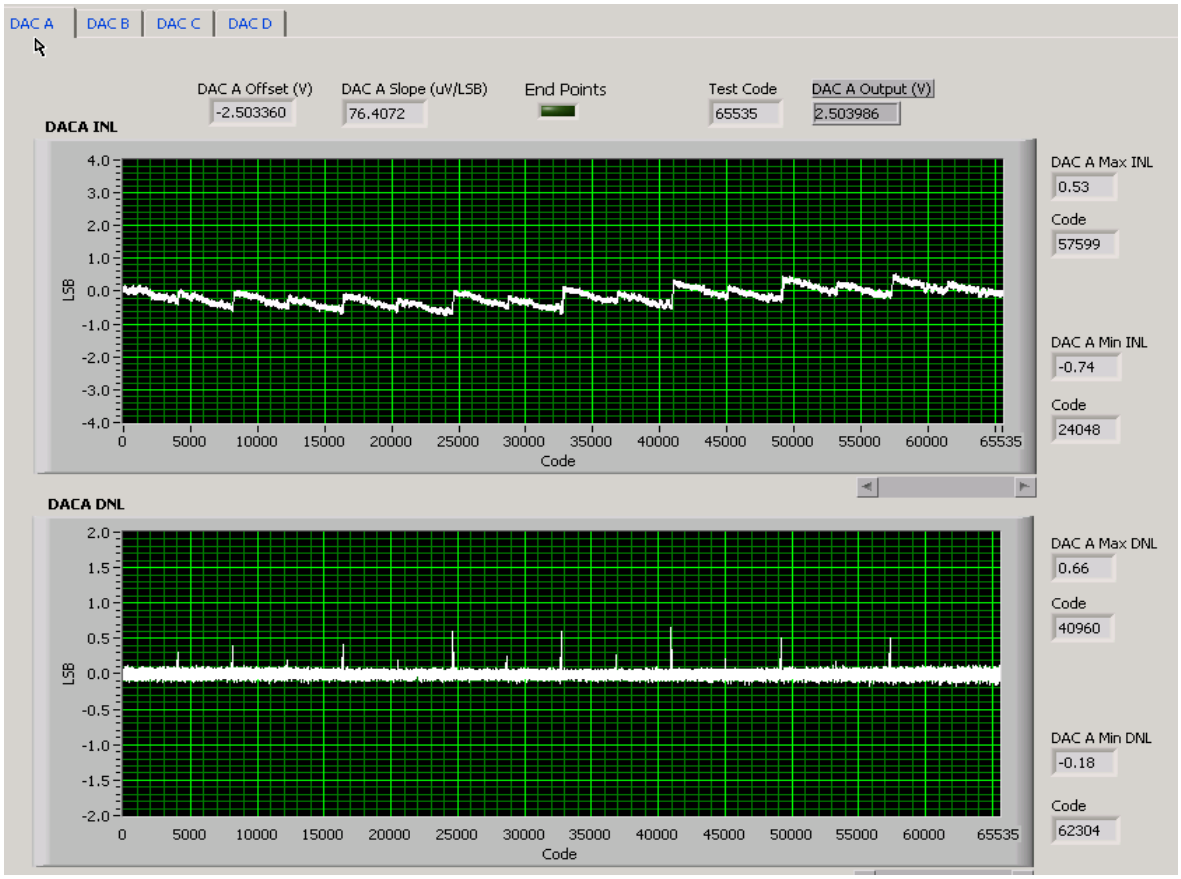


Figure 2−10. INL and DNL Characterization Graph of DAC7654 Channel B

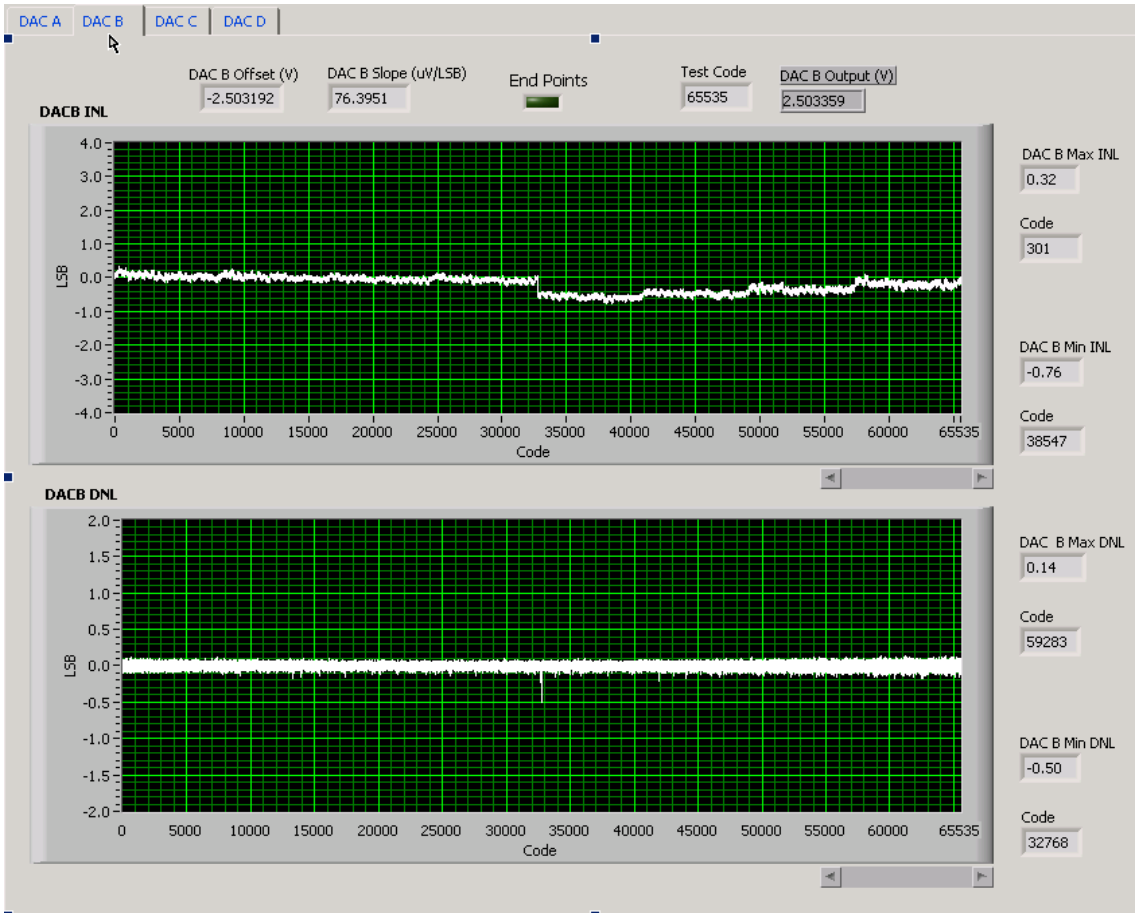


Figure 2−11. INL and DNL Characterization Graph of DAC7654 Channel C

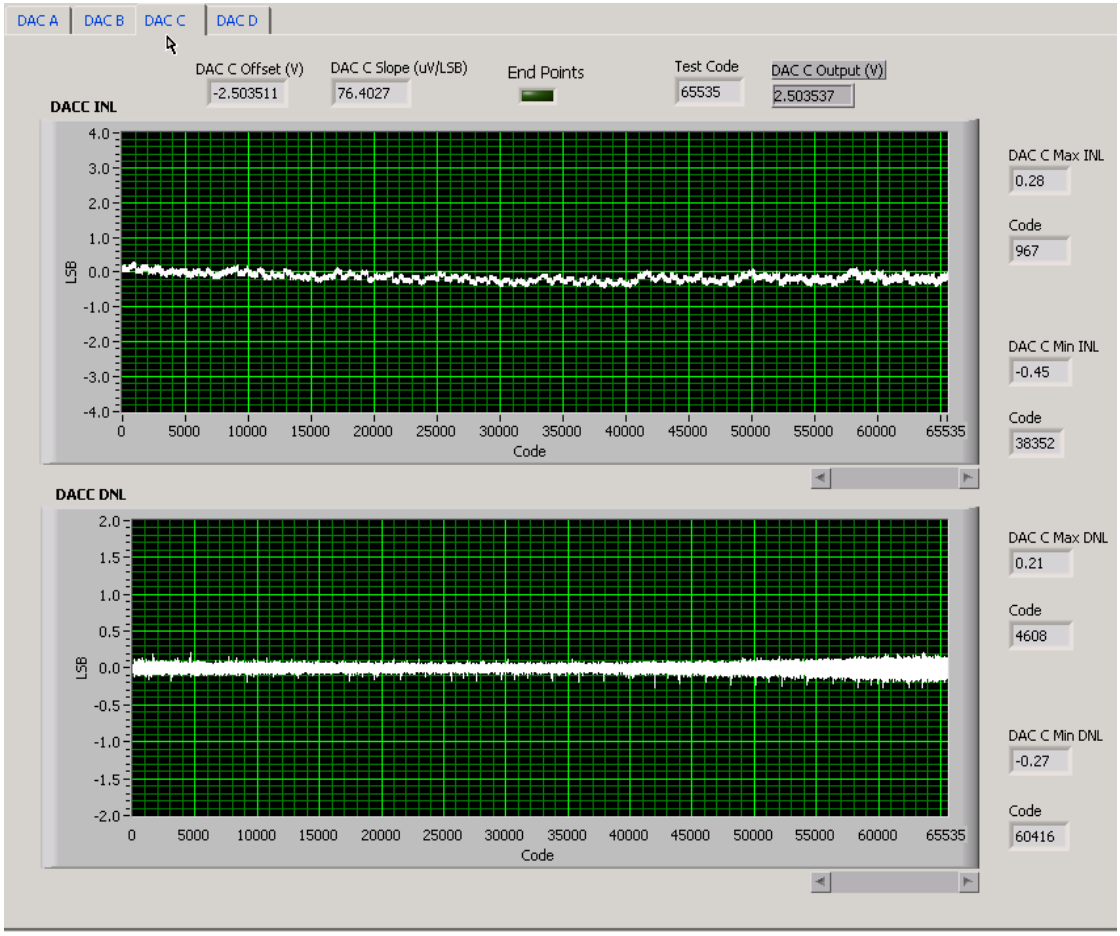
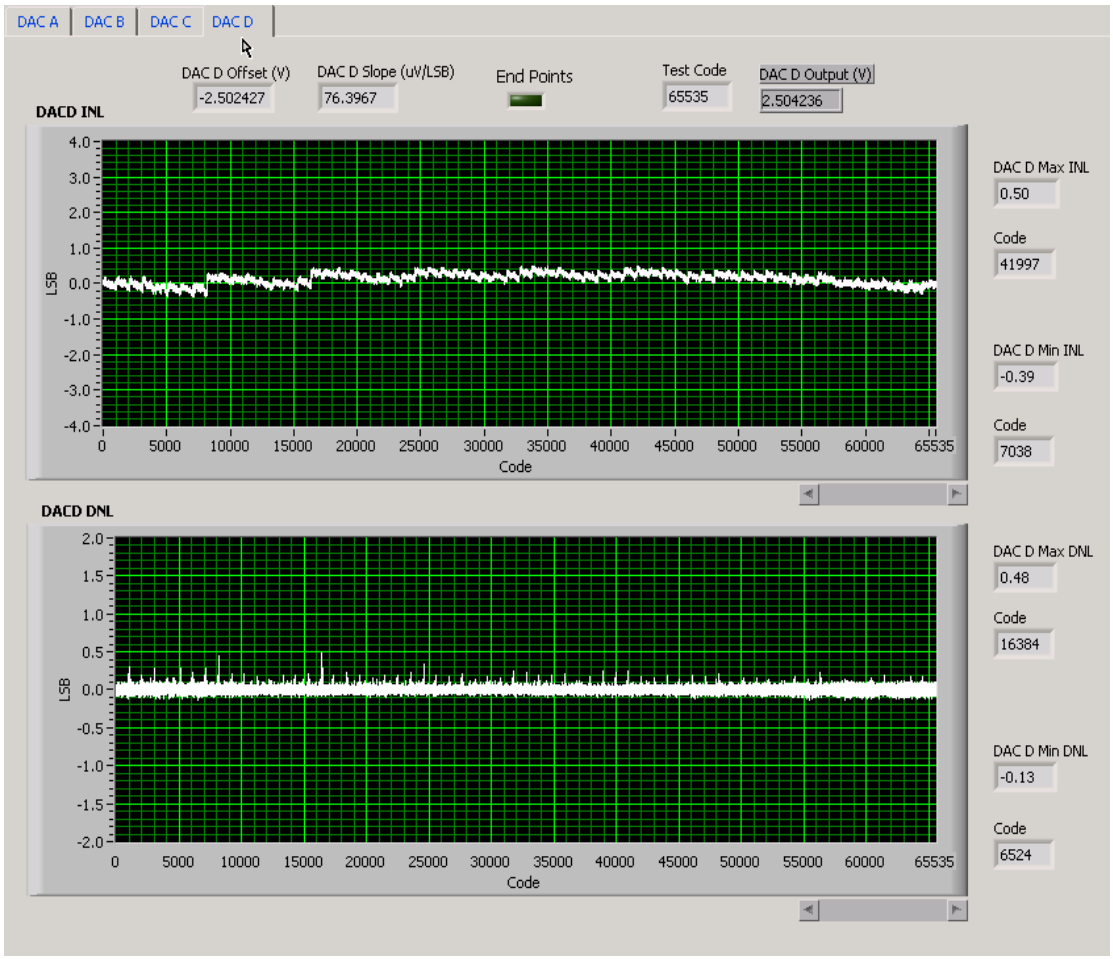


Figure 2−12. INL and DNL Characterization Graph of DAC7654 Channel D



2.3 Bill of Materials

Table 2−1. DAC7654 Bill of Materials

Item #	Qty	Designator	Manufacturer	Part Number	Description
1	2	C9 C10	Panasonic	ECUV1H103KBM	0.01µF, 1206 Multilayer Ceramic Capacitor
2	5	C1 C2 C7 C8 C11	Panasonic	ECJ3VB1C104K	0.1µF, 1206 Multilayer Ceramic Capacitor
3	1	C12	Panasonic	ECUV1H102JCH	1nF, 1206 Multilayer Ceramic Capacitor
4	3	C4 C5 C6	Kemet	C1210C106K8PAC	10µF, 1210 Multilayer Ceramic X5R Capacitor
5	1	C3	Kemet	ECU−V1H471KBM	470pF, 50V, 1206 Multilayer Ceramic Capacitor SMD
6	3	R3 R7 R9	Panasonic	ERJ−8GEY0R00V	0 Ohm, 1/4W 1206 Chip Resistor
7	2	R1 R2	Panasonic	ERJ−8ENF1240V	124 Ohms, 1%, 1/8W 1206 Chip Resistor
8	1	R4	Panasonic	ERJ−8GEYJ101V	100 Ohms, 1/4W 1206 Chip Resistor
9	1	R8	Panasonic	ERJ−8GEYJ202V	2K Ohms, 5%, 1/4W 1206 Chip Resistor
10	4	R5 R6 R12 R13	Panasonic	ERJ−8ENF1002V	10K Ohms, 1/4W 1206 Chip Resistor
11	2	Q1 Q2	Panasonic	2SC24050RL	FET Transistor NPN 35VCEO 50MA MINI−3P
12	1	J5	Molex	22−03−2041	4 Position Jumper_ .1” spacing
13	1	J6	Samtec	TSM−105−01−T−DV	5X2X0.1 10−pin 3A Isolated Power Socket
14	2	J2 J4	Samtec	TSM−110−01−S−DV−M	10X2X.1, 20 Pin .025”sq SMT Socket
15	2	J1 J3	On−Shore Technology	ED555/3DS	3−Pin Terminal Connector
16	1	U1	Texas Instruments	DAC7654IDGS	16−bit, Quad Voltage Output, Serial Input DAC, PQFP−64
17	1	U2	Texas Instruments	OPA627AU	8−SOP(D) Precision Op Amp
18	7	TP1 TP2 TP3 TP4 TP5 TP6 TP7	Mill−Max	2348−2−01−00−00−07−0	Turret Terminal Test Point
19	2	P2 P4 (see Note)	Samtec	SSW−110−22−S−D−VS−P	20PIN .025”sq SMT Terminal Strips
20	1	P6 (see Note)	Samtec	SSW−105−22−F−D−VS−K	3A Isolated 10−pin Power Header
21	9	W6 W7 W8 W9 W14 W15 W16 W22 W24	Molex	22−03−2021	2 Position Jumper_ .1” spacing
22	15	W1 W2 W3 W4 W5 W10 W11 W12 W13 W20 W21 W23 W25 W26 W27	Molex	22−03−2031	3 Position Jumper_ .1” spacing

Note: P2, P4 & P6 parts are not shown in the schematic diagram. All the P designated parts are installed in the bottom side of the PC Board opposite the J designated counterpart. Example, J2 is installed on the topside while P2 is installed in the bottom side opposite of J2. Not all parts listed in the BOM are installed in the EVM as they are specific to the DUT installed.

Chapter 3

EVM Operation

This chapter covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC and interfacing the EVM to a host processor.

See the specific DAC data sheet, as listed in the *Related Documentation from Texas Instruments* section of this user's guide, for more information about the DAC serial interface and other related topics.

The EVM board is factory tested and configured to operate in the bipolar output mode.

Topic **Page**

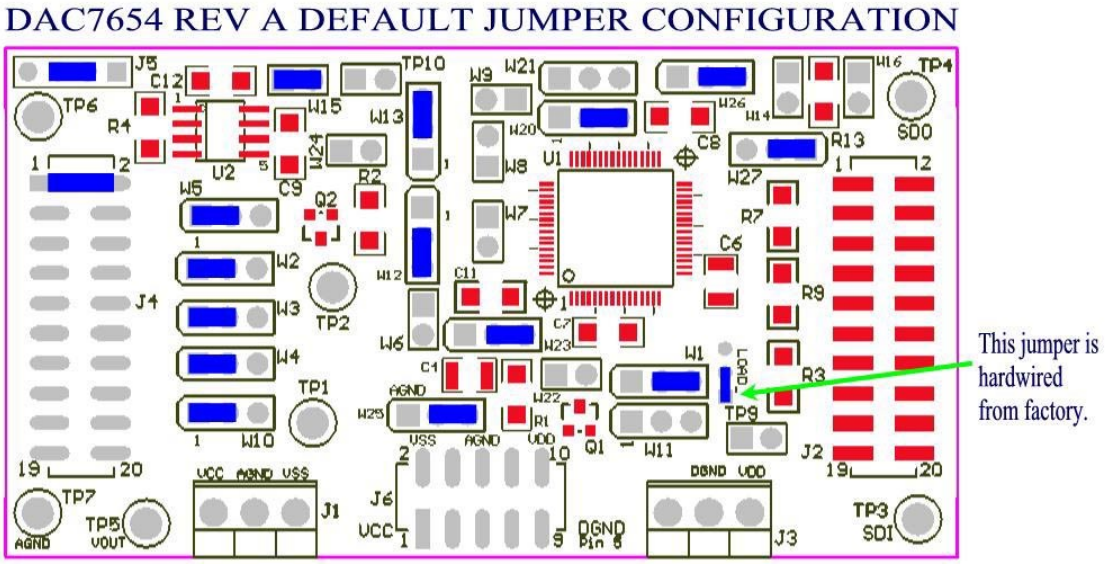
3.1 Factory Default Setting

The EVM board is set to its default configuration from the factory as described in Table 3−1 to operate in bipolar ±2.5-V output operation. The following default jumper settings are shown in Figure 3−1.

Table 3−1. DAC7654 EVM Jumper Default Configuration

Reference	Jumper Position	Function
W1	2−3	Dual supply operation
W2	1−2	DAC output A ($V_{OUT}A$) is routed to J4−2
W3	1−2	DAC output B ($V_{OUT}B$) is routed to J4−4
W4	1−2	DAC output C ($V_{OUT}C$) is routed to J4−6
W5	1−2	Negative supply rail of U2 operational amplifier is supplied with V_{SS}
W6	OPEN	Dual supply operation
W7	OPEN	Dual supply operation
W8	OPEN	Dual supply operation
W9	OPEN	Dual supply operation
W10	1−2	DAC output D ($V_{OUT}D$) is routed to J4−8
W11	OPEN	Use for digitally controlled current source application only.
W12	2−3	Dual supply operation
W13	2−3	Dual supply operation
W14	OPEN	Reset pin high
W15	CLOSED	U2 operational-amplifier configuration jumper set to 2x gain
W16	OPEN	RSTSEL configuration jumper; RSTSEL = 1
W20	2−3	Dual supply operation
W21	OPEN	Use for digitally controlled current source application only.
W22	OPEN	Use for digitally controlled current source application only.
W23	2−3	IOV_{DD} = 5 V
W24	OPEN	Use for digitally controlled current source application only.
W25	2−3	Dual supply operation (V_{SS} = −5 V)
W26	2−3	GPIO0 drives LDAC signal
W27	1−2	$\overline{CS}$ signal routed to drive CS_ line of U1
TP9	OPEN	Use for digitally controlled current source application only.
TP10	OPEN	Use for digitally controlled current source application only.
J4	1−2	DAC output A ($V_{OUT}A$) is routed through LPF onto J5−2 connector
J5	2−3	Selected DAC output connected to output operational amplifier, U2

Figure 3−1. DAC7654 EVM Default Jumper Setting



3.2 Host Processor Interface

The host processor drives the DAC; therefore, the DAC proper operation depends on the successful configuration between the host processor and the EVM board. In addition, a properly written code is required to operate the DAC.

A custom cable can be made specific to the host interface platform. The EVM allows interface to the host processor through J2 header connector for the serial control signals and the serial data input. The output can be monitored through the J4 header connector.

An interface adapter card is also available for a specific TI DSP starter kit as well as an MSP430 based microprocessor as mentioned in Chapter 1 of this manual. Using the interface card alleviates the tedious task of building customize cables and allows easy configuration of a simple evaluation system.

This DAC EVM interfaces with any host processor capable of handling serial communication protocols or the popular TMS320™ DSP family. For more information regarding the serial interface of the particular DAC installed, see the specific DAC data sheet, as listed in the *Related Documentation from Texas Instruments* section of this user's guide.

3.3 EVM Stacking

Stacking the EVM is possible if there is a need to evaluate two DAC7654 to yield a total of eight channel outputs. A maximum of two DAC7654 EVMs are allowed because the output terminal, J4, dictates the number of DAC channels that can be connected without the outputs colliding. Table 3−2 shows how the DAC output channels are mapped into the output terminal, J4, with respect to the jumper positions of W2, W3, W4, and W10.

Table 3−2. DAC7654 Output Channel Mapping

Reference	Jumper Position	Function
W2	1−2	DAC7654 output A ($V_{OUT}A$) is routed to J4−2.
	2−3	DAC7654 output A ($V_{OUT}A$) is routed to J4−10.
W3	1−2	DAC7654 output B ($V_{OUT}B$) is routed to J4−4.
	2−3	DAC7654 output B ($V_{OUT}B$) is routed to J4−12.
W4	1−2	DAC7654 output C ($V_{OUT}C$) is routed to J4−6.
	2−3	DAC7654 output C ($V_{OUT}C$) is routed to J4−14.
W10	1−2	DAC7654 output D ($V_{OUT}D$) is routed to J4−8.
	2−3	DAC7654 output D ($V_{OUT}D$) is routed to J4−16.

3.4 The Output Operational Amplifier

The EVM includes an optional signal-conditioning circuit for the DAC output through an external operational amplifier, U2. Only one DAC output channel can be monitored at any given time for evaluation because the odd-numbered pins (J4−1 to J4−7) are tied together. The output operational amplifier is set to unity gain configuration by default. Nevertheless, the raw outputs of the DAC can be probed through the even pins of J4, the output terminal, which also provides mechanical stability when stacking or plugging into any interface card. In addition, it provides easy access for monitoring up to eight DAC channels when stacking two DAC7654 EVMs together (see Section 3.3).

The inverting input of U2 can be tied to AGND (via W15) or the DAC output (by shorting pins 1 and 2 of the J5 header) or to any voltage source through J5−1.

The following sections describe the different configurations of the output amplifier, U2.

3.4.1 Unity Gain Output

The buffered output configuration is used to prevent loading the DAC, though it may present some slight distortion because of the feedback resistor and capacitor. The user can tailor the feedback circuit to closely match the desired wave shape by removing R6 and C12 and replacing them with the desired values. If desired, the user can remove R6 and C12 and solder a 0-Ω resistor in replacement of R6.

Table 3−3 shows the jumper setting for the unity gain configuration of the DAC external output buffer in unipolar or bipolar supply mode.

Table 3−3. Unity Gain Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W15	OPEN	OPEN	Disconnect the inverting input of operational amplifier, U2, from AGND.
W5	2−3	1−2	Negative rail of operational amplifier is tied to AGND or powered by V_{SS}.

3.4.2 Output Gain of Two (Default Configuration)

Table 3−4 below shows the proper jumper settings of the EVM for the 2x gain output of the DAC.

Table 3−4. Gain of Two Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W15	CLOSED	CLOSED	Inverting input of the output operational amplifier, U2, is connected to AGND to set for a gain of 2.
W5	2−3	1−2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U2, for bipolar supply mode, or ties it to AGND for unipolar supply mode.

3.5 Digitally Programmable Current Source Application

A digitally programmable current-source circuit is added for the convenience of the users. Any DAC channels of the DAC7654 can be selected to generate the voltage output that can be connected to the external operational amplifier, U2. The external operational amplifier is used to perform this operation because of the closed-loop configuration, internal to the device, of each DAC7654 output amplifier. Therefore, the external operational amplifier, U2, is used to drive the transistor for this type of operation. The selected transistor (Q1 or Q2) is placed within the loop (i.e., U2 must be configured for open-loop gain) to implement a digitally programmable, unidirectional current source, as shown in Figure 3−2.

To operate the DAC7654 for the digitally programmable current source application, the DAC7654 must be configured for the unipolar mode of operation. The DAC7654 channels A and D are the only ones shown in the table, but any DAC channel works.

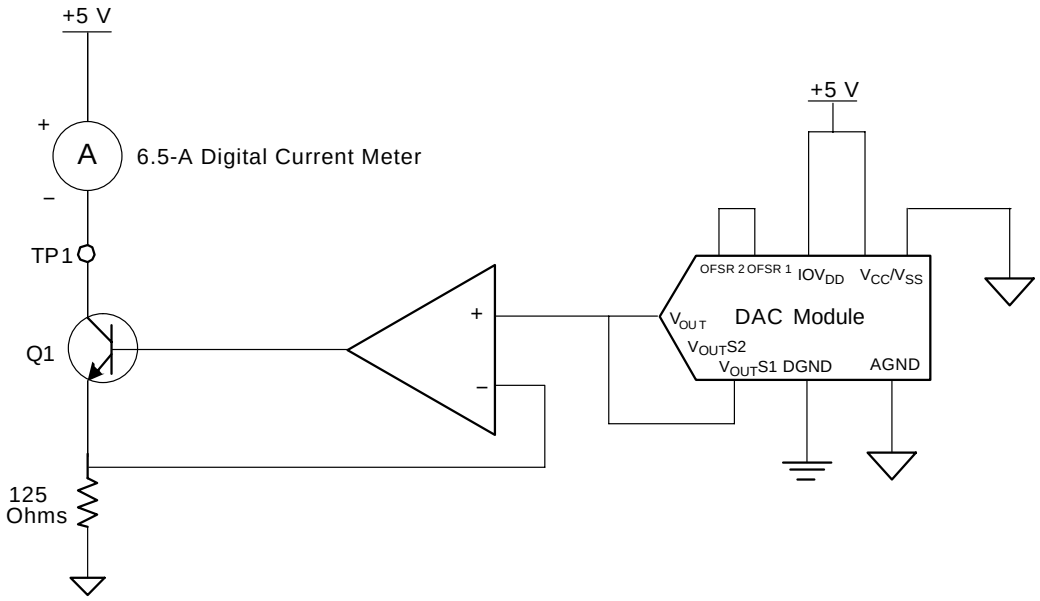
The resistor R6 and the capacitor C12 should be disconnected from the circuit of U2 for open-loop configuration. The resistor R4 can be replaced with a 0-Ω resistor or a jumper wire. An extra wire is needed to connect TP5 to W22−2 or W24−2, as well as the J5−1 to W11−2 or W21−2.

See Table 3−5 for the setup configuration.

Table 3−5. Digitally Programmable Current Source Configuration

Reference	Jumper Setting		Function
	VOUTA	VOUTD	
W25	1−2	1−2	VSS is tied to AGND
W1	1−2	N/A	VOUTS1A is feedback to VOUTA
W20	N/A	1−2	VOUTS1D is feedback to VOUTD
W6	CLOSED	N/A	DAC A is configured for unipolar mode of operation
W9	N/A	CLOSED	DAC D is configured for unipolar mode of operation
W2	1−2	N/A	DAC A is connected to J4−2
W10	N/A	1−2	DAC A is connected to J4−8
J4	1−2	7−8	DAC A or DAC D is connected to J5−2
J5	2−3	2−3	DAC A or DAC D is routed to the positive input of U2
TP9	CLOSED	CLOSED	Transistor, Q1, loop is closed
TP10	CLOSED	CLOSED	Transistor, Q2, loop is closed

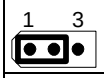
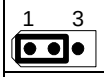
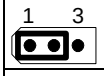
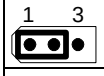
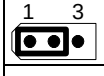
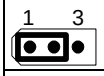
Figure 3−2. Digitally Programmable Current Source

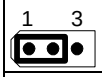
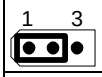
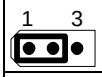
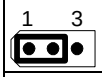
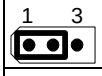


3.6 Jumper Settings

Table 3−6 shows the function of each specific jumper setting of the EVM.

Table 3−6. Jumper Setting Function

Reference	Jumper Setting	Function
W1		V_{OUT}SENSE1A is a feedback to V_{OUT}A.
		V_{OUT}SENSE2A is a feedback to V_{OUT}A.
W2		Routes V_{OUT}A to J4−2.
		Routes V_{OUT}A to J4−10.
W3		Routes V_{OUT}B to J4−4.
		Routes V_{OUT}B to J4−12.
W4		Routes V_{OUT}C to J4−6.
		Routes V_{OUT}C to J4−14.
W5		Negative supply rail of the output operational amplifier, U2, is powered by V_{SS} for bipolar operation.
		Negative supply rail of the output operational amplifier, U2, is tied to AGND for unipolar operation.
W6		OFSR1A and OFSR2A are disconnected for bipolar output mode
		OFSR1A and OFSR2A are connected for unipolar output mode
W7		OFSR1B and OFSR2B are disconnected for bipolar output mode
		OFSR1B and OFSR2B are connected for unipolar output mode
W8		OFSR1C and OFSR2C are disconnected for bipolar output mode
		OFSR1C and OFSR2C are connected for unipolar output mode
W9		OFSR1D and OFSR2D are disconnected for bipolar output mode
		OFSR1D and OFSR2D are connected for unipolar output mode
W10		Routes V_{OUT}D to J4−8.
		Routes V_{OUT}D to J4−16.

W11		V_{OUT}SENSE1A is used for 4−20 mA drive
		Digitally programmable current source application is not used
		V_{OUT}SENSE2A is used for digitally programmable current source
W12		V_{OUT}SENSE1B is a feedback to V_{OUT}B
		V_{OUT}SENSE2B is a feedback to V_{OUT}B
W13		V_{OUT}SENSE1C is a feedback to V_{OUT}C
		V_{OUT}SENSE2C is a feedback to V_{OUT}C
W14		RST is pulled up via R5 resistor
		RST is pulled down to DGND and device is held on reset state
W15		Configures output operational amplifier, U2, to unity gain output.
		Connects AGND to the inverting input of the output operational amplifier, U2
W16		RSTSEL is pulled up via R13 resistor and device resets to mid-scale on power up
		RSTSEL is pulled down to DGND and device resets to minimum-scale on power up
W20		V_{OUT}SENSE1D is a feedback to V_{OUT}D
		V_{OUT}SENSE2D is a feedback to V_{OUT}D
W21		V_{OUT}SENSE1D is used for digitally programmable current source operation
		Digitally programmable current source application is not used
		V_{OUT}SENSE2D is used for digitally programmable current source
W22		V_{OUT}A is not connected for digitally programmable current source operation
		V_{OUT}A is connected for digitally programmable current source operation
W23		3.3-V analog supply is selected for IOV_{DD} of the DUT
		5-V analog supply is selected for IOV_{DD} of the DUT

W24		$V_{OUT}D$ is not connected for digitally programmable current source operation
		$V_{OUT}D$ is connected for digitally programmable current source operation
W25		V_{SS} of the DUT is connected to AGND for unipolar mode of operation
		V_{SS} of the DUT is connected to −5-V supply for bipolar mode of operation
W26		GPIO4 is used to drive the LDAC signal of the DUT
		GPIO0 is used to drive the LDAC signal of the DUT
W27		$\overline{CS}$ is used to drive the $\overline{CS}$ signal of the DUT
		FSX is used to drive the $\overline{CS}$ signal of the DUT
TP9		Disconnects external load for digitally programmable current source operation
		Connects external load for digitally programmable current source operation
TP10		Disconnects external load for digitally programmable current source operation
		Connects external load for digitally programmable current source operation

Legend:  Indicates the corresponding pins that are shorted or closed.

3.7 Schematics

Figure 3−3. DAC7654 Schematic

The EVM schematic is on the following page.

Revision History		
REV	ECN Number	Approved

DAC_VOUT
J4
W2 VoutA
W3 VoutB
W4 VoutC
W10 VoutD

TP1
VoutA W22 Q1 NPN TRANSISTOR
VoutS1A W11 TP9
VoutS2A R1 125

TP2
VoutD W24 Q2 NPN TRANSISTOR
VoutS1D W21 TP10
VoutS2D R2 125

+5VA
C7 0.1µF
C5 10µF
-5VA
C4 10µF
C1 0.1µF

U1 DAC7654

4	VCC	IOVDD	19
1	NC	VDD	18
2	NC	VDD	29
9	NC	RST	26
6	VoutS1A	RSTSEL	27
5	VoutA	NC	14
7	VoutS2A	NC	48
64	OFSR1A	NC	47
63	OFSR2A	NC	43
10	NC	NC	21
59	VoutS1B	CS	22
58	VoutB	SCLK	23
60	VoutS2B	SDI	42
61	OFSR1B	NC	25
62	OFSR2B	LDAC	24
11	NC	LOAD	41
54	VoutS1C	NC	40
55	VoutC	NC	39
53	VoutS2C	NC	38
52	OFSR1C	NC	37
51	OFSR2C	NC	36
12	NC	NC	20
45	VoutS1D	SDO	35
46	VoutD	NC	34
44	VoutS2D	NC	33
49	OFSR1D	NC	32
50	OFSR2D	NC	31
13	NC	NC	30
3	VSS	NC	16
56	GNDR	NC	15
57	GNDR	DGND	28
8	AGND	DGND	17

W1 VoutS1A VoutA VoutS2A
W6 OFSR1A OFSR2A
W12 VoutS1B VoutB VoutS2B
W7 OFSR1B OFSR2B
W13 VoutS1C VoutC VoutS2C
W8 OFSR1C OFSR2C
W20 VoutS1D VoutD VoutS2D
W9 OFSR1D OFSR2D
W25

+3.3VD
W23 IOVDD
C11 0.1µF
VDD
C6 10µF
C2 0.1µF
C8 0.1µF
R5 10K
R13 10K
W14 RST RSTSEL
W16 CS
W27 CE FSX
W26 LDAC LOAD
GPIO4
GPIO0
SDO

P2

CS	1	2	GPIO0
SCLK	3	4	JP4
CLKR	5	6	GPIO1
FSX	7	8	JP8
FSR	9	10	JP10
SDI	11	12	JP12
DR	13	14	GPIO4
RST	15	16	JP16
RSTSEL	17	18	JP18
GPIO5	19	20	JP20

R3 0 TP3
LOAD LOAD_

J2

CS	1	2	GPIO0
R7 0 SCLK	3	4	JP4
CLKR	5	6	GPIO1
R9 0 FSX	7	8	JP8
FSR	9	10	JP10
SDO	11	12	JP12
DR	13	14	GPIO4
RST	15	16	JP16
RSTSEL	17	18	JP18
GPIO5	19	20	JP20

TP4

TP7
J5 4X1X.1
VCC
C9 0.01µF
U2 Op Amp
R4 100 TP5
VSS
W5
C10 0.01µF
R6 10K
C12 1nF
W15
R12 10K

TP6
DAC_VOUT R8 2K
C3 470pF

+3.3VD VD2 +5VA VCC VSS -5VA VD1 VDD
J6

1	2		
3	4		
5	6		
7	8		
9	10		

J1 1 2 3 VSS VCC
J3 1 2 3 VDD +3.3VD

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: DAC7654			
Engineer: J. PARGUIAN	DOCUMENTCONTROL # 6459788		REV: A
Drawn By:			
FILE: DAC7654_RevA.Sch	DATE: 17-Mar-2004	SIZE:	SHEET: 1 OF: 1