CY2DL15110

1:10 Differential LVDS Fanout Buffer with Selectable Clock Input

Features

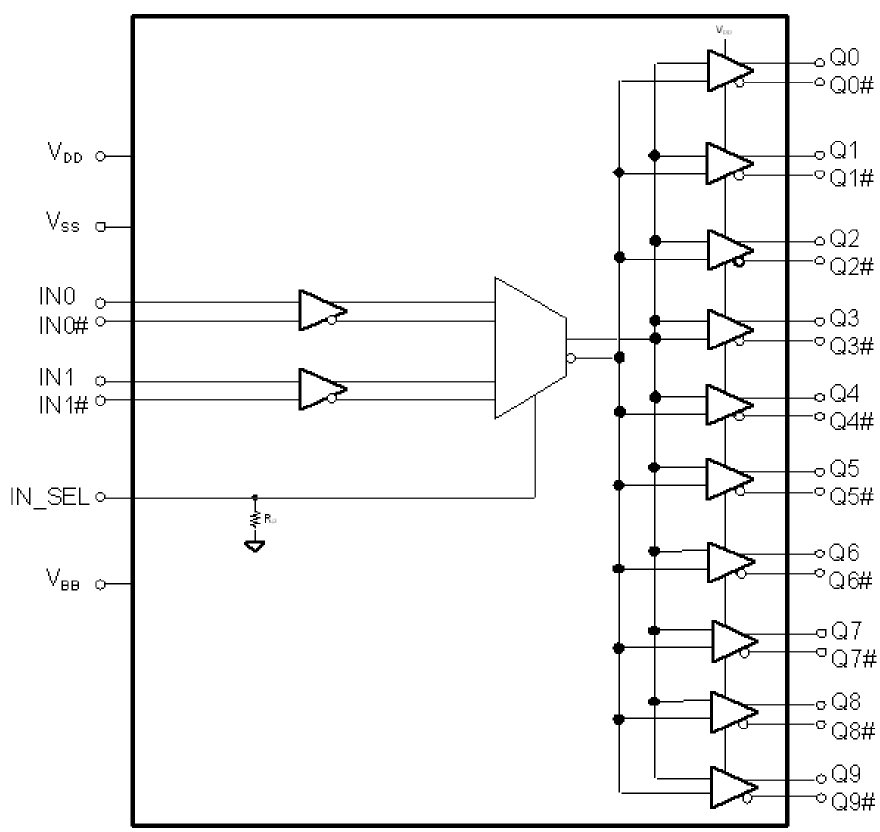
- Select one of two differential (LVPECL, LVDS, HCSL, or CML) input pairs to distribute to 10 LVDS output pairs
- Translate any single-ended input signal to 3.3 V LVDS level with resistor bias on INx# input
- 40-ps maximum output-to-output skew
- 600-ps maximum propagation delay
- 0.11-ps maximum additive RMS phase jitter at 156.25 MHz (12-kHz to 20-MHz offset)
- Up to 1.5-GHz operation
- 32-pin thin quad flat pack (TQFP) package
- 2.5-V or 3.3-V operating voltage [1]
- Commercial and industrial operating temperature range

Functional Description

The CY2DL15110 is an ultra-low noise, low skew, low propagation delay 1:10 LVDS fanout buffer targeted to meet the requirements of high speed clock distribution applications. The CY2DL15110 can select between two separate differential (LVPECL, LVDS, HCSL, or CML) input clock pairs using the IN_SEL pin. The device has a fully differential internal architecture that is optimized to achieve low additive jitter and low skew at operating frequencies of up to 1.5 GHz.

For a complete list of related documentation, click here.

Logic Block Diagram

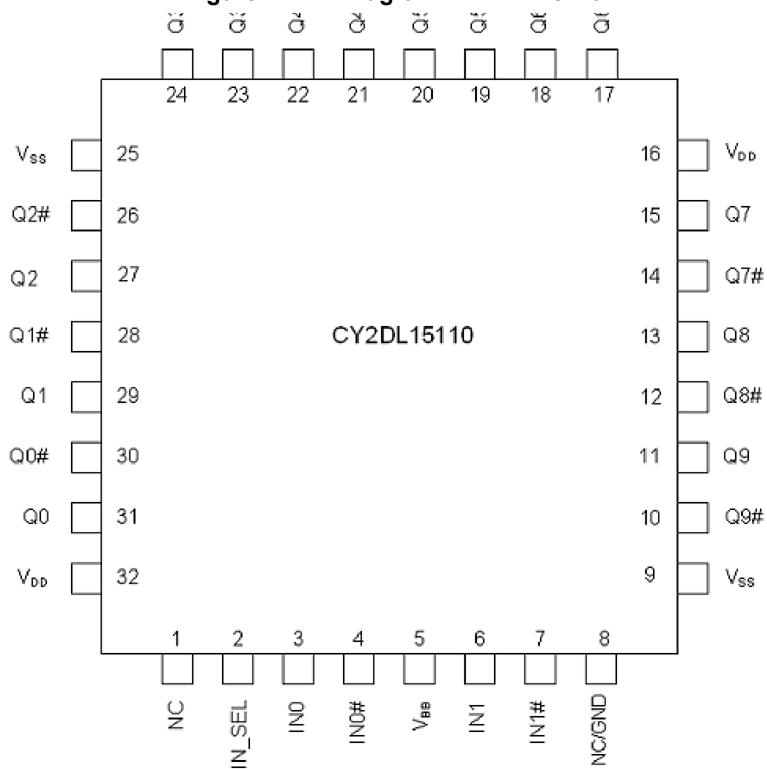


Note
1. Input AC-coupling capacitors are required for voltage-translation applications.

Contents

Pinouts

Figure 1. Pin Diagram - CY2DL15110



Pin Definitions

Pin No.	Pin Name	Pin Type	Description
1	NC		No connection
2	IN_SEL	Input	Input clock select pin. Low-voltage complementary metal oxide semiconductor (LVCMOS)/low-voltage transistor-transistor-logic (LVTTL). When IN_SEL = Low, the IN0/IN0# differential input pair is active When IN_SEL = High, the IN1/IN1# differential input pair is active
3	IN0	Input	Differential (LVPECL, HCSL, LVDS, or CML) input clock. Active when IN_SEL = Low.
4	IN0#	Input	Differential (LVPECL, HCSL, LVDS, or CML) complementary input clock. Active when IN_SEL = Low.
5	V_{BB}	Output	LVDS reference voltage output
6	IN1	Input	Differential (LVPECL, HCSL, LVDS, or CML) input clock. Active when IN_SEL = High.
7	IN1#	Input	Differential (LVPECL, HCSL, LVDS, or CML) complementary input clock. Active when IN_SEL = High.
8	NC/GND	NC	Do not Connect or Ground
9, 25	V_{SS}	Power	Ground
10, 12, 14, 17, 19, 21, 23, 26, 28, 30	Q(0:9)#	Output	LVDS complementary output clocks
11, 13, 15, 18, 20, 22, 24, 27, 29, 31	Q(0:9)	Output	LVDS output clocks
16, 32	V_{DD}	Power	Power supply

Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	Nonfunctional	–0.5	4.6	V
V_{IN}[2]	Input voltage, relative to V_{SS}	Nonfunctional	–0.5	lesser of 4.0 or V_{DD} + 0.4	V
V_{OUT}[2]	DC output or I/O Voltage, relative to V_{SS}	Nonfunctional	–0.5	lesser of 4.0 or V_{DD} + 0.4	V
T_S	Storage temperature	Nonfunctional	–55	150	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection (Human body model)	JEDEC STD 22-A114-B	2000	–	V
L_U	Latch up		Meets or exceeds JEDEC Spec JESD78B IC latch up test		
UL–94	Flammability rating	At 1/8 in.	V–0		
MSL	Moisture sensitivity level		3		
T_J	Junction temperature		–	135	°C

Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.5-V supply	2.375	2.625	V
		3.3-V supply	3.135	3.465	V
T_A	Ambient operating temperature	Commercial	0	70	°C
		Industrial	–40	85	°C
t_{PU}	Power ramp time	Power-up time for V_{DD} to reach minimum supply voltage (power ramp must be monotonic.)	0.05	500	ms
$t_{STARTUP}$	Start up time	Time taken from V_{DD} reaching 95% of its minimum supply voltage to the device being operational.	1	–	ms

Note
2. The voltage on any I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

DC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Max	Unit
I_{DD}	Operating supply current	All LVDS outputs terminated with 100 Ω load [3, 4]	–	125	mA
V_{IH1}	Input high Voltage, LVDS input clocks, IN0, IN0#, IN1, and IN1#		–	V_{DD} + 0.3	V
V_{IL1}	Input low voltage, LVDS input clocks, IN0, IN0#, IN1, and IN1#		–0.3	–	V
V_{IH2}	Input high voltage, IN_SEL	V_{DD} = 3.3 V	2.0	V_{DD} + 0.3	V
V_{IL2}	Input low voltage, IN_SEL	V_{DD} = 3.3 V	–0.3	0.8	V
V_{IH3}	Input high voltage, IN_SEL	V_{DD} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL3}	Input low voltage, IN_SEL	V_{DD} = 2.5 V	–0.3	0.7	V
V_{ID}[5]	Input differential amplitude	See Figure 3 on page 7	0.4	0.8	V
V_{ICM}	Input common mode voltage	See Figure 3 on page 7	0.5	V_{DD} – 0.2	V
I_{IH}	Input high current, All inputs	Input = V_{DD}[6]	–	150	µA
I_{IL}	Input low current, All inputs	Input = V_{SS}[6]	–150	–	µA
V_{PP}	LVDS differential output voltage peak to peak, single-ended	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between Q and Q# pairs [3, 7]	250	470	mV
ΔV_{OCM}	Change in V_{OCM} between complementary output states	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between Q and Q# pairs [3, 7]	–	50	mV
V_{BB}	Output reference voltage	0 to 150 µA output current	1.125	1.375	V
R_P	Internal pull-up / pull-down resistance, LVCMOS logic input	IN_SEL pin has pull-down only	60	140	kΩ
C_{IN}	Input capacitance	Measured at 10 MHz per pin	–	3	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	32-pin TQFP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	69	°C/W
θ_{JC}	Thermal resistance (junction to case)		14	°C/W

Notes
3. Refer to Figure 2 on page 7.
4. I_{DD} includes current that is dissipated externally in the output termination resistors.
5. V_{ID} minimum of 400 mV is required to meet all output AC Electrical Specifications. The device is functional with V_{ID} minimum of greater than 200 mV.
6. Positive current flows into the input pin, negative current flows out of the input pin.
7. Refer to Figure 4 on page 7.
8. These parameters are guaranteed by design and are not tested.

AC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{IN}	Input frequency	Differential input	DC	–	1.5	GHz
		Single-ended CMOS input[9]	DC	–	250	MHz
F_{OUT}	Output frequency	$F_{OUT} = F_{IN}$, differential input	DC	–	1.5	GHz
		$F_{OUT} = F_{IN}$, single-ended CMOS input[9]	DC	–	250	MHz
t_{PD}[10]	Propagation delay input pair to output pair	Input rise/fall time < 1.5 ns (20% to 80%)	–	–	600	ps
t_{ODC}[11]	Output duty cycle	50% duty cycle at input Frequency range up to 1 GHz, differential input	48	–	52	%
		50% duty cycle at input Frequency range up to 250 MHz, Single-ended CMOS input[9]	45	–	55	%
t_{SK1}[12]	Output-to-output skew	Any output to any output, with same load conditions at DUT	–	–	40	ps
$t_{SK1\ D}$[12]	Device-to-device output skew	Any output to any output between two or more devices. Devices must have the same input and have the same output load.	–	–	150	ps
PN_{ADD}	Additive RMS phase noise 156.25-MHz input Rise/fall time < 150 ps (20% to 80%) V_{ID} > 400 mV	Offset = 1 kHz	–	–	–120	dBc/Hz
		Offset = 10 kHz	–	–	–135	dBc/Hz
		Offset = 100 kHz	–	–	–135	dBc/Hz
		Offset = 1 MHz	–	–	–150	dBc/Hz
		Offset = 10 MHz	–	–	–154	dBc/Hz
		Offset = 20 MHz	–	–	–155	dBc/Hz
t_{JIT}[13]	Additive RMS phase jitter (Random)	156.25 MHz, 12 kHz to 20 MHz offset; input rise/fall time < 150 ps (20% to 80%), V_{ID} > 400 mV	–	–	0.11	ps
t_R, t_F[14]	Output rise/fall time, single-ended	50% duty cycle at input, 20% to 80% of full swing (V_{OL} to V_{OH}) Input rise/fall time < 1.5 ns (20% to 80%) Measured at 1 GHz	–	–	300	ps

Notes
9. Refer to Figure 10 on page 9.
10. Refer to Figure 5 on page 7.
11. Refer to Figure 6 on page 7.
12. Refer to Figure 7 on page 8.
13. Refer to Figure 8 on page 8.
14. Refer to Figure 9 on page 8.

Figure 2. LVDS Output Termination

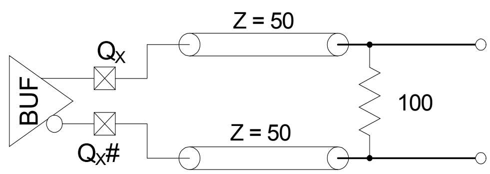


Figure 3. Input Differential and Common Mode Voltages

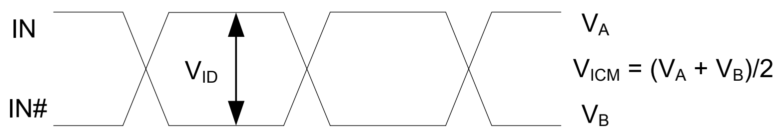


Figure 4. Output Differential and Common Mode Voltages

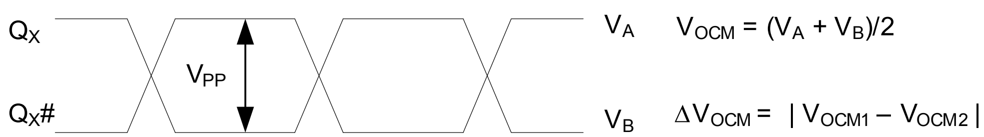


Figure 5. Input to Any Output Pair Propagation Delay

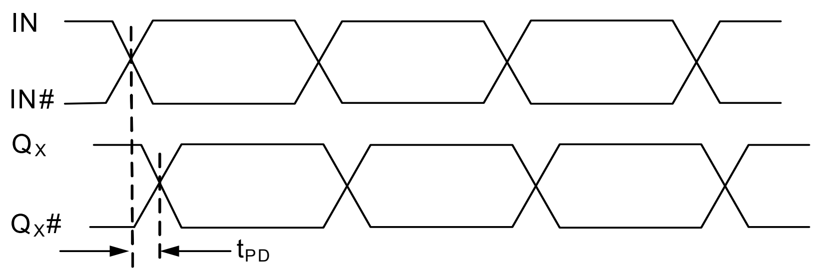


Figure 6. Output Duty Cycle

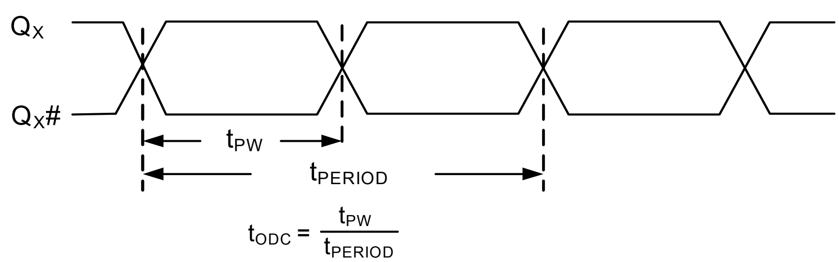


Figure 7. Output-to-output and Device-to-device Skew

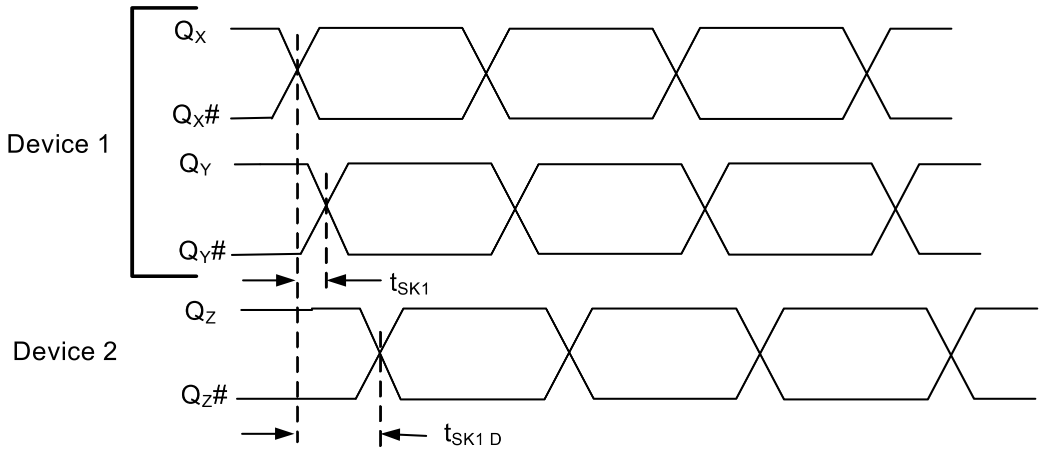
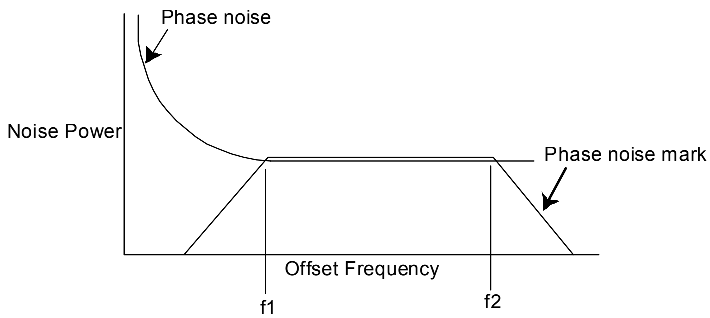
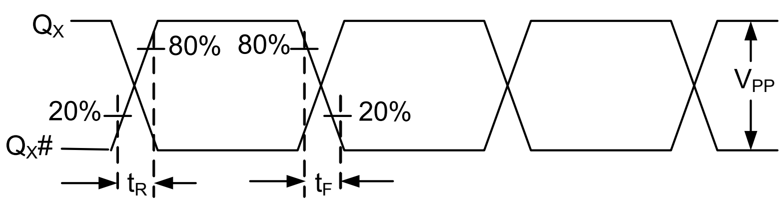


Figure 8. RMS Phase Jitter



$$\text{RMS Jitter} \propto \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

Figure 9. Output Rise/Fall Time



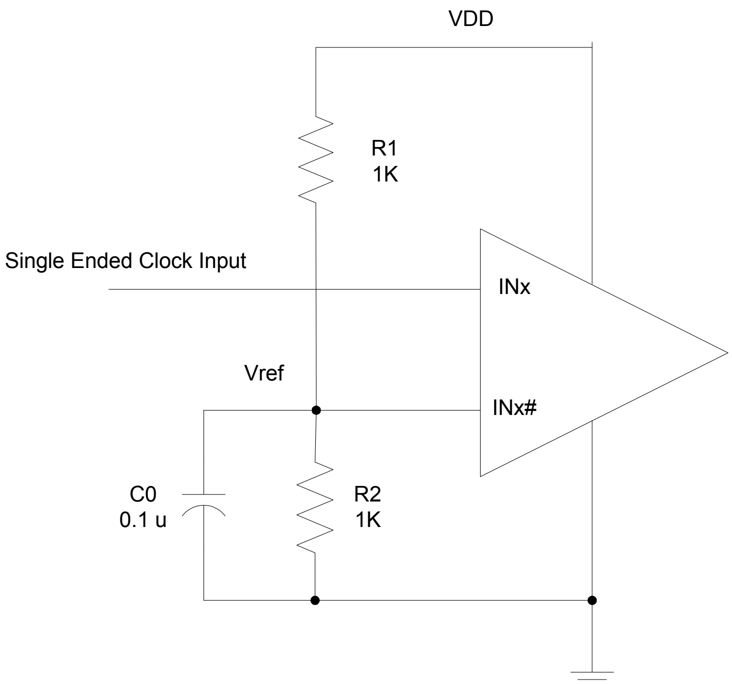
Application Information

CY2DL15110 can be used with a single-ended CMOS input by biasing the Complementary Input Clock (INx#). “True” input pins (INx) of differential input pair can be fed with a single-ended CMOS input signal. The “complementary” input pin (INx#) of the same differential input pair can be biased with VREF.

Figure 10 shows the schematic which can be used to give single-ended CMOS input to the CY2DL15110.

The reference voltage VREF = VDD/2, is generated by the bias resistors R1, R2 and capacitor C0. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the VREF in the center of the input voltage swing. For example, if the input clock swing is 2.5 V and VDD = 3.3 V, VREF should be 1.25 V and R2/R1 = 0.609.

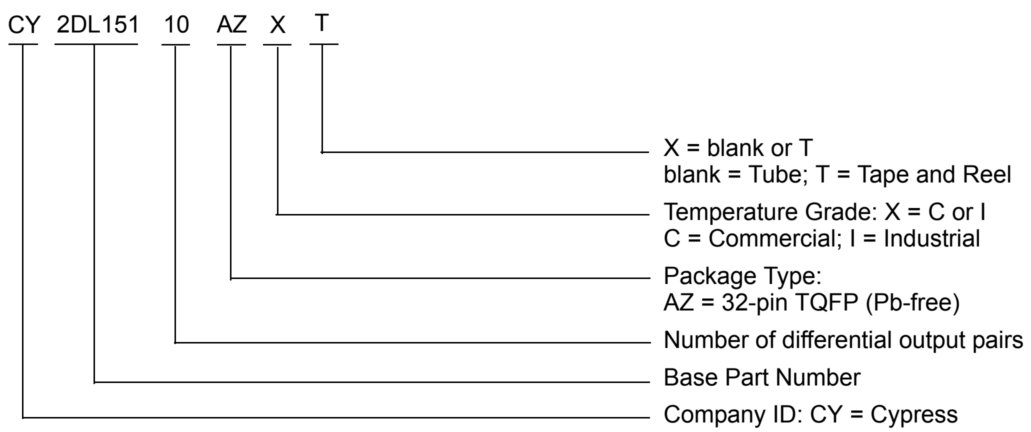
Figure 10. Application Example



Ordering Information

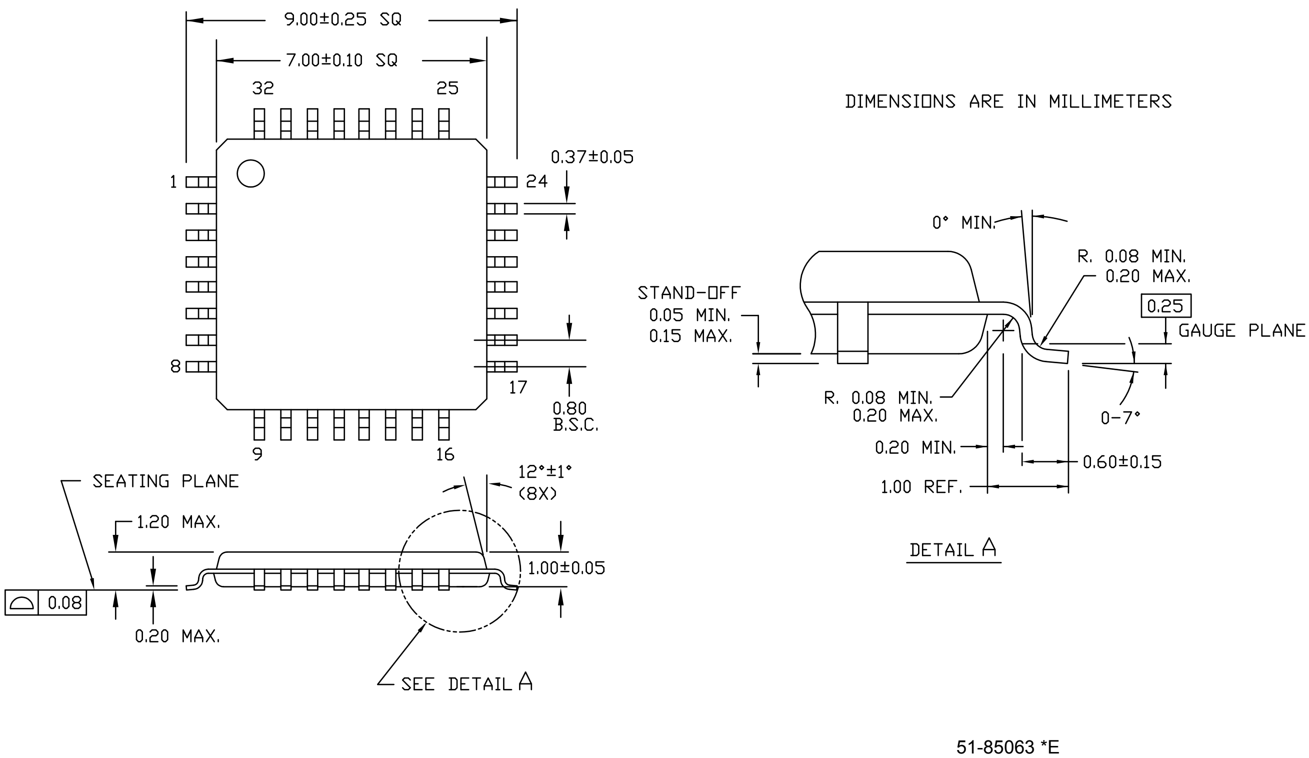
Part Number	Type	Production Flow
Pb-free		
CY2DL15110AZC	32-pin TQFP	Commercial, 0 °C to 70 °C
CY2DL15110AZCT	32-pin TQFP tape and reel	Commercial, 0 °C to 70 °C
CY2DL15110AZI	32-pin TQFP	Industrial, –40 °C to 85 °C
CY2DL15110AZIT	32-pin TQFP tape and reel	Industrial, –40 °C to 85 °C

Ordering Code Definitions



Package Diagram

Figure 11. 32-pin TQFP (7 × 7 × 1.0 mm) A3210 Package Outline, 51-85063



Acronyms

Acronym	Description
ESD	electrostatic discharge
HBM	human body model
I/O	input/output
JEDEC	joint electron devices engineering council
LVDS	low-voltage differential signal
LVCMOS	low-voltage complementary metal oxide semiconductor
LVTTL	low-voltage transistor-transistor logic
RMS	root mean square
TQFP	thin quad flat pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
GHz	gigahertz
Hz	hertz
I/O	input/output
kHz	kilohertz
kΩ	kilohm
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
MHz	megahertz
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2DL15110, 1:10 Differential LVDS Fanout Buffer with Selectable Clock Input Document Number: 001-69398				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3269680	CXQ	06/02/2011	New data sheet.
*A	3292902	CXQ	06/27/2011	Minor edits in Logic Block Diagram (changed the OE resistor value from 100k to R_P). Minor edits in Figure 2 and Figure 4 (Replaced “Q” and “Q#” with “Q_X” and “Q_X#”). Deleted the Notes “Refer to Figure 2.” and “Refer to Figure 4.” in page 7 and their references in Figure 2 and Figure 4.
*B	3357978	BASH	09/07/2011	Updated Operating Conditions (Added a parameter $t_{STARTUP}$ and its details). Updated Package Diagram.
*C	3548521	BASH	03/12/2012	Changed status from Advance to Final. Post to external web.
*D	3979416	PURU	04/23/2013	Updated Logic Block Diagram (Removed OE related information). Updated Pinouts (Removed OE related information). Updated Pin Definitions (Replaced OE with NC/GND in “Pin Name” column and also updated description accordingly). Updated DC Electrical Specifications (Removed OE related information, removed I_{OZ} parameter and its details).
*E	4592452	XHT	12/10/2014	Updated Features. Updated Functional Description: Modified input from LVDS to LVPECL, LVDS, HCSL, or CML. Added “For a complete list of related documentation, click here.” at the end. Updated Pin Definitions. Added Application Information. Added Figure 10. Added Junction temperature 135 °C and Thermal resistance 69 °C/W, in Absolute Maximum Ratings. Updated AC Electrical Specifications. Added output FIN, FOUT, and tODC spec for Single-ended CMOS input.
*F	5275944	PSR	06/02/2016	Updated Absolute Maximum Ratings: Removed θ_{JA} parameter and its details. Added Thermal Resistance. Updated Package Diagram: spec 51-85063 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*G	5965587	AESATMP8	11/13/2017	Updated logo and Copyright.

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