Ultra-Low-Power Narrow-Band Sub-GHz Wireless Microcontroller

AXM0F343

ON Semiconductor®

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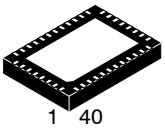


QFN40 7x5, 0.5P
CASE 485EG

MARKING DIAGRAM

XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 32 of this data sheet.

Features

- Ultra−Low−Power System−on−Chip (SoC) with Integrated Arm® Cortex®−M0+ and Narrow−Band Sub−GHz RF Transceiver
- Narrow−Band Sub−GHz RF Transceiver
  - Programmable Carrier from 27 to 1050 MHz
  - Data Rates from 100 bps to 125 kbps
  - FSK/MSK/4−FSK/GFSK/GMSK/ASK/AFSK/PSK
  - Wake on Radio (WOR) for Minimal Average Receiver Current Consumption
  - Compatible with AX50xx Series Transceivers and SoCs
- Advanced Ultra−Low−Power Modes Optimized for Extremely Long Battery Life
  - Hibernate Mode with Wake−up Timer Running at as Low as 600 nA
  - Shutdown Mode with GPIO Wakeup Only 230 nA
- Up to 40 MHz Arm 32−bit Cortex−M0+
  - AXM0F343−64
    64 kB of Embedded FLASH Memory and 8 kB of Internal RAM Memory
  - AXM0F343−256
    256 kB Embedded FLASH Memory and 32 kB Internal RAM Memory
  - Flexible Internal and External Clocking Options
  - 3 Channel Arm PL230 µDMA Controller
  - High Security: AES, CRC, and True Random Number Generator Hardware Accelerators and Debug Port Lock
  - 2 USART, SPI Controller, and I^2C Communication Interfaces
  - System Tick Timer, Three 16−bit General Purpose Timers, 32−bit Tick Timer, 32−bit Wakeup Timer, and 32−bit Watchdog Timer
  - Sigma−delta Modulator
  - Four Capture/Compare/PWM
  - 19 Programmable GPIO
  - 12−bit 1M Sample/s ADC, up to 6 Channels
  - Two Comparators
  - Flexible Pin Mapping with Crossbar
  - Internal 40 MHz High Speed RC Oscillator, with Software Calibration Option Against a Reference Clock for Flexible System Clocking
  - Optional Low Frequency Crystal Oscillator for Accurate Low Power Time Keeping
  - Brown−out and Power−on−Reset Detection
  - Internal Temperature and Voltage Sensor
- This is a Pb−Free Device

Applications

27−1050 MHz Licensed and Unlicensed Radio Systems

- Battery Operated
- Internet of Things (IoT)
- Smart Retail Including Electronic Shelf Labels (ESL)
- Automatic Meter Reading (AMR)
- Security and Tracking Applications
- Agriculture
- Building Automation
- Wireless Networks
- Energy Harvesting Smart Sensors

BLOCK DIAGRAM

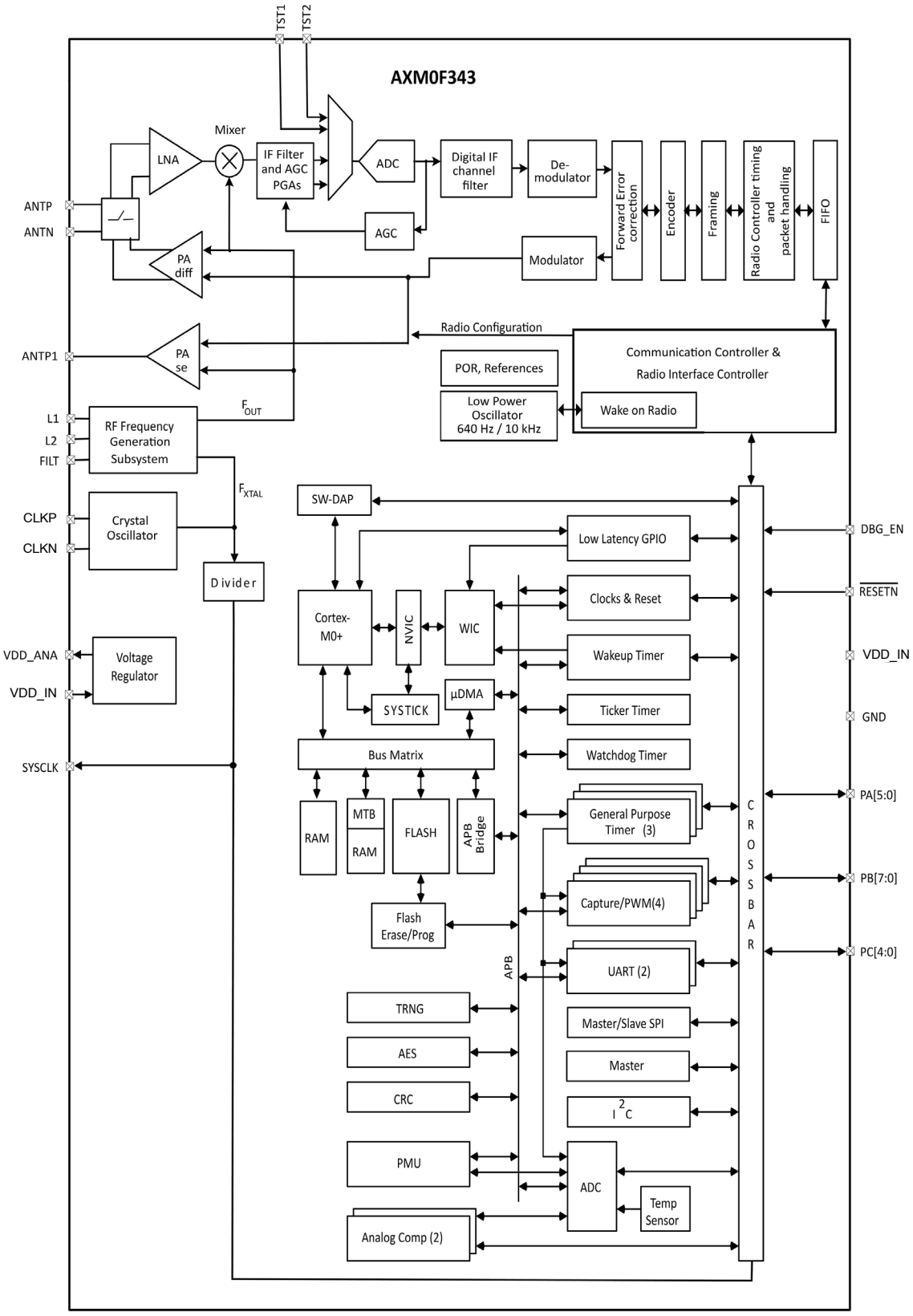


Figure 1. Functional Block Diagram of the AXM0F343

Table 1. PIN FUNCTION DESCRIPTION

Symbol	Pin(s)	Type	Description
VDD_ANA	1	P	Analog power output, decouple to neighboring GND
GND	2	P	Ground, decouple to neighboring VDD_ANA
ANTP	3	A	Differential antenna input/output
ANTN	4	A	Differential antenna input/output
ANTP1	5	A	Single−ended antenna output
GND	6	P	Ground, decouple to neighboring VDD_ANA
VDD_ANA	7	P	Analog power output, decouple to neighboring GND
GND	8	P	Ground
FILT	9	A	Optional synthesizer filter
L2	10	A	Optional synthesizer inductor
L1	11	A	Optional synthesizer inductor
SYSCLK	12	I/O/PU	Default functionality: system clock output
PC4	13	I/O/PU/PD	General purpose IO
PC3	14	I/O/PU/PD	General purpose IO
PC2	15	I/O/PU/PD	General purpose IO
PC1	16	I/O/PU/PD	General purpose IO
PC0	17	I/O/PU/PD	General purpose IO
PB0	18	I/O/PU/PD	General purpose IO
PB1	19	I/O/PU/PD	General purpose IO
PB2	20	I/O/PU/PD	General purpose IO
PB3	21	I/O/PU/PD	General purpose IO
PB4	22	I/O/PU/PD	General purpose IO
PB5	23	I/O/PU/PD	General purpose IO
PB6	24	I/O/PU/PD	General purpose IO, DBG_DATA
PB7	25	I/O/PU/PD	General purpose IO, DBG_CLK
DBG_EN	26	I/PD	In−circuit debugger enable
RESET_N	27	I/PU	Optional reset pin. If this pin is not used it must be connected to VDD_IN
GND	28	P	Ground
VDD_IN	29	P	Power supply input
PA0	30	A/I/O/PU/PD	Analog + General purpose IO
PA1	31	A/I/O/PU/PD	Analog + General purpose IO
PA2	32	A/I/O/PU/PD	Analog + General purpose IO
PA3	33	A/I/O/PU/PD	Analog + General purpose IO
PA4	34	A/I/O/PU/PD	Analog + General purpose IO
PA5	35	A/I/O/PU/PD	Analog + General purpose IO
VDD_IN	36	P	Power supply input
TST1	37	A	GPADC input, must be connected to GND if not used.
TST2	38	A	GPADC input, must be connected to GND if not used.
CLKN	39	A	Crystal oscillator input/output (RF reference oscillator)
CLKP	40	A	Crystal oscillator input/output (RF reference oscillator)
GND	Center pad	P	Ground on center pad of QFN, must be connected

A = analog input
I = digital input signal
O = digital output signal
PU = pull−up
N = not to be connected
P = power or ground
PD = pull−down

PINOUT DRAWING

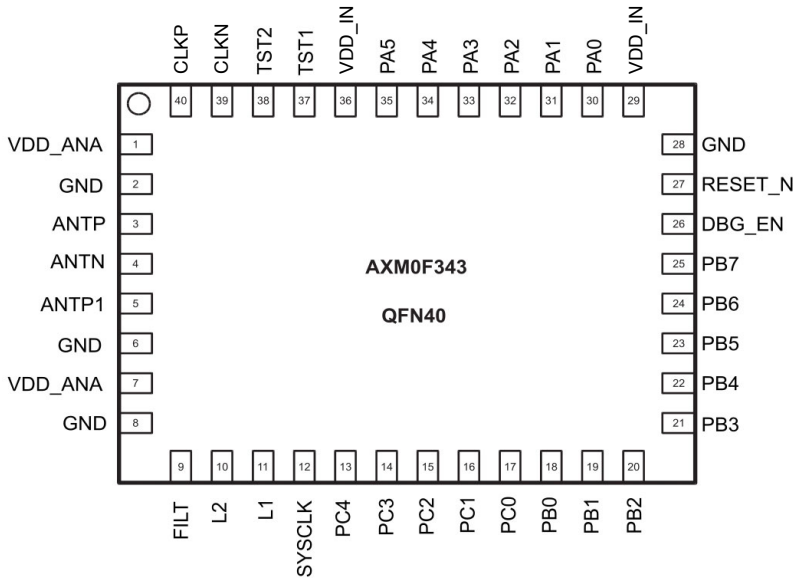


Figure 2. Pinout Drawing (Top View)

I/O PERIPHERALS

General Purpose I/O (GPIO)

AXM0F343 has 19 programmable Inputs/Outputs. These can be used as a general purpose system level interaction or as connectors to internal peripheral functions. The default state of all GPIO's is a digital input with a weak pulldown.

The GPIO is a general−purpose I/O interface unit that provides the following properties:

- Bi−directional capability
- Push−pull or open−drain configuration
- Programmable pull−up, pull−down or neither
- Individually configurable interrupt and DMA enable
- Rising or falling edge and level sensitive interrupts
- Thread safe atomic single−cycle Read−Modify−Write
- Inputs are sampled using a 2 flop synchronizer to avoid metastability.

Crossbar (XBAR)

AXM0F343 has 19 programmable I/O that are shared across various peripherals.

Software must configure the crossbar to connect the desired peripheral to the desired I/O, given system constraints. Typically multiple options exist for each function to avoid conflicts with other functions.

The PA bank of I/O are analog capable and can be used for the ADC and analog comparators.

Each I/O can be used in up to 8 output configurations and various input functions. Output configuration and input functions are independent and can be used simultaneously given compatible operations.

Table 2. CROSSBAR CONFIGURATION TABLE − PA BANK

OUT CFG	PA0	PA1	PA2	PA3	PA4	PA5
0	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5
1	TIM0OUT	TIM2OUT	PWM0H	TIM1OUT	EXTCLK_OUT	PWM3H
2	PWM2H	PWM1H	SDA	SCL	ACMPO0	USART1TX
3	SPI_SEL1	PWM0L	SPI_SCK	SPI_SEL0	SPI_DOUT	SPI_SEL2
4	−	−	−	−	−	PWM1L
5	−	−	−	−	−	−
6	−	TIM1OUT	−	−	−	−
7	−	TIM0OUT	−	−	−	−
IN	CAPT1	TIM0CLK USART1_CLK TSTART	USART1_RX SPI_SEL_IN TSTOP CAPT2 SDA	EXTCLK_IN SPI_SCK_IN SCL	TIM1CLK EXT_INT	CAPT0
ANA	ANA_CH0 HSXOSC_P CMP0/1_MI	ANA_CH1 HSXOSC_N CMP0/1_PL	ANA_CH2 CMP0/1_MI	ANA_CH3 LPXOSC_P CMP0/1_PL	ANA_CH4 LPXOSC_N CMP0/1_MI	ANA_CH5 CMP0/1_PL

Table 3. CROSSBAR CONFIGURATION TABLE − PB BANK

OUT CFG	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7
0	GPIO8	GPIO9	GPIO10	GPIO11	GPIO12	GPIO13	GPIO14	GPIO15
1	USART1TX	PWM2H	PWM3H	PWM0H	USART0TX	TIM1OUT	PWM1H	PWM1L
2	ACMPO0	PWM1H	TIM2OUT	TIM1OUT	−	SPI_SCK	SPI_SEL0	SPI_DOUT
3	EXTCLK_OUT	SDA	SCL	−	SDA	SCL	−	−
4	PWM0L	SPI_DOUT	SPI_SCK	SPI_SEL0	PWM2H	PWM3H	SPI_SEL1	SPI_SEL2
5	−	−	−	−	PC4	−	−	TIM2OUT
6	−	−	TIM1OUT	−	−	−	−	TIM1OUT
7	−	−	TIM0OUT	−	−	−	−	TIM0OUT
IN	CAPT1 ADCTRIG SPI_DIN	USART0_CL USART1_RX TIM0CLK SDA	CAPT0 SPI_SEL_IN SCL	TIM2CLK WAKEUP SPI_SCK_IN	TIM1CLK SPI_DIN TSTART SDA	USART0_RX SPI_SEL_IN TSTOP SCL	SPI_SCK_IN	USART1_CLK EXT_INT USART0_CLK

Table 4. CROSSBAR CONFIGURATION TABLE − PC BANK

OUT CFG	PC0	PC1	PC2	PC3	PC4
0	GPIO16	GPIO17	GPIO18	GPIO19	GPIO20
1	SPI_SEL0	SPI_SCK	SPI_DOUT	−	ACMPO1
2	TIM0OUT	ACMPO1	USART0TX	ACMPO0	PWM2H
3	EXTCLK_OUT	TIM2OUT	SPI_SEL1	SPI_SEL2	TIM2OUT
4	PWM3L	PWM0L	PWM1L	PWM2L	−
5	−	−	−	−	PB4
6	−	−	−	−	TIM1OUT
7	−	−	−	−	TIM0OUT
IN	ADCTRIG SPI_SCK_IN CAPT3 TSATRT TSTOP	TIM0CLK SPI_SEL_IN EXTCLK_IN	CAPT2 EXT_INT TIM2CLK	USART0_RX SPI_DIN	ADCTRIG TIM1CLK USART1_CLK

Legend:
GPIOx = General purpose I/O x
TimxOUT = Timer x roll−over output
TimxCLK = Timer x external clock input
CAPTx = Timer capture x input
PWMxH/PWMxL = High side/low side PWMx output
CMPx_PL = Analog Comparator plus input
CMPx_MI = Analog Comparator minus input
ACMPOx = Analog comparator outputs
WAKEUP = Shutdown mode wake−up pin (PB3)
SDA/SCL = I^2C data I/O and clock (Bidir depending on I^2C configuration)
SPI_[SELx|SCK] = Master/slave SPI select x out and clock out (master mode)
SPI_[SEL_IN|SCK_IN] = Master/slave SPI select in and clock in (slave mode)
SPI_[DOUT|DIN] = Master/slave SPI data output and data input
USARTx_[RX|TX|CLK] = USART x receive data, transmit data, and clock
HSXOSC_P & HSXOSC_N = High Speed Crystal Pins
LPXOSC_P & LPXOSC_N = Low power Crystal Pins
EXT_INT = External interrupt
EXTCLK_[IN|OUT] = External clock in and external clock out
TSTART/TSTOP = Trace start and stop controls
ADCTRIG = ADC trigger
ANA_CHx = Analog ADC Channel Input

SPECIFICATIONS

Table 5. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Condition	Min	Max	Unit
VDD_IN	Supply voltage		−0.3	5	V
IDD	Supply current		–	200	mA
P_i	Absolute maximum input power at receiver input	ANTP and ANTN pins in RX mode	–	10	dBm
I_{I1}	DC current into any pin except ANTP, ANTN, ANTP1		−10	10	mA
I_{I2}	DC current into pins ANTP, ANTN, ANTP1		−100	100	mA
V_{ia}	Input voltage ANTP, ANTN, ANTP1 pins		−0.5	5.5	V
	Input voltage digital pins		−0.3	VDD_IN + 0.3	V
V_{HBM}	Electrostatic handling	Human Body Model	–	2000	V
T_{amb}	Operating temperature		−40	85	°C
T_{stg}	Storage temperature		−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Table 6. SUPPLIES (V_{DDIO} = 3.0 V, T_A = 30°C unless otherwise noted)

Symbol	Description	Condition	Min	Typ	Max	Unit
VDD_{IN}	Voltage regulator supply voltage		2.1	3.0	3.6	V
RADIO						
I_{RX}	Radio Receiver Current consumption RX RF frequency generation subsystem: Internal VCO and internal loop−filter	868 MHz, datarate 6 kbps	–	11.5	–	mA
		868 MHz, datarate 100 kbps		12.5		
I_{WOR}	Typical wake−on−radio duty cycle current	1 s, 100 kbps	–	6	–	μA
$I_{TX-DIFF}$	Radio Current consumption TX differential	868 MHz, Maximum output power setting, CW mode, (Note 2 and 3)	–	55	–	mA
I_{TX-SE}	Radio Current consumption TX single ended	868 MHz, 0 dBm output power, CW mode	–	10	–	mA
I_{LPXTAL}	Crystal oscillator current (RF reference oscillator)	16 MHz	–	160	–	μA

Table 6. SUPPLIES (V_{DDIO} = 3.0 V, T_A = 30°C unless otherwise noted) (continued)

Symbol	Description	Condition	Min	Typ	Max	Unit
AXM0F343−64						
I_{64RUN1}	Run mode without FLASH fetch (Note 5)	All peripherals disabled. Core is running an endless while loop	−	−	155	μA/MHz
I_{64RUN2}	Run mode with constant FLASH fetch (Note 5)	All peripherals disabled. Core is running an endless while loop	−	−	169	μA/MHz
$I_{64SLEEP1}$	Current consumption for the Microcontroller on Sleep mode and Radio on Deep Sleep	All peripherals disabled except Wake−up timer (WUT)	−	25	−	μA/MHz
$I_{64SLEEP3}$	Current consumption for the Microcontroller on Sleep mode (LPOSC) and Radio on Deep Sleep		−	47	−	μA
I_{64HIB}	Current consumption for the Microcontroller on Hibernate mode with no SRAM Retention and Radio on Deep Sleep	Wake−up timer (WUT) enabled (Note 6)	−	0.6	−	μA
I_{64HIB2}	Current consumption for the Microcontroller on Hibernate mode with 2 kB SRAM Retention and Radio on Deep Sleep	Wake−up timer (WUT) enabled (Note 6)	−	1	−	μA
I_{64HIB6}	Current consumption for the Microcontroller on Hibernate mode with 6 kB SRAM Retention and Radio on Deep Sleep	Wake−up timer (WUT) enabled (Note 6)	−	1.45	−	μA
I_{64HIB8}	Current consumption for the Microcontroller on Hibernate mode with 2 kB and 6 kB SRAM Retention and Radio on Deep Sleep	Wake−up timer (WUT) enabled (Note 6)	−	1.8	−	μA
$I_{64SHUTDOWN}$	Current consumption for the Microcontroller on Shutdown mode and Radio on Deep Sleep	All peripherals disabled except PB3 wakeup	−	230	−	nA
AXM0F343−256						
$I_{256RUN1}$	Run mode without FLASH fetch (Note 5)	All peripherals disabled. Core is running an endless while loop	−	−	188	μA/MHz
$I_{256RUN2}$	Run mode with constant FLASH fetch (Note 5)	All peripherals disabled. Core is running an endless while loop	−	−	200	μA/MHz
$I_{256SLEEP1}$	Current consumption for the Microcontroller on Sleep mode and Radio on Deep Sleep	All peripherals disabled except Wake−up timer (WUT)	−	60	−	μA/MHz
$I_{256SLEEP3}$	Current consumption for the Microcontroller on Sleep mode (LPOSC) and Radio on Deep Sleep		−	55	−	μA
I_{256HIB}	Current consumption for the Microcontroller on Hibernate mode with no SRAM Retention and Radio on Deep Sleep	Wake−up timer (WUT) enabled (Note 6)	−	0.6	−	μA
$I_{256HIB8}$	Current consumption for the Microcontroller on Hibernate mode with 8 kB SRAM Retention and Radio on Deep Sleep	Wake−up timer (WUT) enabled (Note 6)	−	1.5	−	μA
$I_{256HIB16}$	Current consumption for the Microcontroller on Hibernate mode with 16 kB SRAM Retention and Radio on Deep Sleep	Wake−up timer (WUT) enabled (Note 6)	−	2.2	−	μA

Table 6. SUPPLIES (V_{DDIO} = 3.0 V, T_A = 30°C unless otherwise noted) (continued)

Symbol	Description	Condition	Min	Typ	Max	Unit
AXM0F343−256						
$I_{256HIB32}$	Current consumption for the Microcontroller on Hibernate mode with 32 kB SRAM Retention and Radio on Deep Sleep	Wake−up timer (WUT) enabled (Note 6)	−	3.5	−	μA
$I_{256SHUTDOWN}$	Current consumption for the Microcontroller on Shutdown mode and Radio on Deep Sleep	All peripherals disabled except PB3 wake−up	−	230	−	nA

2. Measured on ON Semiconductor's reference design board with an optimized RF match network and harmonic filters.
3. RF frequency generation subsystem: Internal VCO and internal loop−filter
   Antenna configuration: Differential PA, internal RX/TX switch
4. RF frequency generation subsystem: Internal VCO and internal loop−filter
   Antenna configuration: Single ended PA, external RX/TX switching
5. Microcontroller only.
6. Wakeup timer adds ~0.1 μA at T = 25°C

Table 7. ELECTRICAL CHARACTERISTICS (V_{DDIO} = 3.0 V, T_A = 30°C unless otherwise noted)

Symbol	Description	Condition	Min	Typ	Max	Unit
DIGITAL I/O						
V_{IL}	Logic input low threshold		0.3	−	−	VDD
V_{IH}	Logic input high threshold		−	−	0.7	VDD
R_{PU}	Internal pull−up resistor		35	−	−	kΩ
R_{PD}	Internal pull−down resistor		35	−	−	kΩ
V_{OL}	Logic output low level	I_{LOAD} = 4 mA I_{LOAD} = 2 mA @ V_{DDIO} = 2.1 V (not valid for SYSCLK pin)	−	−	0.5	V
V_{OH}	Logic output high level	I_{LOAD} = 4 mA I_{LOAD} = 2 mA @ V_{DDIO} = 2.1 V (not valid for SYSCLK pin)	VDD − 0.5	−	−	V
I_{LEAK}	Pin leakage		−1	−	1	μA
FLASH MEMORY						
T_{ACC}	Read access time		−	−	40	ns
T_{PROG}	Program time		−	−	20	μs
T_{ERASE}	Page/Mass erase time		−	−	10	ms
T_{RET}	Data retention		10	−	−	Years
T_{FLEND}	FLASH endurance erase cycles	@ 25C @ 85C	100 k 10 k	−	−	Cycles
POWER−ON RESET (POR) AND BROWN−OUT (BO)						
V_{POR_R}	POR voltage trip point	Rising	1.54	−	1.63	V
V_{POR_F}	POR voltage trip point	Falling	1.45	−	1.63	V
V_{BO_R}	Brownout trip point	Rising	1.52	−	1.70	V
V_{BO_F}	Brownout trip point	Falling	1.50	−	1.68	V
HIGH SPEED RC OSCILLATOR (HSOSC)						
F_{HSOSC}	Oscillator frequency (40 MHz mode)	After optional software calibration, does not include temperature or time drift	38.80	40	41.2	MHz
F_{HSOSC}	Oscillator frequency (32 MHz mode)	After optional software calibration, does not include temperature or time drift	31.5	32	32.8	MHz
ΔF_{HSOSC}	Temperature Drift		−	±3%	−	
T_{HSOSC_SU}	Oscillator startup−up time	At 40 MHz	−	2	−	μs

Table 7. ELECTRICAL CHARACTERISTICS (V_{DDIO} = 3.0 V, T_A = 30°C unless otherwise noted) (continued)

Symbol	Description	Condition	Min	Typ	Max	Unit
I_{HSOSC}	Current Consumption		–	350	–	μA
LOW POWER RC OSCILLATOR (LPOSC)						
F_{LPOSC}	Oscillator frequency (fast mode)	After optional software calibration, does not include temperature or time drift	–	10.24	–	kHz
F_{LPOSC}	Oscillator frequency (slow mode)	After optional software calibration, does not include temperature or time drift	–	640	–	Hz
ΔF_{LPOSC}	Temperature Drift		–	±6%	–	
T_{LPOSC_SU}	Oscillator start−up time (fast mode)		–	0.41	–	ms
T_{LPOSC_SU}	Oscillator start−up time (slow mode)		–	1.4	–	ms
I_{LPOSC}	Current Consumption (fast mode)		–	420	–	nA
I_{LPOSC}	Current Consumption (slow mode)		–	95	–	nA
HIGH SPEED CRYSTAL OSCILLATOR (HSXOSC)						
F_{HSXTAL}	Crystal frequency		8	32	40	MHz
LOW POWER CRYSTAL OSCILLATOR (LPXOSC)						
F_{LPXTAL}	Crystal frequency		–	32.768	–	kHz
I_{LPXTAL}	Current Consumption		–	285	–	nA
ANALOG COMPARATORS (CMP)						
V_{CMIR}	Common mode input range (Note 7, 8)		0.2	–	V_{DDIO} − 0.5	V
T_{COMP}	Response time (Note 7)		–	200	–	ns
ANALOG TO DIGITAL CONVERTER (ADC)						
F_{ADCCLK}	Sample clock frequency		0.01	–	20	MHz
C_{IN}	Input capacitance (when 1:1 divider is selected (single−ended)		–	2	–	pF
R_{IN}	Series resistance to input capacitance		–	1.1	–	kΩ
E_{GAIN}	Gain error (Note 9)		–	±0.75	–	%
E_{OFFSET}	Offset error (Note 9)		–	±15	–	LSB
INL	Integral Non−Linearity (Note 10)	Differential, gain bypass, 1 V reference Differential, 1X gain, 1 V reference Differential ,10X gain, 1 V reference Differential, 1/4 gain, 1 V reference single−ended, 1X gain, 1 V reference, 2 x Vref Range_. Input range limited to Vin+ = (250 mV, 3.05 V). VDDIO = 3.3 V.	−2.5 – – – –	 ±2.5 ±3.5 ±2 ±2	2.5 – – – –	LSB
DNL	Differential Non−Linearity (Note 10)	Differential, gain bypass, 1 V reference Differential, 1X gain, 1 V reference Differential ,10X gain, 1 V reference Differential, 1/4 gain, 1 V reference single−ended, 1X gain, 1 V reference, 2 x Vref Range_. Input range limited to Vin+ = (250 mV, 3.05 V). VDDIO = 3.3 V.	– – – – –	– 1.5 2.0 1.5 1.5	1.5 – – – –	LSB

7. 50 mV overdrive.
8. With extension bit asserted.
9. Does not include reference voltage variation.
10. Excluding gain and offset error

Table 8. CRYSTAL OSCILLATOR (RF REFERENCE OSCILLATOR)

(V_{DDIO} = 3.0 V, T_A = 30°C unless otherwise noted)

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{XTAL}	Crystal or frequency	Note 11, 12, 13	10	16	50	MHz
gm_{osc}	Oscillator transconductance range	Self−regulated see Note 14	0.2	–	20	mS
C_{osc}	Programmable tuning capacitors at pins CLKN and CLKP	AX5043_XTALCAP = 0x00 default	–	3	–	pF
		AX5043_XTALCAP = 0x01	–	8.5	–	pF
		AX5043_XTALCAP = 0xFF	–	40	–	pF
$C_{osc-lsb}$	Programmable tuning capacitors, increment per LSB of AX5043_XTALCAP	AX5043_XTALCAP = 0x01 − 0xFF	–	0.5	–	pF
f_{ext}	External clock input (TCXO)	Note 12, 13, 15	10	16	50	MHz
RIN_{osc}	Input DC impedance		10	–	–	kΩ
$NDIV_{SYSCLK}$	Divider ratio $f_{SYSCLK} = F_{XTAL}/ NDIV_{SYSCLK}$		2^0	2^4	2^{10}	

11. Tolerances and start−up times depend on the crystal used. Depending on the RF frequency and channel spacing the IC must be calibrated to the exact crystal frequency using the readings of the register AX5043_TRKFREQ.
12. The choice of crystal oscillator or TCXO frequency depends on the targeted regulatory regime.
13. To avoid spurious emission, the crystal or TCXO reference frequency should be chosen so that the RF carrier frequency is not an integer multiple of the crystal or TCXO frequency.
14. The oscillator transconductance is regulated for fastest start−up time during start−up and for lowest power curing steady state oscillation. This means that values depend on the crystal used.
15. If an external clock or TCXO is used, it should be input via an AC coupling at pin CLKP with the oscillator powered up and AX5043_XTALCAP = 000000. For detailed TCXO network recommendations depending on the TCXO output swing refer to the AX5043 Application Note: Use with a TCXO Reference Clock.

Table 9. LOW−POWER OSCILLATOR (TRANSCEIVER WAKE ON RADIO CLOCK)

(V_{DDIO} = 3.0 V, T_A = 30°C unless otherwise noted)

Symbol	Description	Condition	Min	Typ	Max	Unit
$f_{osc-slow}$	Oscillator frequency slow mode LPOSC FAST = 0 in AX5043_LPOSCCONFIG register	No calibration	480	640	800	Hz
		After optional software calibration against the crystal oscillator or TCXO, does not include temperature or time drift	630	640	650	
$f_{osc-fast}$	Oscillator frequency fast mode LPOSC FAST = 1 in AX5043_LPOSCCONFIG register	No calibration	7.6	10.2	12.8	kHz
		After optional software calibration against the crystal oscillator or TCXO, does not include temperature or time drift	9.8	10.2	10.8	

Table 10. RF FREQUENCY GENERATION SUBSYSTEM (SYNTHESIZER)

(V_{DDIO} = 3.0 V, T_A = 30°C unless otherwise noted)

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{REF}	Reference frequency	The reference frequency must be chosen so that the RF carrier frequency is not an integer multiple of the reference frequency	10	16	50	MHz
DIVIDERS						
$NDIV_{ref}$	Reference divider ratio range	Controlled directly with bits REFDIV in register AX5043_PLLVCODIV	2^0	–	2^3	
$NDIV_m$	Main divider ratio range	Controlled indirectly with register AX5043_FREQ	4.5	–	66.5	
$NDIV_{RF}$	RF divider range	Controlled directly with bit RFDIV in register AX5043_PLLVCODIV	1	–	2	

Table 10. RF FREQUENCY GENERATION SUBSYSTEM (SYNTHESIZER)
(V_{DDIO} = 3.0 V, T_A = 30°C unless otherwise noted) (continued)

Symbol	Description	Condition	Min	Typ	Max	Unit
CHARGE PUMP						
I_{CP}	Typical charge pump current	Programmable in increments of 8.5 μA via register AX5043_PLLCPI	8.5	–	2168	μA
INTERNAL VCO (VCOSEL = 0)						
f_{RF}	RF frequency range	RFDIV = 1	400	–	525	MHz
		RFDIV = 0	800	–	1050	
f_{step}	RF frequency step	RFDIV = 1 f_{REF} = 16.000000 MHz	–	0.98	–	Hz
BW	Synthesizer loop bandwidth	The synthesizer loop bandwidth an start−up time can be programmed with the registers AX5043_PLLLOOP and AX5043_PLLCPI. For recommendations see the AX5043 Programming Manual, and AX5043 Application Notes on compliance with regulatory regimes.	50	–	500	kHz
T_{start}	Synthesizer start−up time if crystal oscillator and reference are running		5	–	25	μs
VCO WITH EXTERNAL INDUCTORS (VCOSEL = 1, VCO2INT = 1)						
f_{RFrng_lo}	RF frequency range For choice of L_{ext} values as well as VCO gains see Figure 3 and Figure 4	RFDIV = 1	27	–	262	MHz
f_{RFrng_hi}		RFDIV = 0	54	–	525	
EXTERNAL VCO (VCOSEL = 1, VCO2INT = 0)						
f_{RF}	RF frequency range fully external VCO	Note: The external VCO frequency needs to be 2 x f_{RF}	27	–	1000	MHz
V_{amp}	Differential input amplitude at L1, L2 terminals		–	0.7	–	V
V_{inL}	Input voltage levels at L1, L2 terminals		0	–	1.8	V
V_{ctrl}	Control voltage range	Available at FILT in external loop filter mode	0	–	1.8	V

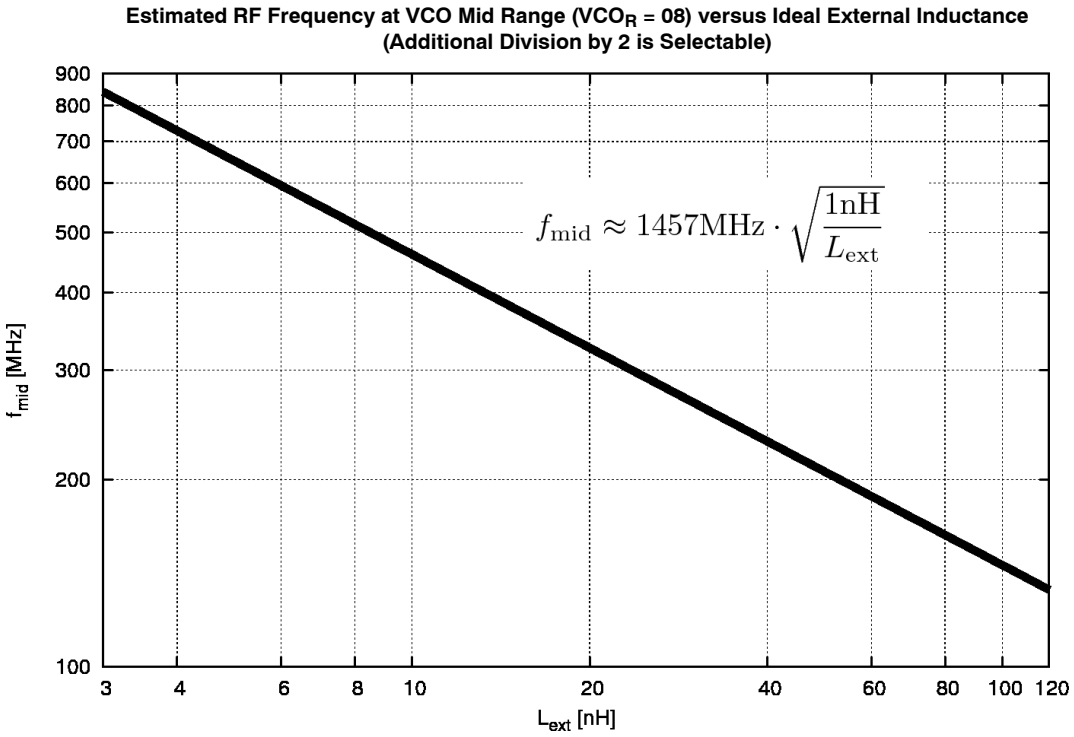


Figure 3. VCO with External Inductors: Estimated Frequency vs. Ideal External Inductor vs. L_{ext}

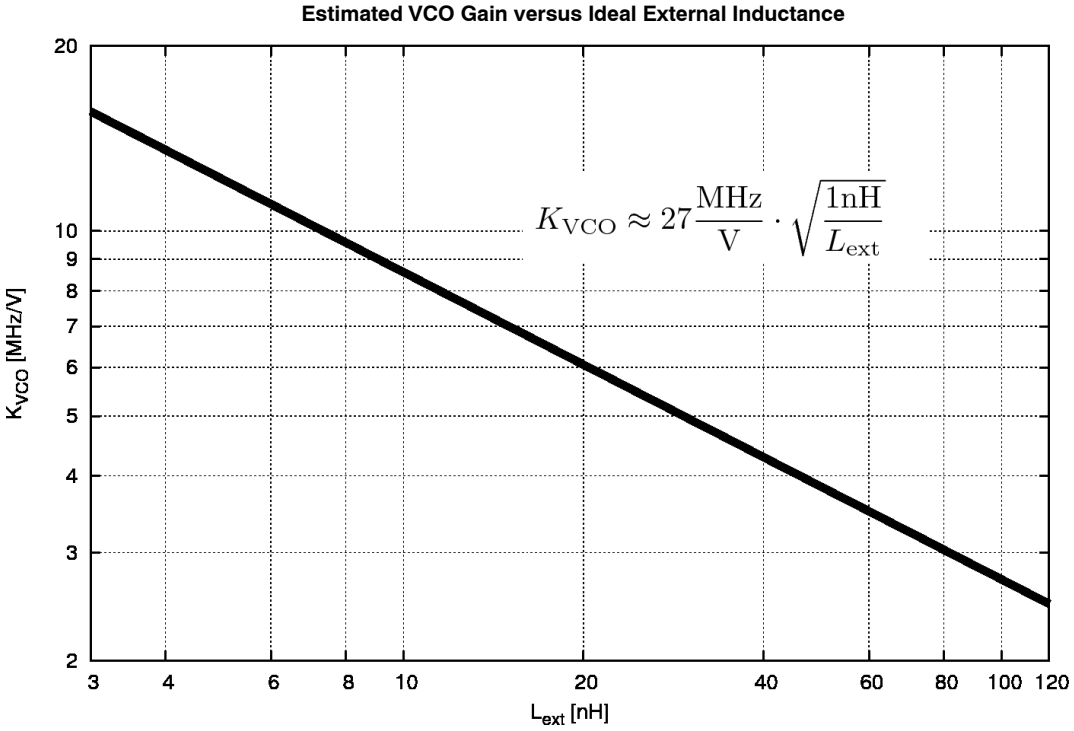


Figure 4. Estimated VCO Gain with Ideal External Inductors: Typical K_{VCO} vs. L_{ext}

The following table estimates the typical frequency ranges for frequency synthesis with an ideal external VCO inductor for different inductor values.

Table 11.

Lext [nH]	Freq [MHz] RFDIV = 0	Freq [MHz] RFDIV = 1	PLL Range
8.2	482	241	0
8.2	437	219	15
10	432	216	0
10	390	195	15
12	415	208	0
12	377	189	15
15	380	190	0
15	345	173	15
18	345	173	0
18	313	157	15
22	308	154	0
22	280	140	14
27	285	143	0
27	258	129	15
33	260	130	0
33	235	118	15
39	245	123	0
39	223	112	14
47	212	106	0
47	194	97	14
56	201	101	0
56	182	91	15
68	178	89	0
68	161	81	15
82	160	80	1
82	146	73	14
100	149	75	1
100	136	68	14
120	136	68	0
120	124	62	14

For tuning or changing of ranges a capacitor can be added in parallel to the inductor.

Table 12. TRANSMITTER

Symbol	Description	Condition	Min	Typ	Max	Units
SBR	Signal bit rate		0.1	–	125	kbps
PTX	Transmitter power @ 868 MHz	Differential PA, 50 Ω single ended measurement at an SMA connector behind the matching network, no harmonic filter	−10	–	16	dBm
	Transmitter power @ 433 MHz		−10	–	16	
	Transmitter power @ 169 MHz		−10	–	16	
PTX_{step}	Programming step size output power	Note 16	–	–	0.5	dB

16. $$P_{out} = \frac{AX5043\_TXPWRCOEFFB}{2^{12}-1} \times P_{max} \qquad \text{(eq. 1)}$$

Table 13. RECEIVER

Symbol	Description	Condition	Min	Typ	Max	Units
RSSIR	RSSI control range	FSK, 500 Hz deviation, 1.2 kbps	−126	–	−46	dB
$RSSIS_1$	RSSI step size	Before digital channel filter; calculated from register AX5043_AGCCOUNTER	–	0.625	–	dB
$RSSIS_2$	RSSI step size	Behind digital channel filter; calculated from registers AX5043_AGCCOUNTER, AX5043_TRKAMPL	–	0.1	–	dB
$RSSIS_3$	RSSI step size	Behind digital channel filter; reading register AX5043_RSSI	–	1	–	dB
R_{AFC}	AFC pull−in range	The AFC pull−in range can be programmed with the AX5043_MAXRFOFFSET registers. The AFC response time can be programmed with the AX5043_FREQGAIND register.	±15	–	–	%
R_{DROFF}	Bitrate offset pull−in range	The bitrate pull−in range can be programmed with the AX5043_MAXDROFFSET registers.	±10	–	–	%

Table 14. RECEIVER AND TRANSMITTER SETTLING PHASES

Symbol	Description	Condition	Min	Typ	Max	Units
T_{xtal}	XTAL settling time	Powermodes: POWERDOWN to STANDBY Note that T_{xtal} depends on the specific crystal used.	–	0.5	–	ms
T_{synth}	Synthesizer settling time	Powermodes: STANDBY to SYNTHTX or SYNTHRX	–	40	–	μs
T_{tx}	TX settling time	Powermodes: SYNTHTX to FULLTX T_{tx} is the time used for power ramping, this can be programmed to be 1 x t_{bit}, 2 x t_{bit}, 4 x t_{bit} or 8 x t_{bit}. (Note 17)	0	1 x t_{bit}	8 x t_{bit}	μs
T_{rx_init}	RX initialization time		–	150	–	μs
T_{rx_rssi}	RX RSSI acquisition time (after T_{rx_init})	Powermodes: SYNTHRX to FULLRX Modulation (G)FSK (Note 17)	–	80 + 3 x t_{bit}	–	μs
$T_{rx\_preamble}$	RX signal acquisition time to valid data RX at full sensitivity/ selectivity (after T_{rx_init})		–	9 x t_{bit}	–	

17. t_{bit} depends on the datarate, e.g. for 10 kbps t_{bit} = 100 μs

Table 15. RADIO STATE TRANSITION TIMES

Symbol	Description	Condition	Min	Typ	Max	Units
T_{tx_on}	TX startup time	Powermodes: STANDBY to FULLTX Note 18	40	40 + 1 x t_{bit}		μs
T_{rx_on}	RX startup time	Powermodes: STANDBY to FULLRX		190		μs
T_{rx_rssi}	RX startup time to valid RSSI	Powermodes: STANDBY to FULLRX Modulation (G)FSK Note 18		270 + 3 x t_{bit}		μs
T_{rx_data}	RX startup time to valid data at full sensitivity/selectivity			190 + 9 x t_{bit}		μs
T_{rxtx}	RX to TX switching	Powermodes: FULLRX to FULLTX		62		μs
T_{txrx}	TX to RX switching (to preamble start)	Powermodes: FULLTX to FULLRX		200		
T_{hop}	Frequency hop	Switch between frequency defined in register AX5043_FREQA and AX5043_FREQB		30		μs

18. t_{bit} depends on the datarate, e.g. for 10 kbps t_{bit} = 100 μs

For additional details on radio related parameters such as receiver performance (e.g. sensitivity, blocking, selectivity) and transmitter performance (e.g. phase noise), please consult the AX5043 datasheet at https://www.onsemi.com/pdf/datasheet/ax5043−d.pdf or visit the Community Forum at https://www.onsemi.com/forum/

CIRCUIT DESCRIPTION

The AXM0F343 is a true single chip Ultra−Low−Power Narrow−Band Sub−GHz Wireless Microcontroller SoC for use in licensed and unlicensed bands ranging from 27 MHz to 1050 MHz. The on−chip transceiver consists of a fully integrated RF front−end with modulator and demodulator. Base band data processing is implemented in an advanced and flexible communication controller that enables user friendly communication.

The AXM0F343 contains a 40 MHz Arm Cortex−M0+ microprocessor.

It is available in two different memory configurations:

- *AXM0F343−64* which contains 64 kBytes of FLASH and 8 kBytes of RAM.
- *AXM0F343−256* which contains 256 kBytes of FLASH and 32 kBytes of RAM.

The AXM0F343 peripherals include 2 USART, SPI controller, I^2C, various multi−function timers, watchdog, 2 comparators, 4 pair of PWM channels, 12−bit ADC, AES

engine, CRC engine, true random number generator and a temperature sensor.

While the radio carrier/LO synthesizer can only be clocked by the crystal oscillator (carrier stability requirements dictate a high stability reference clock in the MHz range), the microcontroller and its peripherals provide extremely flexible clocking options. The system clock that clocks the microcontroller, as well as peripheral clocks, can be selected from one of the following clock sources: the crystal oscillator, an internal high speed oscillator at 32 MHz or 40 MHz, an internal low power 640 Hz / 10.24 kHz oscillator, or the low frequency crystal oscillator running at 32.768 kHz. Both the high speed and low power oscillators can be software calibrated to a reference clock for improved timing resolution. This calibration does not correct for time or temperature drift and should be repeated periodically to ensure the best accuracy possible.

The AXM0F343 sends and receives data in frames. This standard operation mode is called Frame Mode. Pre and post ambles as well as checksums can be generated automatically.

AXM0F343 supports any data rate from 0.1 kbps to 125 kbps for FSK, MSK, 4−FSK, GFSK, GMSK and ASK modulations. To achieve optimum performance for specific data rates and modulation schemes several register settings to configure the AXM0F343 are necessary, they are outlined in the AND9347/D.

The receiver supports multi−channel operation for all data rates and modulation schemes.

Microcontroller

The AXM0F343 incorporates an industry leading 32 bit Arm Cortex−M0+ for high performance, low power, and low−cost processing. The Arm Cortex−M0+ on AXM0F343 includes Wake−up Interrupt Controller (WIC) to support low power mode wake−up. It also includes Micro Trace Buffer (MTB) and Serial Wire Debug Port (SW−DP) for enhanced test and debug capability.

Serial Wire Debug Access Port (SW−DAP)

The Serial Wire Debug Access Port is included in the AXM0F343 implementation. The basic debug functionality includes: processor halts, single−step, processor core register access, reset and hard fault vector catch, unlimited software breakpoints, and full system memory access. The debug mode implementation also includes 4 hardware breakpoints and 2 hardware watchpoints.

The Serial Wire Debug Port connects to pins SWCLK (PB7) and SWDIO (PB6) when DBG_EN pin is high. The Serial Wire Debug Port Interface uses a single bi−directional data connection. Use any Serial Wire Debug (SWD) compliant hardware debugger interface to interact with the internals of AXM0F343. The Debug Port can be disabled with a lock operation for security purposes. PB6 and PB7 return to normal program control when DGB_EN is taken low.

Micro Trace Buffer (MTB)

Micro Trace Buffer is implemented on AXM0F343. When enabled the trace data will be placed in the 2 kB RAM making that address range unusable for normal code execution.

For a full description of all features and operation see the *CoreSight™ MTB−M0+ Technical Reference Manual*.

I/O Port (IOP)

The IOP interface operates entirely in a single HCLK cycle, with transaction address and associated read or write data generated or returned in the same cycle. The GPIO block is on the IOP bus allowing for low−latency, high−resolution GPIO controls.

Direct Memory Access Controller (DMA)

The AXM0F343 contains the PrimeCell® PL230 µDMA configured with 3 channels. The DMA acts as another bus master on the AHB Bus to facilitate data transfers independent of the core. Most peripherals can be configured to trigger the DMA transfers.

Some key features of the DMA controller are:

- Each DMA channel has a programmable priority level
- Each priority level arbitrates using a fixed priority that is determined by the DMA channel number
- Supports memory−to−memory, memory−to−peripheral, and peripheral−to−memory transfer
- Supports multiple DMA cycle types
- Supports multiple DMA transfer data widths
- Each DMA channel can access a primary and alternate, channel control data structure
- All the channel control data is stored in system memory
- The number of transfers in a single DMA cycle is programmable from 1 to 1024
- Indicates when an ERROR condition occurs

For a full description of all features and operation see the *PrimeCell µDMA Controller (PL230) Revision: r0p0 Technical Reference Manual*.

AHB−APB Bridge with Atomic Read−Modify−Write

The Advanced Peripheral Bus (APB) is connected to the Advanced High Performance Bus (AHB) using a bridge that includes support for Atomic Read−Modify−Write capability. Address bits [27:26] are used to configure an APB write as one of four modes:

- *Direct Write (b00)* − A normal write operation which transfers the write data directly into the targeted peripheral register overwriting the previous contents
- *Clear Write (b01)* – Clears each bit with a ‘0’ in the write data word (AND operation with previous data)
- *Set Write (b10)* – Sets each bit with a ‘1’ in the write data word (OR operation with the previous data)

- *Toggle Write (b11)* – Toggles (inverts) each bit with a ‘1’ in the write data word (XOR operation with the previous data)

APB peripheral reads ignore the Atomic R/M/W address bits, reading the target register contents for all address settings.

MEMORY ORGANIZATION

FLASH Program and Erase Controller

The FLASH may be erased and programmed under software or debug port control. The registers used for programming and erasing the FLASH are mapped onto the APB.

Each page may be independently erased, to allow for new content to be programmed. The erased value in the FLASH is all 1s. Programming a word can alter 1s to 0s, but cannot convert 0s to 1s. Only an erase can convert 0s to 1s. Programming a word in the FLASH requires 2 microseconds. Erasing a page of data requires 10 milliseconds.

It is possible to erase the entire 64 kB or 256 kB of FLASH memory, returning the part to factory condition. A mass erase requires 10 milliseconds.

Program and erase operations make read access to the FLASH memory unavailable until completed. The processor will stall while waiting for the AHB Ready signal from the FLASH to return high. If the core needs to keep running, it needs to be running from code in the SRAM.

FLASH Info Block

An additional page within the FLASH is reserved for the information block. It is programmed at the factory and includes trim and traceability. The FLASH info block should not be erased after the factory programming. Certain fields in the info block are open for programming of static values for application configuration. A mass erase of the main FLASH block will not erase the FLASH info block.

FLASH Lock

A protection lock is available in the FLASH to disable the debug port and prevent access to the internal buses and memory for security sensitive applications.

The final word of directly addressable memory in the FLASH is used as a LOCK word. At power−up, before the main system reset is released, the LOCK word is checked by an internal state machine before unlocking the debug port.

As previously mentioned, AXM0F343 is available in two different memory configurations:

AXM0F343−64

64 kB of FLASH memory is directly addressable and is used for program code and non−volatile data storage. Under normal operation, the FLASH block provides single cycle read access via the AHB. The FLASH is divided into 128 pages of 512 bytes each. Memory reads are contiguous across page boundaries.

AXM0F343−64 has a total of 8 kB of internal SRAM divided up into two banks (6 kB and 2 kB). Each of the SRAM banks can be independently powered−off during the ultra−low power Hibernate mode. Data contents of a powered down memory bank are not retained when re−enabled. The 6 kB and 2 kB SRAM banks are logically next to each other in the memory map providing one contiguous 8 kB of SRAM.

AXM0F343−256

256 kB of FLASH memory is directly addressable and is used for program code and non−volatile data storage. Under normal operation, the FLASH block provides single cycle read access via the AHB. The FLASH is divided into 256 pages of 1 kbytes each. Memory reads are contiguous across page boundaries.

AXM0F343−256 has a total of 32 kB of internal SRAM divided up into four banks of 8 kB. Each of the SRAM banks can be independently powered−off during the ultra−low power Hibernate mode. Data contents of a powered down memory bank are not retained when re−enabled. The 8 kB SRAM banks are logically next to each other in the memory map providing one contiguous 32 kB of SRAM.

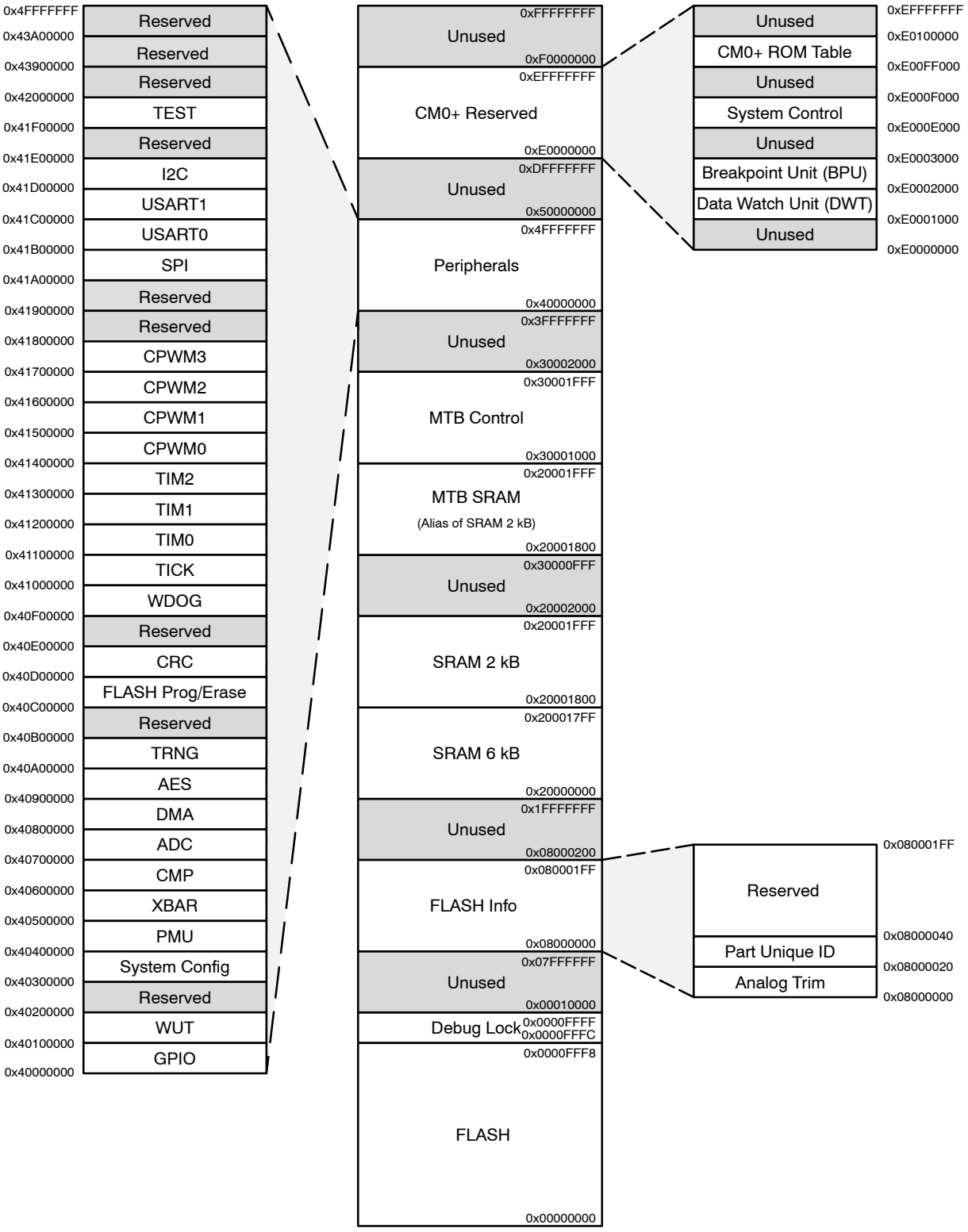


Figure 5. AXM0F343−64 Memory Map

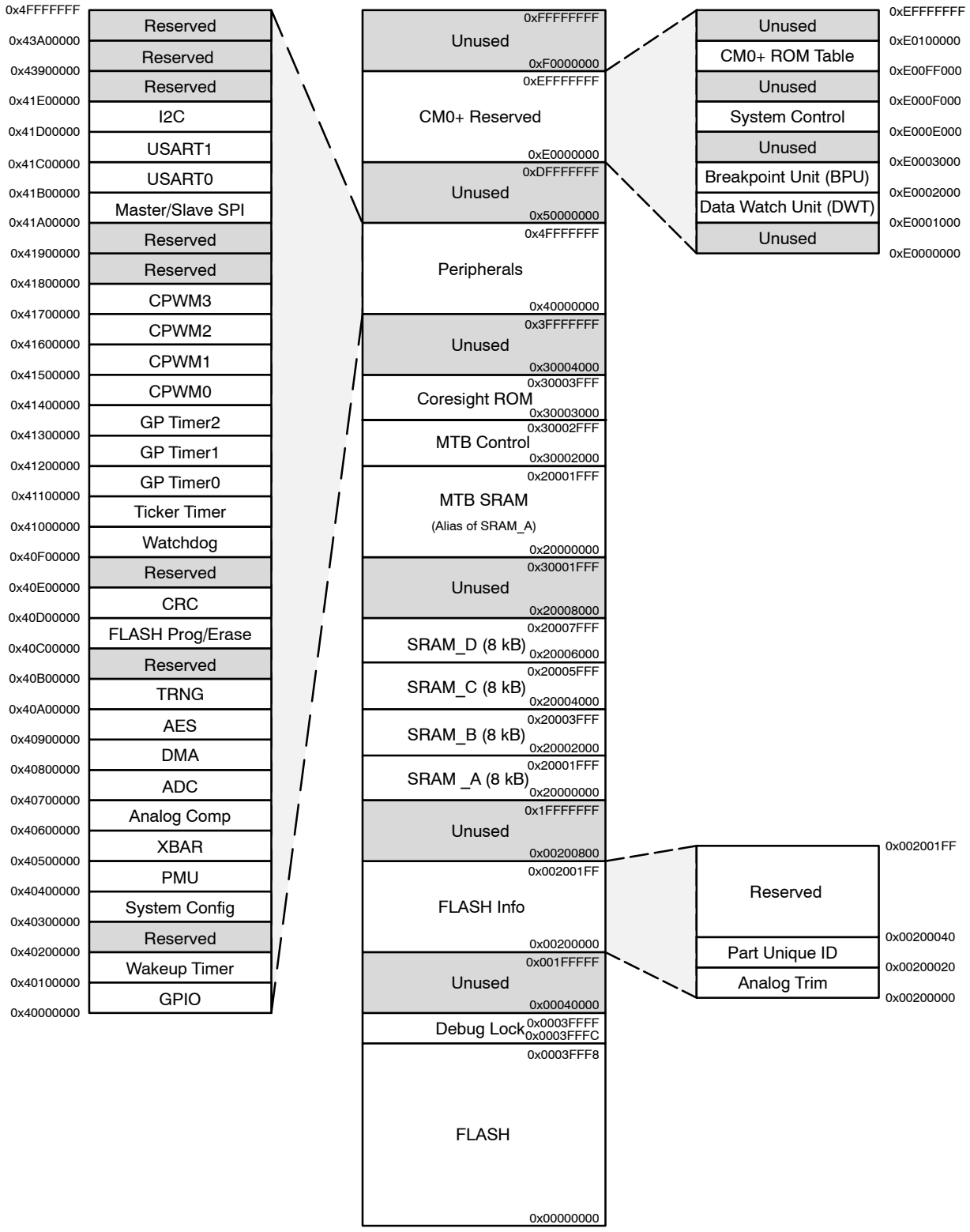


Figure 6. AXM0F343−256 Memory Map

RESET

There are various sources of reset that include: internal power−on reset (POR), external pin reset, software reset, and watchdog timer reset. Internal resets are also generated at the exit of hibernate and shutdown power modes.

Power−on Reset (POR)

The POR reset is asserted when the supply is below threshold levels for proper operation. It also asserts during shutdown mode. POR is released when the internal supply voltage is at a high enough voltage to support the digital logic regulators. When the supply comes out of a reset condition, reset will remain low for at least 10 μs. Hysteresis is included to protect against noise in the supply.

External Reset

When the external reset pin (RESET_N) is driven low, the AXM0F343 is held in reset.

Software Reset

The software reset is called by writing to a given register in the Cortex address space.

Watchdog Timer Reset

To help prevent errant software from locking up the device a watchdog timer (WDOG) is provided. The WDOG is disabled upon power up and must be enabled by software. The watchdog is paused when the debugger halts the processor.

Brown−out (BO) Reset

After power up the internal voltage is monitored. If it gets too low, a brownout interrupt is generated before the digital data is corrupted due to a low power supply. This interrupt can be tied to the non−maskable interrupt (NMI) and can be used to prepare the part for loss of power. For example, a fault code could be written to the “always on” scratch register or to the FLASH, so the system knows the cause of the reset.

CLOCKS

There are five clock sources available to source the core and peripheral functions:

- High speed internal RC oscillator (FRCOSC)
- Low power internal RC oscillator (LPOSC)
- High speed crystal oscillator (XOSC)
- Low power 32 kHz crystal oscillator (LPXOSC)
- External clock (RSYSCLK)

Each clock source can be independently powered down if not in use.

High Speed RC Oscillator Clock (HSOSC)

AXM0F343 has a high frequency internal RC oscillator with trim. It is factory trimmed to operate at 32 MHz or at 40 MHz based on clock configuration. This oscillator can be calibrated to a reference clock for improved performance.

Low Power RC Oscillator Clock (LPOSC)

AXM0F343 has a low frequency, low power internal RC oscillator with trim. The oscillator has a slow mode at 640 Hz or a fast mode at 10.24 kHz. Applications requiring timing accuracy should calibrate this clock to a reference clock.

High Speed Crystal Oscillator Clock (HSXOSC)

AXM0F343 supports a high frequency crystal oscillator running at speeds from 8 – 40 MHz.

Low Power Crystal Oscillator Clock (LPXOSC)

AXM0F343 supports a low frequency crystal oscillator running at 32.768 kHz.

External Clock (EXTCLK_IN)

AXM0F343 offers the possibility to operate from an external clock supplied through a configured GPIO.

The max external clock frequency is 20 MHz. This clock can come external from the chip or can be driven by the AFE.

External Clock Out (EXTCLK_OUT)

AXM0F343 offers the possibility to provide an external clock through a configured GPIO. The max external clock frequency is 40 MHz. This can be the system clock or any of the other active clock sources within AXM0F343.

Clock Gating

Most clocks can be gated either through software configuration or through power modes. Internal use−based clock gating also helps reduce run mode power.

Clock Calibration

Both the high speed and low power oscillators can be calibrated to a reference clock for improved timing resolution. The initial calibration is programmed at the factory. To account for time and temperature drift, periodic software controlled calibration against the crystal reference clock is recommended.

Clock Monitor

A clock monitor can detect the loss of transitions on the selected system clock source. Upon detection, the clock source is switched to the internal high speed oscillator.

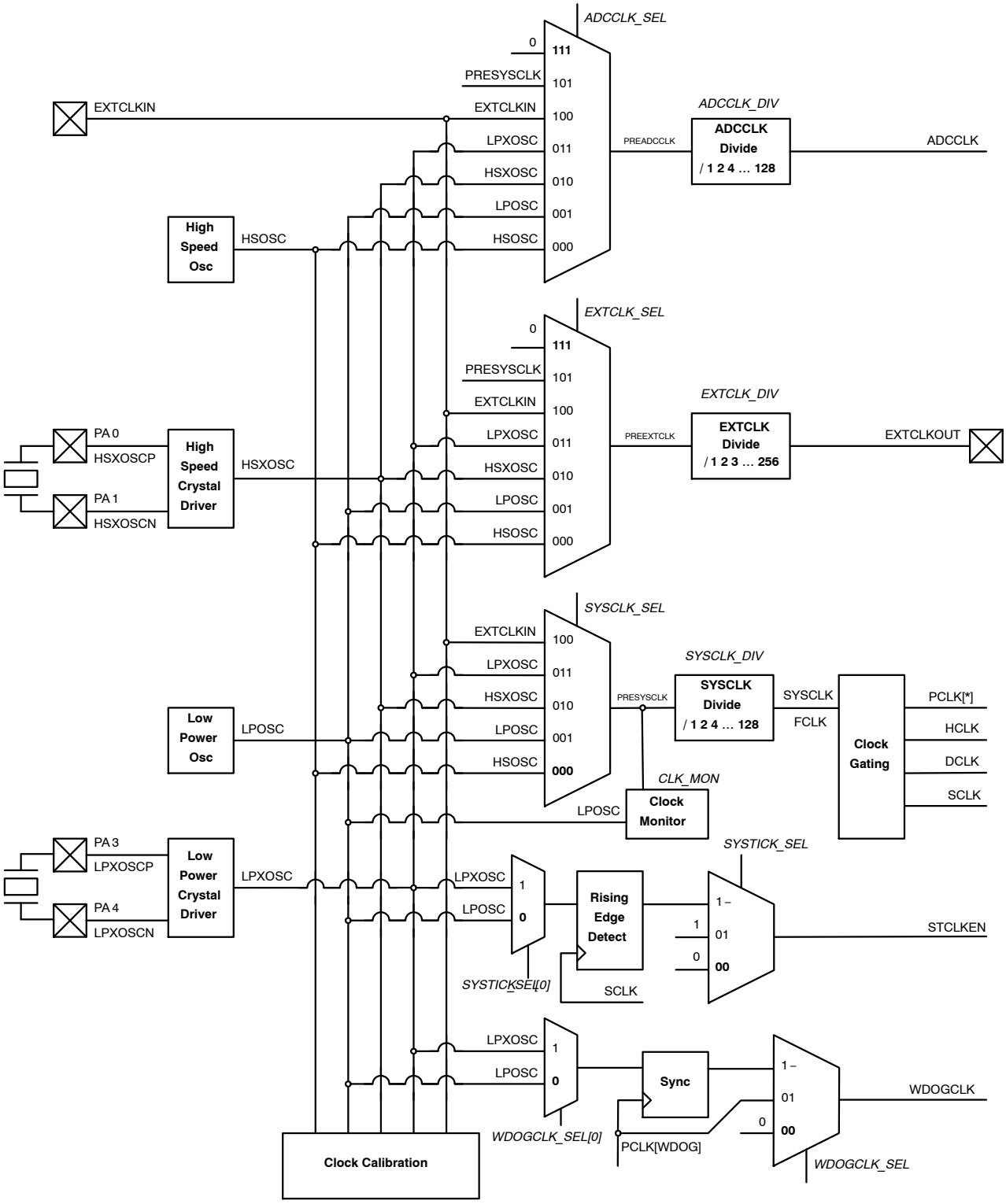


Figure 7. Clock Diagram

POWER MANAGEMENT AND MODES

AXM0F343 includes three power modes to achieve the power targets of various applications and functions. Power modes are configurable through software.

Run Mode

In run mode, all digital systems are powered and running including external and/or internal oscillators. The processor is executing code. Individual peripheral clocks can be gated based on configuration.

Sleep Mode

Sleep mode is the same as run mode except the Arm Cortex−M0+ processor is in sleep mode with the processor clock gated. Since the processor clock is gated, the processor is not executing code and the FLASH is in low power mode.

Some peripherals will maintain their clock in order to generate interrupts based on configuration. When an interrupt is detected, the processor wakes−up and enters run mode. Code execution starts from the last known location.

For lower Sleep Mode current disable the HSOSC and run from an external Crystal or the LPOSC.

Hibernate Mode

Hibernate mode powers off the CPU, FLASH, and most peripherals. Each SRAM bank may be configured to either power−off or retain its contents. The wake−up timer and GPIO pin toggle detection remain operational in Hibernate mode with a 1 V regulated supply to provide the wake−up condition. The low power RC oscillator is the only enabled clock. Waking up from Hibernate mode re−initializes the processor and code execution starts from the reset vector.

Shutdown Mode

In Shutdown mode all circuits are powered−off except for the scratch register and minimal logic used to detect a toggle on the PB3 pin for wake−up. Waking up from Shutdown mode re−initializes the processor and code execution starts from the reset vector.

32−bit Wake−up Timer

A wakeup timer can enable wakeup from Sleep Mode but not from Deep Sleep mode. See timers section.

Always−On Scratch Register

The main purpose of the scratch register is to provide 32−bits of state storage during low power modes. This is helpful in implementing a software flag to differentiate between startup modes (e.g. cold start vs. warm start). The scratch register is retained as long as there is power to the chip.

Table 16. POWER MODE TABLE

AXM0F343 Power Mode	Mode Entry	Mode Exit/Wake−up	Enabled Peripherals	FLASH Enabled	Memory Retention	Reset Core	Description
Run	Default	n/a	All enabled	Yes	All registers and SRAM	No	Core and peripherals enabled, clocks/peripherals active. Radio can be used in whatever mode required by application.
Sleep	WFI/WFE	Any enabled interrupt	All sleep enabled	Yes	All registers and SRAM	No	Core not executing. Most peripherals can be enabled. Radio can be used in whatever mode required by application.
Hibernate	WFI/WFE with deep sleep and hibernate bit set	Wakeup timer, GPIO interrupt, DBG_EN pin, reset	Wakeup timer, GPIO (level sensitive only), DBG_EN pin detection	No	Scratch register, GPIO state, optional SRAM	Yes	Core powered down. Wakeup and GPIO_WAKE powered. All clocks turned off if not needed for wakeup timer. Low voltage SRAM retention. Radio in Deepsleep
Shutdown	WFI/WFE with shutdown bit set	Wakeup pin, DBG_EN pin, reset	Wakup pin, DBG_EN pin	No	Scratch register, GPIO state	Yes	Lowest power mode. GPIO wakeup only.

EXCEPTION HANDLING

Nested Vectored Interrupt Controller (NVIC) and Wake Up Controller (WIC)

Arm Cortex−M0+ processor supports priority based nested vectored interrupts. AXM0F343 has 38 interrupts. It includes the 15 built−in or reserved exceptions and is configured with an additional 23 interrupts. These interrupts have 4 levels of programmable priority.

The priority of each group can be set separately by the firmware. While an interrupt is being serviced, only interrupts from a higher priority group will be serviced. If two interrupts of the same priority arrive at the same time, the earlier one in the polling order will be serviced first.

Only a subset of the interrupts are included in the wake−up controller. The NMI interrupt is optional and can be configured to be triggered by an external pin, the clock loss circuit, or a brownout condition.

For details see the *Cortex−M0+ Technical Reference Manual*.

Table 17. INTERRUPTS TABLE

Interrupt	Exception Number	Priority	Available in Sleep	Available in Hi-bernate	Available in Shutdown
Cortex M0+ – Reset	1	–3 (Highest)	Yes	No	No
Cortex M0+ – NMI (external pin, clock loss, or brownout)	2	–2	Yes	Yes	No
Cortex M0+ – Hard Fault	3	–1	No	No	No
Cortex M0+ Reserved	4 to 10	N/A	N/A	N/A	N/A
Cortex M0+ SVC	11	Programmable	No	No	No
Cortex M0+ Reserved	12 and 13	N/A	N/A	N/A	N/A
Cortex M0+ PendSV	14	Programmable	No	No	No
Cortex M0+ SysTick	15	Programmable	No	No	No
General Purpose I/O (GPIO)	16	Programmable	Yes	Yes	PB3
Wakeup Timer (WUT)	17	Programmable	Yes	Yes	No
Tick Timer (TICK)	18	Programmable	Yes	No	No
External Pin	19	Programmable	Yes	Yes	No
Analog Comparator (CMP)	20	Programmable	Yes	No	No
Analog to Digital Convertor (ADC)	21	Programmable	Yes	No	No
True Random Number Generator (TRNG)	22	Programmable	Yes	No	No
FLASH	23	Programmable	No	No	No
Watchdog (WDOG)	24	Programmable	No	No	No
Clock/System Config (CMU)	25	Programmable	Yes	No	No
Timer0 (TIM0)	26	Programmable	Yes	No	No
Timer1 (TIM1)	27	Programmable	Yes	No	No
Timer2 (TIM2)	28	Programmable	Yes	No	No
Compare/Capture/PWM 0 (CC_PMW0)	29	Programmable	Yes	No	No
Compare/Capture/PWM 1 (CC_PMW1)	30	Programmable	Yes	No	No
Compare/Capture/PWM 2 (CC_PMW2)	31	Programmable	Yes	No	No
Compare/Capture/PWM 3 (CC_PMW3)	32	Programmable	Yes	No	No
––Reserved––	33	N/A	N/A	N/A	N/A
Master/Slave SPI (SPI)	34	Programmable	Yes	No	No
Universal Synchronous/Asynchronous Receiver/Transmitter 0 (USART0)	35	Programmable	Yes	No	No
Universal Synchronous/Asynchronous Receiver/Transmitter 1 (USART1)	36	Programmable	Yes	No	No
I^2C (I2C)	37	Programmable	Yes	No	No
DMA_ERROR	38	Programmable	Yes	No	No
DMA_DONE	39	Programmable	Yes	No	No

EXTERNAL COMMUNICATION INTERFACES

Universal Synchronous/Asynchronous Receiver Transmitter (USART0/1)

AXM0F343 includes 2 USART devices with the following features:

- Standard Universal Synchronous/Asynchronous Receiver/Transmitter (full duplex)
- 5−9 bit word length
- 1−2 Stop bits
- Arbitrary baud rates can be generated using a general purpose 16−bit timer
- Support for even, odd, and no parity modes
- Break initiation and detection
- Optional receiver deglitch for improved noise immunity
- DMA support for RX/TX stream with SW flow control

Master/Slave Serial Peripheral Interface (SPI)

The Master/Slave Serial Peripheral Interface Controller is a synchronous serial data link controller that can be configured as either a SPI slave peripheral or a SPI master controller. A flexible clocking scheme allows it to connect to a variety of external SPI compatible peripherals or master controllers. The SPI controller has configuration options for:

- Data frame width (8, 16, 24, and 32−bit modes)
- Clock phase (CPHA) and polarity (CPOL)
- 4 or 3 wire mode SPI slave (with or without slave select functionality)
- Master clock source and clock pre−scale
- Data direction (MSB or LSB first)
- Interrupt generation for RX/TX events and slave select (SS) events
- DMA support for RX/TX stream

The SPI peripheral can also be used for additional serial data link protocols. It supports the 2−channel audio optimized I^2S protocol including the standard and left justified framing modes. It also supports PCM style data link protocols with both early and late frame syncing.

Master/Slave Inter−Integrated Circuit Controller (I^2C)

The I^2C interface is compatible with the Inter−IC Bus Specification from Philips Semiconductors. The I^2C interface uses a two−wire interface including a bidirectional clock line (SCL) and bidirectional data line (SDA). This interface is designed for communications with external devices. The I^2C interface will support both master and slave mode operation. The I^2C can connect to the DMA to support moving data without frequent intervention of the core.

TIMERS

System Tick Timer (SysTick)

The AXM0F343 implements the integrated system tick timer (SysTick). This system tick timer is owned by the software and is used for event scheduling. The SysTick timer can be clocked by the system clock or one of the low power clock sources.

32−bit Wakeup Timer (WUT)

The main purpose of the wakeup timer is to facilitate scheduled exit from Sleep Mode. It can also be used for general purpose event timing. The wakeup timing resolution depends on the programmable clock source and pre−scale ratios. Typically the slower (low power) clock sources are used to minimize power.

32−bit Tick Timer (TICK)

The tick timer is targeted for general purpose event scheduling. Like the SysTick timer, it is meant to support basic scheduler or RTOS functions during run mode. The tick timing resolution depends on the programmable clock source and pre−scale ratios. Typically the high speed clock sources are used for tighter timing resolution.

16−bit General Purpose Timers (TIM0/1/2)

AXM0F343 has three independent 16−bit general purpose timers. Each timer can be configured independently and differently.

The timers support the following functions:

- Count up, count down, and count up/down
- Timer clock pre−scaler
- Event capture/compare using CCPWM module
- Pulse width modulation (PWM) using CCPWM module
- Event counter (pulse counter)
- Increment by N capability
- Sigma−Delta DAC modulation mode
- USART baud rate generation

Watchdog Timer (WDOG)

The watchdog timer applies a reset to the system in the event of a software failure, providing a way to recover from software crashes. The watchdog timer is disabled by default and must be enabled through software. The watchdog module is based on a 32−bit down−counter that is initialized from a reload register. An interrupt is generated when the counter reaches 0. The counter then reloads and continues to count down. If the interrupt has not been serviced by the time the counter reaches 0 a second time a watchdog reset is issued.

The watchdog is protected with a lock mechanism to prevent rogue software from disabling the watchdog functionality. A special value has to be written to the lock register to access watchdog control.

Compare/Capture/PWM (CC_PWM0/1/2/3)

AXM0F343 has four 16−bit compare/capture/PWM units (CCPWM). They are used to capture event timing, compare timer values, and to generate pulse width modulated (PWM) outputs. Each CCPWM unit can be independently tied to any of the 16−bit general purpose timers. Multiple CCPWM units can be tied to the same timer.

Timer capture functionality can be triggered through various internal and external events.

Alignment of multiple PWM signals can be achieved by connecting multiple CCPWM to the same timer. If the timer is configured in either up or down count mode an edge aligned PWM stream is generated. If the timer is configured to ramp up to a count and then ramp down again a center aligned PWM stream is generated.

Each CCPWM unit can generate differential PWM signals with a programmable dead time in between transitions. This is useful in generation of non−overlapping (break before make) control signals.

SECURITY PERHIPHERALS

Advanced Encryption Standard (AES) Acceleration

Hardware Accelerated AES Encryption and Decryption is enabled with the AES block. In conjunction with software, the AES block allows a significant reduction in clocks cycles for AES encryption and decryption compared to a software−only solution.

Four functions are available to accelerate AES encryption and decryption:

- SubByte
- InvSubByte
- MixColumns
- InvMixColumns

The SubByte and InvSubByte each takes four clock cycles to complete, the MixColumns and InvMixColumns functions are each performed in a single clock cycle, thus dramatically improving the speed of AES encryption/decryption.

True Random Number Generator (TRNG)

The TRNG can produce 32−bit random numbers. It uses on−chip sources to generate a string of random bits. This is in contrast to pseudo−random number generators often used, which only look random but are generated by a deterministic algorithm.

For high security applications, bits from the TRNG should not be used directly. Bits should be mixed into an entropy pool first. The AES block can be used for this operation.

Cyclic Redundancy Check (CRC)

The CRC module is a peripheral that calculates a 32−bit CRC using the standard Ethernet polynomial 0x04C11DB7 (EN/IEC 60335−1 standard). This provides a means to verify the integrity of the FLASH memory or other range of addresses. The CRC calculation is in a single processor cycle for each new word that is written to the CRC. The DMA can be used to facilitate the CRC check over a specified address range.

ANALOG PERIPHERALS

Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture ADC with up to 12 bits of resolution. It supports both differential sampling as well as (pseudo) single−ended sampling. Internal analog signal multiplexing allows sampling of 6 external single−ended signals or 3 differential pairs channels on the analog capable PA I/O bank. It can also sample various internal references, supplies, and the internal temperature sensor. A programmed sequence of sampling over multiple channels can be configured. The ADC can operate up to 1.25 MSPS. The actual sample rate is controlled by the selected clock source and divide value. The reference voltage for the ADC is programmable to be either the 1.0 V reference voltage, VDDIO / 2 reference, or an external reference. The common mode input voltage is approximately AVDD / 2 (1.8 V / 2 = 0.9 V)

A gain block feeds into the ADC. It has programmable gain options of 10x gain, unity gain, and 1/4x gain. The gain block can also be bypassed.

When using the gain block, the output signal swing is limited to the range within 250 mV of GND and AVDD (the internal 1.8 V regulator). If using the gain block, the maximum input voltage applied to the ADC is limited to the lesser of VDDIO or 3.3 V. If the gain block is in bypass mode, the maximum input voltage applied to the ADC is limited to the lesser of AVDD or 2.1 V.

Temperature Sensor

AXM0F343 has a temperature sensor circuit that feeds into the input of the ADC. The ADC converted temperature sensor provides internal temperature measurement.

Analog Comparators (CMP0/1)

AXM0F343 includes two comparators with hysteresis. Comparator inputs can be selected from a subset of I/O pins from the analog capable PA bank or internal references.

RF TRANSCEIVER BLOCK

Crystal Oscillator and TCXO Interface (RF Reference Oscillator)

The AXM0F343 is normally operated with an external TCXO, which is required by most narrow−band regulation with a tolerance of 0.5 ppm to 1.5 ppm depending on the regulation. The on−chip crystal oscillator allows the use of an inexpensive quartz crystal as the RF generation subsystem's timing reference when possible from a regulatory compliance perspective.

A wide range of crystal frequencies can be handled by the crystal oscillator circuit. As the reference frequency impacts both the spectral performance of the transmitter as well as the current consumption of the receiver, the choice of reference frequency should be made according to the regulatory regime targeted by the application.

The crystal or TCXO reference frequency should be chosen so that the RF carrier frequency is not an integer multiple of the crystal or TCXO frequency. If the reference frequency is chosen as an integer multiple of the crystal frequency undesired spurs will be in the Tx spectrum and are likely to cause regulatory compliance problems.

The oscillator circuit is enabled by programming the AX5043_PWRMODE register. At Power On Reset it is enabled. To adjust the circuit's characteristics to the quartz crystal being used, without using additional external components, the tuning capacitance of the crystal oscillator can be programmed. The transconductance of the oscillator is automatically regulated, to allow for fastest start−up times together with lowest power operation during steady−state oscillation.

The integrated programmable tuning capacitor bank makes it possible to connect the quartz crystal directly to pins CLKN and CLKP without the need for external capacitors. It is programmed using bits XTALCAP[5:0] in register AX5043_XTALCAP.

To synchronize the receiver frequency to a carrier signal, the oscillator frequency could be tuned using the capacitor bank. The recommended method to implement frequency synchronization is to make use of the high resolution RF frequency generation sub−system together with the Automatic Frequency Control, both are described later in the document.

Alternatively a single ended reference (TXCO, VCXO) may be used. The CMOS levels should be applied to CLKP via an AC coupling with the crystal oscillator enabled. For detailed TCXO network recommendations depending on TCXO output swing refer to the AND9405/D.

Low Power Oscillator and Wake on Radio (WOR) Mode

The AXM0F343 transceiver features an internal ultra−low power oscillator. In default mode the frequency of oscillation is 640 Hz ±1.5%, in fast mode it is 10.2 kHz ±1.5%.

If Wake on Radio Mode is enabled, the receiver wakes up periodically at a user selectable interval, and checks for a radio signal on the selected channel. If no signal is detected, the receiver shuts down again. If a radio signal is detected, and a valid packet is received, the microcontroller is alerted by asserting an interrupt.

SYSCLK Output

The SYSCLK pin outputs the RF reference clock signal divided by a programmable integer. Divisions from 1 to 2048 are possible. For divider ratios > 1 the duty cycle is 50%. Bits SYSCLK[3:0] in the AX5043_PINCFG1 register set the divider ratio. Certain choices of output frequencies may negatively impact the transmit spectrum. Receiving at an integer multiple of the SYSCLK frequency comes at a significant sensitivity penalty. The SYSCLK output should be disabled if not used.

RF Frequency Generation Subsystem

The RF frequency generation subsystem consists of a fully integrated synthesizer, which multiplies the reference frequency from the crystal oscillator to get the desired RF frequency. The advanced architecture of the synthesizer enables frequency resolutions of 1 Hz, as well as fast settling times of 5 – 50 μs depending on the settings (see section AC Characteristics). Fast settling times mean fast start−up and fast RX/TX switching, which enables low−power system design.

For receive operation the RF frequency is fed to the mixer, for transmit operation to the power−amplifier.

The frequency must be programmed to the desired carrier frequency.

The synthesizer loop bandwidth can be programmed, this serves three purposes:

1. Start−up time optimization, start−up is faster for higher synthesizer loop bandwidths
2. TX spectrum optimization, phase−noise at 300 kHz to 1 MHz distance from the carrier improves with lower synthesizer loop bandwidths
3. Adaptation of the bandwidth to the data−rate. For transmission of FSK and MSK the synthesizer bandwidth must be large enough to let the modulation signal pass.

VCO

An on−chip VCO converts the control voltage generated by the charge pump and loop filter into an output frequency. This frequency is used for transmit as well as for receive operation. The frequency can be programmed in 1 Hz steps in the AX5043_FREQ registers. For operation in the 433 MHz band, the RFDIV bit in the AX5043_PLLVCODIV register must be programmed.

The fully integrated VCO allows to operate the device in the frequency ranges 800 – 1050 MHz and 400 – 520 MHz. The carrier frequency range can be extended to 54 – 525 MHz and 27 – 262 MHz by using an appropriate external inductor between device pins L1 and L2. The bits VCO2INT and VCOSEL in the AX5043_PLLVCODIV register must be set high to enter this mode.

It is also possible to use a fully external VCO by setting bits VCO2INT = 0 and VCOSEL = 1 in the AX5043_PLLVCODIV register. A differential input at a frequency of double the desired RF frequency must be input at device pins L1 and L2. The control voltage for the VCO can be output at device pin FILT when using external filter mode. The voltage range of this output pin is 0 – 1.8 V. This mode of operation is recommended for special applications where the phase noise requirements are not met when using the fully internal VCO or the internal VCO with external inductor.

VCO Auto−Ranging

The AXM0F343 has an integrated auto−ranging function, which allows to set the correct VCO range for specific frequency generation subsystem settings automatically. Typically it has to be executed after power−up. The function is initiated by setting the RNG_START bit in the AX5043_PLLRANGINGA or AX5043_PLLRANGINGB register. The bit is readable and a 0 indicates the end of the ranging process. Setting RNG_START in the AX5043_PLLRANGINGA register ranges the frequency in AX5043_FREQA, while setting RNG_START in the AX5043_PLLRANGINGB register ranges the frequency in AX5043_FREQB. The RNGERR bit indicates the correct execution of the auto−ranging. VCO auto−ranging works with the fully integrated VCO and with the internal VCO with external inductor.

Loop Filter and Charge Pump

The AXM0F343 internal loop filter configuration together with the charge pump current sets the synthesizer loop band width. The internal loop−filter has three configurations that can be programmed via the register bits FLT[1:0] in registers AX5043_PLLLOOP or AX5043_PLLLOOPBOOST the charge pump current can be programmed using register bits PLLCPI[7:0] in registers AX5043_PLLCPI or AX5043_PLLCPIBOOST.

Synthesizer bandwidths are typically 50 – 500 kHz depending on the AX5043_PLLLOOP or AX5043_PLLLOOPBOOST settings, for details see the section: AC Characteristics.

The AXM0F343 can be setup in such a way that when the synthesizer is started, the settings in the registers AX5043_PLLLOOPBOOST and

AX5043_PLLCPIBOOST are applied first for a programmable duration before reverting to the settings in AX5043_PLLLOOP and AX5043_PLLCPI. This feature enables automated fastest start−up.

Setting bits FLT[1:0] = 00 bypasses the internal loop filter and the VCO control voltage is output to an external loop filter at pin FILT. This mode of operation is recommended for achieving lower bandwidths than with the internal loop filter and for usage with a fully external VCO.

Table 18. RF FREQUENCY GENERATION REGISTERS

Register	Bits	Purpose
AX5043_PLLLOOP AX5043_PLLLOOPBOOST	FLT[1:0]	Synthesizer loop filter bandwidth and selection of external loop filter, recommended usage is to increase the bandwidth for faster settling time, bandwidth increases of factor 2 and 5 are possible.
AX5043_PLLCPI AX5043_PLLCPIBOOST		Synthesizer charge pump current, recommended usage is to decrease the bandwidth (and improve the phase−noise) for low data−rate transmissions.
AX5043_PLLVCODIV	REFDIV	Sets the synthesizer reference divider ratio.
	RFDIV	Sets the synthesizer output divider ratio.
	VCOSEL	Selects either the internal or the external VCO
	VCO2INT	Selects either the internal VCO inductor or an external inductor between pins L1 and L2
AX5043_FREQA, AX5043_FREQB		Programming of the carrier frequency
AX5043_PLLRANGINGA, AX5043_PLLRANGINGB		Initiate VCO auto−ranging and check results

RF Input and Output Stage (ANTP/ANTN/ANTP1)

The AXM0F343 has two main antenna interface modes:

1. Both RX and TX use differential pins ANTP and ANTN. RX/TX switching is handled internally. This mode is recommended for highest output powers, highest sensitivities and for direct connection to dipole antennas.
2. RX uses the differential antenna pins ANTP and ANTN. TX uses the single ended antenna pin ANTP1. RX/TX switching is handled externally. This can be done either with an external RX/TX switch or with a direct tie configuration. This mode is recommended for low output powers at high efficiency.

When antenna diversity is enabled, the radio controller will, when not in the middle of receiving a packet, periodically probe both antennas and select the antenna with the highest signal strength. The radio controller can be instructed to periodically write both RSSI values into the FIFO. Antenna diversity mode is fully automatic.

LNA

The LNA amplifies the differential RF signal from the antenna and buffers it to drive the I/Q mixer. An external matching network is used to adapt the antenna impedance to the IC impedance. A DC feed to GND must be provided at the antenna pins.

PA

In TX mode the PA drives the signal generated by the frequency generation subsystem out to either the differential antenna terminals or to the single ended antenna pin. The antenna terminals are chosen via the bits TXDIFF and TXSE in register AX5043_MODECFGA.

The output power of the PA is programmed via the register AX5043_TXPWRCOEFFB.

The PA can be digitally pre−distorted for high linearity.

The output amplitude can be shaped (raised cosine), this mode is selected with bit AMPLSHAPE in register AX5043_MODECFGA PA ramping is programmable in increments of the bit time and can be set to 1 – 8 bit times via bits SLOWRAMP in register AX5043_MODECFGA.

The output power as well as harmonic content will depend on the external impedance seen by the PA.

Digital IF Channel Filter and Demodulator

The digital IF channel filter and the demodulator extract the data bit−stream from the incoming IF signal. They must be programmed to match the modulation scheme as well as the data−rate. Inaccurate programming will lead to loss of sensitivity.

The channel filter offers bandwidths of 995 Hz up to 221 kHz.

An overview of the registers involved is given in the following table as reference, for details see the AND9347/D. The register setups typically must be done once at power−up of the device.

Registers

Table 19. CHANNEL FILTER AND DEMODULATOR REGISTERS

Register	Remarks
AX5043_DECIMATION	This register programs the bandwidth of the digital channel filter.
AX5043_RXDATARATE2… AX5043_RX− DATARATE0	These registers specify the receiver bit rate, relative to the channel filter bandwidth.
AX5043_MAXDROFFSET2… AX5043_MAXDROFFSET0	These registers specify the maximum possible data rate offset
AX5043_MAXRFOFFSET2… AX5043_MAXRFOFFSET0	These registers specify the maximum possible RF frequency offset
AX5043_TIMEGAIN, AX5043_DRGAIN	These registers specify the aggressiveness of the receiver bit timing recovery. More aggressive settings allow the receiver to synchronize with shorter preambles, at the expense of more timing jitter and thus a higher bit error rate at a given signal−to−noise ratio.
AX5043_MODULATION	This register selects the modulation to be used by the transmitter and the receiver, i.e. whether ASK, FSK should be used.
AX5043_PHASEGAIN, AX5043_FREQGAINA, AX5043_FREQGAINB, AX5043_FREQGAINC, AX5043_FREQGAIND, AX5043_AMPLGAIN	These registers control the bandwidth of the phase, frequency offset and amplitude tracking loops.
AX5043_AGCGAIN	This register controls the AGC (automatic gain control) loop slopes, and thus the speed of gain adjustments. The faster the bit−rate, the faster the AGC loop should be.
AX5043_TXRATE	These registers control the bit rate of the transmitter.
AX5043_FSKDEV	These registers control the frequency deviation of the transmitter in FSK mode. The receiver does not explicitly need to know the frequency deviation, only the channel filter bandwidth has to be set wide enough for the complete modulation to pass.

Encoder

The encoder is located between the Framing Unit, the Demodulator and the Modulator. It can optionally transform the bit−stream in the following ways:

- It can invert the bit stream.
- It can perform differential encoding. This means that a zero is transmitted as no change in the level, and a one is transmitted as a change in the level.

- It can perform Manchester encoding. Manchester encoding ensures that the modulation has no DC content and enough transitions (changes from 0 to 1 and from 1 to 0) for the demodulator bit timing recovery to function correctly, but does so at doubling of the data rate.
- It can perform spectral shaping (also know as whitening). Spectral shaping removes DC content of the bit stream, ensures transitions for the demodulator bit timing recovery, and makes sure that the transmitted spectrum does not have discrete lines even if the transmitted data is cyclic. It does so without adding additional bits, i.e. without changing the data rate.

Spectral Shaping uses a self synchronizing feedback shift register.

The encoder is programmed using the register AX5043_ENCODING, details and recommendations on usage are given in the AND9347/D.

Framing and FIFO

Most radio systems group data into packets. The framing unit is responsible for converting these packets into a bit−stream suitable for the modulator, and to extract packets from the continuous bit−stream arriving from the demodulator.

The Framing unit supports two different modes:

- Packet modes
- Raw modes

The microcontroller communicates with the framing unit through a 256 byte FIFO. Data in the FIFO is organized in Chunks. The chunk header encodes the length and what data is contained in the payload. Chunks may contain packet data, but also RSSI, Frequency offset, Timestamps, etc.

The AXM0F343 contains one FIFO. Its direction is switched depending on whether transmit or receive mode is selected.

The FIFO can be operated in polled or interrupt driven modes. In polled mode, the microcontroller must periodically read the FIFO status register or the FIFO count register to determine whether the FIFO needs servicing.

In interrupt mode EMPTY, NOT EMPTY, FULL, NOT FULL and programmable level interrupts are provided. Interrupts are acknowledged by removing the cause for the interrupt, i.e. by emptying or filling the FIFO.

Packet Modes

The AXM0F343 offers different packet modes. For arbitrary packet sizes HDLC is recommended. The AXM0F343 also offers packet modes with fixed packet length with a byte indicating the length of the packet.

In packet modes a CRC can be computed automatically. HDLC Mode is the main framing mode of the AXM0F343. In this mode, the AXM0F343 performs automatic packet delimiting, and optional packet correctness check by inserting and checking a cyclic redundancy check (CRC) field.

NOTE: HDLC mode follows High−Level Data Link Control (HDLC, ISO 13239) protocol.

The packet structure is given in the following table.

Table 20. HDLC PACKET STRUCTURE

Flag	Address	Control	Information	FCS	(Optional Flag)
8 bit	8 bit	8 or 16 bit	Variable length, 0 or more bits in multiples of 8	16 / 32 bit	8 bit

HDLC packets are delimited with flag sequences of content 0x7E.

In AXM0F343 the meaning of address and control is user defined. The Frame Check Sequence (FCS) can be programmed to be CRC−CCITT, CRC−16 or CRC−32.

The receiver checks the CRC, the result can be retrieved from the FIFO, the CRC is appended to the received data.

In Wireless M−Bus framing mode, the packet structure is given in the following table.

NOTE: Wireless M−Bus mode follows EN13757−4

Table 21. WIRELESS M−BUS PACKET STRUCTURE

Preamble	L	C	M	A	FCS	Optional Data Block (Optionally Repeated with FCS)	FCS
variable	8 bit	8 bit	8 bit	8 bit	16 bit	8 – 96 bit	16 bit

Raw Modes (Advanced Users)

In Raw mode, the AXM0F343 does not perform any packet delimiting or byte synchronization. It simply serializes transmit bytes and de−serializes the received bit−stream and groups it into bytes. This mode is ideal for implementing legacy protocols in software.

Raw mode with preamble match is similar to raw mode. In this mode, however, the receiver does not receive anything until it detects a user programmable bit pattern (called the preamble) in the receive bit−stream. When it detects the preamble, it aligns the de−serialization to it.

The preamble can be between 4 and 32 bits long.

Customers still need to program parts of the radio to use raw mode, more details can be found in the AND9347/D.

RX AGC and RSSI

AXM0F343 features three receiver signal strength indicators (RSSI):

1. RSSI before the digital IF channel filter.
   The gain of the receiver is adjusted in order to keep the analog IF filter output level inside the working range of the ADC and demodulator. The register AX5043_AGCCOUNTER contains the current value of the AGC and can be used as an RSSI. The step size of this RSSI is 0.625 dB. The value can be used as soon as the RF frequency generation sub−system has been programmed.
2. RSSI behind the digital IF channel filter.
   The register AX5043_RSSI contains the current value of the RSSI behind the digital IF channel filter. The step size of this RSSI is 1 dB.
3. RSSI behind the digital IF channel filter high accuracy. The demodulator also provides amplitude information in the AX5043_TRK_AMPLITUDE register. By combining both the AX5043_AGCCOUNTER and the AX5043_TRK_AMPLITUDE registers, a high resolution (better than 0.1 dB) RSSI value can be computed at the expense of a few arithmetic operations on the micro−controller.

Modulator

Depending on the transmitter settings the modulator generates various inputs for the PA:

Table 22. MODULATIONS

Modulation	Bit = 0	Bit = 1	Main Lobe Bandwidth	Max. Bitrate
ASK	PA off	PA on	BW = BITRATE	125 kBit/s
FSK/MSK/GFSK/GMSK	$\Delta f = -f_{deviation}$	$\Delta f = +f_{deviation}$	BW = (1 + h) · BITRATE	125 kBit/s
PSK	$\Delta\Phi = 0°$	$\Delta\Phi = 180°$	BW = BITRATE	125 kBit/s

h = modulation index. It is the ratio of the deviation compared to the bit−rate; $f_{deviation} = 0.5 \cdot h \cdot BITRATE$, AXM0F343 can demodulate signals with $h < 32$.

ASK = amplitude shift keying FSK = frequency shift keying

MSK= minimum shift keying; MSK is a special case of FSK, where h = 0.5, and therefore

$f_{deviation} = 0.25 \cdot BITRATE$; the advantage of MSK over FSK is that it can be demodulated more robustly.

PSK = phase shift keying

All modulation schemes, except 4−FSK, are binary. Amplitude can be shaped using a raised cosine waveform.

Amplitude shaping will also be performed for constant amplitude modulation ((G)FSK, (G)MSK) for ramping up and down the PA. Amplitude shaping should always be enabled.

Frequency shaping can either be hard (FSK, MSK), or Gaussian (GMSK, GFSK), with selectable BT = 0.3 or BT = 0.5.

4−FSK Frequency is always hard shaping.

Table 23. 4−FSK MODULATION

Modulation	DiBit = 00	DiBit = 01	DiBit = 11	DiBit = 10	Main Lobe Bandwidth	Max. Bitrate
4−FSK	$\Delta f = -3f_{deviation}$	$\Delta f = -f_{deviation}$	$\Delta f = +f_{deviation}$	$\Delta f = +3f_{deviation}$	BW = (1 + 3 h) · BITRATE	125 kBit/s

Automatic Frequency Control (AFC)

The AXM0F343 features an automatic frequency tracking loop which is capable of tracking the transmitter frequency within the RX filter band width. On top of that the AXM0F343 has a frequency tracking register AX5043_TRKRFFREQ to synchronize the receiver frequency to a carrier signal. For AFC adjustment, the frequency offset can be computed with the following formula:

$$\Delta f = \frac{AX5043\_TRKRFFREQ}{2^{32}} f_{XTAL} \qquad \text{(eq. 2)}$$

PWRMODE Register

The AXM0F343 transceiver features its own independent power management, independent from the microcontroller. The AX5043_PWRMODE register controls which parts of the transceiver are operating.

Table 24. RADIO PWRMODE REGISTER

AX5043_PWRMODE Register	Name	Description
0000	POWERDOWN	All digital and analog functions, except the register file, are disabled. The core supply voltages are switched off to conserve leakage power. Register contents are preserved. Access to the FIFO is not possible and the contents are not preserved. POWERDOWN mode is only entered once the FIFO is empty.
0001	DEEPSLEEP	The transceiver is fully turned off. All digital and analog functions are disabled. All register contents are lost. To leave DEEPSLEEP mode the pin SEL has to be pulled low. This will initiate startup and reset of the transceiver. Then the MISO line should be polled, as it will be held low during initialization and will rise to high at the end of the initialization, when the chip becomes ready for operation. It is recommended to use the functions ax5043_enter_deepsleep() and ax5043_wakeup_deepsleep() provided in libmf
0101	STANDBY	The crystal oscillator and the reference are powered on; receiver and transmitter are off. Register contents are preserved and accessible. Access to the FIFO is not possible and the contents are not preserved. STANDBY is only entered once the FIFO is empty.
0110	FIFO	The reference is powered on. Register contents are preserved and accessible. Access to the FIFO is possible and the contents are preserved.
1000	SYNTHRX	The synthesizer is running on the receive frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for receive.
1001	FULLRX	Synthesizer and receiver are running.
1011	WOR	Receiver wakeup−on−radio mode. The mode the same as POWERDOWN, but the 640 Hz internal low power oscillator is running.
1100	SYNTHTX	The synthesizer is running on the transmit frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for transmit.
1101	FULLTX	Synthesizer and transmitter are running. Do not switch into this mode before the synthesizer has completely settled on the transmit frequency (in SYNTHTX mode), otherwise spurious spectral transmissions will occur.

Table 25. A TYPICAL AX5043_PWRMODE SEQUENCE FOR A TRANSMIT SESSION

Step	PWRMODE	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3 ms.
3	FULLTX	Data transmission
4	POWERDOWN	

Table 26. A TYPICAL AX5043_PWRMODE SEQUENCE FOR A RECEIVE SESSION

Step	PWRMODE [3:0]	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3 ms.
3	FULLRX	Data reception
4	POWERDOWN	

Voltage Regulator

The AXM0F343 transceiver uses its own dedicated on−chip voltage regulator system to create stable supply voltages for the internal circuitry from the primary supply VDD_IN. The I/O level of the digital pins is VDD_IN.

Pins VDD_ANA are supplied for external decoupling of the power supply used for the on−chip PA.

The voltage regulator system must be set into the appropriate state before receive or transmit operations can be initiated. This is handled automatically when programming the device modes via the AX5043_PWRMODE register.

Register AX5043_POWSTAT contains status bits that can be read to check if the regulated voltages are ready (bit SVIO) or if VDD_IN has dropped below the brown−out level of 1.3 V (bit SSUM).

In power−down mode the core supply voltages for digital and analog functions are switched off to minimize leakage power. Most register contents are preserved but access to the FIFO is not possible and FIFO contents are lost.

In deep−sleep mode all supply voltages are switched off. All digital and analog functions are disabled. All register contents are lost.

Typical Application Diagrams and Components

For details on possible radio application diagrams and choice of components for the matching network at different operating frequencies, please consult the AX5043 datasheet at https://www.onsemi.com/pdf/datasheet/ax5043−d.pdf or visit the Community Forum at https://www.onsemi.com/forum/.

ORDERING INFORMATION

Device	FLASH Size	RAM Size	Package	OPN	Shipping†
AXM0F343−64	64 kB	8 kB	QFN40 (Pb−Free, Halide Free)	AXM0F343−64−1−TX40	4000 / Tape & Reel
AXM0F343−256	256 kB	32 kB	QFN40 (Pb−Free, Halide Free)	AXM0F343−256−1−TX40	4000 / Tape & Reel

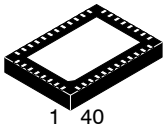
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

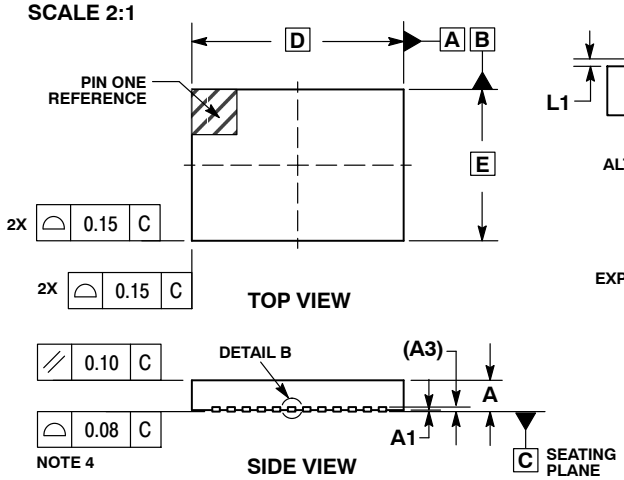
ON Semiconductor®

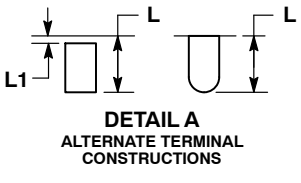
QFN40 7x5, 0.5P
CASE 485EG
ISSUE B

DATE 26 APR 2017

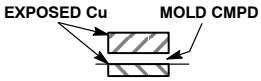


SCALE 2:1

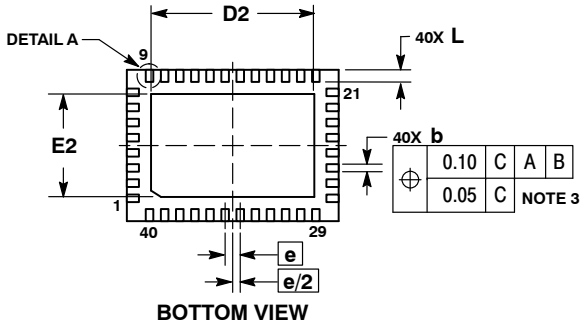




DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION

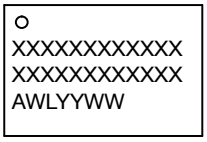


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	7.00 BSC	
D2	5.30	5.50
E	5.00 BSC	
E2	3.30	3.50
e	0.50 BSC	
L	0.30	0.50
L1	---	0.15

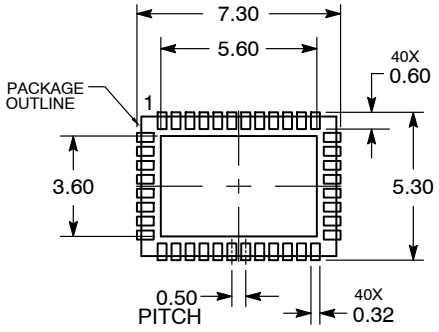
GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**QFN40 7X5, 0.5P**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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