ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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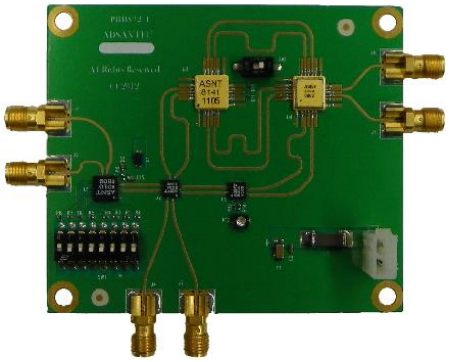
ASNT_PRBS32_1
8*Gbps*-34*Gbps* 2^7-1 PRBS Generator with Sync Output



- Broadband frequency range from 8*Gbps* – 34*Gbps*
- On board data rate multiplexer to reduce the input clock frequency rate
- Adjustable phase shift for multiplexer clock input
- 1-256 divide sync output
- Differential inputs and outputs
- Minimal insertion jitter
- Fast rise and fall times
- 50% duty cycle sync output on all divide ratios
- Single +3.3*V* supply

DESCRIPTION

The ASNT_PRBS32_1 is a broadband 2^7-1 PRBS generator intended for test, prototyping, microwave, and communication applications. A single-ended or differential clock from 4*GHz* to 17*GHz* can be used. A differential Sync Output can divide an input clock from 1 to 256. The Sync Output is capable of displaying an eye diagram at divide-by-16, and a PRBS waveform output for 127 or 254. The PRBS 2^7-1 waveform output is multiplexed to double the data rate, giving a maximum data rate of 34*Gbps*. An on board trim potentiometer allows to phase adjust the multiplexer clock input for all input clock frequencies in a specified range to ensure the best output is achieved. To set up the PRBS waveform output, set the divider ratio to 127 for sync and adjust the trim potentiometer to get the best pulse waveform at the output of the PRBS generator. An on board PRBS reset switch is included to preset the generator to avoid the all zero state lock-up.

The ASNT_PRBS32_1 board contains six Emerson SMA connectors MFG PN: 142-0761-881, 50*Ohm* transmission lines to the device, and power supply decoupling networks on the evaluation board. Power is supplied through a two-pin MOLEX connector P/N: 39-28-1023.

Sync Output

The Sync Output can be configured to output any divide ratio from 1 to 256 of the clock input. It contains eight switches that represent 8 bits. The LSB starts at SW1 and the MSB ends at SW8. The binary value of zero gives a decimal n value of 256. Increasing binary values increases the decimal value n as shown in Table 1.

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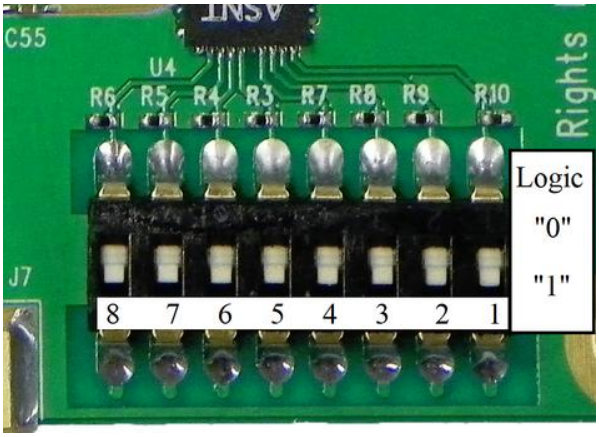
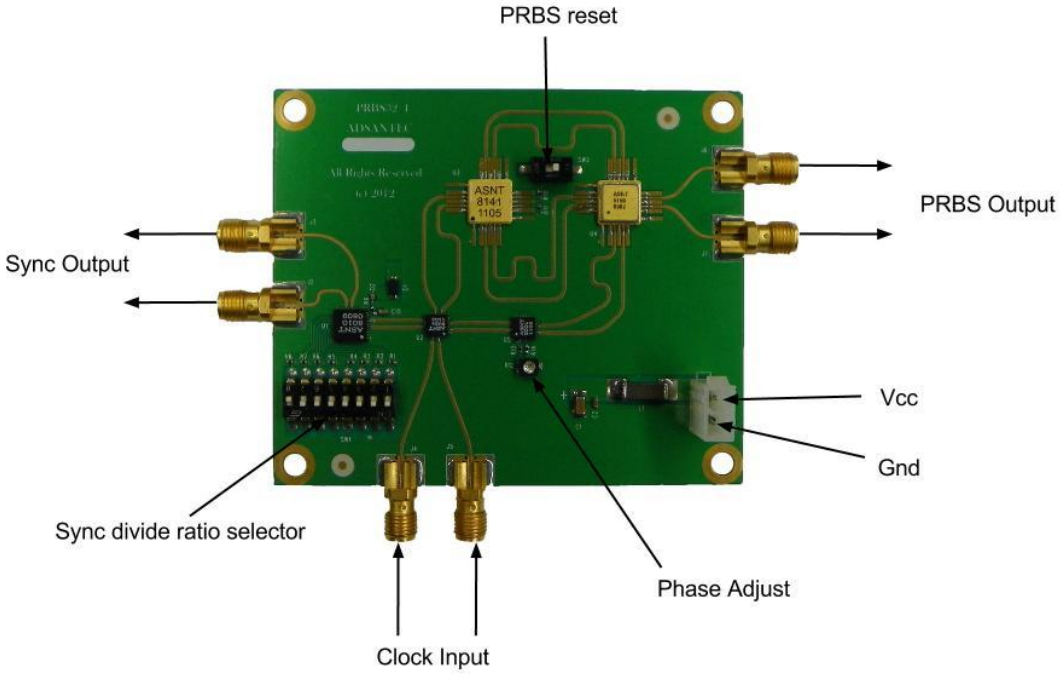


Table 1. Divide ratio

DIP SW #	n Divide Ratio	
8 7 6 5 4 3 2 1		
0 0 0 0 0 0 0 1	1	
0 0 0 0 0 0 1 0	2	
0 0 0 1 0 0 0 0	16	Eye diagram
.		
0 1 1 1 1 1 1 1	127	pattern
1 1 1 1 1 1 1 0	254	pattern
0 0 0 0 0 0 0 0	256	

TERMINAL FUNCTIONS



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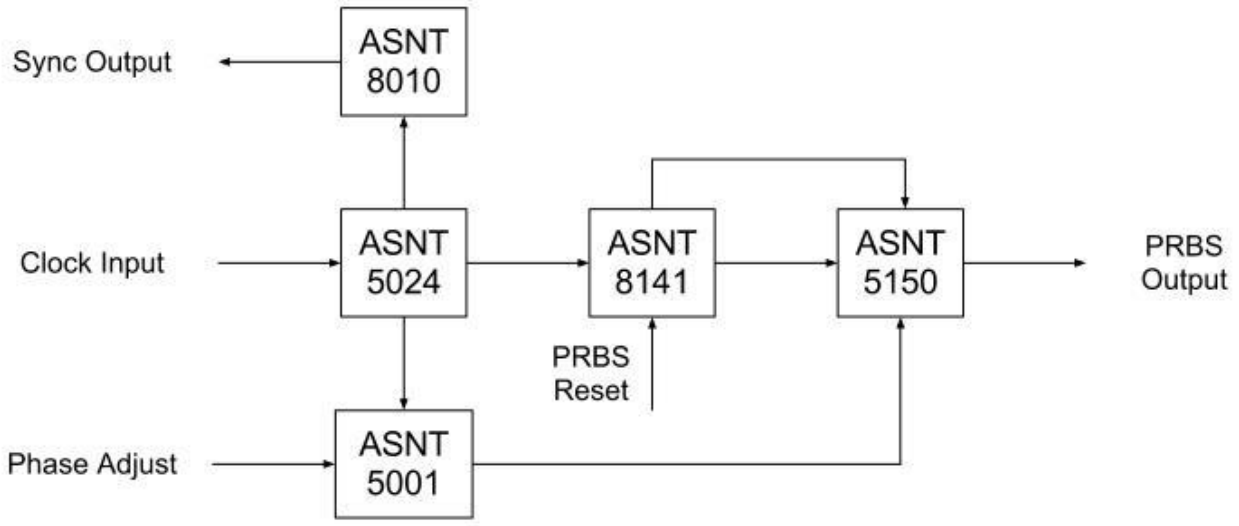
FUNCTIONAL BLOCK DIAGRAM



OPERATION

1. Measure 50*Ohms* on all SMA connectors referenced to vcc.
2. Set the PRBS Reset switch to the off position.
3. Set the power supply to 0*V* and current limit it to 1.7*A*.
4. Connect the power supply to the board and slowly increase to +3.3*V*.
5. Apply an AC coupled single-ended/differential clock signal to the Clock Input.
6. Connect PRBS Output to a 50*Ohm* terminated oscilloscope single-ended/differentially.
7. Connect Sync Output to trigger single-ended/differentially.

   Note: If using single-ended input/output only, apply an AC coupled 50*Ohm* termination to the unused input/output. This will reduce any noise present.

7. Toggle PRBS Reset to turn on the PRBS pattern.
8. Use a divide by 16 for the Sync Output to view the eye pattern on the oscilloscope.
9. Change Phase Adjust to tune the sampling point and achieve the best eye waveform output.

   Note: If the clock input rate is changed, repeat steps 7 and 9.

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MEASURED RESULTS

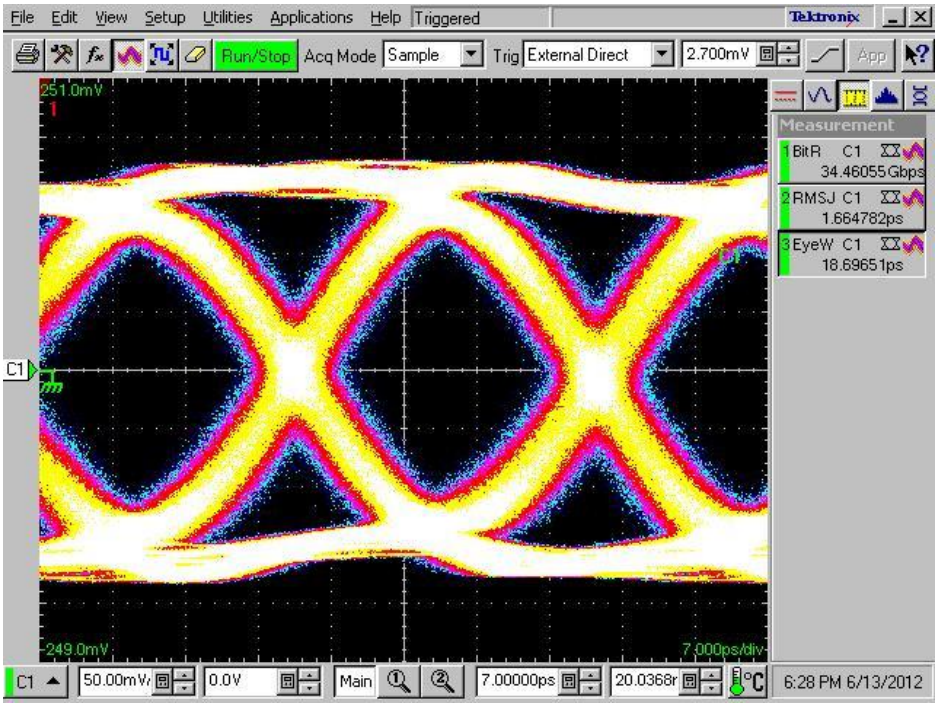

Fig. 1. 34Gbps eye diagram

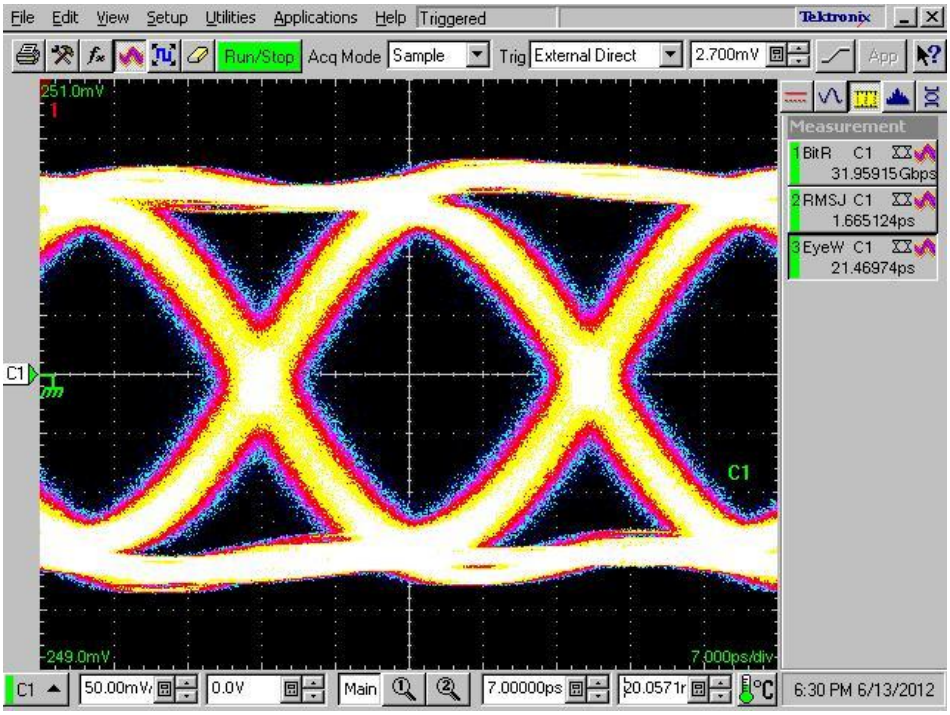

Fig. 2. 32Gbps eye diagram

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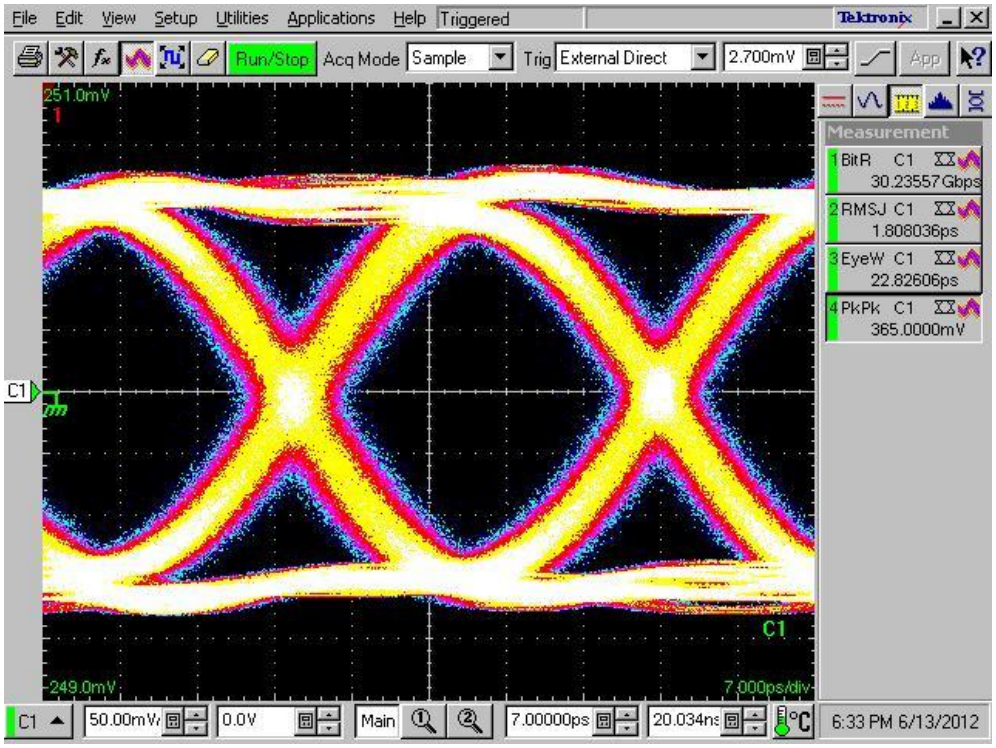

Fig. 3. 30Gbps eye diagram

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ELECTRICAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Comments
vee		0		*V*	External ground
vcc	3.1	3.3	3.5	*V*	
I_{VCC}	1.32	1.65	1.98	*A*	
Power		5.4		*W*	
Operating Temperature	-25	50	85	*°C*	
Clock Input					
Frequency	4		17	*GHz*	
Single-Ended Swing	50	400	1000	*mV*	Peak-to-Peak
Common mode level	vcc -0.8	vcc -0.2	vcc	*V*	
Duty Cycle	40%	50%	60%		Range of input tolerance
Sync Output					
Frequency	0.007		17	*GHz*	
Single-Ended Swing	570	600	630	*mV*	Peak-to-Peak
Common-Mode Level	vcc - (Single-Ended Swing)/2				
Rise/Fall Times	15	17	19	*ps*	20% to 80%
Duty Cycle	45%	50%	55%		For clock signal
PRBS Output					
Data rate	8		34	*Gbps*	
Single-Ended Voltage Level	380	400	420	*mV*	Peak-to-Peak
Common Mode Level	vcc - (Single-Ended Swing)/2			*V*	
Duty Cycle	40%	50%	60%		
Rise/Fall Time	6	8	10	*ps*	20% to 80%

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REVISION HISTORY

Revision	Date	Changes
1.8.2	07-2019	Updated Letterhead
1.8.1	04-2019	Added P/N of connectors to board description
1.7.1	06-2017	Revised Electrical Characteristics
1.6.1	04-2014	Changed Minimum Data Output Rate to 8Gbps
1.5.1	08-2013	Changed Diagrams & Pictures Changed Minimum Data Output Rate
1.4.1	07-2013	Updated Title & Formatting Revised Electrical Characteristics
1.3.1	06-2013	Data Rate Update Updated Formatting Added Eye Diagrams
1.2	06-2012	Title file name revised
1.1	05-2012	Updated specifications
1.0	04-2012	Initial release