

Description

The 9ZXL revision E family of Zero-Delay/Fanout Buffers (ZDB, FOB) with SMBus Write Protect are 2nd-generation enhanced performance buffers for PCIe and CPU applications. The devices have hardware SMBUS write protection to prevent accidental writes. The family meets all published QPI/UPI, DB2000Q and PCIe Gen1–5 jitter specifications. Devices range from 6 to 12 outputs, with each output having an OE# pin to support the PCIe CLKREQ# function for low power states. All devices meet DB2000Q, DB1200ZL and DB800ZL jitter and skew requirements.

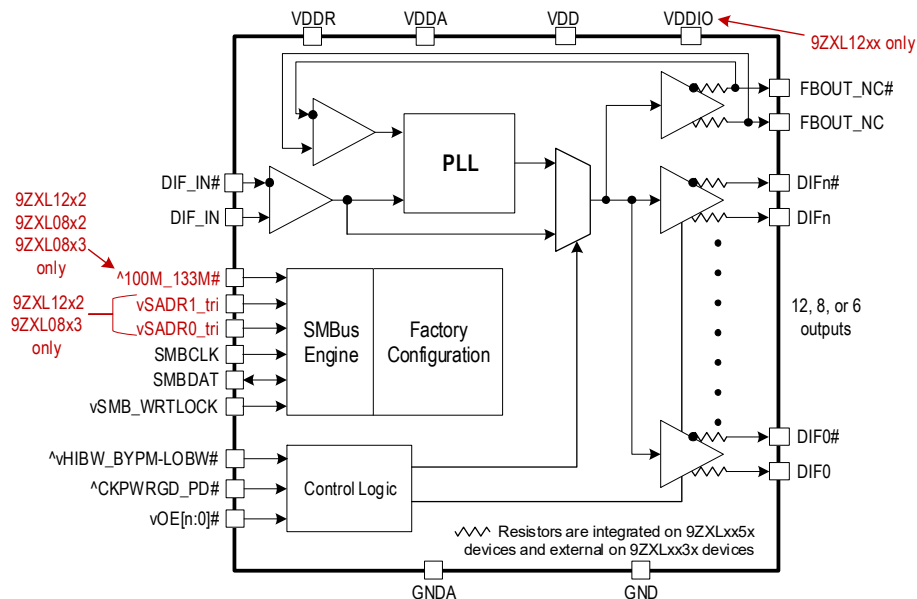
PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum (SRIS, SRNS)

Key Specifications

- Fanout Buffer Mode additive phase jitter:
 - PCIe Gen5 CC, UPI $\geq 20\text{Gb/s}$ < 24fs RMS
 - DB2000Q additive jitter < 39fs RMS
 - QPI/UPI 11.4GB/s < 40fs RMS
 - IF-UPI additive jitter < 70fs RMS
- ZDB Mode phase jitter:
 - PCIe Gen5 CC, UPI $\geq 20\text{Gb/s}$ < 22fs RMS
 - QPI/UPI 11.4GB/s < 120fs RMS
 - IF-UPI additive jitter < 130fs RMS
- Cycle-to-cycle jitter < 50ps
- Output-to-output skew < 50ps

Block Diagram



Features

- SMBus Write Protect pin prevents SMBus against accidental writes
- 6–12 Low-power HCSL (LP-HCSL) outputs
- Integrated terminations eliminate up to 4 resistors per output pair
- Dedicated OE# pins support PCIe CLKREQ# function
- Up to 9 selectable SMBus addresses (9ZXL12xx, 9ZXL0853)
- Selectable PLL bandwidths minimizes jitter peaking in cascaded PLL topologies
- Hardware/SMBus control of ZDB and FOB modes allow change without power cycle
- Spread spectrum compatible
- 1–400MHz FOB operation (all devices)
- 100MHz and 133.33MHz ZDB mode (9ZXL12xx, 9ZXL08xx)
- 100MHz ZDB mode (9ZXL06xx)
- 40°C to +85°C operating temperature range
- Packages: See [Ordering Information](#) for more details

Typical Applications

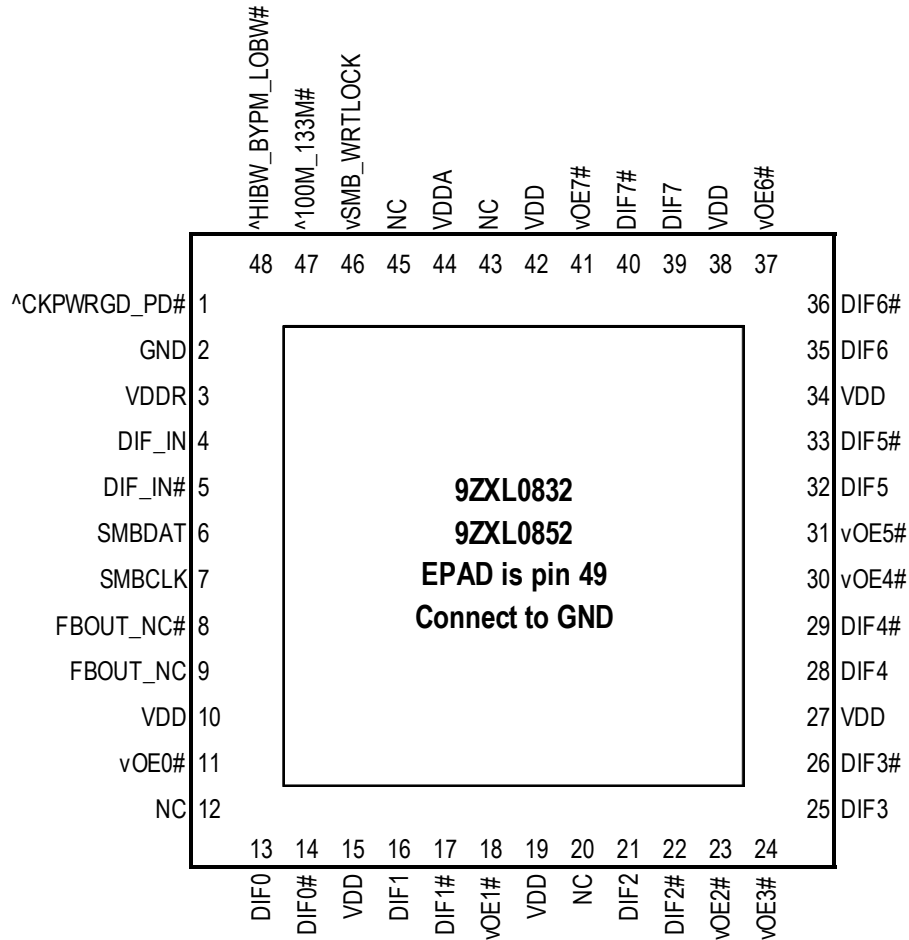
- Servers/High-performance Computing
- nVME Storage
- Networking
- Accelerators
- Industrial Control

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9ZXL08x2E Pin Assignment

Figure 2. Pin Assignment for 6 × 6 mm 48-VFQFPN Package – Top View

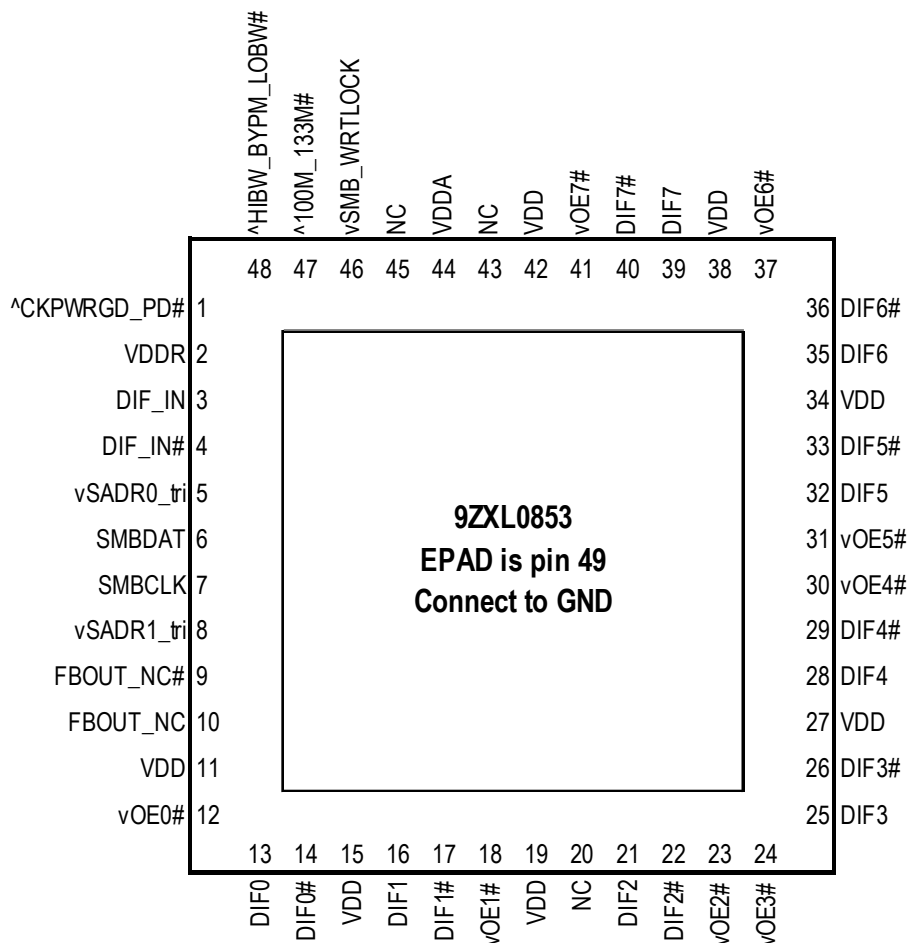


6 x 6 mm, 0.4mm pitch 48-VFQFPN

Pins with ^ prefix have internal 120kohm pull-up
 Pins with v prefix have internal 120kohm pull-down

9ZXL0853E Pin Assignment

Figure 3. Pin Assignment for 6 × 6 mm 48-VFQFPN Package – Top View

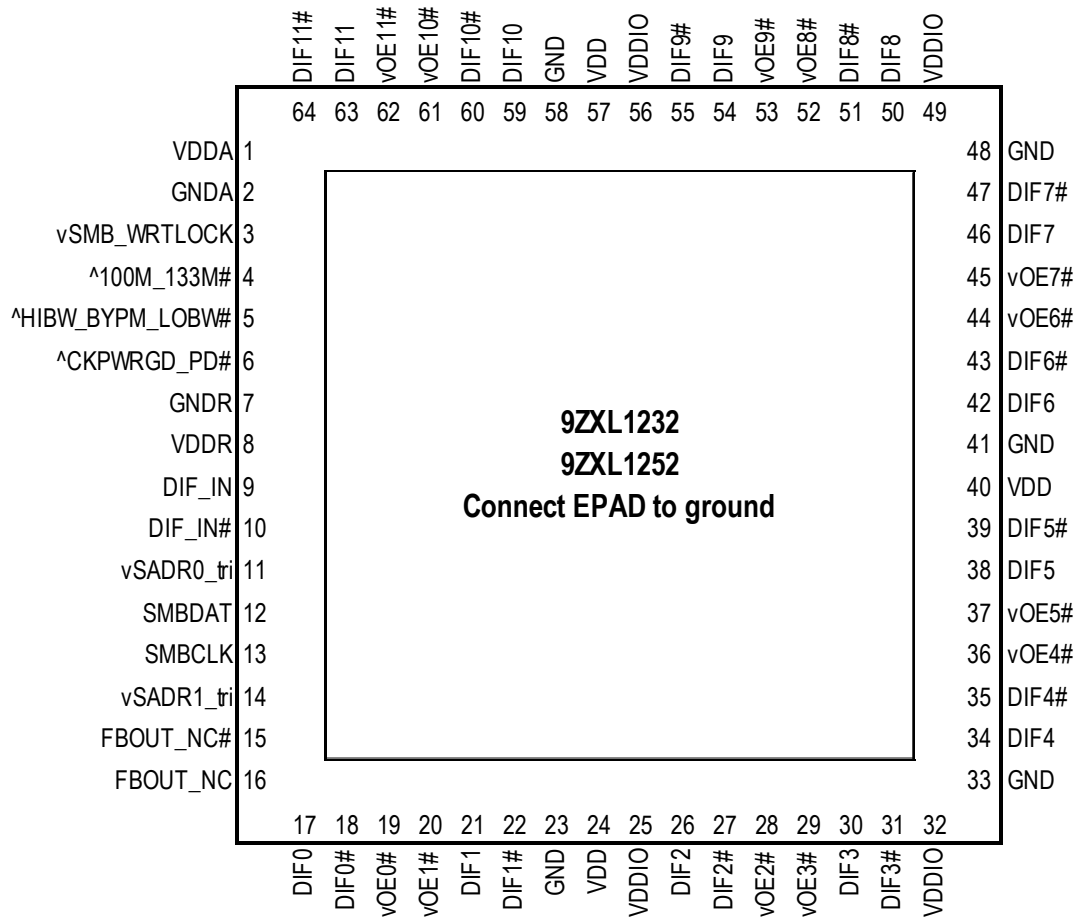


6 x 6 mm, 0.4mm pitch 48-VFQFPN

Pins with ^ prefix have internal 120kohm pull-up
 Pins with v prefix have internal 120kohm pull-down

9ZXL12x2E Pin Assignment

Figure 4. Pin Assignment for 9 × 9 mm 64-VFQFPN Package – Top View



9 x 9 mm, 0.5mm pitch 64-VFQFPN

Pins with ^ prefix have internal 120kohm pull-up
 Pins with v prefix have internal 120kohm pull-down

Pin Descriptions

Table 1. Pin Descriptions

| Name | Type | Description | 9ZXL12x2 Pin No. | 9ZXL08x2 Pin No. | 9ZXL0853 Pin No. | 9ZXL06x2 Pin No. |
|-------------------|------------|---|---------------------|---------------------|---------------------|---------------------|
| ^100M_133M# | Latched In | 3.3V Input to select operating frequency. This pin has an internal pull-up resistor. See Frequency Selection (PLL Mode) table for definition. | 4 | 47 | 47 | — |
| ^CKPWRGD_PD# | Input | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. | 6 | 1 | 1 | 3 |
| ^HIBW_BYPM_LO BW# | Latched In | Tri-level input to select High BW, Bypass or Low BW Mode. This pin has an internal pull-up resistor. See PLL Operating Mode table for details. | 5 | 48 | 48 | 2 |
| DIF_IN | Input | HCSL true input. | 9 | 4 | 3 | 6 |
| DIF_IN# | Input | HCSL complementary input. | 10 | 5 | 4 | 7 |
| DIF0 | Output | Differential true clock output. | 17 | 13 | 13 | 14 |
| DIF0# | Output | Differential complementary clock output. | 18 | 14 | 14 | 15 |
| DIF1 | Output | Differential true clock output. | 21 | 16 | 16 | 17 |
| DIF1# | Output | Differential complementary clock output. | 22 | 17 | 17 | 18 |
| DIF10 | Output | Differential true clock output. | 59 | — | — | — |
| DIF10# | Output | Differential complementary clock output. | 60 | — | — | — |
| DIF11 | Output | Differential true clock output. | 63 | — | — | — |
| DIF11# | Output | Differential complementary clock output. | 64 | — | — | — |
| DIF2 | Output | Differential true clock output. | 26 | 21 | 21 | 23 |
| DIF2# | Output | Differential complementary clock output. | 27 | 22 | 22 | 24 |
| DIF3 | Output | Differential true clock output. | 30 | 25 | 25 | 26 |
| DIF3# | Output | Differential complementary clock output. | 31 | 26 | 26 | 27 |
| DIF4 | Output | Differential true clock output. | 34 | 28 | 28 | 33 |
| DIF4# | Output | Differential complementary clock output. | 35 | 29 | 29 | 34 |
| DIF5 | Output | Differential true clock output. | 38 | 32 | 32 | 36 |
| DIF5# | Output | Differential complementary clock output. | 39 | 33 | 33 | 37 |
| DIF6 | Output | Differential true clock output. | 42 | 35 | 35 | — |
| DIF6# | Output | Differential complementary clock output. | 43 | 36 | 36 | — |
| DIF7 | Output | Differential true clock output. | 46 | 39 | 39 | — |
| DIF7# | Output | Differential complementary clock output. | 47 | 40 | 40 | — |
| DIF8 | Output | Differential true clock output. | 50 | — | — | — |
| DIF8# | Output | Differential complementary clock output. | 51 | — | — | — |
| DIF9 | Output | Differential true clock output. | 54 | — | — | — |
| DIF9# | Output | Differential complementary clock output. | 55 | — | — | — |

Table 1. Pin Descriptions (Cont.)

| Name | Type | Description | 9ZXL12x2 Pin No. | 9ZXL08x2 Pin No. | 9ZXL0853 Pin No. | 9ZXL06x2 Pin No. |
|-----------|--------|---|---------------------|--------------------------|--------------------------|------------------------------------|
| EPAD | GND | Connect EPAD to ground. | 65 | 49 | 49 | 41 |
| FBOUT_NC | Output | True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. | 16 | 9 | 10 | 11 |
| FBOUT_NC# | Output | Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. | 15 | 8 | 9 | 10 |
| GND | GND | Ground pin. | 23 | 49 | 49 | 41 |
| GND | GND | Ground pin. | 33 | 49 | 49 | 41 |
| GND | GND | Ground pin. | 41 | 49 | 49 | — |
| GND | GND | Ground pin. | 48 | 49 | 49 | — |
| GND | GND | Ground pin. | 58 | — | — | — |
| GND | GND | Ground pin for the PLL core. | 2 | 49 | 49 | 41 |
| GND | GND | Analog ground pin for the differential input (receiver). | 7 | 2 | 49 | 4 |
| NC | — | No connect. | | 12,20,43,45 | 20,43,45 | 30 |
| SMBCLK | Input | Clock pin of SMBUS circuitry. | 13 | 7 | 7 | 9 |
| SMBDAT | I/O | Data pin of SMBUS circuitry. | 12 | 6 | 6 | 8 |
| VDD | Power | Power supply, nominally 3.3V. | 24 | 10,15,19,27, 34,38,42 | 11,15,19,27, 34,38,42 | 12,16,20, 21,25,29, 31,35,39 |
| VDD | Power | Power supply, nominally 3.3V. | 40 | — | — | — |
| VDD | Power | Power supply, nominally 3.3V. | 57 | — | — | — |
| VDDA | Power | Power supply for PLL core. | 1 | 44 | 44 | 40 |
| VDDIO | Power | Power supply for differential outputs. | 25 | — | — | — |
| VDDIO | Power | Power supply for differential outputs. | 32 | — | — | — |
| VDDIO | Power | Power supply for differential outputs. | 49 | — | — | — |
| VDDIO | Power | Power supply for differential outputs. | 56 | — | — | — |
| VDDR | Power | Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V. | 8 | 3 | 2 | 5 |
| vOE0# | Input | Active low input for enabling output 0. This pin has an internal pull-down. 1 = disable output, 0 = enable output. | 19 | 11 | 12 | 13 |
| vOE1# | Input | Active low input for enabling output 1. This pin has an internal pull-down. 1 = disable output, 0 = enable output. | 20 | 18 | 18 | 19 |

Table 1. Pin Descriptions (Cont.)

| Name | Type | Description | 9ZXL12x2 Pin No. | 9ZXL08x2 Pin No. | 9ZXL0853 Pin No. | 9ZXL06x2 Pin No. |
|--------------|-------|--|---------------------|---------------------|---------------------|---------------------|
| vOE10# | Input | Active low input for enabling output 10. This pin has an internal pull-down. 1 = disable output, 0 = enable output. | 61 | — | — | — |
| vOE11# | Input | Active low input for enabling output 11. This pin has an internal pull-down. 1 = disable output, 0 = enable output. | 62 | — | — | — |
| vOE2# | Input | Active low input for enabling output 2. This pin has an internal pull-down. 1 = disable output, 0 = enable output. | 28 | 23 | 23 | 22 |
| vOE3# | Input | Active low input for enabling output 3. This pin has an internal pull-down. 1 = disable output, 0 = enable output. | 29 | 24 | 24 | 28 |
| vOE4# | Input | Active low input for enabling output 4. This pin has an internal pull-down. 1 = disable output, 0 = enable output. | 36 | 30 | 30 | 32 |
| vOE5# | Input | Active low input for enabling output 5. This pin has an internal pull-down. 1 = disable output, 0 = enable output. | 37 | 31 | 31 | 38 |
| vOE6# | Input | Active low input for enabling output 6. This pin has an internal pull-down. 1 = disable output, 0 = enable output. | 44 | 37 | 37 | — |
| vOE7# | Input | Active low input for enabling output 7. This pin has an internal pull-down. 1 = disable output, 0 = enable output. | 45 | 41 | 41 | — |
| vOE8# | Input | Active low input for enabling output 8. This pin has an internal pull-down. 1 = disable output, 0 = enable output. | 52 | — | — | — |
| vOE9# | Input | Active low input for enabling output 9. This pin has an internal pull-down. 1 = disable output, 0 = enable output. | 53 | — | — | — |
| vSADR0_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has an internal pull-down resistor. See the SMBus Addressing table. | 11 | — | 5 | — |
| vSADR1_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has an internal pull-down resistor. See the SMBus Addressing table. | 14 | — | 8 | — |
| vSMB_WRTLOCK | Input | This pin prevents SMBus writes when asserted. SMBus reads are not affected. This pin has an internal pull-down. 0 = SMBus writes allows, 1 = SMBus writes blocked. | 3 | 46 | 46 | 1 |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZXL06x2E/9ZXL08xxE/9ZXL12x2E. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 2. Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|----------------------|--------------------|-----------------------------|-----------|---------|-----------------------|-------|-------|
| Supply Voltage | VDDx | | | | 3.9 | V | 1,2 |
| Input Low Voltage | V _{IL} | | GND - 0.5 | | | V | 1 |
| Input High Voltage | V _{IH} | Except for SMBus interface. | | | V _{DD} + 0.5 | V | 1,3 |
| Input High Voltage | V _{IHSMB} | SMBus clock and data pins. | | | 3.9 | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD Protection | ESD prot | Human Body Model. | 2500 | | | V | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Operation under these conditions is neither implied nor guaranteed.

³ Not to exceed 3.9V.

Thermal Characteristics

Table 3. Thermal Characteristics

| Parameter | Symbol | Conditions | Package | Typical Values | Units | Notes |
|---------------------------|----------------|----------------------------------|---------|----------------|-------|-------|
| 9ZXL12 Thermal Resistance | θ_{JC} | Junction to case. | NLG64 | 14 | °C/W | 1 |
| | θ_{Jb} | Junction to base. | | 1 | °C/W | 1 |
| | θ_{JA0} | Junction to air, still air. | | 28 | °C/W | 1 |
| | θ_{JA1} | Junction to air, 1 m/s air flow. | | 21 | °C/W | 1 |
| | θ_{JA3} | Junction to air, 3 m/s air flow. | | 19 | °C/W | 1 |
| | θ_{JA5} | Junction to air, 5 m/s air flow. | | 18 | °C/W | 1 |
| 9ZXL08 Thermal Resistance | θ_{JC} | Junction to case. | NDG48 | 19 | °C/W | 1 |
| | θ_{Jb} | Junction to base. | | 0 | °C/W | 1 |
| | θ_{JA0} | Junction to air, still air. | | 30 | °C/W | 1 |
| | θ_{JA1} | Junction to air, 1 m/s air flow. | | 23 | °C/W | 1 |
| | θ_{JA3} | Junction to air, 3 m/s air flow. | | 20 | °C/W | 1 |
| | θ_{JA5} | Junction to air, 5 m/s air flow. | | 19 | °C/W | 1 |

Table 3. Thermal Characteristics (Cont.)

| Parameter | Symbol | Conditions | Package | Typical Values | Units | Notes |
|---------------------------|----------------|----------------------------------|---------|----------------|-------|-------|
| 9ZXL06 Thermal Resistance | θ_{JC} | Junction to case. | NDG40 | 32 | °C/W | 1 |
| | θ_{Jb} | Junction to base. | | 2 | °C/W | 1 |
| | θ_{JA0} | Junction to air, still air. | | 44 | °C/W | 1 |
| | θ_{JA1} | Junction to air, 1 m/s air flow. | | 37 | °C/W | 1 |
| | θ_{JA3} | Junction to air, 3 m/s air flow. | | 33 | °C/W | 1 |
| | θ_{JA5} | Junction to air, 5 m/s air flow. | | 31 | °C/W | 1 |

¹ EPAD soldered to ground.

Electrical Characteristics

$T_A = T_{AMB}$. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

Table 4. SMBus Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---------------------------|--------------|---|---------|---------|-------------|-------|-------|
| SMBus Input Low Voltage | V_{ILSMB} | | | | 0.8 | V | |
| SMBus Input High Voltage | V_{IHSMB} | | 2.1 | | V_{DDSMB} | V | |
| SMBus Output Low Voltage | V_{OLSMB} | At I_{PULLUP} . | | | 0.4 | V | |
| SMBus Sink Current | I_{PULLUP} | At V_{OL} . | 4 | | | mA | |
| Nominal Bus Voltage | V_{DDSMB} | | 2.7 | | 3.6 | V | 1 |
| SCLK/SDATA Rise Time | t_{RSMB} | (Max $V_{IL} - 0.15V$) to (Min $V_{IH} + 0.15V$). | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t_{FSMB} | (Min $V_{IH} + 0.15V$) to (Max $V_{IL} - 0.15V$). | | | 300 | ns | 1 |
| SMBus Operating Frequency | f_{SMB} | SMBus operating frequency. | | | 400 | kHz | 5 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200mV.

⁴ DIF_IN input.

⁵ The differential input clock must be running for the SMBus to be active.

Table 5. DIF_IN Clock Input Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|----------------------------------|-------------|---|---------|---------|---------|-------|-------|
| Input Crossover Voltage – DIF_IN | V_{CROSS} | Crossover voltage. | 150 | | 900 | mV | 1 |
| Input Swing – DIF_IN | V_{SWING} | Differential value. | 300 | | | mV | 1 |
| Input Slew Rate – DIF_IN | dv/dt | Measured differentially. | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I_{IN} | $V_{IN} = V_{DD}$, $V_{IN} = GND$. | -5 | | 5 | μA | |
| Input Duty Cycle | d_{tIn} | Measurement from differential waveform. | 45 | | 55 | % | 1 |
| Input Jitter – Cycle to Cycle | J_{DIFIn} | Differential measurement. | 0 | | 125 | ps | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through ±75mV window centered around differential zero.

Table 6. Input/Supply/Common Parameters

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|------------------------------------|-----------------|---|-----------|------------|----------------|---------------|-------|
| Supply Voltage | V_{DDX} | Supply voltage for core and analog. | 3.135 | 3.3 | 3.465 | V | |
| Output Supply Voltage | V_{DDIO} | Supply voltage for DIF outputs, if present. | 0.95 | 1.05 | 3.465 | V | 5 |
| Ambient Operating Temperature | T_{AMB} | Extended Industrial range (T_{EXIND}). | -40 | 25 | 105 | °C | 7 |
| | | Industrial range (T_{IND}). | -40 | 25 | 85 | °C | |
| Input High Voltage | V_{IH} | Single-ended inputs, except SMBus, tri-level inputs. | 2 | | $V_{DD} + 0.3$ | V | |
| Input Low Voltage | V_{IL} | Single-ended inputs, except SMBus, tri-level inputs. | GND - 0.3 | | 0.8 | V | |
| Input High Voltage | V_{IH} | Tri-level inputs. | 2.2 | | $V_{DD} + 0.3$ | V | |
| Input Mid Voltage | V_{IM} | Tri-level inputs. | 1.2 | $V_{DD}/2$ | 1.8 | V | |
| Input Low Voltage | V_{IL} | Tri-level inputs. | GND - 0.3 | | 0.8 | V | |
| Input Current | I_{IN} | Single-ended inputs, $V_{IN} = \text{GND}$, $V_{IN} = V_{DD}$. | -5 | | 5 | μA | |
| | I_{INP} | Single-ended inputs. $V_{IN} = 0 \text{ V}$; inputs with internal pull-up resistors. $V_{IN} = V_{DD}$; inputs with internal pull-down resistors. | -50 | | 50 | μA | |
| Input Frequency | F_{ibyp} | $V_{DD} = 3.3\text{V}$, Bypass Mode. | 1 | | 400 | MHz | |
| | F_{ipll} | $V_{DD} = 3.3\text{V}$, 100MHz PLL Mode. | 98.5 | 100.00 | 102.5 | MHz | |
| | F_{ipll} | $V_{DD} = 3.3\text{V}$, 133.33MHz PLL Mode. | 132 | 133.33 | 135 | MHz | 6 |
| ppm Error Contribution | ppm | ppm error contributed to input clock. | 0 | | | ppm | |
| Pin Inductance | L_{pin} | | | | 7 | nH | 1 |
| Capacitance | C_{IN} | Logic inputs, except DIF_IN. | 1.5 | | 5 | pF | 1 |
| | C_{INDIF_IN} | DIF_IN differential clock inputs. | 1.5 | | 2.7 | pF | 1,4 |
| | C_{OUT} | Output pin capacitance. | | | 6 | pF | 1 |
| Clk Stabilization | T_{STAB} | From V_{DD} power-up and after input clock stabilization or deassertion of PD# to 1st clock. | | 1 | 1.8 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | $f_{MODINPCIe}$ | Allowable frequency for PCIe applications (Triangular modulation). | 30 | | 33 | kHz | |
| OE# Latency | $t_{LATO\#}$ | DIF start after OE# assertion. DIF stop after OE# deassertion. | 4 | 5 | 10 | clocks | 1,2,3 |
| Tdrive_PD# | t_{DRVPD} | DIF output enable after PD# deassertion. | | 49 | 300 | μs | 1,3 |
| Tfall | t_F | Fall time of control inputs. | | | 5 | ns | 2 |
| Trise | t_R | Rise time of control inputs. | | | 5 | ns | 2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200mV.

⁴ DIF_IN input.

⁵ 9ZXL12x2 only.

⁶ 9ZXL12x2 and 9ZXL08x2 only.

⁷ Not all devices are available in this temperature range. See [Ordering Information](#) for details.

Table 7. Current Consumption – 9ZXL12

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|--------------------------|--------------------|---|---------|---------|---------|-------|-------|
| Operating Supply Current | I _{DDA} | V _{DDA} , PLL Mode at 100MHz. | | 38 | 46 | mA | 1 |
| | | V _{DDA} , Fanout Buffer Mode at 100MHz. | | 4 | 5 | mA | 1 |
| | I _{DD} | All other V _{DD} pins. | | 25 | 34 | mA | |
| | I _{DDOIO} | V _{DDIO} for LP-HCSL outputs, if applicable. | | 83 | 107 | mA | |
| Power Down Current | I _{DDAPD} | V _{DDA} , CKPWRGD_PD# = 0. | | 3 | 4 | mA | 1 |
| | I _{DDPD} | All other V _{DD} pins, CKPWRGD_PD# = 0. | | 1 | 2 | mA | |

¹ Includes V_{DDR}.

Table 8. Current Consumption – 9ZXL08

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|--------------------------|--------------------|--|---------|---------|---------|-------|-------|
| Operating Supply Current | I _{DDA} | V _{DDA} , PLL Mode at 100MHz. | | 37 | 45 | mA | 1 |
| | | V _{DDA} , Fanout Buffer Mode at 100MHz. | | 4 | 5 | mA | 1 |
| | I _{DD} | All other V _{DD} pins at 100MHz. | | 55 | 68 | mA | |
| Power Down Current | I _{DDAPD} | V _{DDA} , CKPWRGD_PD# = 0. | | 3 | 4 | mA | 1 |
| | I _{DDPD} | All other V _{DD} pins, CKPWRGD_PD# = 0. | | 1 | 2 | mA | |

¹ Includes V_{DDR}.

Table 9. Current Consumption – 9ZXL06

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|--------------------------|--------------------|--|---------|---------|---------|-------|-------|
| Operating Supply Current | I _{DDA} | V _{DDA} , PLL Mode at 100MHz. | | 37 | 45 | mA | 1 |
| | | V _{DDA} , Fanout Buffer Mode at 100MHz. | | 4 | 5 | mA | 1 |
| | I _{DD} | All other V _{DD} pins at 100MHz. | | 41 | 50 | mA | |
| Power Down Current | I _{DDAPD} | V _{DDA} , CKPWRGD_PD# = 0. | | 3 | 4 | mA | 1 |
| | I _{DDPD} | All other V _{DD} pins, CKPWRGD_PD# = 0. | | 1 | 2 | mA | |

¹ Includes V_{DDR}.

Table 10. Skew and Differential Jitter Parameters

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|------------------------|-----------------|---|---------|---------|---------|----------|-----------|
| CLK_IN, DIF[x:0] | t_{SPO_PLL} | Input-to-output skew in PLL Mode at 100MHz, nominal temperature and voltage. | -100 | -21.3 | 100 | ps | 1,2,4,5,7 |
| CLK_IN, DIF[x:0] | t_{PD_BYP} | Input-to-output skew in Bypass Mode at 100MHz, nominal temperature and voltage. | 2 | 2.6 | 3 | ns | 1,2,3,5,7 |
| CLK_IN, DIF[x:0] | t_{DSPO_PLL} | Input-to-output skew variation in PLL Mode at 100MHz, across voltage and temperature. | -50 | 0.0 | 50 | ps | 1,2,3,5,7 |
| CLK_IN, DIF[x:0] | t_{DSPO_BYP} | Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, $T_{AMB} = 0C$ to $+70^{\circ}C$. | -250 | | 250 | ps | 1,2,3,5,7 |
| | | Input-to-output skew variation in Bypass mode at 100MHz, across voltage and temperature, $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$. | -350 | | 350 | ps | 1,2,3,5,7 |
| CLK_IN, DIF[x:0] | t_{DTE} | Random differential tracking error between two 9ZX devices in Hi BW Mode. | | 3 | 5 | ps (rms) | 1,2,3,5,7 |
| CLK_IN, DIF[x:0] | t_{DSSTE} | Random differential spread spectrum tracking error between two 9ZX devices in Hi BW Mode. | | 23 | 50 | ps | 1,2,3,5,7 |
| DIF[x:0] | t_{SKEW_ALL} | Output-to-output skew across all outputs, common to PLL and Bypass Mode, at 100MHz. | | | 50 | ps | 1,2,3,7 |
| PLL Jitter Peaking | $j_{peak-hibw}$ | LOBW#_BYPASS_HIBW = 1. | 0 | 1.3 | 2.5 | dB | 6,7 |
| PLL Jitter Peaking | $j_{peak-lobw}$ | LOBW#_BYPASS_HIBW = 0. | 0 | 1.3 | 2 | dB | 6,7 |
| PLL Bandwidth | pll_{HIBW} | LOBW#_BYPASS_HIBW = 1. | 2 | 2.6 | 4 | MHz | 7,8 |
| PLL Bandwidth | pll_{LOBW} | LOBW#_BYPASS_HIBW = 0. | 0.7 | 1.0 | 1.4 | MHz | 7,8 |
| Duty Cycle | t_{DC} | Measured differentially, PLL Mode. | 45 | 50.3 | 55 | % | 1 |
| Duty Cycle Distortion | t_{DCD} | Measured differentially, Bypass Mode at 100MHz. | -1 | 0 | 1 | % | 1,9 |
| Jitter, Cycle to Cycle | $t_{jyc-cyc}$ | PLL Mode. | | 14 | 50 | ps | 1,10 |
| | | Additive jitter in Bypass Mode. | | 0.1 | 5 | ps | 1,10 |

¹ Measured into fixed 2pF load cap. Input-to-output skew is measured at the first output edge following the corresponding input.

² Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

³ All Bypass Mode input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

⁴ This parameter is deterministic for a given device.

⁵ Measured with scope averaging on to find mean value.

⁶ Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

⁷ Guaranteed by design and characterization, not 100% tested in production.

⁸ Measured at 3db down or half power point.

⁹ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in Bypass Mode.

¹⁰ Measured from differential waveform.

Table 11. LP-HCSL Outputs

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limits | Units | Notes |
|------------------------|------------|--|---------|---------|---------|----------------------|-------|-------|
| Slew Rate | dV/dt | Scope averaging on. | 2 | 2.9 | 4 | 1–4 | V/ns | 1,2,3 |
| Slew Rate Matching | ΔdV/dt | Single-ended measurement. | | 7.1 | 20 | 20 | % | 1,4,7 |
| Maximum Voltage | Vmax | Measurement on single-ended signal using absolute value (scope averaging off). | 700 | 792 | 850 | 660–1150 | mV | 7,8 |
| Minimum Voltage | Vmin | | -150 | -35 | 150 | -300 | | 7,8 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off. | 300 | 372 | 462 | 250–550 | mV | 1,5,7 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off. | | 15 | 50 | 140 | mV | 1,6,7 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform.

³ Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

⁷ At default SMBus settings.

⁸ Includes previously separate values of +300mV overshoot and -300mV of undershoot.

Table 12. PCIe Phase Jitter Parameters

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Limits | Units | Notes |
|---|-----------------------------|-------------------------------|---------|---------|---------|--------|----------|-----------|
| PCIe Phase Jitter, Low Bandwidth ZDB Mode (Common Clocked Architecture) | t _{jphPCIeG1-CC} | PCIe Gen 1 (2.5 GT/s) | | 2.6 | 6.8 | 86 | ps (p-p) | 1,2 |
| | t _{jphPCIeG2-CC} | PCIe Gen 2 Hi Band (5.0 GT/s) | | 0.09 | 0.16 | 3 | ps (RMS) | 1,2 |
| | | PCIe Gen 2 Lo Band (5.0 GT/s) | | 0.08 | 0.12 | 3.1 | ps (RMS) | 1,2 |
| | t _{jphPCIeG3-CC} | PCIe Gen 3 (8.0 GT/s) | | 0.05 | 0.07 | 1 | ps (RMS) | 1,2 |
| | t _{jphPCIeG4-CC} | PCIe Gen 4 (16.0 GT/s) | | 0.05 | 0.07 | 0.5 | ps (RMS) | 1,2,3,4 |
| | t _{jphPCIeG5-CC} | PCIe Gen 5 (32.0 GT/s) | | 0.018 | 0.022 | 0.15 | ps (RMS) | 1,2,3,5,7 |
| PCIe Phase Jitter, Low Bandwidth ZDB Mode (SRIS Architecture) | t _{jphPCIeG1-SRIS} | PCIe Gen 1 (2.5 GT/s) | | 8.71 | 8.73 | N/A | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG2-SRIS} | PCIe Gen 2 (5.0 GT/s) | | 0.81 | 0.83 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG3-SRIS} | PCIe Gen 3 (8.0 GT/s) | | 0.329 | 0.335 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG4-SRIS} | PCIe Gen 4 (16.0 GT/s) | | 0.222 | 0.235 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG5-SRIS} | PCIe Gen 5 (32.0 GT/s) | | 0.084 | 0.091 | | ps (RMS) | 1,2,6 |

Table 12. PCIe Phase Jitter Parameters (Cont.)

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Limits | Units | Notes |
|--|-----------------------------|-------------------------------|---------|---------|---------|----------|-----------|---------|
| PCIe Phase Jitter, High Bandwidth ZDB Mode (Common Clocked Architecture) | t _{jphPCIeG1-CC} | PCIe Gen 1 (2.5 GT/s) | | 5.4 | 6.9 | 86 | ps (p-p) | 1,2 |
| | t _{jphPCIeG2-CC} | PCIe Gen 2 Hi Band (5.0 GT/s) | | 0.19 | 0.25 | 3 | ps (RMS) | 1,2 |
| | | PCIe Gen 2 Lo Band (5.0 GT/s) | | 0.09 | 0.13 | 3.1 | ps (RMS) | 1,2 |
| | t _{jphPCIeG3-CC} | PCIe Gen 3 (8.0 GT/s) | | 0.10 | 0.13 | 1 | ps (RMS) | 1,2 |
| | t _{jphPCIeG4-CC} | PCIe Gen 4 (16.0 GT/s) | | 0.10 | 0.13 | 0.5 | ps (RMS) | 1,2,3,4 |
| t _{jphPCIeG5-CC} | PCIe Gen 5 (32.0 GT/s) | | 0.032 | 0.042 | 0.15 | ps (RMS) | 1,2,3,5,7 | |
| PCIe Phase Jitter, High Bandwidth ZDB Mode (SRIS Architecture) | t _{jphPCIeG1-SRIS} | PCIe Gen 1 (2.5 GT/s) | | 8.61 | 8.63 | N/A | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG2-SRIS} | PCIe Gen 2 (5.0 GT/s) | | 0.88 | 0.96 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG3-SRIS} | PCIe Gen 3 (8.0 GT/s) | | 0.354 | 0.375 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG4-SRIS} | PCIe Gen 4 (16.0 GT/s) | | 0.271 | 0.305 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG5-SRIS} | PCIe Gen 5 (32.0 GT/s) | | 0.097 | 0.109 | | ps (RMS) | 1,2,6 |

¹ The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the [Test Loads](#) section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all results.

² Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

³ SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.

⁴ Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

⁵ Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

⁶ The PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, however, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by $\sqrt{2}$. An additional consideration is the value for which to divide by $\sqrt{2}$. The conservative approach is to divide the ref clock jitter limit, and the case can be made for dividing the channel simulation values by $\sqrt{2}$, if the ref clock is close to the Tx clock input. An example for Gen4 is as follows. A "rule-of-thumb" SRIS limit would be either $0.5\text{ps RMS}/\sqrt{2} = 0.35\text{ps RMS}$ if the clock chip is far from the clock input, or $0.7\text{ps RMS}/\sqrt{2} = 0.5\text{ps RMS}$ if the clock chip is near the clock input.

⁷ This specification also applied to UPI data rates $\geq 20\text{Gb/s}$.

Table 13. Additive PCIe Phase Jitter for Fanout Buffer Mode

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Limits | Units | Notes |
|---|-----------------------------|------------------------------|---------|---------|---------|----------|-----------|---------|
| Additive PCIe Phase Jitter, Fanout Buffer Mode ⁷ (Common Clocked Architecture) | t _{jphPCIeG1-CC} | PCIe Gen1 (2.5 GT/s) | | 1.3 | 1.9 | 86 | ps (p-p) | 1,2 |
| | t _{jphPCIeG2-CC} | PCIe Gen2 Hi Band (5.0 GT/s) | | 0.089 | 0.126 | 3 | ps (RMS) | 1,2 |
| | | PCIe Gen2 Lo Band (5.0 GT/s) | | 0.023 | 0.034 | 3.1 | ps (RMS) | 1,2 |
| | t _{jphPCIeG3-CC} | PCIe Gen3 (8.0 GT/s) | | 0.044 | 0.062 | 1 | ps (RMS) | 1,2 |
| | t _{jphPCIeG4-CC} | PCIe Gen4 (16.0 GT/s) | | 0.044 | 0.062 | 0.5 | ps (RMS) | 1,2,3,4 |
| t _{jphPCIeG5-CC} | PCIe Gen5 (32.0 GT/s) | | 0.017 | 0.024 | 0.15 | ps (RMS) | 1,2,3,5,8 | |
| Additive PCIe Phase Jitter, Fanout Buffer Mode ⁷ (SRIS Architecture) | t _{jphPCIeG1-SRIS} | PCIe Gen1 (2.5 GT/s) | | 0.127 | 0.181 | N/A | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG2-SRIS} | PCIe Gen2 (5.0 GT/s) | | 0.112 | 0.159 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG3-SRIS} | PCIe Gen3 (8.0 GT/s) | | 0.029 | 0.042 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG4-SRIS} | PCIe Gen4 (16.0 GT/s) | | 0.031 | 0.043 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG5-SRIS} | PCIe Gen5 (32.0 GT/s) | | 0.027 | 0.038 | | ps (RMS) | 1,2,6 |

¹ The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the [Test Loads](#) section of the data sheet for the exact measurement setup. The total Ref Clk jitter limits for each data rate are listed for convenience. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all results.

² Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

³ SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.

⁴ Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

⁵ Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

⁶ The PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, however, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by $\sqrt{2}$. An additional consideration is the value for which to divide by $\sqrt{2}$. The conservative approach is to divide the ref clock jitter limit, and the case can be made for dividing the channel simulation values by $\sqrt{2}$, if the ref clock is close to the Tx clock input. An example for Gen4 is as follows. A "rule-of-thumb" SRIS limit would be either $0.5\text{ps RMS}/\sqrt{2} = 0.35\text{ps RMS}$ if the clock chip is far from the clock input, or $0.7\text{ps RMS}/\sqrt{2} = 0.5\text{ps RMS}$ if the clock chip is near the clock input.

⁷ Additive jitter for RMS values is calculated by solving for "b" where $b = \sqrt{c^2 - a^2}$ and "a" is rms input jitter and "c" is rms output jitter.

⁸ This specification also applied to UPI data rates $\geq 20\text{Gb/s}$.

Table 14. Filtered Phase Jitter Parameters – QPI/UPI, IF-UPI and DB2000Q

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limits | Units | Notes |
|------------------------------------|-------------------------|--|---------|---------|---------|----------------------|----------|-------|
| Phase Jitter, ZDB Mode | t _{jphQPI_UPI} | QPI and UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.16 | 0.37 | 0.5 | ps (RMS) | 1,2 |
| | | QPI and UPI (100MHz, 8.0Gb/s, 12UI) | | 0.10 | 0.15 | 0.3 | ps (RMS) | 1,2 |
| | | QPI and UPI (100MHz, ≤11.4Gb/s, 12UI) | | 0.08 | 0.12 | 0.2 | ps (RMS) | 1,2 |
| Additive Phase Jitter, Fanout Mode | t _{jphQPI_UPI} | QPI and UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.03 | 0.05 | N/A | ps (RMS) | 1,2,3 |
| | | QPI and UPI (100MHz, 8.0Gb/s, 12UI) | | 0.03 | 0.05 | | ps (RMS) | 1,2,3 |
| | | QPI and UPI (100MHz, ≤11.4Gb/s, 12UI) | | 0.02 | 0.04 | | ps (RMS) | 1,2,3 |
| | t _{jphIF-UPI} | IF-UPI, Lo-BW ZDB Mode | | 0.10 | 0.13 | 1 | ps (RMS) | 1,4,5 |
| | | IF-UPI, Hi-BW ZDB Mode | | 0.17 | 0.20 | 1 | ps (RMS) | 1,4,5 |
| | | IF-UPI, Fanout Mode | | 0.06 | 0.07 | 1 | ps (RMS) | 1,4 |
| | t _{jphDB2000Q} | DB2000Q, Fanout Mode | | 28 | 39 | 80 | fs (RMS) | 1,4,5 |

¹ Applies to all differential outputs, guaranteed by design and characterization. See [Test Loads](#) for measurement setup details.

² Calculated from Intel-supplied clock jitter tool.

³ For RMS values, additive jitter is calculated by solving for “b” where $b = \sqrt{c^2 - a^2}$, “a” is rms input jitter and “c” is rms total jitter.

⁴ Calculated from phase noise analyzer with Intel-specified brick-wall filter applied. This is an additive jitter specification regardless of buffer operating mode.

⁵ The IF-UPI specification is an additive specification, regardless of the buffer operating mode. The enhanced 9ZXL devices meet this specification in all operating modes.

Table 15. Phase Jitter Parameters – 12kHz to 20MHz

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limits | Units | Notes |
|---|----------------------------|-------------------------------------|---------|---------|---------|----------------------|----------|-------|
| 12kHz–20MHz Additive Phase Jitter, Fanout Buffer Mode | t _{jph12k-20MFOB} | Fanout Buffer Mode, SSC OFF, 100MHz | | 98 | 125 | N/A | fs (RMS) | 1,2,3 |

¹ Applies to all differential outputs, guaranteed by design and characterization. See [Test Loads](#) for measurement setup details.

² 12kHz to 20MHz brick wall filter.

³ For RMS values, additive jitter is calculated by solving for “b” where $b = \sqrt{c^2 - a^2}$, “a” is rms input jitter and “c” is rms total jitter.

Power Management

Table 16. Power Management

| CKPWRGD_PD# | DIF_IN | SMBus EN bit | OE[x]# Pin | DIF[x] | PLL State (in ZDB Mode) |
|-------------|---------|--------------|------------|---------|-------------------------|
| 0 | X | X | X | Low/Low | OFF |
| 1 | Running | 0 | 0 | Low/Low | ON |
| | | 0 | 1 | Low/Low | ON |
| | | 1 | 0 | Running | ON |
| | | 1 | 1 | Low/Low | ON |

Table 17. Frequency Selection (PLL Mode)

| 100M_133M# | DIF_IN MHz | DIF[x] |
|------------|------------|--------|
| 1 | 100.00 | DIF_IN |
| 0 | 133.33 | DIF_IN |

Note: 9ZXL12xx and 9ZXL08xx only. 9ZXL06xx is 100MHz only.

Table 18. PLL Operating Mode

| HiBW_BypM_LoBW# | Mode | PLL |
|-----------------|-----------|---------|
| Low | PLL Lo BW | Running |
| Mid | Bypass | Off |
| High | PLL Hi BW | Running |

Note: See SMBus Byte 0, bits 7 and 6 for additional information.

Test Loads

Figure 5. Test Load for AC/DC Measurements

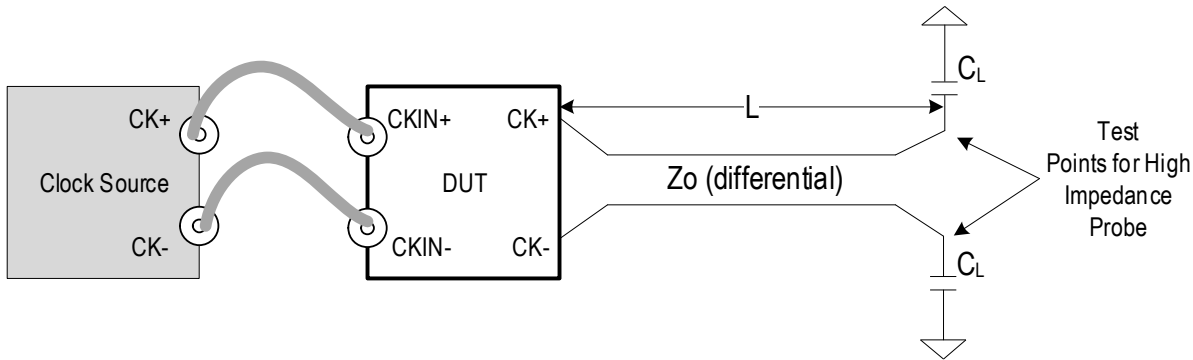


Table 19. Parameters for AC/DC Measurements

| Clock Source | Device Under Test (DUT) | R_s (Ω) | Differential Z_o (Ω) | L (cm) | C_L (pF) | Parameters Measured |
|--------------|-------------------------|--------------------|---------------------------------|--------|------------|---------------------|
| SMA100B | 9ZXLxx3x | 27 External | 85 | 25.4 | 2 | AC/DC parameters |
| SMA100B | 9ZXLxx5x | Internal | 85 | 25.4 | 2 | |

Figure 6. Test Load for Phase Jitter Measurements using Phase Noise Analyzer

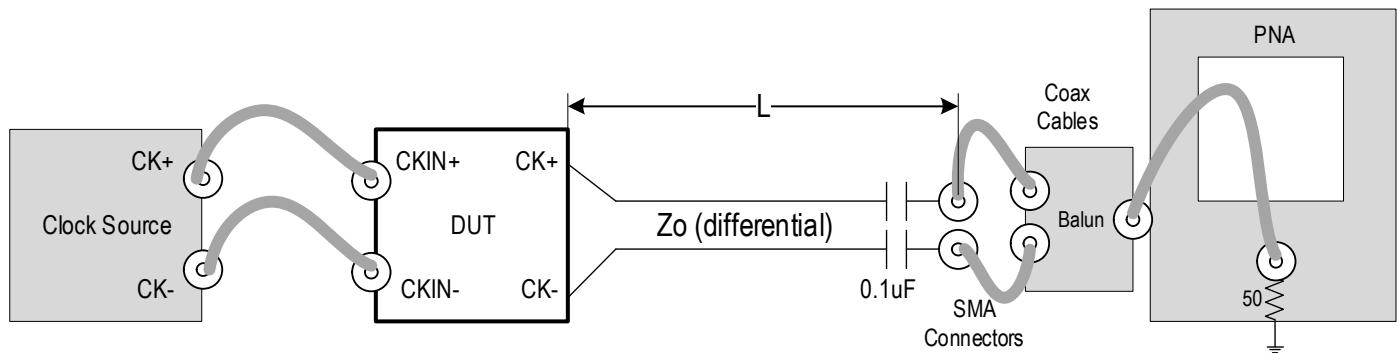


Table 20. Parameters for Phase Jitter Measurements using Phase Noise Analyzer

| Clock Source | Device Under Test (DUT) | R_s (Ω) | Differential Z_o (Ω) | L (cm) | C_L (pF) | Notes | Parameters Measured |
|--------------|-------------------------|--------------------|---------------------------------|--------|------------|-------------|-----------------------|
| SMA100B | 9ZXLxx3x | 27 External | 85 | 25.4 | N/A | Fanout Mode | PCIe, IF-UPI, DB2000Q |
| 9FGV1006 | 9ZXLxx3x | 27 External | 85 | 25.4 | | ZDB Mode | |
| SMA100B | 9ZXLxx5x | Internal | 85 | 25.4 | | Fanout Mode | |
| 9FGV1006 | 9ZXLxx5x | Internal | 85 | 25.4 | | ZDB Mode | |

Figure 7. Test Load for Phase Jitter Measurements using Oscilloscope

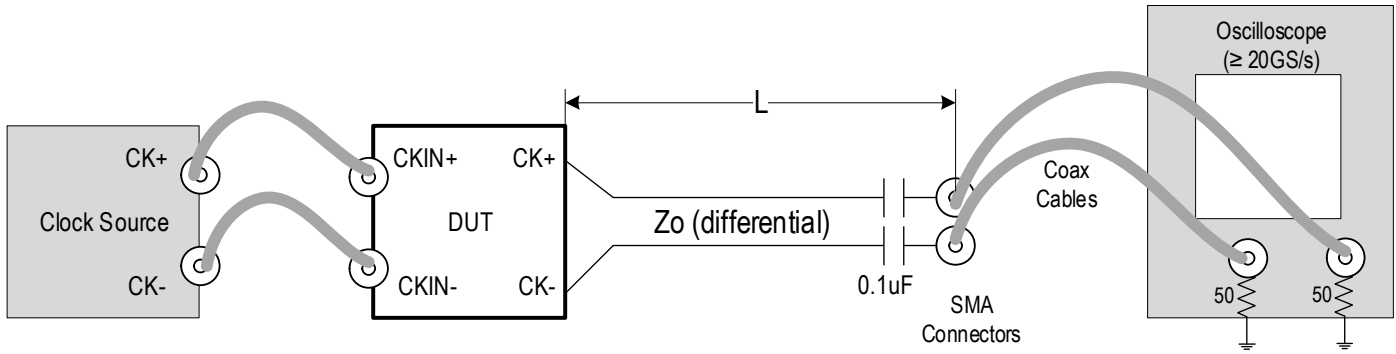


Table 21. Parameters for Phase Jitter Measurements using Oscilloscope

| Clock Source | Device Under Test (DUT) | Rs (Ω) | Differential Zo (Ω) | L (cm) | CL (pF) | Notes | Parameters Measured |
|--------------|-------------------------|-------------|---------------------|--------|---------|-------------|---------------------|
| SMA100B | 9ZXLxx3x | 27 External | 85 | 25.4 | N/A | Fanout Mode | QPI/UPI |
| 9FGV1006 | 9ZXLxx3x | 27 External | 85 | 25.4 | | ZDB Mode | |
| SMA100B | 9ZXLxx5x | Internal | 85 | 25.4 | | Fanout Mode | |
| 9FGV1006 | 9ZXLxx5x | Internal | 85 | 25.4 | | ZDB Mode | |

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|--------------------------|
| Controller (Host) | | Renesas (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| | | ACK |
| Data Byte Count = X | | ACK |
| Beginning Byte N | | ACK |
| O | X Byte | O |
| O | | O |
| O | | O |
| Byte N + X - 1 | | O |
| | | ACK |
| P | stoP bit | |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte N+X-1
- Renesas clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | |
|----------------------------|-----------------|-------------------|
| Controller (Host) | | Renesas |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| | | ACK |
| RT | Repeat starT | |
| Slave Address | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count=X |
| ACK | | Beginning Byte N |
| ACK | | O |
| O | | O |
| O | | O |
| O | | |
| | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

Table 22. SMBus Addressing

| Pin | | SMBus Address | | |
|-----------|-----------|----------------------|----------|----------|
| SADR1_tri | SADR0_tri | 9ZXL12x2 9ZXL0853 | 9ZXL08x2 | 9ZXL06x2 |
| 0 | 0 | D8 | D8 | D8 |
| 0 | M | DA | — | — |
| 0 | 1 | DE | — | — |
| M | 0 | C2 | — | — |
| M | M | C4 | — | — |
| M | 1 | C6 | — | — |
| 1 | 0 | CA | — | — |
| 1 | M | CC | — | — |
| 1 | 1 | CE | — | — |

Note: 9ZXL08x2 and 9ZXL06x2 do not have SMBus address select pins. Their address is D8.

Table 23. Byte 0: PLL Mode and Frequency Select Register

| Byte 0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------|-------------------------------|-------------------------------|----------|----------|-----------------------------------|----------------------|-----------------------------|---------------------------|
| Control Function | PLL Operating Mode Readback 1 | PLL Operating Mode Readback 0 | Reserved | Reserved | Enable software control of PLL BW | PLL Operating Mode 1 | PLL Operating Mode 0 | Frequency Select Readback |
| Type | R | R | | | RW | RW | RW | R |
| 0 | 00 = Low BW ZDB Mode | 01 = Bypass (Fanout Buffer) | | | HW Latch | 00 = Low BW ZDB Mode | 01 = Bypass (Fanout Buffer) | 133MHz |
| 1 | 10 = Reserved | 11 = High BW ZDB Mode | | | SMBus Control | 10 = Reserved | 11 = High BW ZDB Mode | 100MHz |
| Name | PLL Rdbk[1] | PLL Rdbk[0] | | | PLL_SW_EN | PLL Mode[1] | PLL Mode[0] | 100M_133M# |
| Default | Latch | Latch | 0 | 0 | 0 | 1 | 1 | Latch |

Note: Setting bit 3 to '1' allows the user to override the latch value from pin 5 via use of bits 2 and 1. A warm system reset is required if the user changes these bits. Bit 0 defaults to 1 on the 9ZXL06x2 devices.

Table 24. Byte 1: Output Control Register 1

| Byte 1 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------------|-----------------|---------|---------|----------|----------|---------|---------|----------|
| Control Function | Output Enable | | | | | | | |
| Type | RW | | | | | | | |
| 0 | Low/Low | | | | | | | |
| 1 | OE# Pin Control | | | | | | | |
| 9ZXL12xx Name | DIF7_en | DIF6_en | DIF5_en | DIF4_en | DIF3_en | DIF2_en | DIF1_en | DIF0_en |
| 9ZXL12xx Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 9ZXL08xx Name | DIF5_en | DIF4_en | DIF3_en | DIF2_en | Reserved | DIF1_en | DIF0_en | Reserved |
| 9ZXL08xx Default | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 9ZXL06xx Name | Reserved | DIF3_en | DIF2_en | Reserved | Reserved | DIF1_en | DIF0_en | Reserved |
| 9ZXL06xx Default | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

Table 25. Byte 2: Output Control Register 2

| Byte 2 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------------|-----------------|----------|----------|----------|----------|----------|----------|----------|
| Control Function | Output_enable | | | | | | | |
| Type | RW | | | | | | | |
| 0 | Low/Low | | | | | | | |
| 1 | OE# Pin Control | | | | | | | |
| 9ZXL12xx Name | Reserved | Reserved | Reserved | Reserved | DIF11_en | DIF10_en | DIF9_en | DIF8_en |
| 9ZXL12xx Default | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 9ZXL08xx Name | Reserved | Reserved | Reserved | Reserved | Reserved | DIF7_en | Reserved | DIF6_en |
| 9ZXL08xx Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 9ZXL06xx Name | Reserved | Reserved | Reserved | Reserved | Reserved | DIF5_en | DIF4_en | Reserved |
| 9ZXL06xx Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

Bytes 3 and 4 are Reserved

Table 26. Byte 5: Revision and Vendor ID Register

| Byte 5 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------------|--------------|------|------|------|--------------------|------|------|------|
| Control Function | Revision ID | | | | Vendor ID | | | |
| Type | R | R | R | R | R | R | R | R |
| 0 | E rev = 0010 | | | | IDT/Renesas = 0001 | | | |
| 1 | | | | | | | | |
| Name | RID3 | RID2 | RID1 | RID0 | VID3 | VID2 | VID1 | VID0 |
| Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

Table 27. Byte 6: Device ID Register

| Byte 6 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------------|-----------|---------|---------|---------|---------|---------|---------|---------|
| Control Function | N/A | | | | | | | |
| Type | R | R | R | R | R | R | R | R |
| 0 | Device ID | | | | | | | |
| 1 | | | | | | | | |
| Name | DevID 7 | DevID 6 | DevID 5 | DevID 4 | DevID 3 | DevID 2 | DevID 1 | DevID 0 |
| 9ZXL1232E | 0hE8 | | | | | | | |
| 9ZXL1252E | 0hF8 | | | | | | | |
| 9ZXL0832E | 0hE6 | | | | | | | |
| 9ZXL0852E | 0hF6 | | | | | | | |
| 9ZXL0853E | | | | | | | | |
| 9ZXL0632E | 0hE4 | | | | | | | |
| 9ZXL0652E | 0hF4 | | | | | | | |

Table 28. Byte 7: Byte Count Register

| Byte 7 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------------|----------|----------|----------|---|------|------|------|------|
| Control Function | Reserved | Reserved | Reserved | Writing to this register configures how many bytes will be read back on a block read. | | | | |
| Type | | | | RW | RW | RW | RW | RW |
| 0 | | | | Default value is 8. | | | | |
| 1 | | | | | | | | |
| Name | | | | BC4 | BC3 | BC2 | BC1 | BC0 |
| Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

9ZXL06x2E:

www.idt.com/document/psc/ndndg40-package-outline-50-x-50-mm-bodyepad-350mm-sq-040-mm-pitch-qfn

9ZXL08xxE:

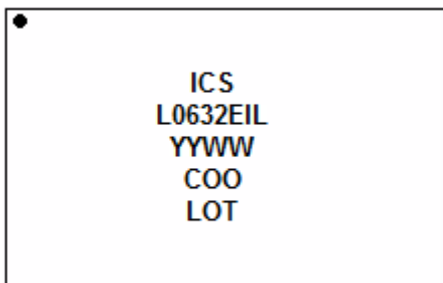
www.idt.com/document/psc/48-vfqfn-package-outline-drawing-60-x-60-x-090-mm-body-epad-42-x-42-mm-040mm-pitch-ndg48p2

9ZXL12x2E:

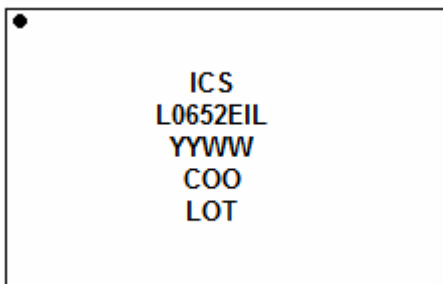
www.idt.com/document/psc/64-vfqfn-package-outline-drawing-90-x-90-x-09-mm-body-05mm-pitch-epad-615-x-615-mm-nlg64p2

Marking Diagrams

9ZXL06x2E



- Lines 1 and 2: truncated part number
- Line 3: "YYWW" is the last two digits of the year and the work week the part was assembled.
- Line 4: "COO" denotes country of origin.
- Line 5: "LOT" denotes the lot number.



9ZXL08xxE

•
 ICS
 XL0832EIL
 YYWW
 COO
 LOT

- Lines 1 and 2: truncated part number
- Line 3: "YYWW" is the last two digits of the year and the work week the part was assembled.
- Line 4: "COO" denotes country of origin.
- Line 5: "LOT" denotes the lot number.

•
 ICS
 XL0852EIL
 YYWW
 COO
 LOT

•
 ICS
 XL0853EIL
 YYWW
 COO
 LOT

9ZXL12x2E

•
 ICS
 9ZXL1232EIL
 LOT
 COO YYWW

- Lines 1 and 2: truncated part number
- Line 3: "LOT" denotes the lot number.
- Line 4: "COO" denotes country of origin; "YYWW" is the last two digits of the year and the work week the part was assembled.

•
 ICS
 9ZXL1252EIL
 LOT
 COO YYWW

Ordering Information

Table 29. Ordering Information

| Number of Clock Outputs | Output Impedance | Orderable Part Number | Temperature Range | Package | Part Number Suffix and Shipping Method |
|-------------------------|------------------|-----------------------|-------------------|-----------------------------|---|
| 6 | 33Ω | 9ZXL0632EKILF | -40° to +85°C | 5 × 5 × 0.4 mm 40-VFQFPN | None = Trays "T" = Tape and Reel, Pin 1 Orientation: EIA-481C (see Table 30 for more details) |
| | | 9ZXL0632EKILFT | | | |
| | 85Ω | 9ZXL0652EKILF | | | |
| | | 9ZXL0652EKILFT | | | |
| 8 | 33Ω | 9ZXL0832EKILF | -40° to +85°C | 6 × 6 × 0.4 mm 48-VFQFPN | |
| | | 9ZXL0832EKILFT | | | |
| | 85Ω | 9ZXL0852EKILF | | | |
| | | 9ZXL0852EKILFT | | | |
| | 85Ω | 9ZXL0853EKILF | | | |
| | | 9ZXL0853EKILFT | | | |
| 12 | 33Ω | 9ZXL1232EKILF | -40° to +85°C | 9 × 9 × 0.5 mm 64-VFQFPN | |
| | | 9ZXL1232EKILFT | | | |
| | 85Ω | 9ZXL1252EKILF | | | |
| | | 9ZXL1252EKILFT | | | |

"E" is the device revision designator (will not correlate with the datasheet revision).

"LF" denotes Pb-free configuration, RoHS compliant.

Table 30. Pin 1 Orientation in Tape and Reel Packaging

| Part Number Suffix | Pin 1 Orientation | Illustration |
|--------------------|------------------------|--------------|
| T | Quadrant 1 (EIA-481-C) | |

Revision History

| Revision Date | Description of Change |
|-----------------|--|
| August 25, 2020 | Updated PCIe Gen5 CC, DB2000Q, and QPI/UPI specifications in Key Specifications section on front page. |
| May 21, 2020 | Initial release. |

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(Rev.1.0 Mar 2020)

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www.renesas.com

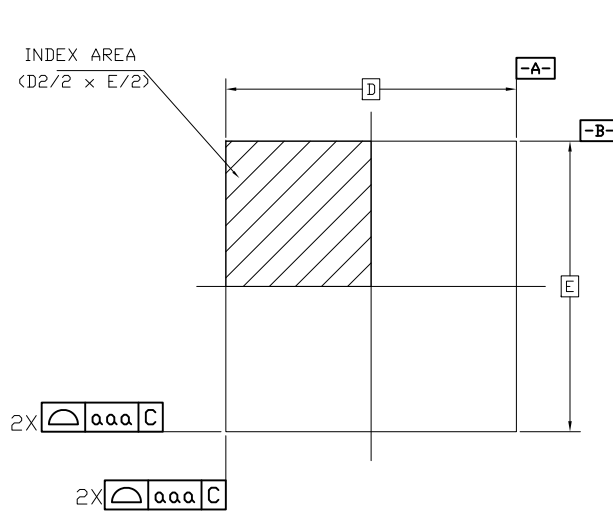
Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

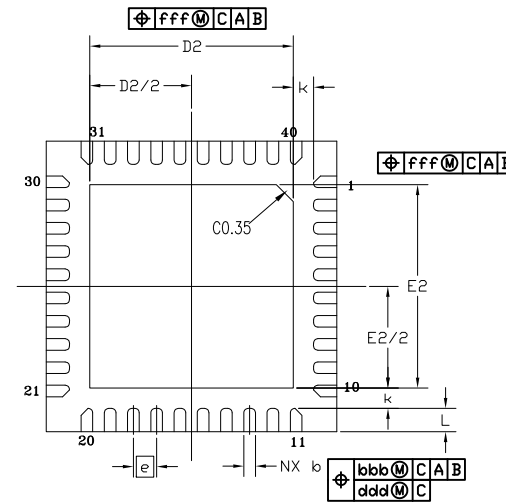
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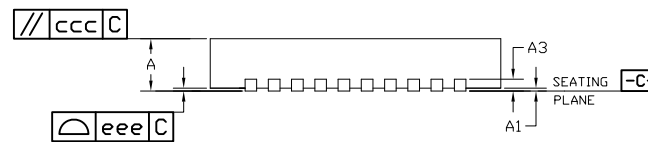
| REVISIONS | | | |
|-----------|-----------------|---------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 5/17/16 | JH |



TOP VIEW



BOTTOM VIEW




SIDE VIEW

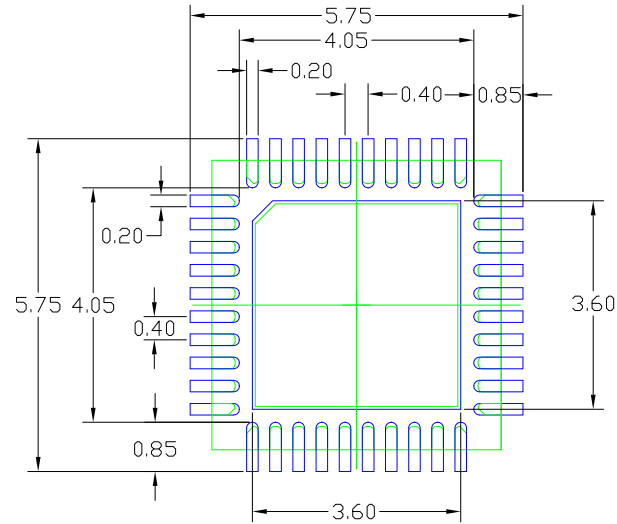
| SYMBOL | DIMENSION | | |
|--------|-------------|------|------|
| | MIN | NOM | MAX |
| b | 0.15 | 0.20 | 0.25 |
| D | 5.00 BSC | | |
| E | 5.00 BSC | | |
| D2 | 3.40 | 3.50 | 3.60 |
| E2 | 3.40 | 3.50 | 3.60 |
| L | 0.30 | 0.40 | 0.50 |
| e | 0.40 BSC | | |
| N | 40 | | |
| ND | 10 (note 3) | | |
| NE | 10 (note 3) | | |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.2 REF | | |
| k | 0.35 REF | | |
| aaa | 0.10 | | |
| bbb | 0.07 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

| | | | |
|-----------------------------|----------|--|---|
| TOLERANCES UNLESS SPECIFIED | |  www.IDT.com | 6024 SILVER CREEK VALLEY ROAD, SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572 |
| DECIMAL | ANGULAR | | |
| X±.1 | ±1° | TITLE/NDG40 PACKAGE OUTLINE | |
| XX±.05 | | 5.0 x 5.0 mm BODY, EPAD 3.50mm SQ. | |
| XXX±.030 | | 0.40 mm PITCH QFN | |
| APPROVALS | DATE | SIZE | DRAWING No. |
| DRAWN <i>ma</i> | 05/31/10 | C | PSC-4292-02 |
| CHECKED | | | REV 00 |
| DO NOT SCALE DRAWING | | | SHEET 1 OF 2 |


| REVISIONS | | | |
|-----------|-----------------|---------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 5/17/16 | JH |

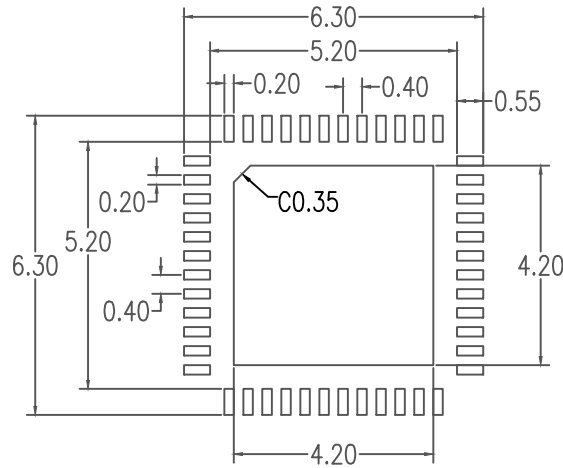


RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| | | | | | |
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| DECIMAL | ANGULAR | | | PHONE: (408) 284-8200 | |
| X±.1 | ±1° | FAX: (408) 284-3572 | | | |
| XX±.05 | | APPROVALS | | | |
| XXX±.030 | | DATE | TITLE | | |
| | | 05/31/10 | END/NDG40 PACKAGE OUTLINE | | |
| | | | 5.0 x 5.0 mm BODY, EPAD 3.50mm SQ. | | |
| | | | 0.40 mm PITCH QFN | | |
| | | SIZE | DRAWING No. | REV | |
| | | C | PSC-4292-02 | 00 | |
| DO NOT SCALE DRAWING | | | | SHEET 2 OF 2 | |

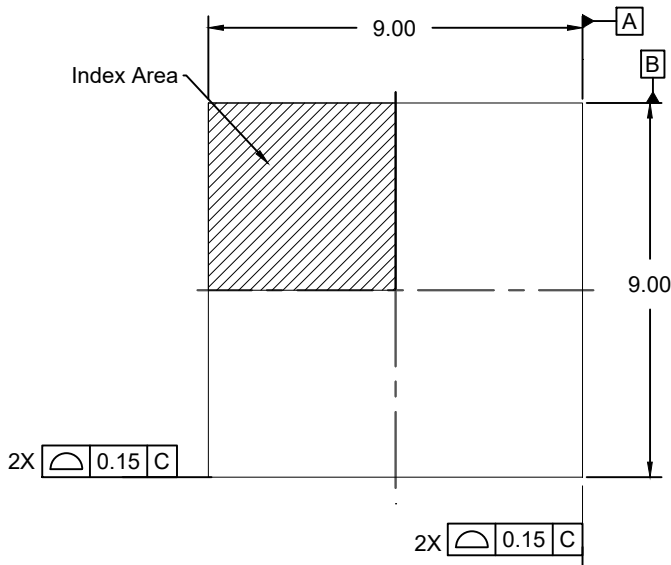


RECOMMENDED LAND PATTERN DIMENSION

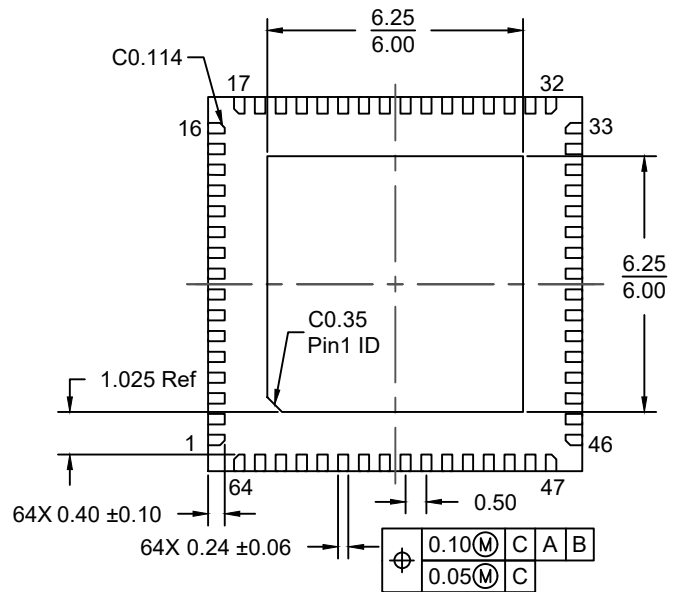
NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

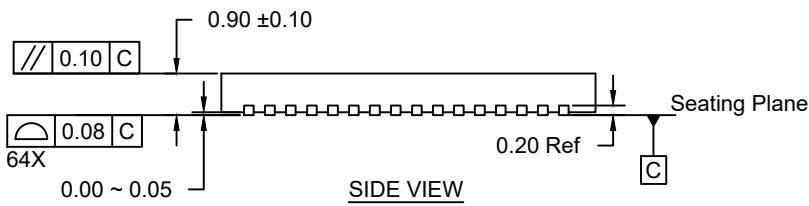
| Package Revision History | | |
|--------------------------|---------|---|
| Date Created | Rev No. | Description |
| July 24, 2018 | Rev 02 | New Format Change QFN to VFQFPN, Recalculate Land Pattern |
| Feb 25, 2020 | Rev 03 | Tolerance Format Change |



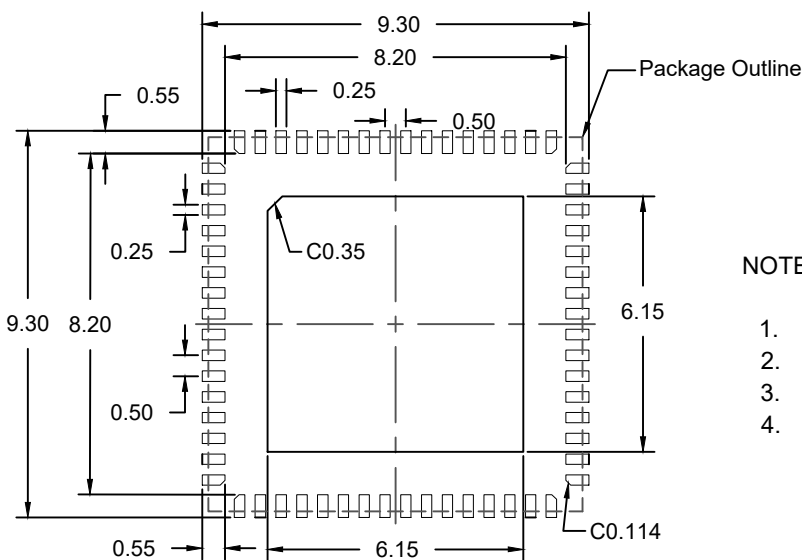
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.