3-Lane 3-Port PCI Express® Switch

89HPES3T3
Data Sheet

Device Overview

The 89HPES3T3 is a member of IDT's PRECISE™ family of PCI Express switching solutions. The PES3T3 is a 3-lane, 3-port peripheral chip that performs PCI Express Base switching. It provides connectivity and switching functions between a PCI Express upstream port and up to four downstream ports and supports switching between downstream ports.

Features

- High Performance PCI Express Switch
  - *Three 2.5Gbps PCI Express lanes*
  - *Three switch ports*
  - *x1 Upstream port*
  - *Two x1 Downstream ports*
  - *Low latency cut-through switch architecture*
  - *Support for Max payload sizes up to 256 bytes*
  - *One virtual channel*
  - *Eight traffic classes*
  - *PCI Express Base Specification Revision 1.1 compliant*
- Flexible Architecture with Numerous Configuration Options
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion on all lanes*
  - *Ability to load device configuration from serial EEPROM*
- Legacy Support
  - *PCI compatible INTx emulation*
  - *Bus locking*
- Highly Integrated Solution
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates three 2.5 Gbps embedded SerDes with 8B/10B encoder/decoder (no separate transceivers needed)*
- Reliability, Availability, and Serviceability (RAS) Features
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports ECRC and Advanced Error Reporting*
  - *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
  - *Compatible with Hot-Plug I/O expanders used on PC mother-boards*
- Power Management
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Supports PCI Power Management Interface specification (PCI-PM 1.2)*
  - *Unused SerDes are disabled.*
  - *Supports Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI) supporting active link state*
- Testability and Debug Features
  - *Built in Pseudo-Random Bit Stream (PRBS) generator*
  - *Numerous SerDes test modes*
  - *Ability to bypass link training and force any link into any mode*
  - *Provides statistics and performance counters*

Block Diagram

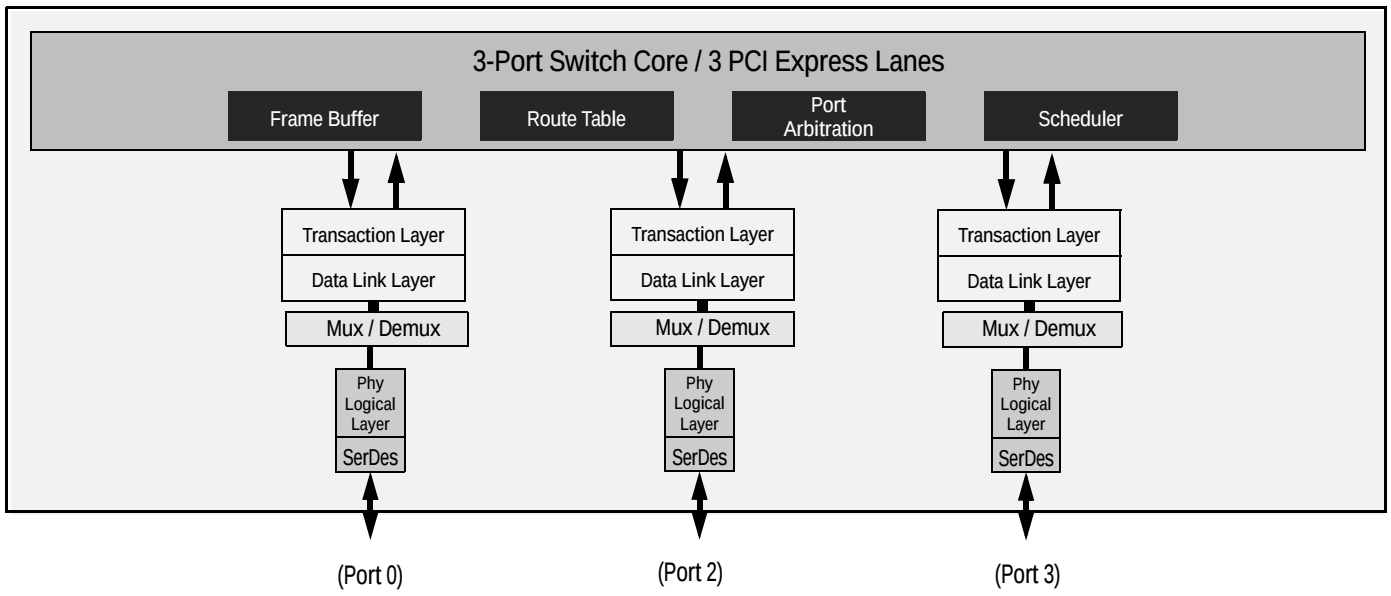


Figure 1 Internal Block Diagram

- Five General Purpose Input/Output Pins
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Four pins have selectable alternate functions*
- Option A Package: 13mm x 13mm 144-ball BGA with 1mm ball spacing
- Option B Package: 10mm x 10mm 132-ball QFN with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES3T3 provides the most efficient fan-out solution for applications requiring x1 connectivity, low latency, and simple board layout with a minimum number of board layers. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.1.

The PES3T3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.1. The PES3T3 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to allow efficient switching for applications requiring additional narrow port connectivity and also some high-end connectivity.

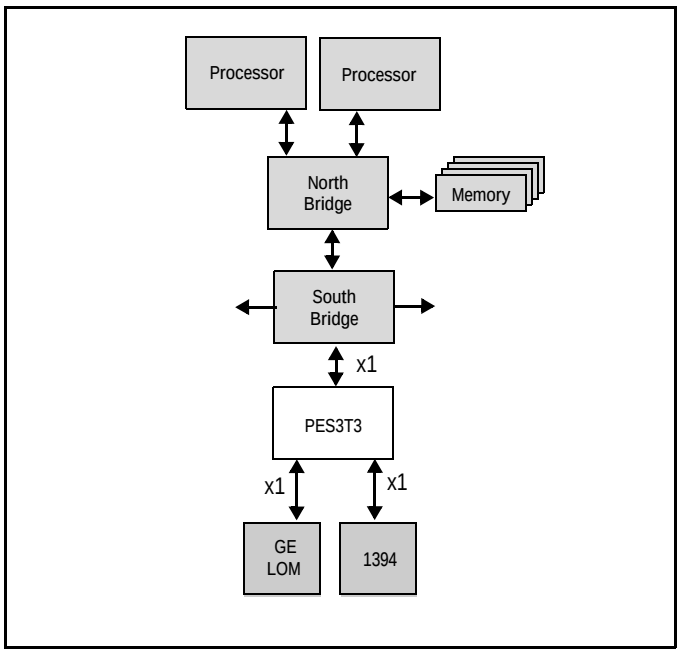


Figure 2 I/O Expansion Application

SMBus Interface

The PES3T3 contains an SMBus master interface. This master interface allows the default configuration register values of the PES3T3 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander. Two pins make up the SMBus master interface. These pins consist of an SMBus clock pin and an SMBus data pin.

Hot-Plug Interface

The PES3T3 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES3T3 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES3T3 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES3T3. In response to an I/O expander interrupt, the PES3T3 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES3T3 provides 5 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control, and each GPIO pin is shared with another on-chip function. These alternate functions may be enabled via software or serial configuration EEPROM.

Pin Description

The following tables lists the functions of the pins provided on the PES3T3. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE0RP[0] PE0RN[0]	I	PCI Express Port 0 Serial Data Receive. Differential PCI Express receive pair for port 0.
PE0TP[0] PE0TN[0]	O	PCI Express Port 0 Serial Data Transmit. Differential PCI Express transmit pair for port 0.
PE2RP[0] PE2RN[0]	I	PCI Express Port 2 Serial Data Receive. Differential PCI Express receive pair for port 2.
PE2TP[0] PE2TN[0]	O	PCI Express Port 2 Serial Data Transmit. Differential PCI Express transmit pair for port 2.
PE3RP[0] PE3RN[0]	I	PCI Express Port 3 Serial Data Receive. Differential PCI Express receive pair for port 3.
PE3TP[0] PE3TN[0]	O	PCI Express Port 3 Serial Data Transmit. Differential PCI Express transmit pair for port 3.
PEREFCLKP PEREFCLKN	I	PCI Express Reference Clock. Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is 100 MHz.

Table 1 PCI Express Interface Pins

Signal	Type	Name/Description
MSMBCLK	I/O	Master SMBus Clock. This bidirectional signal is used to synchronize transfers on the master SMBus.
MSMBDAT	I/O	Master SMBus Data. This bidirectional signal is used for data on the master SMBus.

Table 2 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O Expander interrupt 0 input
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P3RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 3

Table 3 General Purpose I/O Pins

Signal	Type	Name/Description
APWRDISN	I	Auxiliary Power Disable Input. When this pin is active, it disables the device from using auxiliary power supply.
CCLKDS	I	Common Clock Downstream. The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices.This bit is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be override by modifying the SCLK bit in the downstream port's PCIELSTS register.
CCLKUS	I	Common Clock Upstream. The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This bit is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the PA_PCIELSTS register.
PERSTN	I	Fundamental Reset. Assertion of this signal resets all logic inside the PES3T3 and initiates a PCI Express fundamental reset.

Table 4 System Pins (Part 1 of 2)

Signal	Type	Name/Description
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, the PES3T3 executes the reset procedure and remains in a reset state with the Master SMBus active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register by the SMBus master.
SWMODE[2:0]	I	**Switch Mode.** These configuration pins determine the PES3T3 switch operating mode. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 - through 0xF Reserved
WAKEN	I/O	**Wake Input/Output.** The WAKEN signal is an input or output. The WAKEN signal input/output selection can be made through WAKEDIR bit setting in the WAKEUPCNTL register.

Table 4 System Pins (Part 2 of 2)

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock.** This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input.** This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output.** This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode.** The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset.** This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 5 Test Pins

Signal	Type	Name/Description
V_{DD}CORE	I	**Core VDD.** Power supply for core logic.
V_{DD}I/O	I	**I/O VDD.** LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power.** PCI Express digital power used by the digital power of the SerDes.
V_{DD}APE	I	**PCI Express Analog Power.** PCI Express analog power used by the PLL and bias generator.
V_{TT}PE	I	**PCI Express Termination Power.**
V_{SS}	I	**Ground.**

Table 6 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the PES3T3 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface	PE0RN[0]	I	CML	Serial Link		
	PE0RP[0]	I				
	PE0TN[0]	O				
	PE0TP[0]	O				
	PE2RN[0]	I				
	PE2RP[0]	I				
	PE2TN[0]	O				
	PE2TP[0]	O				
	PE3RN[0]	I				
	PE3RP[0]	I				
	PE3TN[0]	O				
	PE3TP[0]	O				
	PEREFCLKN	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 8
	PEREFCLKP	I				
SMBus	MSMBCLK	I/O	LVTTL	STI[1]		
	MSMBDAT	I/O		STI		
General Purpose I/O	GPIO[9,7,2:0]	I/O	LVTTL	High Drive	pull-up	
System Pins	APWRDISN	I	LVTTL	Input	pull-down	
	CCLKDS	I			pull-up	
	CCLKUS	I			pull-up	
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[2:0]	I			pull-down	
	WAKEN	I/O			open-drain	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	

Table 7 Pin Characteristics

1. Schmitt Trigger Input (STI).

Logic Diagram — PES3T3

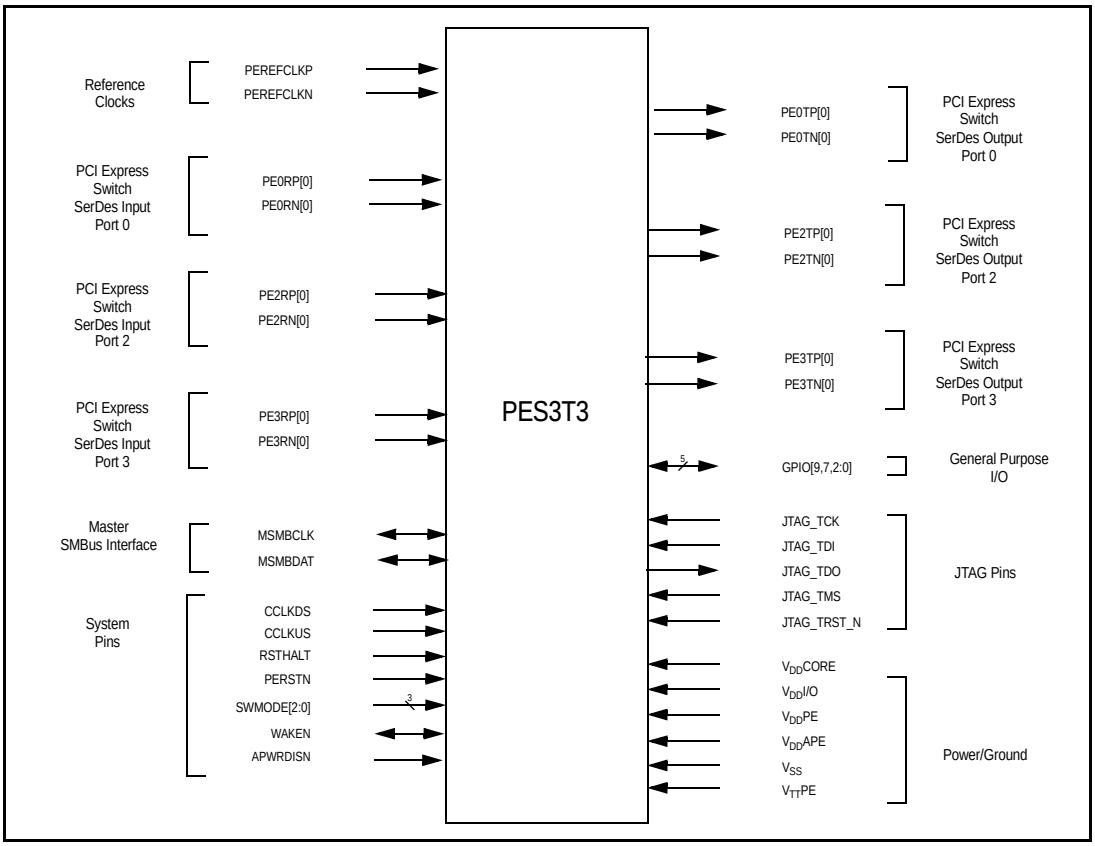


Figure 3 PES3T3 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 12 and 13.

Parameter	Description	Min	Typical	Max	Unit
PEREFCLK					
$Refclk_{FREQ}$	Input reference clock frequency range	100			MHz
$Refclk_{DC}$[1]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[2]
V_{SW}	Differential input voltage swing[3]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps

Table 8 Input Clock Requirements

1. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
2. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
3. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX- IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
T_{BTEn}	Time from asserting Beacon TxEn to beacon being transmitted on the lane		30	80	ns
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
$T_{RX-EYE (with jitter)}$	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI
$T_{RX-EYE-MEDIUM TO MAX JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

Table 9 PCIe AC Timing Characteristics

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[9,7,2:0][1]	Tpw_13b[2]	None	50	—	ns	See Figure 4.

Table 10 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

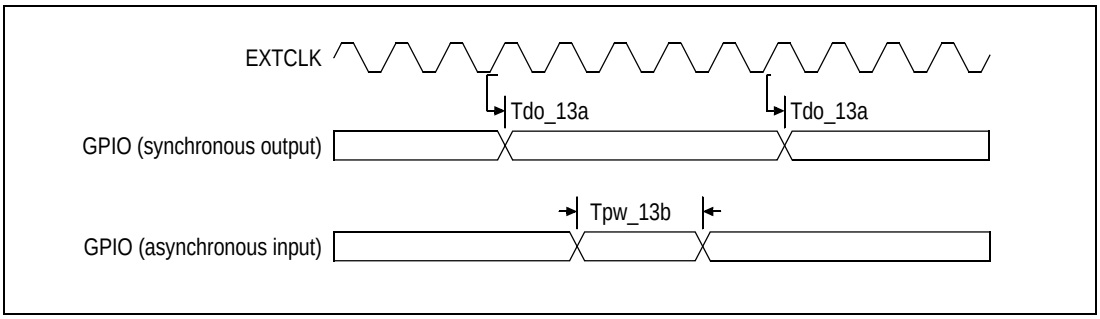


Figure 4 GPIO AC Timing Waveform

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	25.0	50.0	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	11.3	ns	
	Tdz_16c[2]		—	11.3	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 11 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

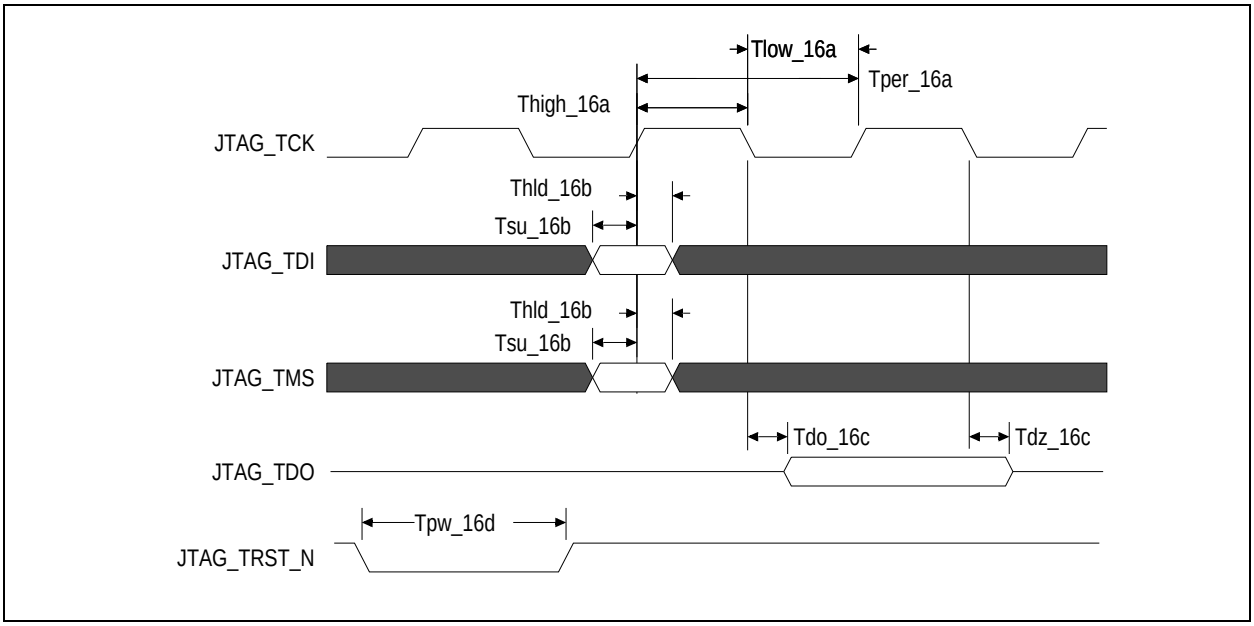


Figure 5 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.135	3.3	3.465	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 12 PES3T3 Operating Voltages

Power-Up/Power-Down Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES3T3, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels.

The power-down sequence must be in the reverse order of the power-up sequence.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 13 PES3T3 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 12.

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 12.

All power measurements assume that the part is mounted on a 10 layer printed circuit board with 0 LFM airflow.

Number of Connected Lanes		Core Supply		PCIe Digital Supply		PCIe Analog Supply		PCIe Termination Supply		I/O Supply		Total (Watts)	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.5V	Max 1.575V	Typ 3.3V	Max 3.465V	Typ	Max
1/1/1	mA	254	330	173	220	99	117	75	94	3	3.3		
	Watts	0.25	0.36	0.17	0.24	0.10	0.13	0.11	0.15	0.01	0.01	0.65	0.89

Table 14 PES3T3 Power Consumption

Thermal Considerations — Option A Package

This section describes thermal considerations for the PES3T3 (13mm^2 BCG144 package). The data in Table 15 below contains information that is relevant to the thermal performance of the PES3T3 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	^{0}C	Maximum
$T_{A(max)}$	Ambient Temperature	70	^{0}C	Maximum for commercial-rated products
$T_{A(max)}$	Ambient Temperature	85	^{0}C	Maximum for industrial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	34.6	^{0}C/W	Zero air flow
		30.3	^{0}C/W	1 m/S air flow
		28.4	^{0}C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	18.8	^{0}C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	10	^{0}C/W	
P	Power Dissipation of the Device	0.89	Watts	Maximum

Table 15 Thermal Specifications for PES3T3, 13x13mm BCG144 Package

Thermal Considerations — Option B Package

This section describes thermal considerations for the PES3T3 (10mm^2 NQG132 package). The data in Table 16 below contains information that is relevant to the thermal performance of the PES3T3 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	^{0}C	Maximum
$T_{A(max)}$	Ambient Temperature	70	^{0}C	Maximum for commercial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	23.5	^{0}C/W	Zero air flow
		19.6	^{0}C/W	1 m/S air flow
		17.4	^{0}C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	0.2	^{0}C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	7.6	^{0}C/W	
P	Power Dissipation of the Device	0.89	Watts	Maximum

Table 16 Thermal Specifications for PES3T3, 10x10mm NQG132 Package

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 12.

Note: See Table 7, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	PCIe Transmit						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	10			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	10			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 17 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	V_{DD}I/O (max)

Table 17 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1.

Option A Package — 144-BGA Signal Pinout for PES3T3

The following table lists the pin numbers and signal names for the PES3T3 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		C11	V_{DD}CORE		F9	V_{DD}CORE		J7	V_{SS}	
A2	V_{DD}IO		C12	V_{SS}		F10	V_{DD}IO		J8	V_{DD}CORE	
A3	APWRDISN		D1	JTAG_TDO		F11	V_{DD}IO		J9	V_{SS}	
A4	V_{TT}PE		D2	MSMBCLK		F12	GPIO_01		J10	V_{SS}	
A5	V_{TT}PE		D3	V_{DD}CORE		G1	V_{SS}		J11	V_{DD}IO	
A6	PE0TP00		D4	V_{SS}		G2	JTAG_TRST_N		J12	GPIO_09	1
A7	V_{DD}PE		D5	V_{SS}		G3	V_{SS}		K1	V_{SS}	
A8	PE0RP00		D6	V_{SS}		G4	V_{DD}CORE		K2	V_{DD}CORE	
A9	V_{DD}IO		D7	V_{DD}CORE		G5	V_{SS}		K3	V_{DD}IO	
A10	SWMODE_0		D8	V_{SS}		G6	V_{DD}CORE		K4	V_{DD}CORE	
A11	SWMODE_1		D9	V_{SS}		G7	V_{SS}		K5	V_{DD}PE	
A12	V_{SS}		D10	V_{SS}		G8	V_{DD}CORE		K6	V_{SS}	
B1	V_{DD}CORE		D11	PERSTN		G9	V_{SS}		K7	V_{DD}PE	
B2	WAKEN		D12	RSTHALT		G10	V_{DD}CORE		K8	V_{SS}	
B3	CCLKUS		E1	JTAG_TDI		G11	V_{SS}		K9	V_{DD}CORE	
B4	V_{DD}PE		E2	MSMBDAT		G12	GPIO_02	1	K10	V_{DD}IO	
B5	V_{DD}PE		E3	V_{DD}IO		H1	PEREFCLKP		K11	V_{SS}	
B6	PE0TN00		E4	V_{DD}CORE		H2	V_{DD}IO		K12	V_{SS}	
B7	V_{DD}PE		E5	V_{SS}		H3	V_{DD}APE		L1	PE2RN00	
B8	PE0RN00		E6	V_{DD}CORE		H4	V_{SS}		L2	V_{SS}	
B9	CCLKDS		E7	V_{SS}		H5	V_{SS}		L3	PE2TP00	
B10	SWMODE_2		E8	V_{SS}		H6	V_{SS}		L4	V_{SS}	
B11	V_{SS}		E9	V_{SS}		H7	V_{DD}CORE		L5	PE3TN00	
B12	V_{SS}		E10	V_{DD}CORE		H8	V_{SS}		L6	V_{DD}APE	
C1	JTAG_TMS		E11	V_{SS}		H9	V_{SS}		L7	PE3RN00	
C2	V_{SS}		E12	GPIO_00	1	H10	V_{DD}CORE		L8	V_{TT}PE	
C3	V_{SS}		F1	JTAG_TCK		H11	V_{SS}		L9	NC	
C4	V_{DD}CORE		F2	V_{DD}IO		H12	GPIO_07	1	L10	V_{SS}	
C5	V_{DD}APE		F3	V_{DD}CORE		J1	PEREFCLKN		L11	NC	
C6	V_{DD}APE		F4	V_{SS}		J2	V_{SS}		L12	V_{DD}CORE	
C7	V_{SS}		F5	V_{DD}CORE		J3	V_{SS}		M1	PE2RP00	
C8	V_{DD}CORE		F6	V_{SS}		J4	V_{SS}		M2	V_{SS}	
C9	V_{DD}CORE		F7	V_{DD}CORE		J5	V_{SS}		M3	PE2TN00	
C10	V_{SS}		F8	V_{SS}		J6	V_{DD}CORE		M4	V_{TT}PE	

Table 18 PES3T3 (13x13, 144-pin) Signal Pin-Out (Part 1 of 2)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
M5	PE3TP00		M7	PE3RP00		M9	NC		M11	NC	
M6	V_{SS}		M8	V_{DD}APE		M10	V_{SS}		M12	V_{SS}	

Table 18 PES3T3 (13x13, 144-pin) Signal Pin-Out (Part 2 of 2)

Option A Package — Alternate Signal Functions

Pin	GPIO	Alternate
E12	GPIO_00	P2RSTN
G12	GPIO_02	IOEXPINTN0
H12	GPIO_07	GPEN
J12	GPIO_09	P3RSTN

Table 19 PES3T3 (13x13, 144-pin) Alternate Signal Functions

Option A Package — Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}I/O	V_{DD}PE	V_{DD}APE	V_{TT}PE
B1	F9	A2	A7	C5	A4
C4	G4	A9	B4	C6	A5
C8	G6	E3	B5	H3	L8
C9	G8	F2	B7	L6	M4
C11	G10	F10	K5	M8	
D3	H7	F11	K7		
D7	H10	H2			
E4	J6	J11			
E6	J8	K3			
E10	K2	K10			
F3	K4				
F5	K9				
F7	L12				

Table 20 PES3T3 (13x13, 144-pin) Power Pins

Option A Package — Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	D10	G11	K1
A12	E5	H4	K6
B11	E7	H5	K8
B12	E8	H6	K11
C2	E9	H8	K12
C3	E11	H9	L2
C7	F4	H11	L4
C10	F6	J2	L10
C12	F8	J3	M2
D4	G1	J4	M6
D5	G3	J5	M10
D6	G5	J7	M12
D8	G7	J9	
D9	G9	J10	

Table 21 PES3T3 (13x13, 144-pin) Ground Pins

Option A Package — Signals Listed Alphabetically

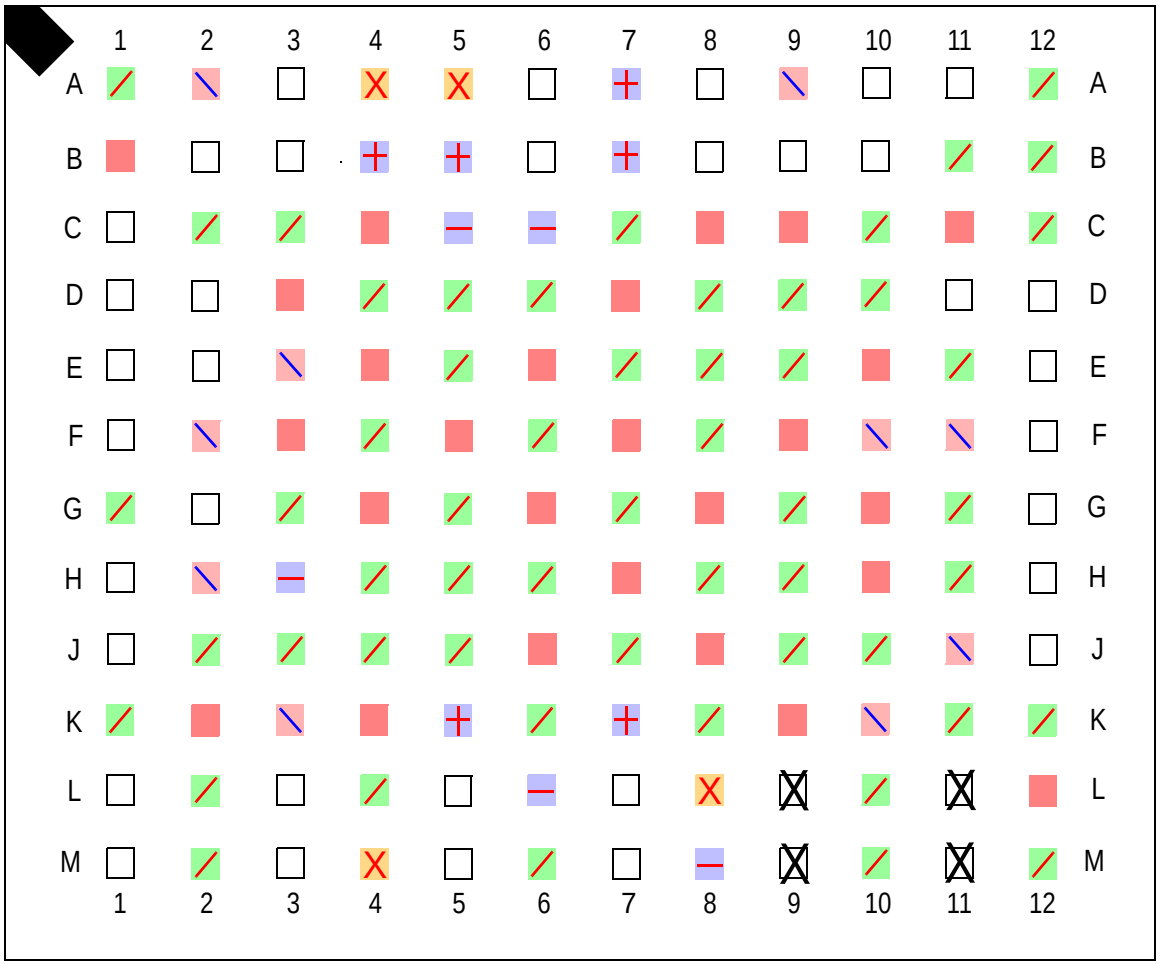
Signal Name	I/O Type	Location	Signal Category
APWRDISN	I	A3	System
CCLKDS	I	B9	
CCLKUS	I	B3	
GPIO_00	I/O	E12	General Purpose Input/Output
GPIO_01	I/O	F12	
GPIO_02	I/O	G12	
GPIO_07	I/O	H12	
GPIO_09	I/O	J12	
JTAG_TCK	I	F1	JTAG
JTAG_TDI	I	E1	
JTAG_TDO	I	D1	
JTAG-TMS	O	C1	
JTAG-TRST_N	I	G2	
MSMBCLK	I/O	D2	SMBus
MSMBDAT	I/O	E2	

Table 22 89PES3T3 (13x13, 144-pin) Alphabetical Signal List (Part 1 of 2)

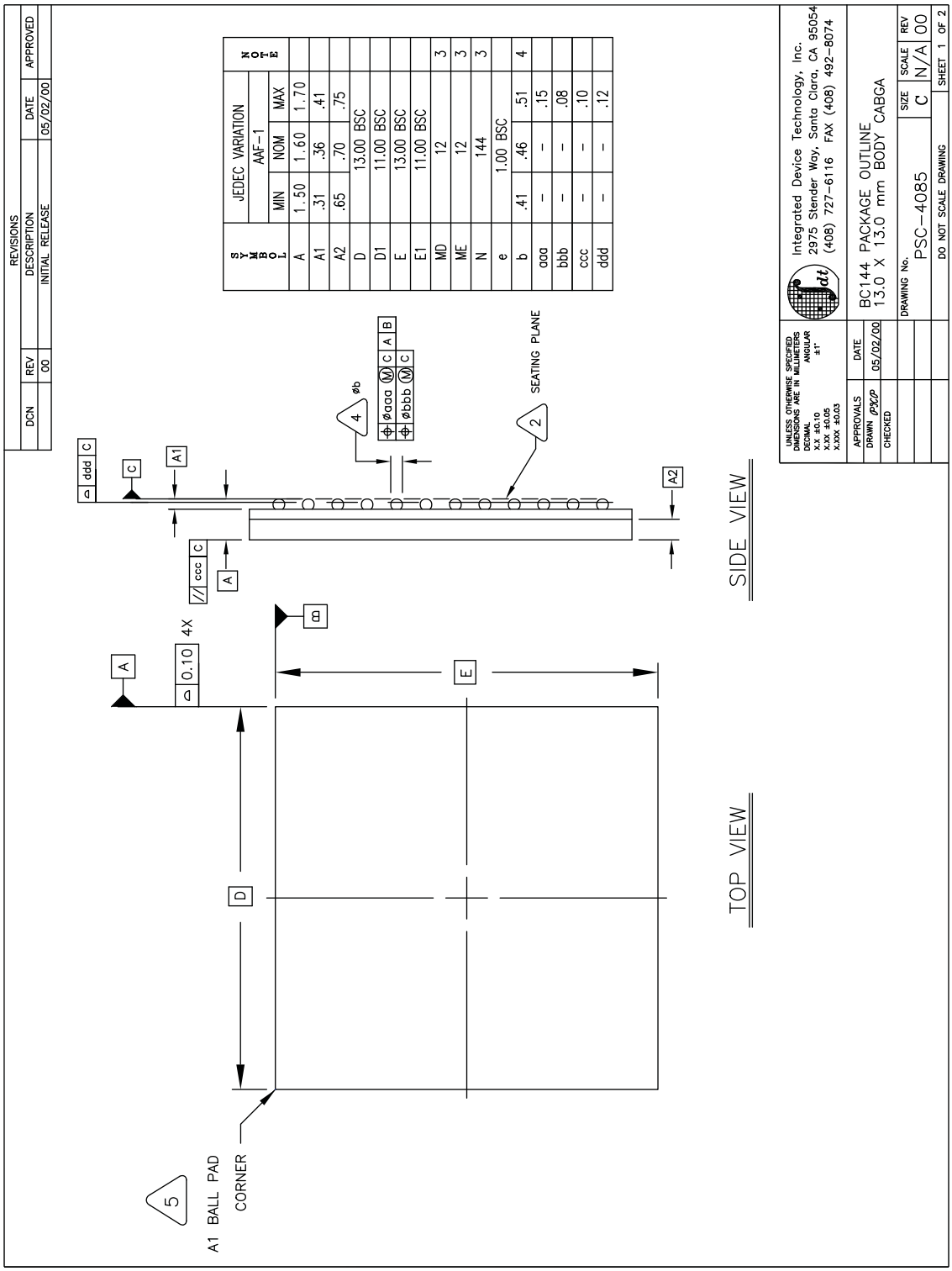
Signal Name	I/O Type	Location	Signal Category
No Connection		L9, L11, M9, M11	
PE0RN00	I	B8	PCI Express
PE0RP00	I	A8	
PE0TN00	O	B6	
PE0TP00	O	A6	
PE2RN00	I	L1	
PE2RP00	I	M1	
PE2TN00	O	M3	
PE2TP00	O	L3	
PE3RN00	I	L7	
PE3RP00	I	M7	
PE3TN00	O	L5	
PE3TP00	O	M5	
PEREFCLKN	I	J1	
PEREFCLKP	I	H1	
PERSTN	I	D11	System
RSTHALT	I	D12	
SWMODE_0	I	A10	
SWMODE_1	I	A11	
SWMODE_2	I	B10	
WAKEN	I/O	B2	
V_{DD}CORE, V_{DD}APE, V_{DD}I/O, V_{DD}PE, V_{TT}PE	See Table 20 for a listing of power pins.		
V_{SS}	See Table 21 for a listing of ground pins.		

Table 22 89PES3T3 (13x13, 144-pin) Alphabetical Signal List (Part 2 of 2)

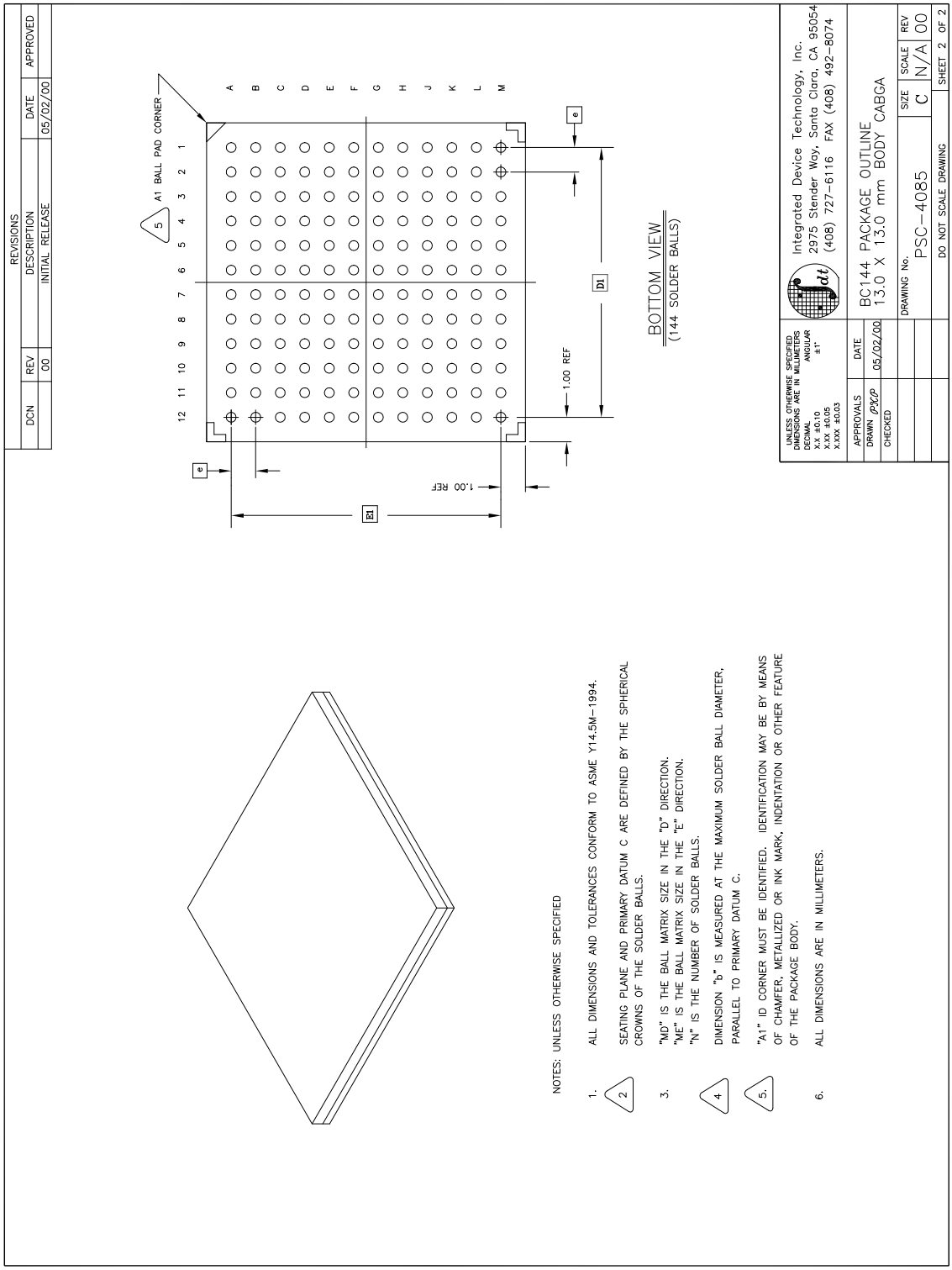
Option A Package Pinout — Top View



Option A Package Drawing — 144-Pin BC144/BCG144



Option A Package Drawing — Page Two



Package B Package Pinout — 132-QFN Signal Pinout for PES3T3

The following table lists the pin numbers and signal names for the PES3T3 132-pin device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	NC		A34	V_{DD}CORE		A67	V_{DD}PE		B28	V_{DD}PE	
A2	NC		A35	NC		A68	V_{DD}CORE		B29	V_{DD}PE	
A3	V_{DD}I/O		A36	NC		A69	V_{DD}I/O		B30	V_{DD}CORE	
A4	V_{DD}I/O		A37	NC		A70	WAKEN		B31	V_{DD}CORE	
A5	V_{DD}CORE		A38	NC		A71	NC		B32	V_{SS}	
A6	V_{DD}CORE		A39	GPIO_09	1	A72	NC		B33	V_{DD}CORE	
A7	MSMBDAT		A40	V_{DD}CORE		B1	V_{SS}		B34	V_{SS}	
A8	MSMBCLK		A41	V_{DD}CORE		B2	V_{SS}		B35	V_{DD}I/O	
A9	V_{SS}		A42	GPIO_07	1	B3	V_{DD}I/O		B36	V_{SS}	
A10	JTAG_TRST_N		A43	V_{SS}		B4	V_{SS}		B37	V_{DD}CORE	
A11	JTAG_TMS		A44	NC		B5	V_{DD}CORE		B38	V_{DD}I/O	
A12	JTAG_TDO		A45	NC		B6	V_{SS}		B39	V_{DD}CORE	
A13	JTAG_TDI		A46	V_{SS}		B7	V_{SS}		B40	V_{DD}CORE	
A14	JTAG_TCK		A47	V_{DD}I/O		B8	V_{DD}CORE		B41	V_{DD}I/O	
A15	PEREFCLKP		A48	GPIO_02	1	B9	V_{DD}I/O		B42	V_{DD}CORE	
A16	PEREFCLKN		A49	GPIO_01	1	B10	V_{DD}CORE		B43	V_{SS}	
A17	NC		A50	GPIO_00	1	B11	V_{SS}		B44	RSTHALT	
A18	NC		A51	V_{DD}I/O		B12	V_{DD}CORE		B45	PERSTN	
A19	NC		A52	V_{DD}CORE		B13	V_{SS}		B46	SWMODE_2	
A20	NC		A53	NC		B14	V_{DD}APE		B47	V_{SS}	
A21	V_{DD}CORE		A54	NC		B15	V_{SS}		B48	V_{DD}CORE	
A22	PE2RP00		A55	NC		B16	V_{DD}I/O		B49	CCLKDS	
A23	PE2TP00		A56	NC		B17	PE2RN00		B50	V_{SS}	
A24	PE2TN00		A57	SWMODE_1		B18	V_{SS}		B51	V_{DD}PE	
A25	PE3TN00		A58	SWMODE_0		B19	V_{DD}PE		B52	V_{DD}PE	
A26	PE3TP00		A59	V_{DD}I/O		B20	V_{TT}PE		B53	V_{TT}PE	
A27	PE3RP00		A60	PE0RN00		B21	V_{DD}PE		B54	V_{DD}APE	
A28	PE3RN00		A61	PE0RP00		B22	V_{SS}		B55	V_{DD}APE	
A29	V_{DD}APE		A62	PE0TP00		B23	V_{SS}		B56	V_{DD}APE	
A30	NC		A63	PE0TN00		B24	V_{DD}APE		B57	V_{SS}	
A31	NC		A64	V_{DD}PE		B25	V_{SS}		B58	APWRDISN	
A32	NC		A65	V_{DD}APE		B26	V_{SS}		B59	V_{DD}CORE	
A33	NC		A66	V_{DD}APE		B27	V_{TT}PE		B60	CCLKUS	

Table 23 PES3T3 (10x10, 132-pin) Signal Pin-Out

Package B Alternate Signal Functions

Pin	GPIO	Alternate
A50	GPIO_00	P2RSTN
A49	GPIO_01	P4RSTN
A48	GPIO_02	IOEXPINTN0
A42	GPIO_07	GPEN
A39	GPIO_09	P3RSTN

Table 24 PES3T3 (10x10, 132-pin) Alternate Signal Functions

Package B Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}I/O	V_{DD}PE	V_{DD}APE	V_{TT}PE
A5	B12	A3	A64	A29	B20
A6	B30	A4	A67	A65	B27
A21	B31	A47	B19	A66	B53
A34	B33	A51	B21	B14	
A40	B37	A59	B28	B24	
A41	B39	A69	B29	B54	
A52	B40	B3	B51	B55	
A68	B42	B9	B52	B56	
B5	B48	B16			
B8	B59	B35			
B10	—	B38			
		B41			

Table 25 PES3T3 (10x10, 132-pin) Power Pins

Package B Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}
A9	B6	B22	B36
A43	B7	B23	B43
A46	B11	B25	B47
B1	B13	B26	B50
B2	B15	B32	B57
B4	B18	B34	—

Table 26 PES3T3 (10x10, 132-pin) Ground Pins

Package B No Connection Pins

NC	NC
A1	A36
A2	A37
A17	A38
A18	A44
A19	A45
A20	A53
A30	A54
A31	A55
A32	A56
A33	A71
A35	A72

Table 27 PES3T3 (10x10, 132-pin) No Connection Pins

Package B Pin Signals Listed Alphabetically

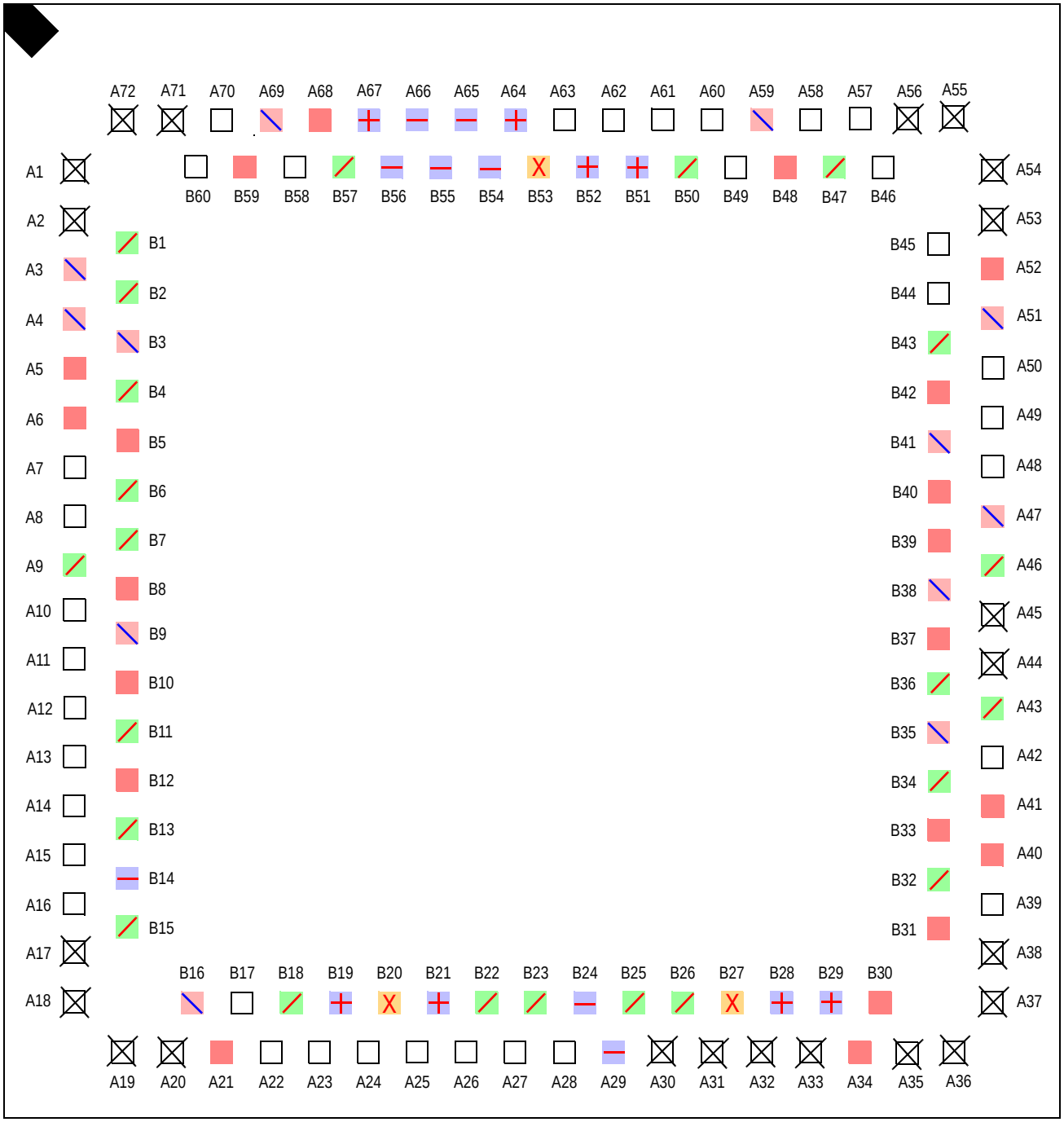
Signal Name	I/O Type	Location	Signal Category
APWRDISN	I	B58	System
CCLKDS	I	B49	
CCLKUS	I	B60	
GPIO_00	I/O	A50	General Purpose Input/Output
GPIO_01	I/O	A49	
GPIO_02	I/O	A48	
GPIO_07	I/O	A42	
GPIO_09	I/O	A39	
JTAG_TCK	I	A14	JTAG
JTAG_TDI	I	A13	
JTAG_TDO	I	A12	
JTAG-TMS	O	A11	
JTAG-TRST_N	I	A10	
MSMBCLK	I/O	A8	SMBus
MSMBDAT	I/O	A7	
NC	See Table 27 for a listing of no connection pins.		
PE0RN00	I	A60	PCI Express
PE0RP00	I	A61	
PE0TN00	O	A63	
PE0TP00	O	A62	
PE2RN00	I	B17	
PE2RP00	I	A22	
PE2TN00	O	A24	
PE2TP00	O	A23	
PE3RN00	I	A28	
PE3RP00	I	A27	
PE3TN00	O	A25	
PE3TP00	O	A26	
PEREFCLKN	I	A16	
PEREFCLKP	I	A15	

Table 28 89PES3T3 (10x10, 132-pin) Alphabetical Signal List (Part 1 of 2)

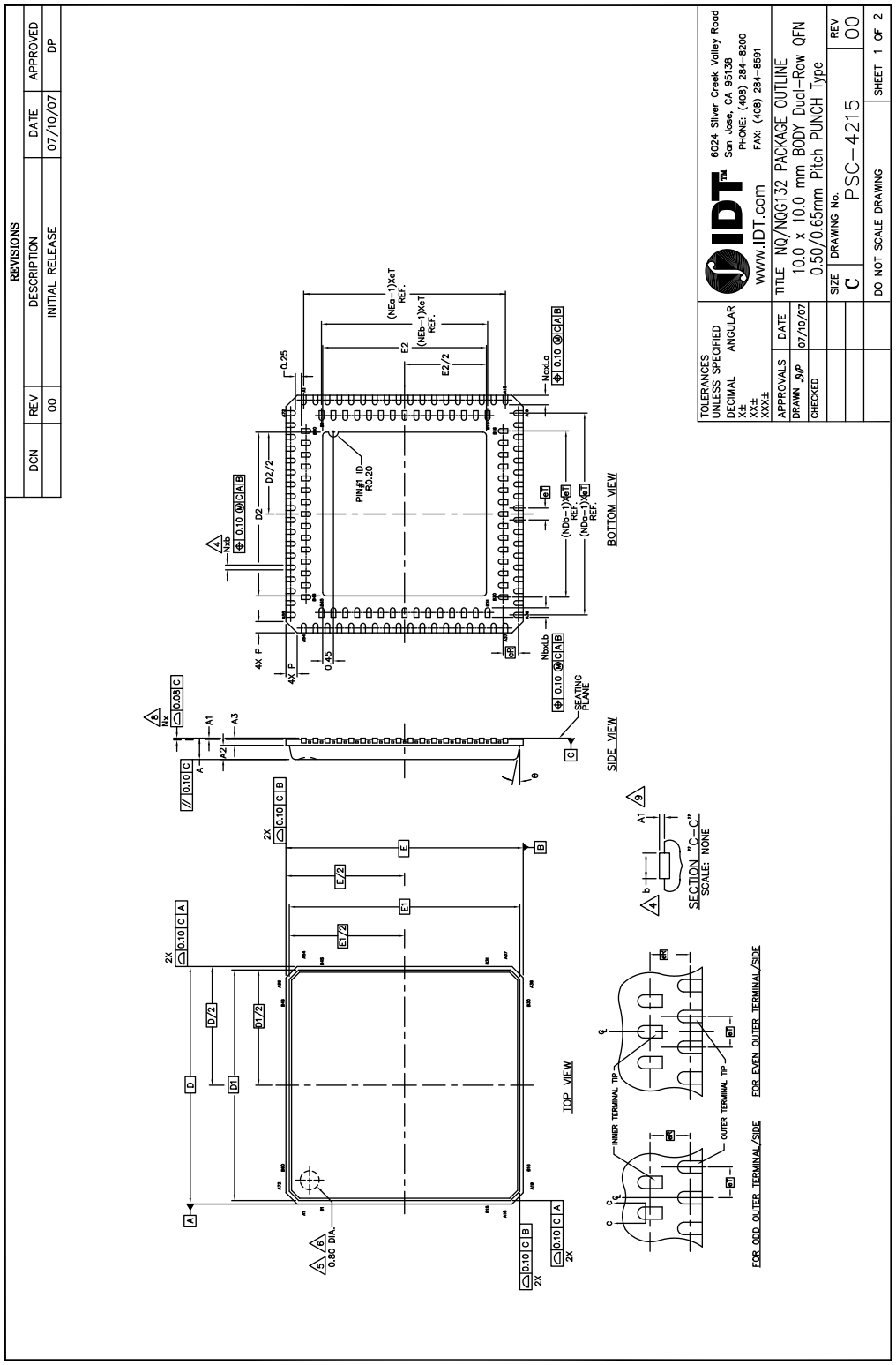
Signal Name	I/O Type	Location	Signal Category
PERSTN	I	B45	System
RSTHALT	I	B44	
SWMODE_0	I	A58	
SWMODE_1	I	A57	
SWMODE_2	I	B46	
WAKEN	I/O	A70	
V_{DD}CORE, V_{DD}APE, V_{DD}I/O, V_{DD}PE, V_{TT}PE	See Table 25 for a listing of power pins.		
V_{SS}	See Table 26 for a listing of ground pins.		

Table 28 89PES3T3 (10x10, 132-pin) Alphabetical Signal List (Part 2 of 2)

Package B Pinout — Top View



Package B Package Drawing — 132-Pin NQ132/NQG132



REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	07/10/07	DP

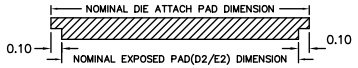
NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   NDa, NDb ARE THE NUMBER OF TERMINALS IN X–DIRECTION &
   NEa, NEb ARE THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
9. APPLIED ONLY FOR TERMINALS.
   <STANDARD>
10. DIMENSIONS OF D2 & E2 : 6.5mm x 6.5mm

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	8
A2	0.55	0.60	0.65	
A3		0.25 REF.		
D		10.00 BSC		
D1		9.73 BSC		
E		10.00 BSC		
E1		9.73 BSC		

SYMBOL	PITCH VARIATION			NOTE
	MIN.	NOM.	MAX.	
eT		0.50 BSC		
eR		0.65 BSC		
N		132		3
NDa		18		3
NDb		15		3
NEa		18		3
NEb		15		3
La	0.30	0.40	0.50	
Lb	0.30	0.40	0.50	
b	0.17	0.22	0.27	4
D2		SEE NOTE		
E2		SEE NOTE		
θ	–	–	12°	
P	0.24	0.42	0.60	

GENERAL ; NOMINAL EXPOSED PAD(D2/E2) DIMENSION = NOMINAL DIE ATTACH PAD DIMENSION–0.20



<DIE ATTACH PAD X–SECTION VIEW>

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DECIMAL ANGULAR X± XX± XXX±			
APPROVALS	DATE	TITLE	NQ/NQG132 PACKAGE OUTLINE 10.0 x 10.0 mm BODY Dual–Row QFN 0.50/0.65mm Pitch PUNCH Type
DRAWN SJP	07/10/07		
CHECKED		SIZE C	DRAWING No. PSC–4215 REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 2

Revision History

March 31, 2008: Publication of final data sheet.

June 4, 2008: For the 132-QFN package, changed pins A44 and A45 from GPIO to No Connect and changed pin B6 from V_{DD}CORE to V_{SS}.

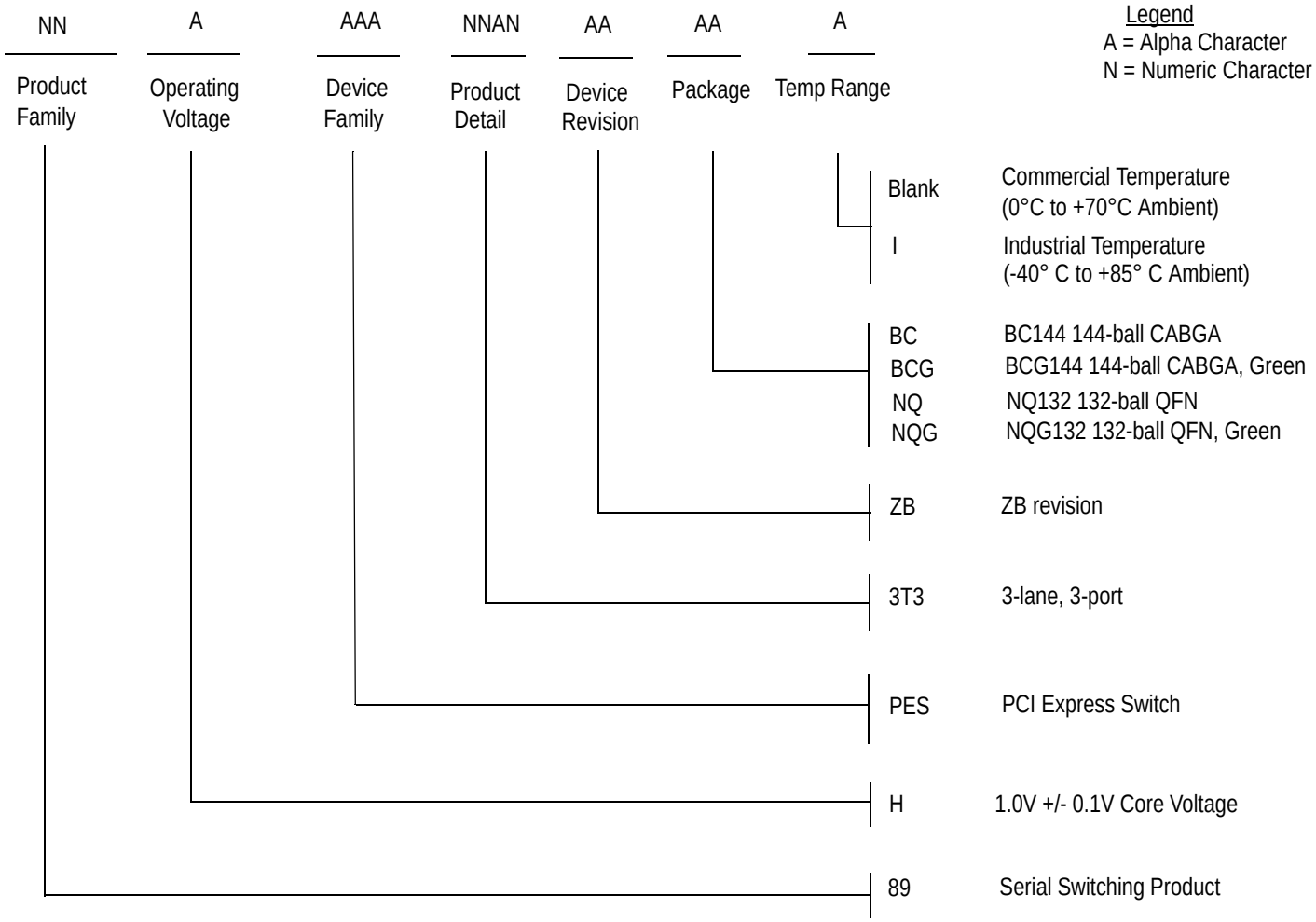
August 6, 2008: Added industrial temperature information to Tables 13 and 15 and to Ordering Information section. Revised Package B Pinout Top View graphic to match page 3 of the Package B drawing.

May 7, 2009: Revised labels in Table 14, Power Consumption, for greater clarification.

October 8, 2010: Added package height data to Note 10 on Page Two of Package B drawing and removed page 3 of Package B drawing.

June 12, 2014: Changed symbol A in Option A Package Drawing — 144-Pin BC144/BCG144 to match the package characteristics of the part. The new definition for the symbol is 1.50 minimum, 1.60 nominal, and 1.70 maximum.

Ordering Information



Valid Combinations

Option A Package

89HPES3T3ZBBC	144-pin BC144 package, Commercial Temperature
89HPES3T3ZBBCG	144-pin Green BC144 package, Commercial Temperature
89HPES3T3ZBBCI	144-pin BC144 package, Industrial Temperature
89HPES3T3ZBBCGI	144-pin Green BC144 package, Industrial Temperature

Option B Package

89HPES3T3ZBNQ	132-pin NQ132 package, Commercial Temperature
89HPES3T3ZBNQG	132-pin Green NQ132 package, Commercial Temperature

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(Rev.1.0 Mar 2020)

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