

74LVC2G241

Dual buffer/line driver; 3-state

Rev. 16 — 31 July 2019

Product data sheet

1. General description

The 74LVC2G241 is a dual non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and 2OE:

- A HIGH level at pin $1\overline{OE}$ causes output 1Y to assume a high-impedance OFF-state.
- A LOW level at pin 2OE causes output 2Y to assume a high-impedance OFF-state.

Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of the 74LVC2G241 as a translator in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC2G241DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G241DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G241GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm	SOT833-1
74LVC2G241GF	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm	SOT1089
74LVC2G241GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm	SOT1116
74LVC2G241GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1.0 x 0.35 mm	SOT1203

4. Marking

Table 2. Marking codes

Type number	Marking code ^[1]
74LVC2G241DP	V241
74LVC2G241DC	V41
74LVC2G241GT	V41
74LVC2G241GF	V1
74LVC2G241GN	V1
74LVC2G241GS	V1

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

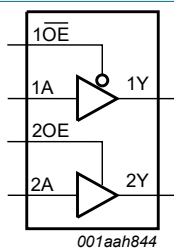


Fig. 1. Logic symbol

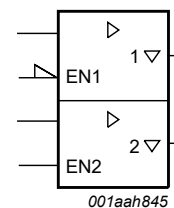
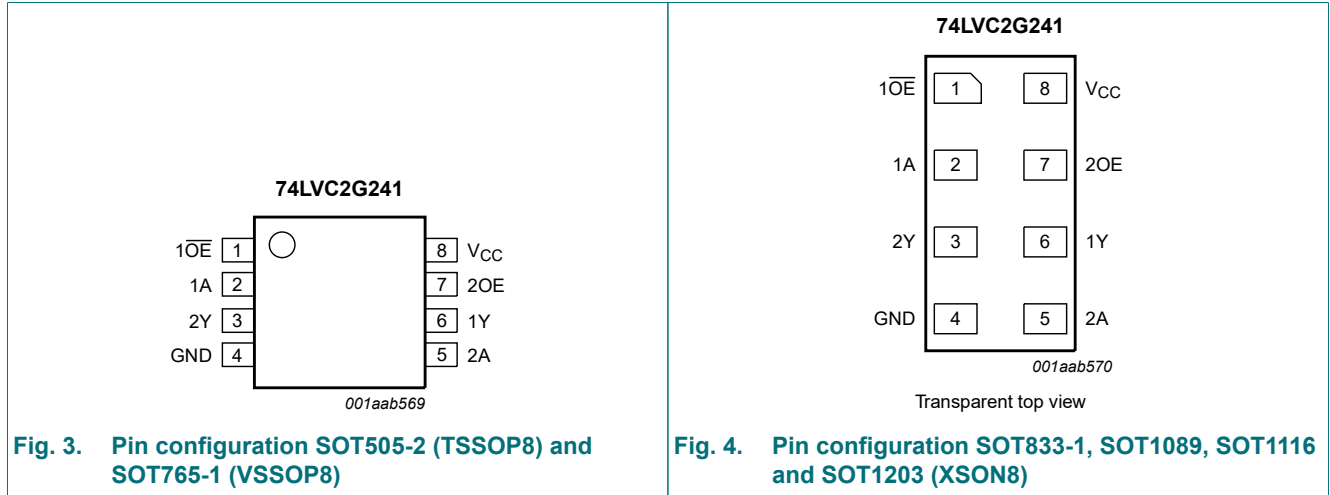


Fig. 2. IEC logic symbol

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1OE	1	output enable input (active LOW)
1A, 2A	2, 5	data input
GND	4	ground (0 V)
1Y, 2Y	6, 3	data output
2OE	7	output enable input (active HIGH)
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input				Output	
1OE	1A	2OE	2A	1Y	2Y
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
V_O	output voltage	enable mode [1]	-0.5	$V_{CC} + 0.5$	V
		disable mode [1]	-0.5	+6.5	V
		$V_{CC} = 0$ V; Power-down mode [1]	-0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT505-2 (TSSOP8) packages: P_{tot} derates linearly with 4.6 mW/K above 96 °C.
 For SOT765-1 (VSSOP8) packages: P_{tot} derates linearly with 4.9 mW/K above 99 °C.
 For SOT833-1 (XSON8) packages: P_{tot} derates linearly with 3.1 mW/K above 68 °C.
 For SOT1089 (XSON8) packages: P_{tot} derates linearly with 4.0 mW/K above 88 °C.
 For SOT1116 (XSON8) packages: P_{tot} derates linearly with 4.2 mW/K above 90 °C.
 For SOT1203 (XSON8) packages: P_{tot} derates linearly with 3.6 mW/K above 81 °C.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	$V_{CC} = 1.65$ V to 5.5 V; enable mode	0	V_{CC}	V
		$V_{CC} = 1.65$ V to 5.5 V; disable mode	0	5.5	V
		$V_{CC} = 0$ V; Power-down mode	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.3	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 μA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.3	-	-	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±1	μA
		V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; V _{CC} = 3.6 V	-	±0.1	±2	μA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	±0.1	±2	μA
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	0.1	4	μA
ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	-	5	500	μA
C _I	input capacitance		-	2	-	pF

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.70	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.80	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.80	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 μA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	0.95	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.7	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	1.9	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.0	-	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.4	-	-	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	±1	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; V _{CC} = 3.6 V	-	-	±2	μA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	-	±2	μA
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	-	4	μA
ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	-	-	500	μA

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Fig. 5 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	4.5	8.8	1.0	11.0	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.8	4.9	0.5	6.3	ns
		V _{CC} = 2.7 V	1.0	2.8	4.7	1.0	5.9	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.6	4.3	0.5	5.4	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	2.1	3.7	0.5	4.6	ns
t _{en}	enable time	1OE to 1Y; see Fig. 6 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.5	5.2	9.9	1.5	12.4	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.1	5.6	1.0	7.0	ns
		V _{CC} = 2.7 V	1.5	3.2	5.5	1.5	6.9	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.7	4.7	0.5	5.9	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	2.0	3.8	0.5	4.8	ns
		2OE to 2Y; see Fig. 7 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	4.3	8.8	1.0	11.0	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.7	4.7	1.0	5.9	ns
		V _{CC} = 2.7 V	1.0	2.7	4.6	1.0	5.8	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.5	4.1	1.0	5.1	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.9	3.3	0.5	4.1	ns
t _{dis}	disable time	1OE to 1Y; see Fig. 6 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	3.2	11.6	1.0	14.1	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.2	5.8	0.5	7.6	ns
		V _{CC} = 2.7 V	1.0	2.8	4.6	1.0	5.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.6	4.4	1.0	5.7	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	2.0	3.4	0.5	4.6	ns
		2OE to 2Y; see Fig. 7 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	3.6	12.5	1.0	15.2	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.0	5.2	0.5	6.9	ns
		V _{CC} = 2.7 V	1.5	3.2	4.9	1.5	6.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.8	4.2	1.0	5.4	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	2.0	3.3	0.5	4.4	ns
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} [3]						
		output enabled	-	20	-	-	-	pF
		output disabled	-	5	-	-	-	pF

[1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZH} and t_{PZL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

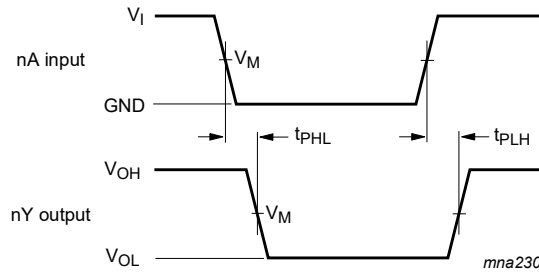
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF;

V_{CC} = supply voltage in V; N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit



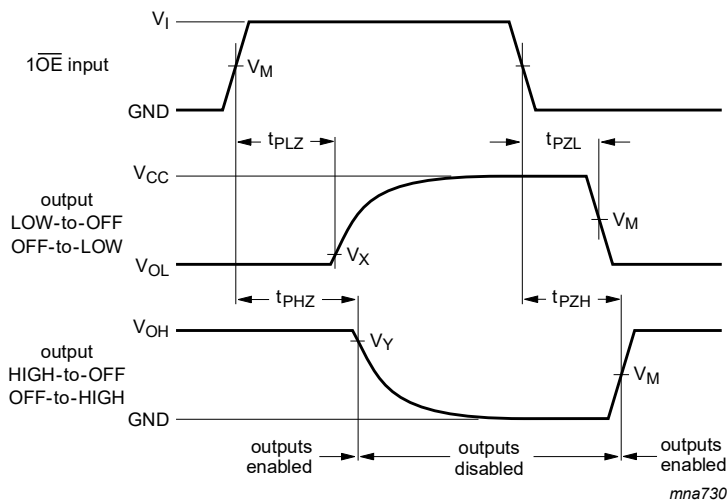
Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The data input (nA) to output (nY) propagation delays

Table 9. Measurement points

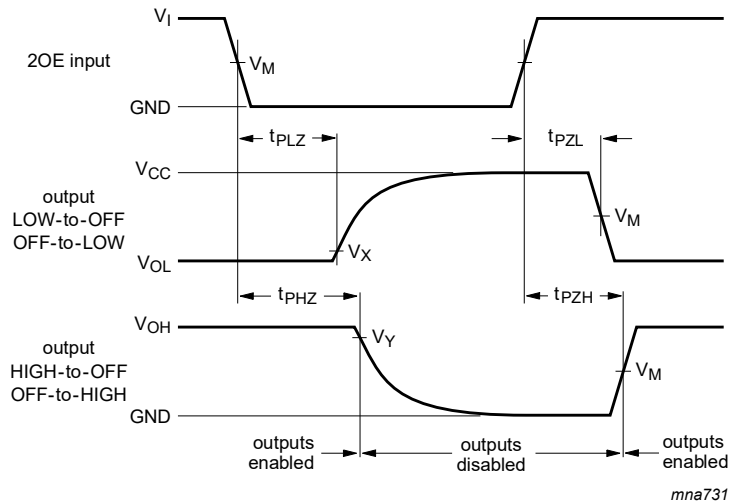
Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

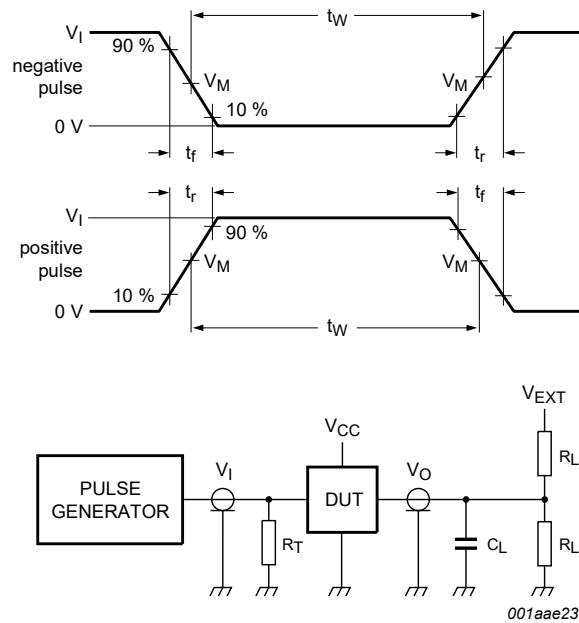
Fig. 6. Enable and disable times for input 1OE



Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. Enable and disable times for input 2OE



Test data is given in [Table 10](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance; R_L = Load resistance.

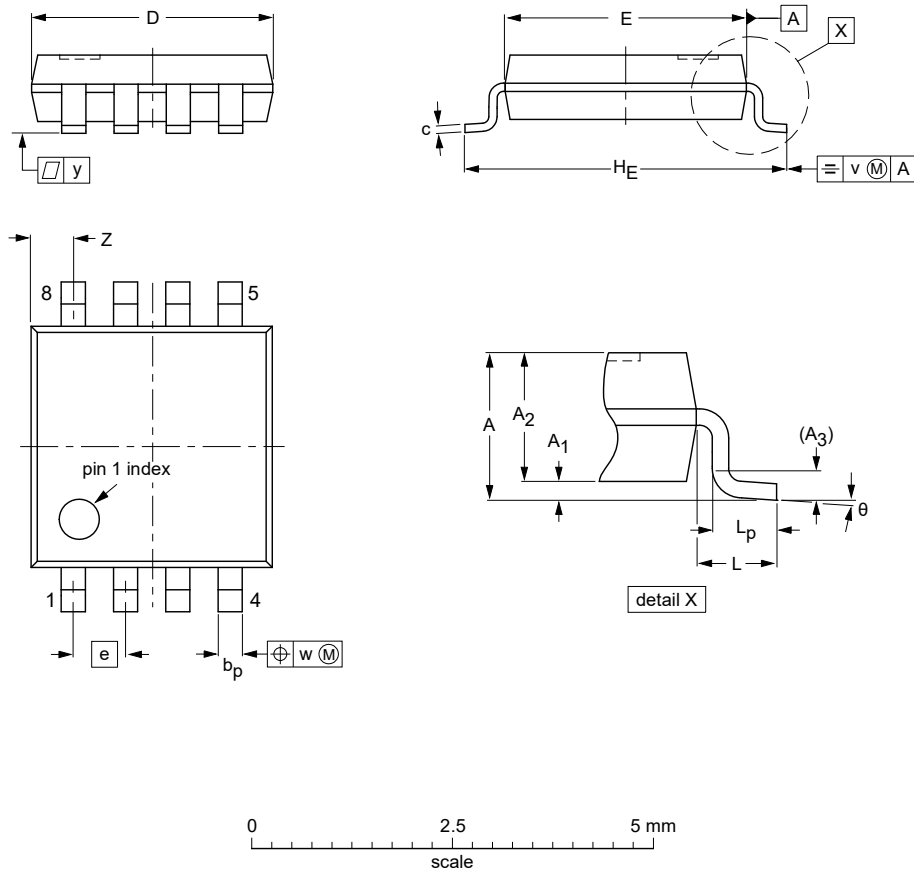
Fig. 8. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load		V_{EXT}		
	V_I	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	30 pF	1 k Ω	open	GND	2 x V_{CC}
2.3 V to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	2 x V_{CC}
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	50 pF	500 Ω	open	GND	2 x V_{CC}

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

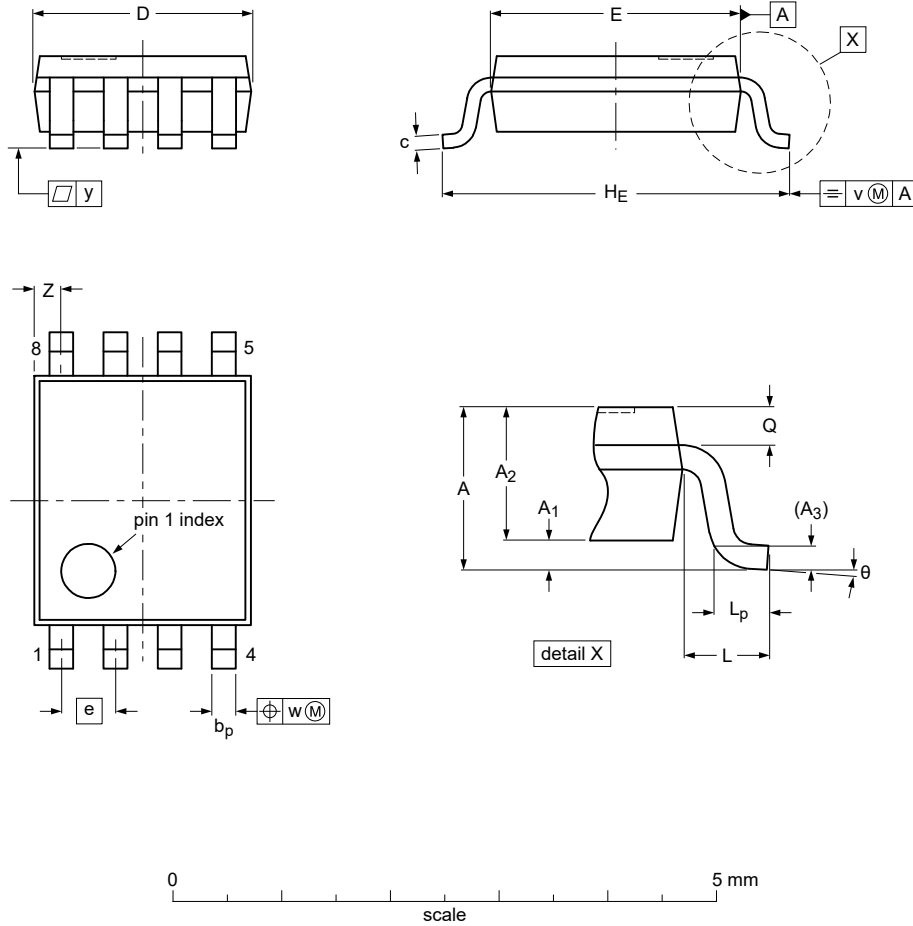
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

Fig. 9. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Dimensions (mm are the original dimensions)

Unit	A ^A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
max		0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
mm	nom	1		0.12				0.5		0.4				0.2	0.08	0.1		
	min		0.00	0.60	0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

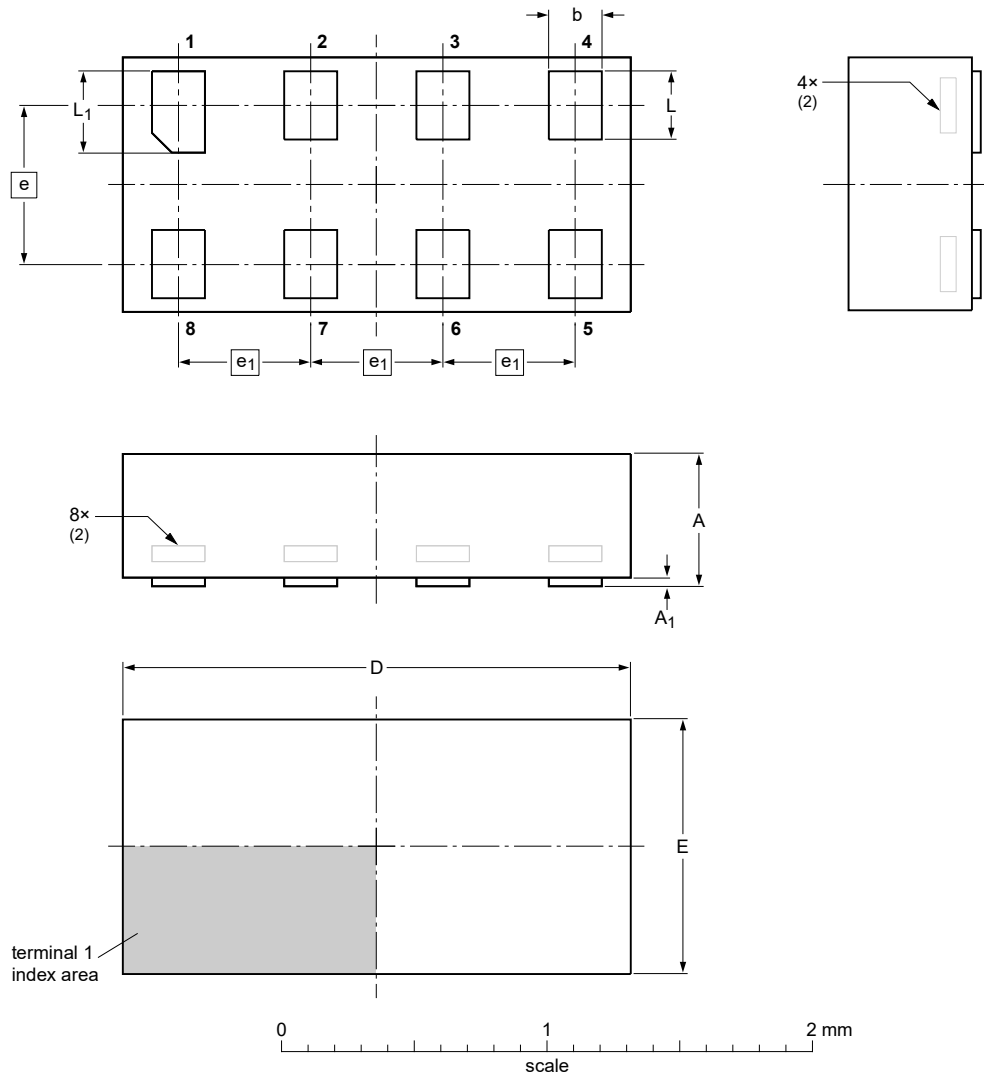
sot765-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT765-1		MO-187			-07-06-02-16-05-31

Fig. 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

- Including plating thickness.
- Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT833-1	---	MO-252	---		-07-11-14 07-12-07

Fig. 11. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1 x 0.5 mm

SOT1089

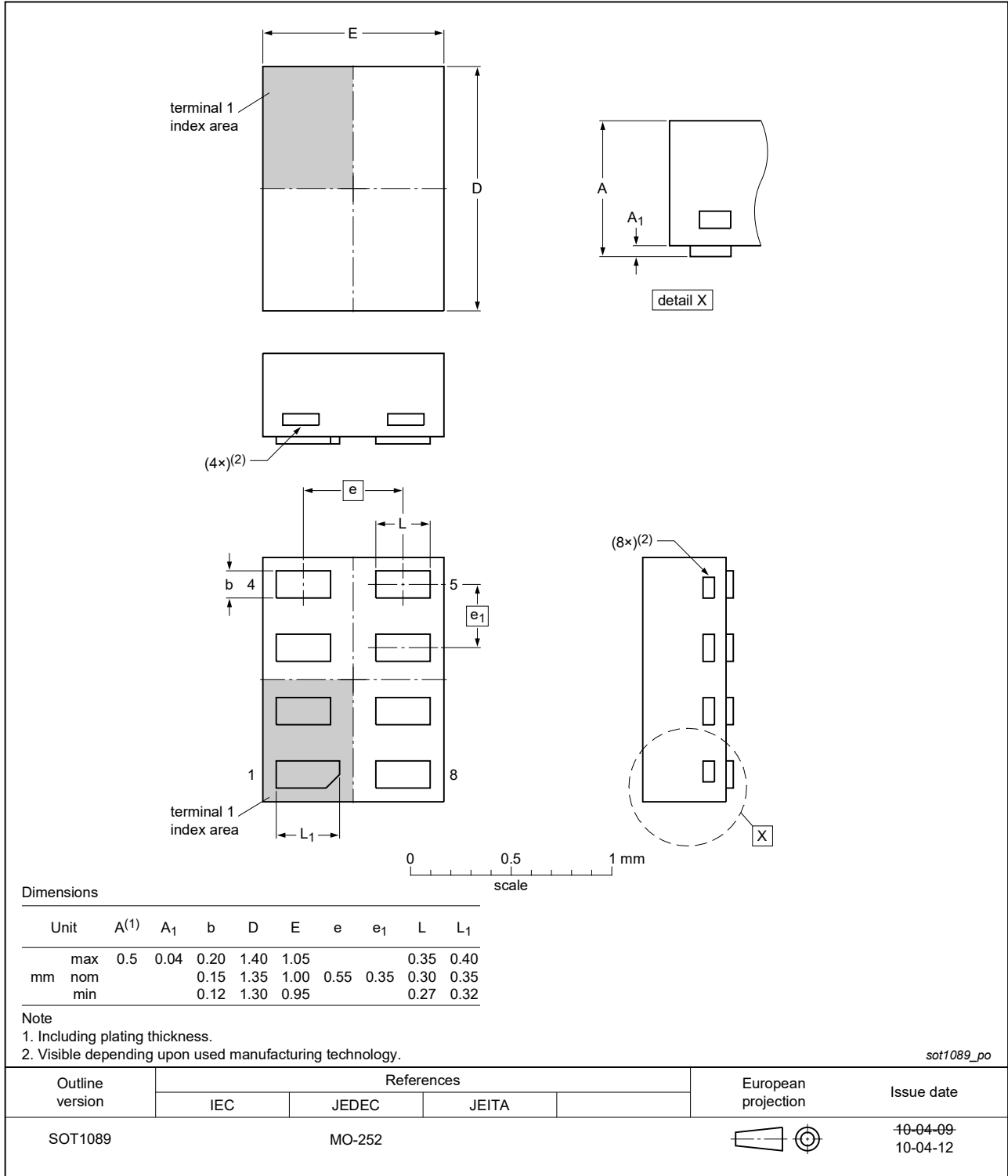
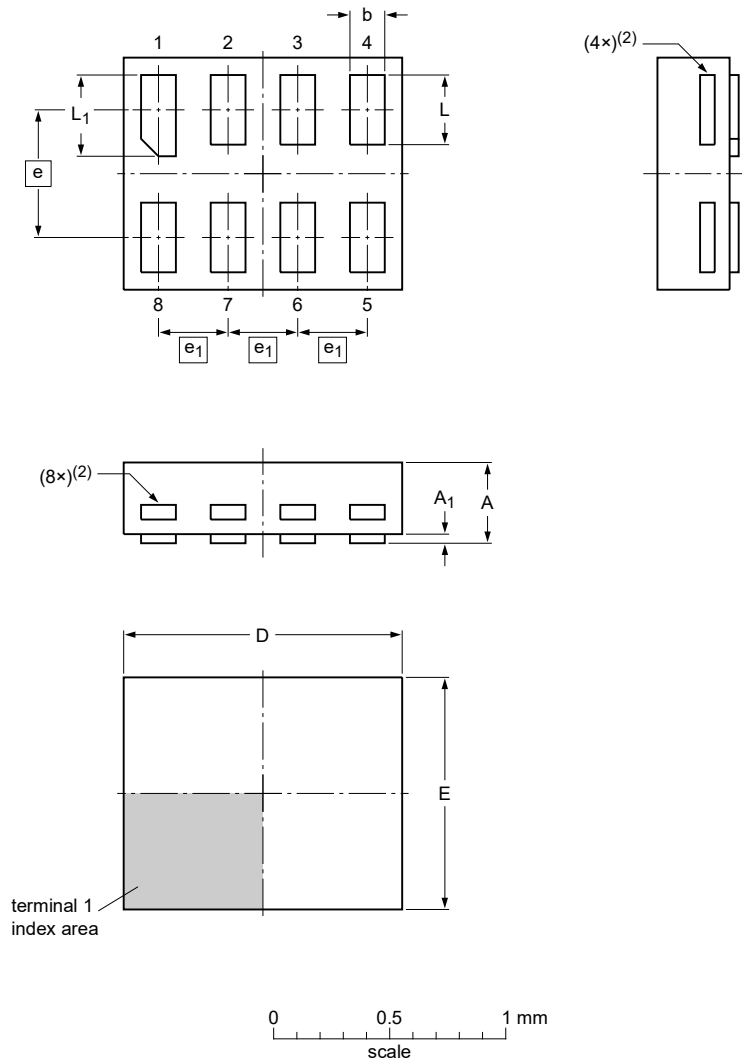


Fig. 12. Package outline SOT1089 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max 0.35	0.04	0.20	1.25	1.05			0.35	0.40
	nom		0.15	1.20	1.00	0.55	0.3	0.30	0.35
	min		0.12	1.15	0.95			0.27	0.32

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

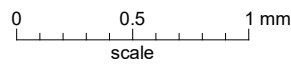
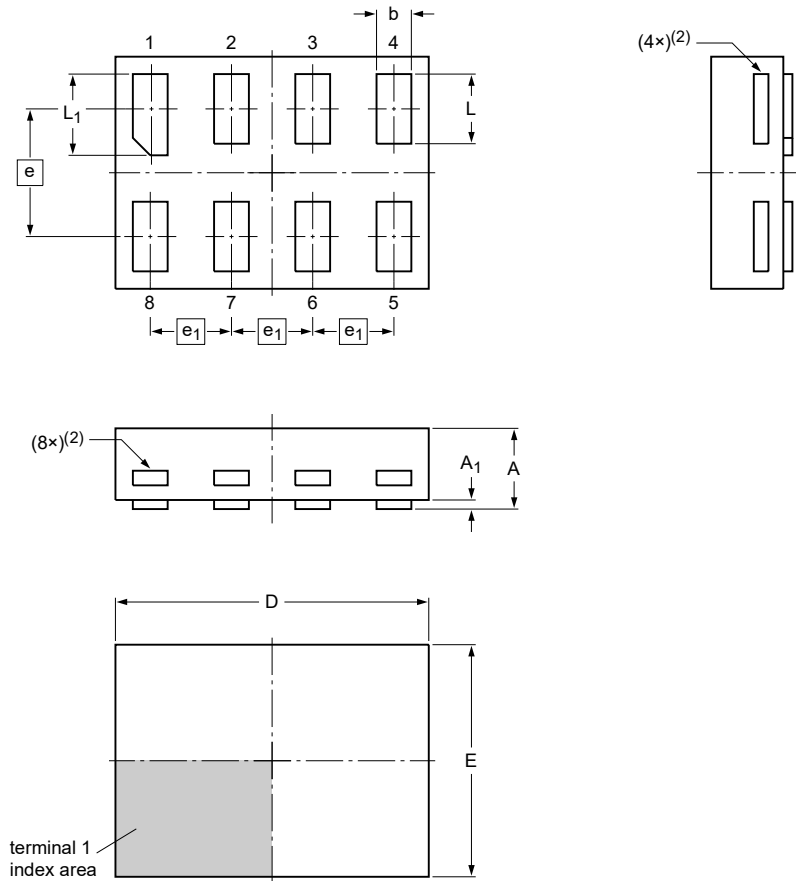
sot1116_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1116					-10-04-02- 10-04-07

Fig. 13. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max 0.35	0.04	0.20	1.40	1.05			0.35	0.40
	nom		0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min		0.12	1.30	0.95			0.27	0.32

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

sot1203_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1203						-10-04-02- 10-04-06

Fig. 14. Package outline SOT1203 (XSON8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G241 v.16	20190731	Product data sheet	-	74LVC2G241 v.15
Modifications:	<ul style="list-style-type: none"> Type number 74LVC2G241GM (SOT902-2/XQFN8) removed. Table 5: Derating values for P_{tot} total power dissipation updated. 			
74LVC2G241 v.15	20181122	Product data sheet	-	74LVC2G241 v.14
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74LVC2G241GD (SOT996-2/XSON8) removed. 			
74LVC2G241 v.14	20161215	Product data sheet	-	74LVC2G241 v.13
Modifications:	<ul style="list-style-type: none"> Table 7: The maximum limits for leakage current and supply current have changed. 			
74LVC2G241 v.13	20130408	Product data sheet	-	74LVC2G241 v.12
Modifications:	<ul style="list-style-type: none"> For type number 74LVC2G241GD XSON8U has changed to XSON8. 			
74LVC2G241 v.12	20120622	Product data sheet	-	74LVC2G241 v.11
Modifications:	<ul style="list-style-type: none"> For type number 74LVC2G241GM the SOT code has changed to SOT902-2. 			
74LVC2G241 v.11	20111129	Product data sheet	-	74LVC2G241 v.10
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74LVC2G241 v.10	20100806	Product data sheet	-	74LVC2G241 v.9
74LVC2G241 v.9	20080610	Product data sheet	-	74LVC2G241 v.8
74LVC2G241 v.8	20080312	Product data sheet	-	74LVC2G241 v.7
74LVC2G241 v.7	20071005	Product data sheet	-	74LVC2G241 v.6
74LVC2G241 v.6	20060922	Product data sheet	-	74LVC2G241 v.5
74LVC2G241 v.5	20050202	Product specification	-	74LVC2G241 v.4
74LVC2G241 v.4	20040922	Product specification	-	74LVC2G241 v.3
74LVC2G241 v.3	20030311	Product specification	-	74LVC2G241 v.2
74LVC2G241 v.2	20030129	Product specification	-	74LVC2G241 v.1
74LVC2G241 v.1	20021030	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	2
4. Marking	2
5. Functional diagram	2
6. Pinning information	3
6.1. Pinning.....	3
6.2. Pin description.....	3
7. Functional description	3
8. Limiting values	4
9. Recommended operating conditions	4
10. Static characteristics	5
11. Dynamic characteristics	7
11.1. Waveforms and test circuit.....	8
12. Package outline	10
13. Abbreviations	16
14. Revision history	16
15. Legal information	17

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