数字双路同步降压功率驱动器

查询样片: UCD7242-EP

特性

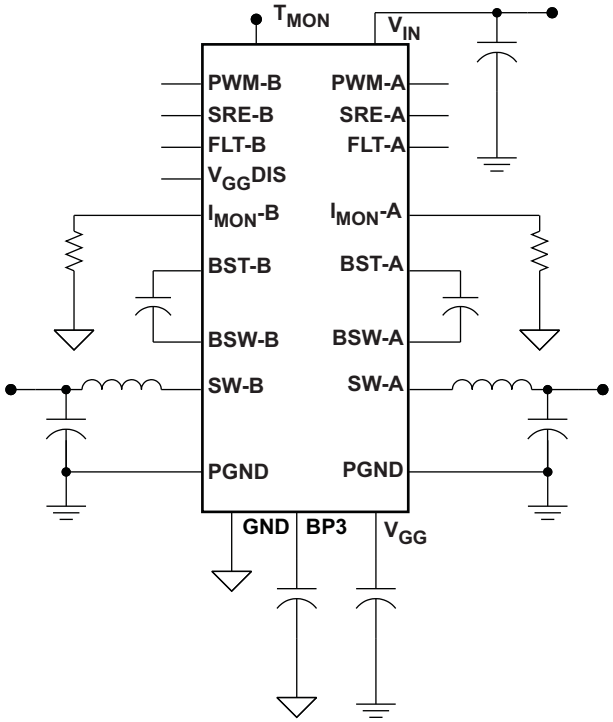
- 具有针对双路同步降压转换器的驱动器的全集成电源开关
- 完全兼容 **TI** 整合数字电源 **(Fusion Digital Power)** 控制器，如 **UCD92xx** 系列
- 宽输入电压范围：**4.75V** 至 **18V**
  运行低至具有一个外部偏置电源的 **2.2V** 输入
- 每通道高达 **10A** 输出电流
- 工作开关频率 **2 MHz**
- 具有电流限值标记的高侧电流限值
- 来自 V_{IN} 的板载经稳压 **6V** 驱动器电源
- 过热保护
- 热感测输出 **-** 电压与芯片温度成比例
- 欠压闭锁 **(UVLO)** 和过压闭锁 **(OVLO)** 确保适当的驱动电压
- 符合 **RoHS** 环保标准
- 精确的芯片上电流感测 **(±5%)**

应用范围

- 数控同步降压功率级
- 针对台式机、服务器、电信和笔记本处理器的高电流双相位电压调整模块和企业级降压稳压器 **(VRM/EVRD)** 稳压器

支持国防、航空航天、和医疗应用

- 受控基线
- 同一组装和测试场所
- 一个制造场所
- 支持军用（**-55°C** 至 **125°C**）温度范围
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性



说明

UCD7242 是一款可驱动两个独立降压电源的完整电源系统（请见 图 1）。 在一个单片解决方案中完全集成高侧金属氧化物半导体场效应晶体管 (MOSFET)，低侧 MOSFET，驱动器，电流感测电路以及必要的保护功能，以最大限度地减小尺寸和提高效率。 驱动器电路可在同步降压电路中为高侧 NMOS 开关和低侧 NMOS 同步整流器提供高充电及放电电流。 MOSFET 栅极可由内部经稳压 V_{GG} 电源驱动至 +6.25V 电压。 可禁用内部 V_{GG} 稳压器，以允许用户提供一个独立的栅极驱动电压。 这种高灵活性支持 2.2V 至 18V 宽电源转换输入电压范围。内部欠压闭锁 (UVLO) 逻辑可在允许芯片工作之前确保 V_{GG} 良好。

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

说明（继续）

同步整流器使能 (SRE) 引脚在 PWM 信号为低电平时控制低侧 MOSFET 是否打开。 当 SRE 为高电平时，此部件针对所有负载以连续传导模式运行。 在这个模式下，此驱动逻辑模块使用脉宽调制 (PWM) 信号来控制高侧与低侧栅极驱动信号。 还优化了死区时间以防止交叉传导。 当 SRE 为低电平时，此部件在轻负载时运行在断续传导模式下。 在这个模式下，低侧 MOSFET 始终保持关闭。

板载比较器监控流经高侧开关的电流，以保护功率级不受突发高电流负载的影响。 针对高侧比较器设置消隐延迟，以避免与开关边沿噪声同时发生故障报告。 如果发生过流故障，高侧 FET 被关闭并且故障标志 (FLT) 被置为有效以警告控制器。

由一个高精度集成电流感测元件测量和监控 MOSFET 电流。 这个方法在大多数负载范围内提供 ±5% 的精度。 I_{MON} 引脚上的控制器可使用这个被放大的信号。

一个片载温度感测将芯片温度转换为供控制器使用的 T_{MON} 上的电压。 如果芯片温度超过 170°C，此温度传感器发起一个暂停输出切换的热关断并且将 FLT 标志置位。 当芯片温度下降到低于热滞后频带时，正常运行恢复。

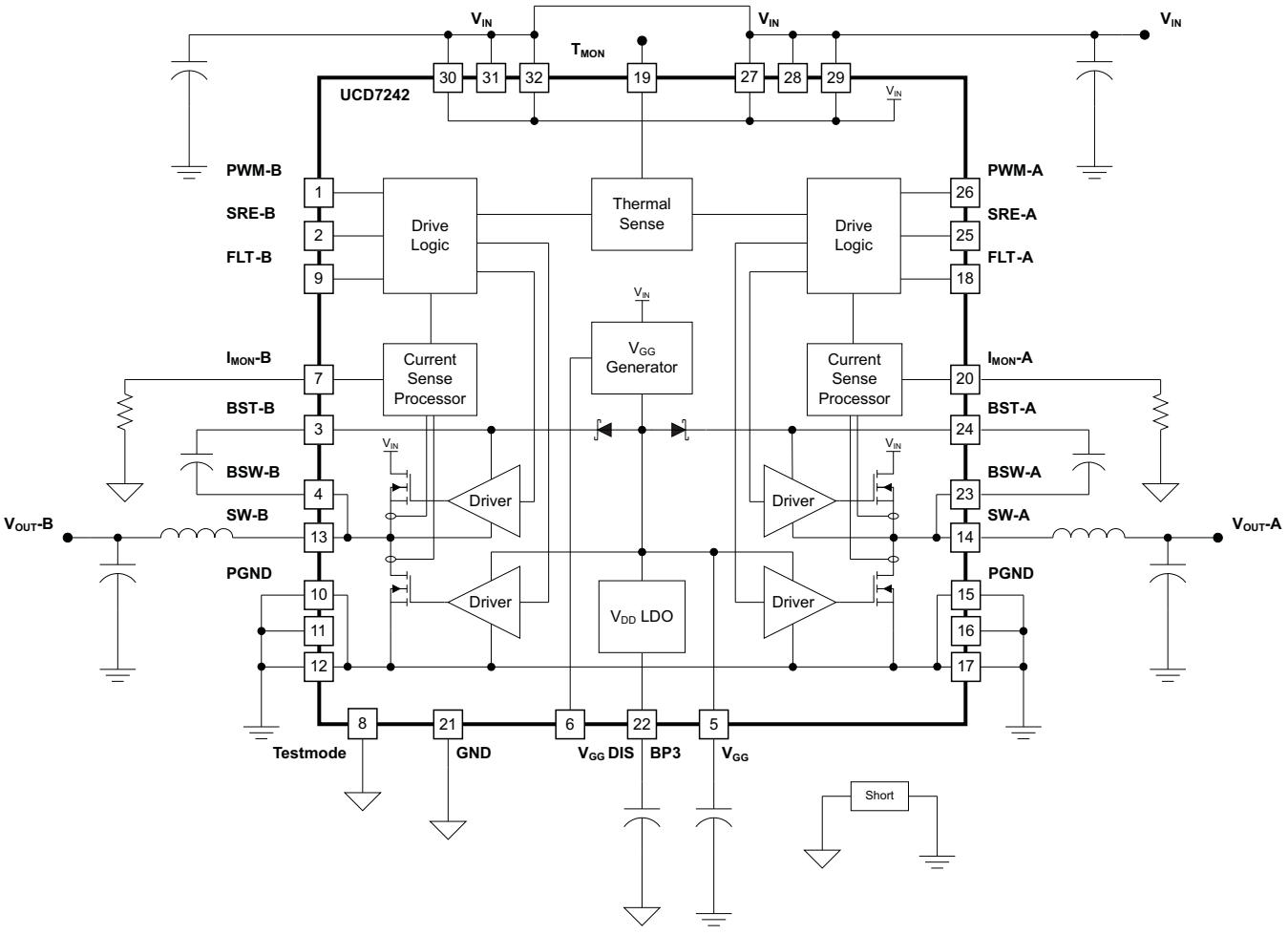


图 **1.** 典型应用电路和方框图

ORDERING INFORMATION

T_J	PIN COUNT	ORDERABLE PART NUMBER	SUPPLY	PACKAGE	TOP SIDE MARKING	VID NUMBER
–55°C to 125°C	32-pin	UCD7242MRSJREP	Reel of 2500	QFN	UCD7242EP	V62/14601-01XE

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			RATING	VALUE
VIN	Supply voltage		–0.3 to 20	V
BST	Boot voltage	DC	–0.3 to SW + 7	V
		AC(2)	34	V
V_{GG}, V_{GG}_DIS	Gate supply voltage		7	V
BP3	Logic supply voltage		4	V
SW, BSW	Switch voltage	DC	–2 to VIN + 1	V
		AC(2)	34	V
TMON, IMON, Testmode	Analog outputs		–0.3 to 3.6	V
PWM-A, PWM-B, SRE-A, SRE-B, FLT-A, FLT-B	Digital I/O's		–0.3 to 5.5	V
T_J	Junction temperature		–55 to 150	°C
T_{stg}	Storage temperature		–55 to 150	°C
ESD rating	HBM: Human Body model		2000	V
	CDM: Charged device model		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult company packaging information for thermal limitations and considerations of packages.
(2) AC levels are limited to within 5 ns.

THERMAL INFORMATION

THERMAL METRIC(1)		UCD7242-EP RSJ 32 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	40.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	17.8	
θ_{JB}	Junction-to-board thermal resistance(4)	12	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.1	
ψ_{JB}	Junction-to-board characterization parameter(6)	11.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.3	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 （文献号：ZHCA543）。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的规定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然对流条件下的结至环境热阻抗。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结至电路板的热阻。
(5) 结至顶部的特征参数，(ψ_{JT})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(6) 结至电路板的特征参数，(ψ_{JB})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到了内容接近的说明。

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Power input voltage (internally generated V_{GG})	4.75	12	18	V
V_{IN}	Power input voltage (externally generated V_{GG})	2.2	12	18	V
V_{GG}	Externally supplied gate drive voltage	4.75	6.2		V
T_J	Operating junction temperature range	–55		125	°C
f_s	Switching frequency	300	750	2000	kHz

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V; 1µF from BP3 to GND, 0.22µF from BST to BSW, 4.7µF from V_{GG} to PGND, $T_A = T_J$ = –55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY SECTION						
	Supply current	Outputs not switching, V_{IN} = 2.2 V, PWM(INH) = LOW, SRE(INL) = HIGH, V_{GG}_DIS = HIGH, V_{GG} = 5V		6		mA
		Outputs not switching, V_{IN} = 18 V, PWM(INH) = LOW, SRE(INL) = HIGH, V_{GG}_DIS = LOW		6		mA
GATE DRIVE UNDER VOLTAGE LOCKOUT						
V_{GG}	UVLO ON	BP3 Rising		4.0		V
	UVLO OFF	BP3 Falling		3.8		V
	UVLO hysteresis			200		mV
V_{GG} SUPPLY GENERATOR						
V_{GG}		V_{IN} = 7 to 18 V	5.2	6.25	6.8	V
	V_{GG} drop out	V_{IN} = 4.75 to 7 V, I_{VGG} < 50 mA			850	mV
BP3 SUPPLY VOLTAGE						
	BP3	I_{DD} = 0 to 10 mA	3.14	3.3	3.45	V
INPUT SIGNAL (PWM, SRE)						
V_{IH}	Positive-going input threshold voltage			2.1	2.3	V
V_{IL}	Negative-going input threshold voltage		1	1.2		V
	3-state Condition		1.4		1.9	V
t_{HLD_R}	3-state hold-off time	V_{PWM} = 1.65 V		275		ns
I_{PWM}	Input current	V_{PWM} = 5.0 V		133		µA
		V_{PWM} = 3.3 V		66		
		V_{PWM} = 0 V		–66		
I_{SRE}	Input current	V_{SRE} = 5.0 V		1		µA
		V_{SRE} = 3.3 V		1		
		V_{SRE} = 0 V		1		
V_{GG} DISABLE (V_{GG}_DIS)						
	Input resistance to AGND	V_{GG}_DIS	45	100	150	kΩ
	Threshold		1.35		1.6	V
	Hysteresis			550		mV
FAULT FLAG (FLT)						
	FLT Output High Level	I_{OH} = 2 mA	2.7			V
	FLT Output Low Level	I_{OL} = –2 mA			0.6	V

ELECTRICAL CHARACTERISTICS (continued)

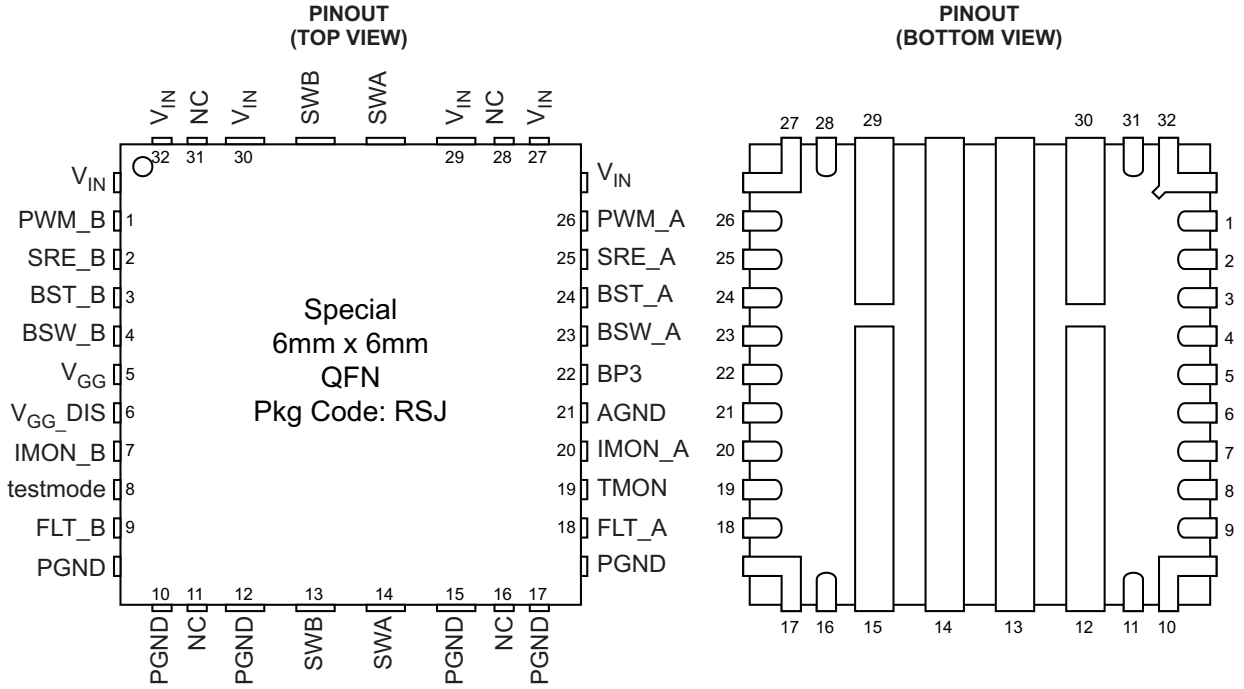
V_{IN} = 12V; 1µF from BP3 to GND, 0.22µF from BST to BSW, 4.7µF from V_{GG} to PGND, $T_A = T_J$ = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
CURRENT LIMIT					
Over current threshold		12	15	18.5	A
T_{fault_HS} delay until HS FET off(1)				80	ns
T_{fault_FF} delay until FLT asserted(1)				100	ns
Propagation delay from PWM to reset FLT(1)	1st falling edge of PWM without a fault event			100	ns
High side blanking time(1)	Over currents during this period will not be detected			60	ns
CURRENT SENSE AMPLIFIER					
Gain	I_{MON}/ I_{OUT}, (see **Figure 14**)	17	20	26	µA/A
Bandwidth(1)		5			kHz
THERMAL SENSE					
Thermal shutdown(1)			170		°C
Thermal shutdown hysteresis(1)			20		°C
Temperature Sense T(1)	Gain, T_J = –20°C to 125°C		10		mV/°C
Temperature Sense T Offset(1)	T_J = 0°C, –100 µA ≤ I_{TMON} ≤ 100 µA		470		mV
POWER MOSFETS					
Propagation delay from PWM to switch node going high			32		ns
High side MOSFET $R_{DS(ON)}$			15.5		mΩ
Low side MOSFET $R_{DS(ON)}$			6.5		mΩ
High side MOSFET turn on – Dead Time(1)			5	10	ns
Low side MOSFET turn on – Dead Time(1)			6	11	ns

(1) As designed and characterized. Not 100% tested in production. These specifications apply for –40°C ≤ T_J ≤ 125°C.

DEVICE INFORMATION

PINOUT



PIN FUNCTIONS

UCD7242 –BUCK POWER STAGE			
QFN	**PIN NAME**	**I/O**	**FUNCTION**
1	PWM-B	I	High impedance digital input capable of accepting 3.3V or 5 V logic level signals up to 2 MHz. A Schmitt trigger input comparator desensitizes this pin from external noise. This pin controls the state of the high side MOSFET and the low side MOSFET when SRE-B is high.

	PWM = high	PWM = low	PWM = 1.65 V
SRE = high	HS = on, LS = off	HS = off, LS = on	HS = off, LS = off
SRE = low	HS = on, LS = off	HS = off, LS = off	HS = off, LS = off

2	SRE-B	I	Synchronous Rectifier Enable input for the B-channel. High impedance digital input capable of accepting 3.3V or 5V logic level signals used to control the synchronous rectifier switch. An appropriate anti-cross-conduction delay is used during synchronous mode.
3	BST_B	I	Connection for the B-channel charge pump capacitor that provides a floating supply for the high side driver. Connect a 0.22µF ceramic capacitor from this pin to BSW-B (pin 4).
4	BSW-B	I	Connection for B-channel charge pump capacitor. Internally connected to SW-B.
5	V_{GG}	I/O	Gate drive voltage for the power MOSFETs. For $V_{IN} \geq 4.75V$, the internal V_{GG} generator can be used. For $V_{IN} < 4.75$ V, this pin should be driven from an external bias supply. When externally driven, V_{GG}_DIS must be tied to V_{GG}. In all cases, bypass this pin with a 4.7µF (min), 10V (min) ceramic capacitor to PGND.
6	V_{GG}_DIS	I	When tied to V_{GG}, disables the on-chip V_{GG} generator to allow gate drive voltage to be supplied from an external source. This is required when V_{IN} is < 4.75V. To use the internal V_{GG} generator, tie to GND.
7	IMON-B	O	MOSFET current sense monitor output. Provides a current source output that is proportional to the current flowing in the power MOSFETs. The gain on this pin is equal to 20µA/A. The I_{MON} pin should be connected to a resistor to GND to produce a voltage proportional to the power-stage load current.
8	testmode	I	Test mode only. Tie to GND.

PIN FUNCTIONS (continued)

UCD7242 –BUCK POWER STAGE			
QFN	**PIN NAME**	**I/O**	**FUNCTION**
9	FLT-B	O	Fault flag for the B-channel. This signal is a 3.3V digital output which is latched high when the current in the B-channel high-side FET exceeds the current limit trip point. When tripped, high-side FET drive pulses are truncated to limit output current. FLT is cleared after one complete switching cycle without a fault. Additionally, if the die temperature exceeds 170°C, the temperature sensor will initiate a thermal shutdown that halts output switching and sets the FLT flag. Normal operation resumes when the die temperature falls below the thermal hysteresis band.
10, 12, 15, 17	PGND	–	Shared power ground return for the buck power stage
11, 16	NC	–	No internal connection. It is recommended that these pins be tied to PGND.
13	SW-B	–	Switching node of the B-channel buck power stage and square wave input to the buck inductor. Electrically this is the connection of the high side MOSFET source to the low side MOSFET drain.
14	SW-A	–	Switching node of the A-channel buck power stage and square wave input to the buck inductor. Electrically this is the connection of the high side MOSFET source to the low side MOSFET drain.
18	FLT-A	O	Fault flag for the A-channel. This signal is a 3.3V digital output which is latched high when the current in the A-channel high-side FET exceeds the current limit trip point. When tripped, high-side FET drive pulses are truncated to limit output current. FLT is cleared after one complete switching cycle without a fault. Additionally, if the die temperature exceeds 170°C, the temperature sensor initiates a thermal shutdown that halts output switching and sets the FLT flag. Normal operation resumes when the die temperature falls below the thermal hysteresis band.
19	TMON	O	Temperature sense pin. The voltage on this pin is proportional to the die temperature. The gain is 10mV/°C. At T_J = 0°C, the output voltage has an offset of 0.47V. When the die temperature reaches the thermal shutdown threshold, this pin is pulled to BP3 and the power FETs are switched off. When the die temperature falls below the thermal hysteresis band, the FLT flag clears and normal operation resumes.
20	IMON -A	O	MOSFET current sense monitor output. Provides a current source output that is proportional to the current flowing in the power MOSFETs. The gain on this pin is equal to 20µA/A. The IMON pin should be connected to a resistor to GND to produce a voltage proportional to the power-stage load current.
21	GND	–	Analog ground return.
22	BP3	O	Output of internal 3.3V LDO regulator for powering internal logic circuits. Bypass this pin with 1µF (min) to GND. This LDO is supplied by the V_{GG} pin.
23	BSW-A	–	Connection for A-channel charge pump capacitor. Internally connected to SW-A.
24	BST-A	–	Connection for the A-channel charge pump capacitor that provides a floating supply for the high side driver. Connect a 0.22µF ceramic cap from this pin to BSW-A (pin 23).
25	SRE-A	I	Synchronous Rectifier Enable input for the A-channel. High impedance digital input capable of accepting 3.3V or 5V logic level signals used to control the synchronous rectifier switch. An appropriate anti-cross-conduction delay is used during synchronous mode.
26	PWM -A	I	High impedance digital input capable of accepting 3.3V or 5 V logic level signals up to 2 MHz. A Schmitt trigger input comparator desensitizes this pin from external noise. This pin controls the state of the high side MOSFET and the low side MOSFET when SRE-A is high.
27, 29, 30, 32	VIN	–	Input Voltage to the buck power stage and driver circuit
28, 31	NC	–	No internal connection. It is recommended that these pins be tied to VIN.

	PWM = high	PWM = low	PWM = 1.65 V
SRE = high	HS = on, LS = off	HS = off, LS = on	HS = off, LS = off
SRE = low	HS = on, LS = off	HS = off, LS = off	HS = off, LS = off

TYPICAL CHARACTERISTICS

Inductor used in the following plots is a 0.47μH BI Technologies inductor (HM72A). All data taken at room ambient.

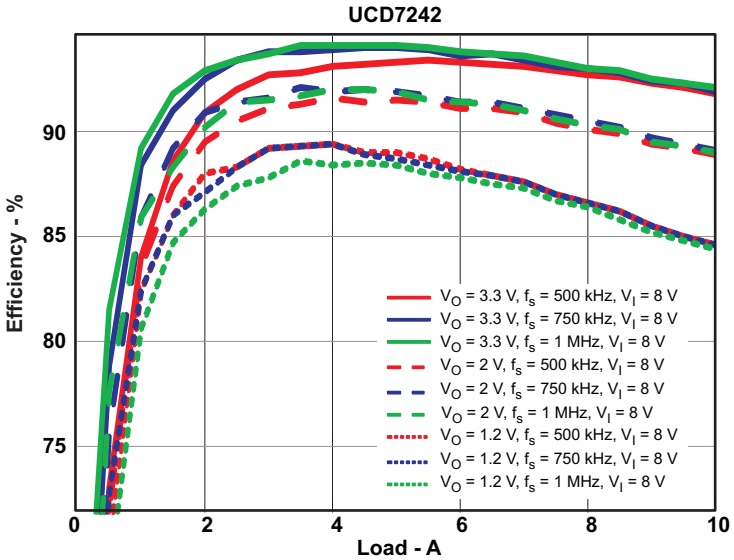


Figure 2.

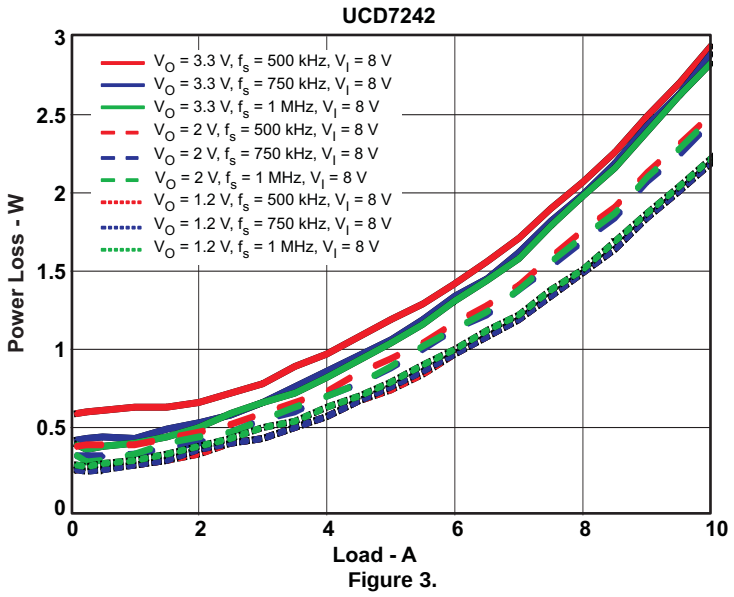


Figure 3.

TYPICAL CHARACTERISTICS (continued)

Inductor used in the following plots is a 0.47µH BI Technologies inductor (HM72A). All data taken at room ambient.

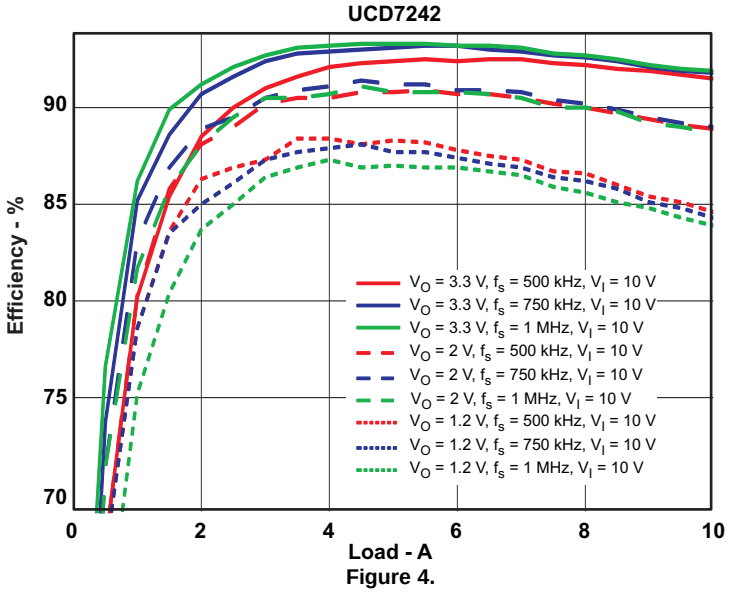


Figure 4.

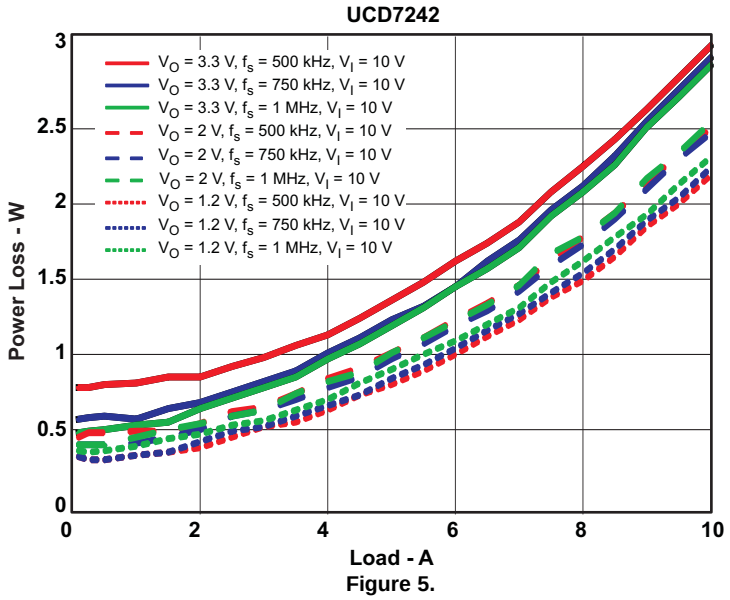


Figure 5.

TYPICAL CHARACTERISTICS (continued)

Inductor used in the following plots is a 0.47µH BI Technologies inductor (HM72A). All data taken at room ambient.

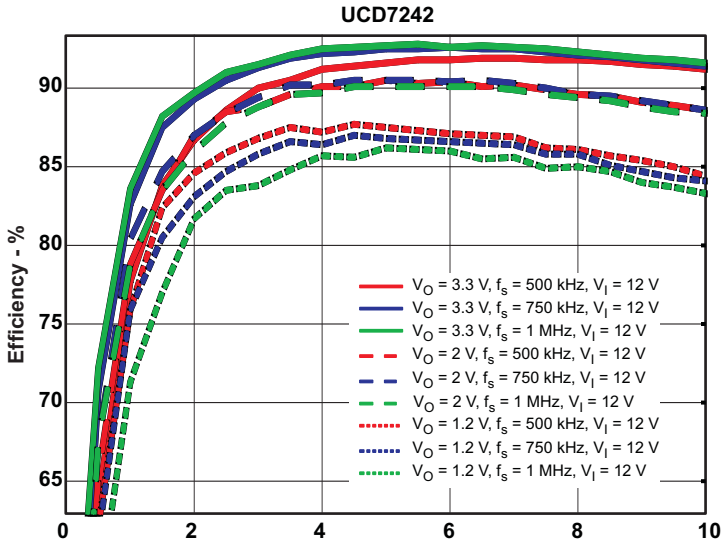


Figure 6.

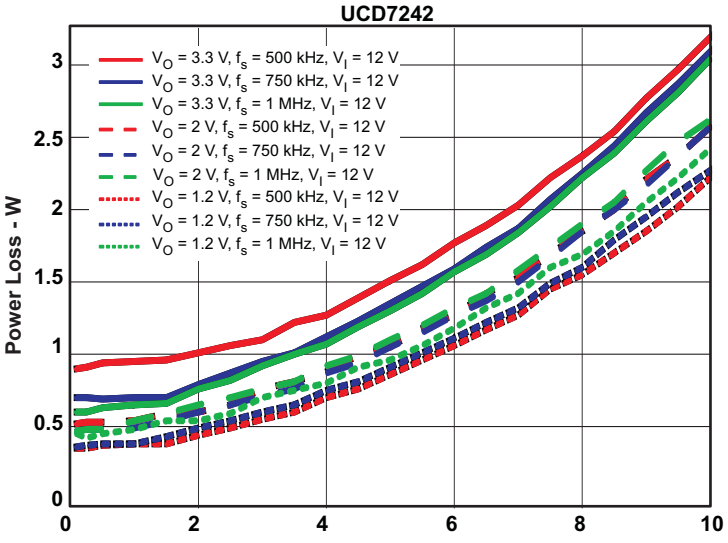


Figure 7.

TYPICAL CHARACTERISTICS (continued)

Inductor used in the following plots is a 0.47µH BI Technologies inductor (HM72A). All data taken at room ambient.

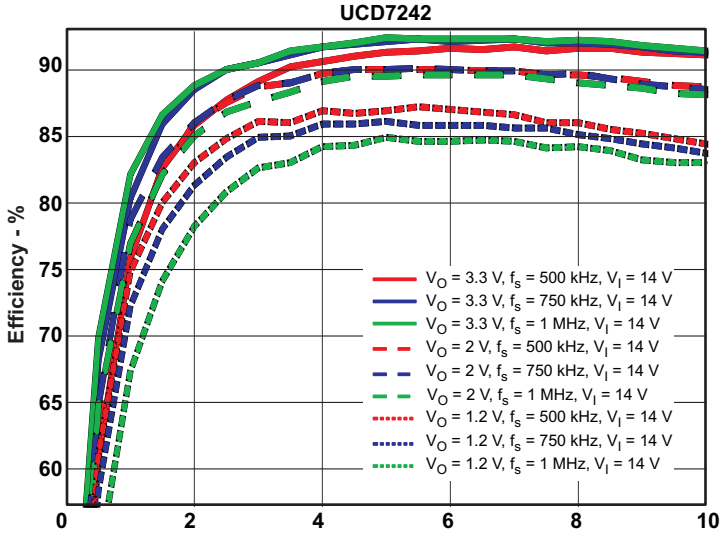


Figure 8.

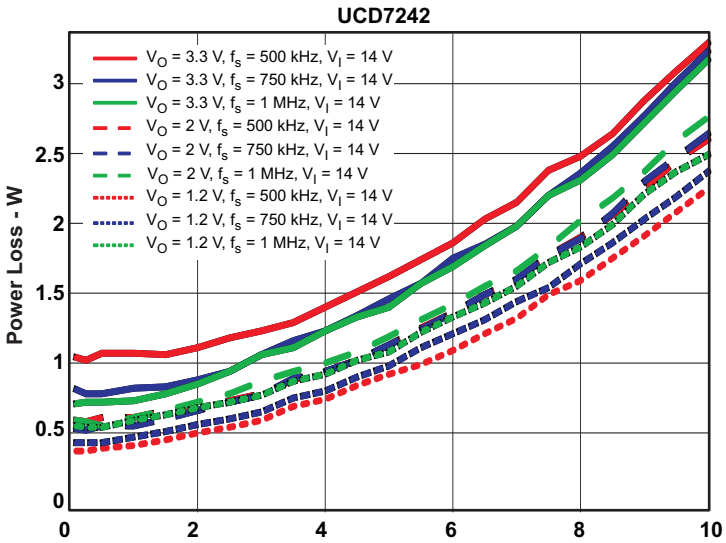


Figure 9.

TYPICAL CHARACTERISTICS (continued)

Inductor used in the following plots is a 0.47µH BI Technologies inductor (HM72A). All data taken at room ambient.

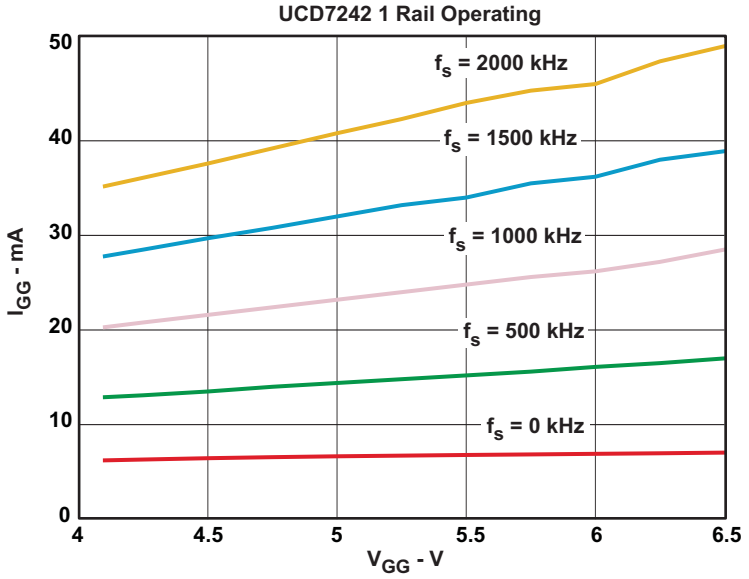


Figure 10. V_{GG} Supply Current with 1 Rail Operating and 1 Rail Off

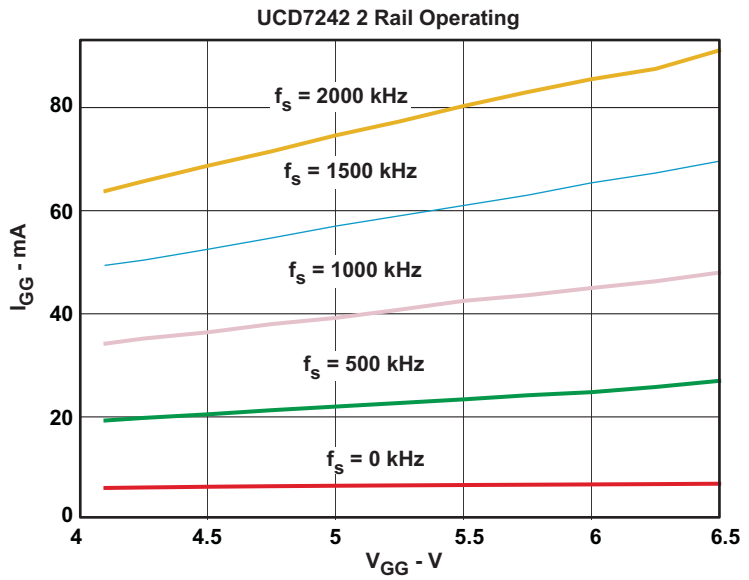


Figure 11. V_{GG} Supply Current with 2 Rails Operating

TYPICAL CHARACTERISTICS (continued)

Inductor used in the following plots is a 0.47µH BI Technologies inductor (HM72A). All data taken at room ambient.

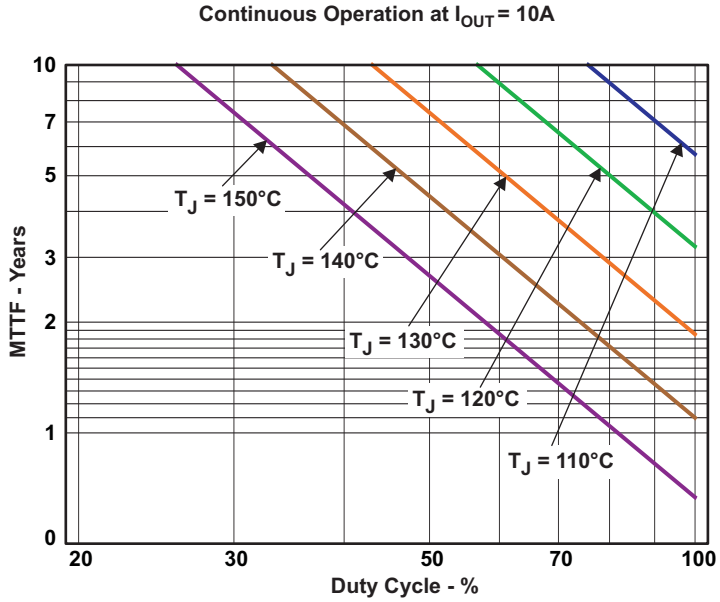


Figure 12.

Figure 12 shows the mean time to failure (MTTF) for an output load current of 10A on a single output, or an output load current of 10A on both outputs.

DETAILED DESCRIPTION

PWM INPUT

The PWM input pin accepts the digital signal from the controller that represents the desired high-side FET on time. This input is designed to accept 3.3V logic levels, but is also tolerant of 5V input levels. The SRE pin sets the behavior of the PWM pin. When the SRE pin is asserted high, the device is placed in synchronous mode. In this mode, the timing duration of the high-side gate drive and the low-side gate drive are both controlled by the PWM input signal. When PWM is high, the high-side MOSFET is on and the low-side MOSFET is off. When PWM is low, the high-side MOSFET is off and the low-side MOSFET is on. An optimized anti-cross-conduction delay is introduced to ensure the proper FET is turned off before the other FET is turned on. When the SRE pin is asserted low, the device is placed in non-synchronous mode. In this mode the PWM input only controls the high-side MOSFET. When PMW is high, the high-side MOSFET is on. The low side FET is always held off.

The PWM input supports a 3-state detection feature. It can detect if the PWM input signal has entered a 3-state mode. When 3-state mode is detected, both the high-side and low-side MOSFETs are held off. To support this mode, the PWM input pin has an internal pull-up resistor of approximately 50kΩ to 3.3V and a 50kΩ pull-down resistor to ground. During normal operation, the PWM input signal swings below 0.8V and above 2.5V. If the source driving the PWM pin enters a 3-state or high impedance state, the internal pull-up/pull down resistors will tend to pull the voltage on the PWM pin to 1.65V. If the voltage on the PWM pin remains within the 0.8V to 2.5V 3-state detection band for longer than t_{HLD_R}, 3-state detection hold-off time, then the device enters 3-state mode and turns both MOSFETs off. This behavior occurs regardless of the state of the SRE pin. When exiting 3-state mode, PWM should first be asserted low and SRE High. This ensures that the bootstrap capacitor is recharged before attempting to turn on the high-side FET. The logic threshold of this pin typically exhibits 900mV of hysteresis to provide noise immunity and ensure glitch-free operation.

SRE INPUT

The SRE (Synchronous Rectifier Enable) pin is a high impedance digital input. It is designed to accept 3.3V logic levels, but is also tolerant of 5V levels. When asserted high, the operation of the low-side synchronous rectifier FET is enabled. The state of the low-side MOSFET is governed by the PWM input. When SRE is asserted low, the low-side FET is continuously held low, keeping the FET off. While held off, current flow in the low-side FET is restricted to its intrinsic body diode. The logic threshold of this pin typically exhibits 900mV of hysteresis to provide noise immunity and ensure glitch-free operation.

V_{IN}

V_{IN} supplies power to the internal circuits of the device. The input power is conditioned by an internal linear regulator that provides the V_{GG} gate drive voltage. A second regulator that operates off of the V_{GG} rail produces an internal 3.3V supply that powers the internal analog and digital functional blocks. The V_{GG} regulator produces a nominal 6.2V. The output of the V_{GG} regulator is monitored by the Under-Voltage Lock Out (UVLO) circuitry. The device will not attempt to produce gate drive pulses until the V_{GG} voltage is above the UVLO threshold. This ensures that there is sufficient voltage available to drive the power FETs into saturation when switching activity begins. To use the internal V_{GG} regulator, V_{IN} should be at least 4.7V. When performing power conversion with V_{IN} values less than 4.7V, the gate drive voltage must be supplied externally. (See V_{GG} and VGG DIS sections for details.)

V_{GG}

The V_{GG} pin is the gate drive voltage for the high current gate driver stages. For $V_{IN} \geq 4.75V$, the internal V_{GG} generator can be used. For $V_{IN} < 4.75$ V, this pin should be driven from an external bias supply. When using the internal regulator, the VGG_DIS pin should be tied low. When using an external V_{GG}, VGG_DIS must be tied to V_{GG}. Current is drawn from the V_{GG} supply in fast, high-current pulses. A 4.7μF ceramic capacitor (10V minimum) should be connected from the V_{GG} pin to the PGND pin as close as possible to the package. Whether internally or externally supplied, the voltage on the V_{GG} pin is monitored by the ULVO circuitry. The voltage must be higher than the UVLO threshold before power conversion can occur. The average current drawn from the V_{GG} supply is dependant on the switching frequency, the absolute value of V_{GG} and the total gate charge of the power FETs inside the device.

V_{GG}_DIS

This pin, when asserted high, disables the on-chip V_{GG} linear regulator. When tied low, the VGG linear regulator is used to derive V_{GG} from V_{IN}. This pin is designed to be permanently tied high or low depending on the power architecture being implemented. It is not intended to be switched dynamically while the device is in operation.

SW

The SW pin is the switching node of the power conversion stage. When configured as a synchronous buck, the voltage swing on SW normally traverses from slightly below ground to above V_{IN}. Parasitic inductance in the high-side FET conduction path and the output capacitance (Coss) of the low side FET form a resonant circuit than can produce high frequency (> 100MHz) ringing on this node. The voltage peak of this ringing will exceed V_{IN}. Care must be taken not to exceed the maximum voltage rating of this pin. The main areas available to impact this amplitude are: the driver voltage magnitude (V_{GG}) and the parasitic source and return paths for the MOSFET (V_{IN}, PGND). In some cases, a series resistor and capacitor snubber network connected from this pin to PGND can be helpful in damping the ringing and decreasing the peak amplitude. In general this should not be necessary due to the integrated nature of this part.

BST

The BST pin provides the drive voltage for the high-side FET. A bootstrap capacitor is connected from this pin to the BST-SW node. Internally, a diode connects the BST pin to the V_{GG} supply. In normal operation, when the high side FET is off and the low-side FET is on, the SW node is pulled to ground and, thus, holds one side of the bootstrap capacitor at ground potential. The other side of the bootstrap capacitor is clamped by the internal diode to V_{GG}. The voltage across the bootstrap capacitor at this point is the magnitude of the gate drive voltage available to switch-on the high-side FET. The bootstrap capacitor should be a low ESR ceramic type, a minimum value of 0.22µF is recommended.

In order to ensure that the bootstrap capacitor has sufficient time to recharge, the steady-state duty cycle must not exceed what is shown in Figure 13. The curve in Figure 13 is for C_{BST}= 0.22µF. Different values of C_{BST} will have different DMAX limitations.

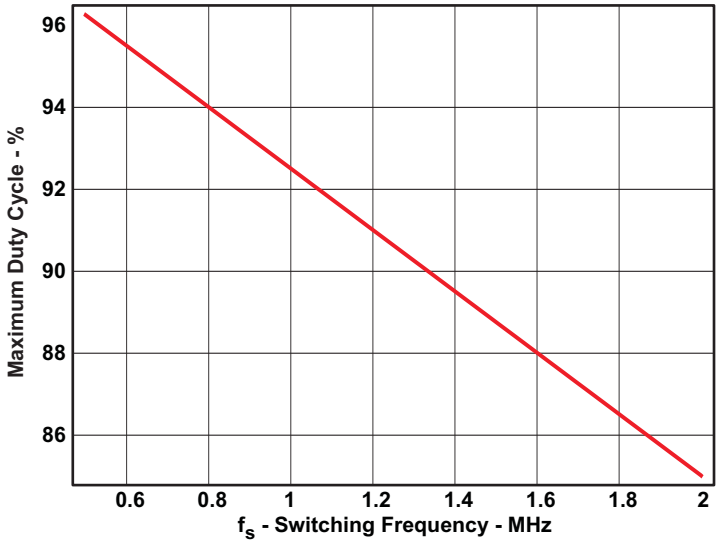


Figure 13.

BST-SW

Electrically this node is the same as the SW pin. However, it is physically closer to the BST pin so as to minimize parasitic inductance effects of trace routing to the BST capacitor. Keeping the external traces short should minimize turn on and off times.

This pin is not sized for conducting inductor current and should not be tied to the SW pin. It is only for the BST pin capacitor connection.

IMON

MOSFET current sense monitor output. This pin provides a current source output that is proportional to the current flowing in the power MOSFETs. The gain on this pin is equal to 20µA/A. The I_{MON} pin should be connected to a resistor to GND to produce a voltage proportional to the power-stage load current. For example, a value of 10kΩ to ground produces a voltage of 2.0V when the power stage current is 10A.The accuracy of the reported current is a function of the peak to peak ripple current in the inductor (ΔI). The nominal behavior is described by Equation 1. The plot illustrates the possible variability in the sensed current as a function of load for a ΔI=4A. If no PWM is detected for 8µs IMON will report 0V.

$$I_{MON}(I_{OUT},\Delta I) = \begin{cases} 20\frac{\mu A}{A} I_{OUT} & \text{If } I_{OUT} \geq \frac{\Delta I}{2} \\ 10\frac{\mu A}{A} I_{OUT} + 5\frac{\mu A}{A}\Delta I & \text{If } I_{OUT} < \frac{\Delta I}{2} \end{cases} \quad (1)$$

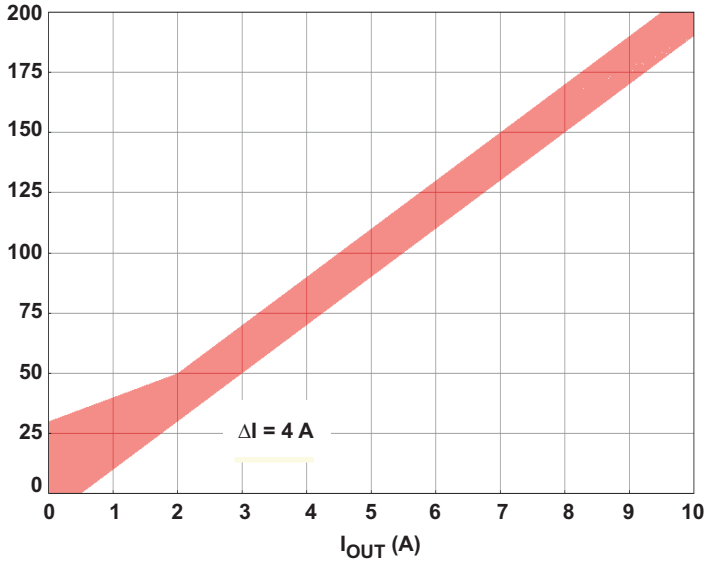


Figure 14. Sensed Current Variability

TMON

The voltage on this pin is proportional to the die temperature with a gain of 10 mV/°C and an offset voltage of 0.47 V at T_J = 0°C (Equation 2):

$$T_{MON}(T_J) = 0.47\ V + \frac{10mV}{°C}(T_J) \quad (2)$$

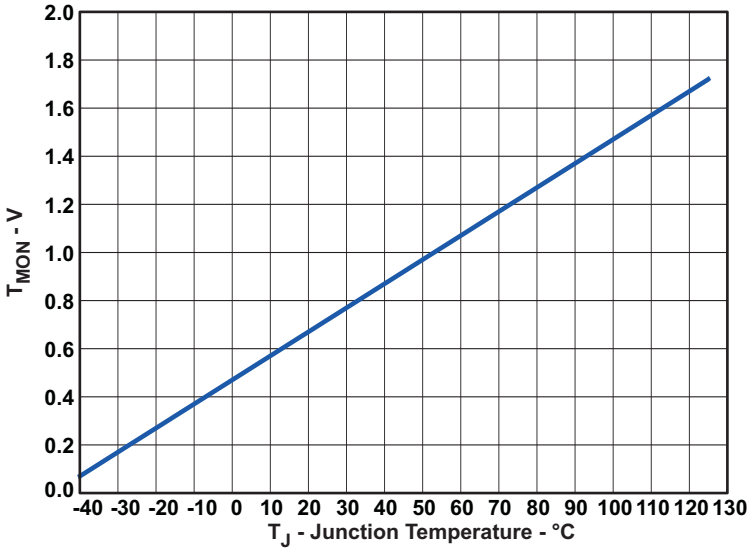


Figure 15. Typical Characteristics

If the junction temperature exceeds approximately 170°C, the device will enter thermal shutdown. This will assert the FLT pin, both MOSFETs will be turned off and the switch node will go high impedance. When the junction temperature cools by approximately 20°C, the device will exit thermal shutdown and resume switching as directed by the PWM and SRE pins. During a thermal shutdown event, the voltage on the Temp pin is driven to 3.3V.

FLT

This signal is a 3.3V digital output which is latched high when the current in the high-side FET exceeds the current limit trip point. When tripped, high-side FET drive pulses are truncated to limit output current. FLT is cleared on the falling edge of the first PWM pulse without a fault. Additionally, if the die temperature exceeds 170°C, the temperature sensor will initiate a thermal shutdown that halts output switching and sets the FLT flag. Normal operation resumes when the die temperature falls below the thermal hysteresis band. The FLT flag will clear after a PWM pulse occurs without a fault. Current limit is ignored during the high side blanking time. If an over current event occurs during the blanking time the part will not initiate current limit for ~50ns.

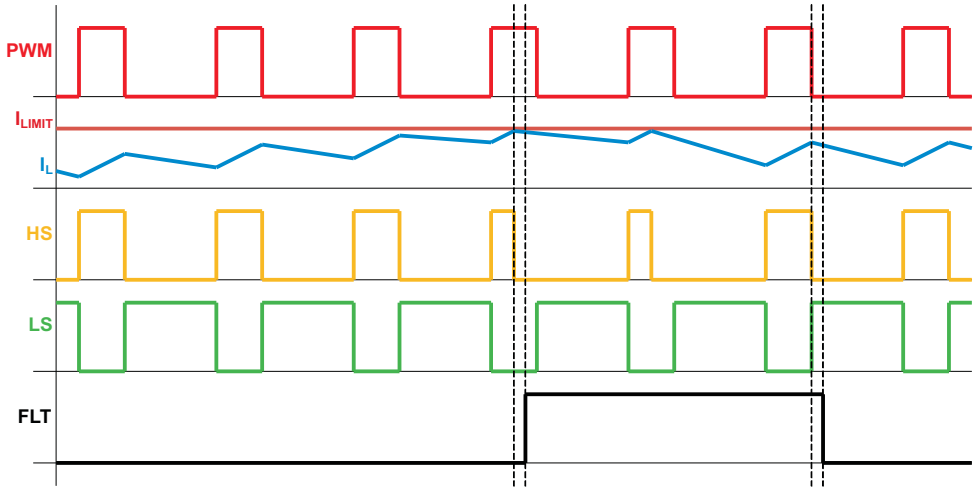
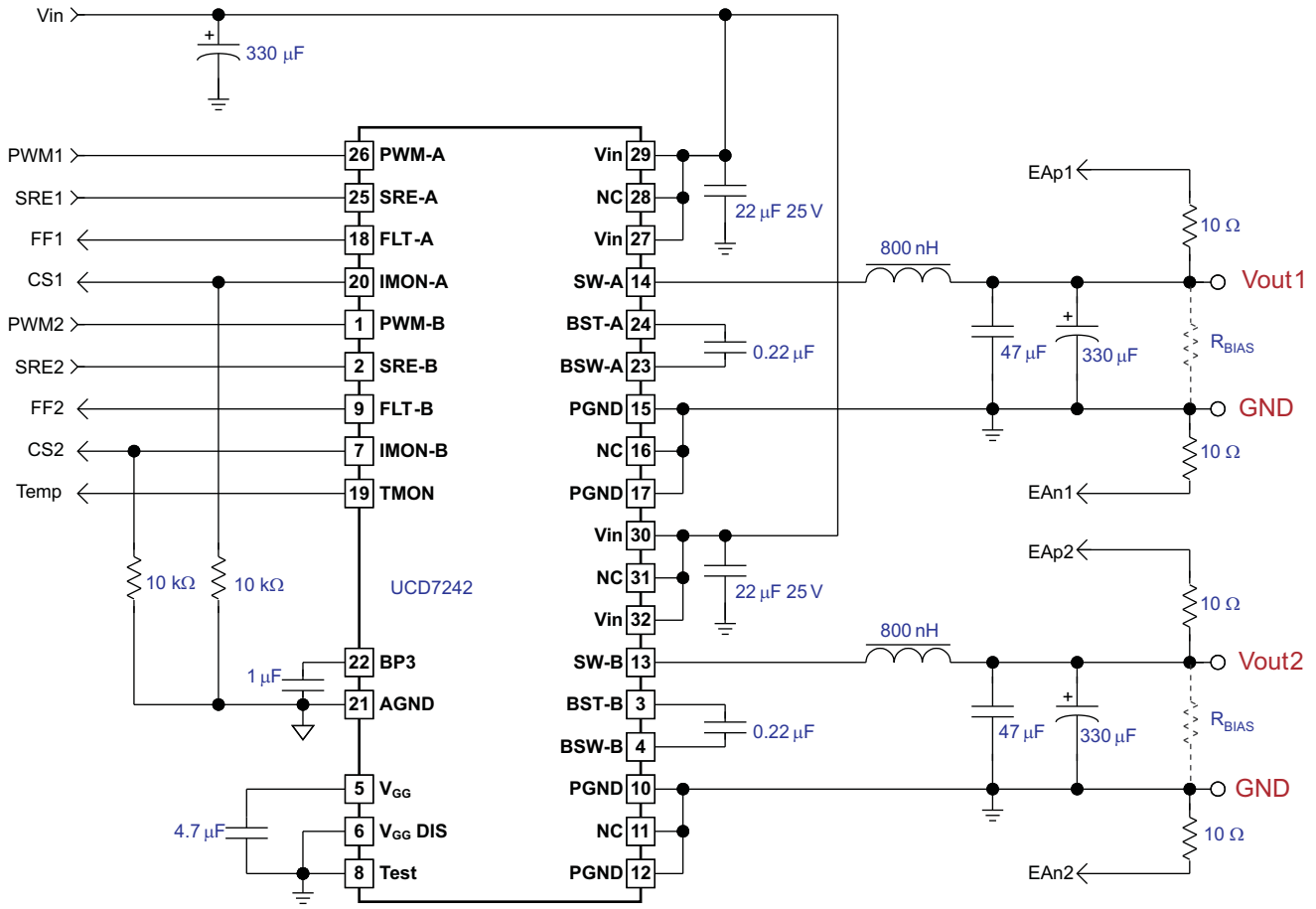


Figure 16. FLT Signal

APPLICATION INFORMATION

A partial schematic of a power supply application using the UCD7242 power stage is provided below. Although not shown the IC controlling the output is from the UCD92XX family of digital controllers.



PRE-BIAS OPERATION

The UCD7242 has no problem starting up into pre-biased output voltages. However, when one channel is held in tri-state and the second channel is actively switching, the tri-stated channel may generate a DC voltage through weak capacitive coupling between SW-A and SW-B. This coupling comes principally from the close proximity of the switch nodes on the silicon and the PWB layout.

There are several options to address this concern.

1. The device(s) that the UCD7242 is powering on a 3-stated channel has a known current draw at sub-regulation voltage levels. This current draw may be sufficient to hold the voltage down.
2. Instead of holding the off channel in a 3-state condition, drive PWM actively low. This forces the synchronous rectifier to turn on and prevent the pre-bias voltage from rising. If this option is elected, it is important to verify that there are no other sources of leakage in the system.
3. Add a small load resistor, R_{BIAS}. In most cases a value of 1kΩ should keep the output voltage below 200mV. Some experimentation may be needed to determine the appropriate value. In many cases, the feedback divider may provide a sufficient load.

It is important that V_{BIAS} be less than or equal to the steady state output voltage during regulation. If this condition is not enforced the controller in charge of regulating this rail will be unable to start up. If start up is forced, damage may result.

OPERATING FREQUENCY

Switching frequency is a key place to start the design of any DC/DC converter. This will set performance limits on things such as: maximum efficiency, minimum size, and achievable closed loop bandwidth. A higher switching frequency is, generally, going to yield a smaller design at the expense of a lower efficiency. The size benefit is principally a result of the smaller inductor and capacitor energy storage elements needed to maintain ripple and transient response requirements. The additional losses result from a variety of factors, however, one of the largest contributors is the loss incurred by switching the MOSFETs on and off. The integrated nature of the UCD7242 makes these losses drastically smaller and subsequently enables excellent efficiency from a few hundred kHz up to the low MHz. For a reasonable trade off of size versus efficiency, 750kHz is a good place to start.

V_{GG}

If 4.75V < V_{IN} ≤ 6V a simple efficiency enhancement can be achieved by connecting V_{GG}_DIS and V_{GG} directly to V_{IN}. This allows the solution to bypass the drop out voltage of the internal V_{GG} linear regulator, subsequently improving the enhancement of the MOSFETs. When doing this it is critical to make sure that V_{GG} never exceeds the absolute maximum rating of 7V.

INDUCTOR SELECTION

There are three main considerations in the selection of an inductor once the switching frequency has been determined. Any real world design is an iterative trade off of each of these factors.

1. The electrical value which in turn is driven by:
   (a) RMS current
   (b) The maximum desired output ripple voltage
   (c) The desired transient response of the converter
2. Losses
   (a) Copper (P_{Cu})
   (b) Core (P_{fe})
3. Saturation characteristics of the core

INDUCTANCE VALUE

The principle equation used to determine the inductance is:

$$v_L(t) = L \frac{di_L(t)}{dt} \tag{3}$$

During the on time of the converter the inductance can be solved to be:

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \frac{D}{f_s} \tag{4}$$

Where:

V_{IN}	Input Voltage
V_{OUT}	Output voltage
f_s	Switching frequency
D	Duty cycle (V_{OUT}/V_{IN} for a buck converter)
ΔI	The target peak to peak inductor current.

In general, it is desirable to make ΔI large to improve transient response and small to reduce output ripple voltage and RMS current. A number of considerations go into this however, ΔI = 0.4 I_{OUT} results in a small I_{LRMS} without an unnecessary penalty on transient response. It also creates a reasonable ripple current that most practical capacitor banks can handle. Here I_{OUT} is defined as the maximum expected steady state current.

Plugging these assumptions into the above inductance equation results in:

$$L = 5 \frac{V_{IN} - V_{OUT}}{2 \times I_{OUT}} \frac{D}{fs} \quad (5)$$

For example, plotting this result as a function of V_{IN} and V_{OUT} results in:

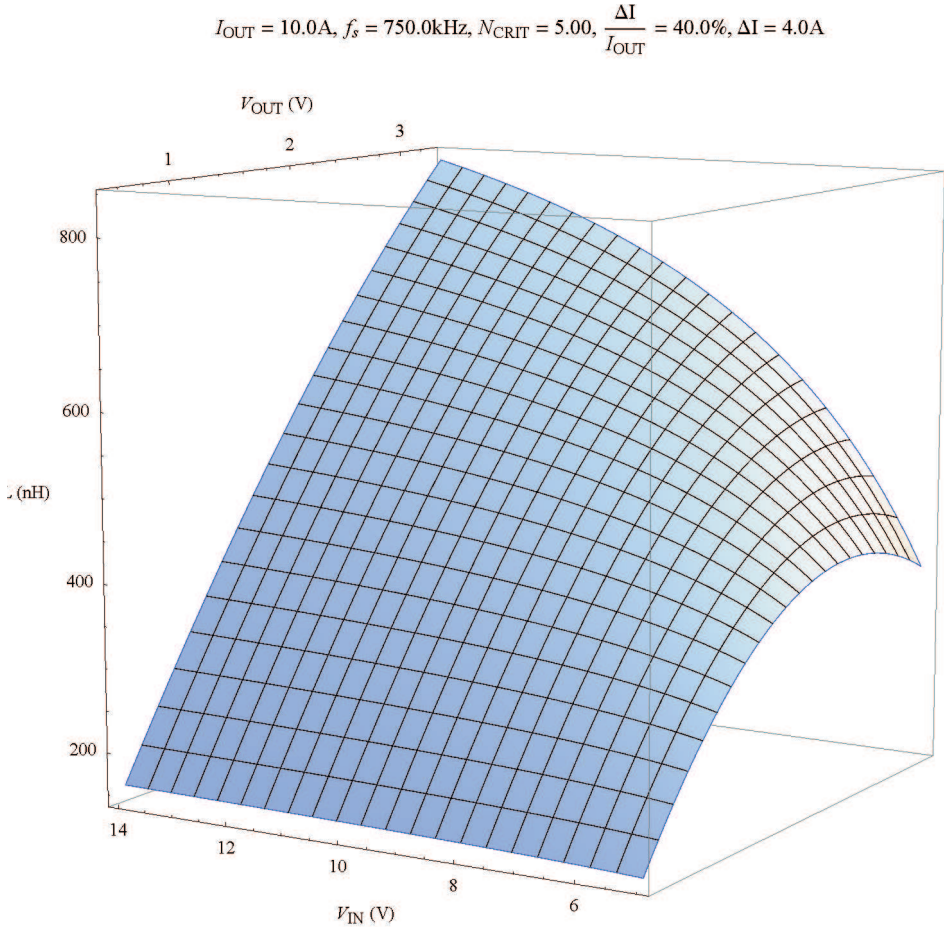


Figure 17. Inductance vs. V_{IN} and V_{OUT}

In this graph I_{OUT} is 10A, the switching frequency is 750kHz and the inductor ΔI is 4A. If the switching frequency is cut in half then the resulting inductance would be twice the value shown. Notice that the maximum inductance occurs at the maximum V_{IN} and V_{OUT} shown on the plot. In general, this inductance value should be used in order to keep the inductor ripple current from becoming too large over the range of supported V_{IN} and V_{OUT}.

INDUCTOR LOSSES AND SATURATION

The current rating of an inductor is based on two things: the current necessary to raise the component temperature by 40°C and the current level necessary to reduce the inductance to 80% of its initial value (saturation current (1)). The current rating is the lower of these two numbers. Both of these factors are influenced by the choice of core material. Popular materials currently in use are: ferrite, powdered alloy and powdered iron.

Ferrite is regarded as the highest performance material and as such is the lowest loss and the highest cost. Solid ferrite all by itself will saturate with a relatively small amount of current. This can be addressed by inserting a gap into the core. This, in effect, makes the inductor behave in a linear manner over a wide DC current range. However, once the inductance begins to roll off, these gapped materials exhibit a “sharp” saturation characteristic. In other words, the inductance value reduces rapidly with increases in current above the saturation level. This small inductance that results, can produce dangerously high current levels.

(1) Although “saturation current” is standard terminology among many inductor vendors, technically saturation does not occur until the relative permeability of the core is reduced to approximately 1. This is a value much larger than what is typically seen on data sheets.

Powdered iron has the advantage of lower cost and a soft saturation characteristic; however, its losses can be very large as switching frequencies increase. This can make it undesirable for a UCD7242 based application where higher switching frequency may be desired. It's also worth noting that many powdered iron cores exhibit an aging characteristic where the core losses increase over time. This is a wear-out mechanism that needs to be considered when using these materials.

The powdered alloy cores bring the soft saturation characteristics of powdered iron with considerable improvements in loss without the wear-out mechanism observed in powdered iron. These benefits come at a cost premium.

In general the following relative figure of merits can be made:

	Ferrite	Powdered Alloy	Powdered Iron
Cost	High	Medium	Low
Loss	Low	Medium	High
Saturation	Rapid	Soft	Soft

When selecting an inductor with an appropriate core it's important to have in mind the following:

1. I_{LRMS}, maximum RMS current
2. ΔI, maximum peak to peak current
3. I_{MAX}, maximum peak current

The RMS current can be determined by Equation 6:

$$I_{LRMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I^2}{12}} \tag{6}$$

When the 40% ripple constraint is used at maximum load current, this equation simplifies to: $I_{LRMS} \approx I_{OUT}$.

It is widely recognized that the Steinmetz equation (P_{fe}) is a good representation of core losses for sinusoidal stimulation. It is important to recognize that this approximation applies to sinusoidal excitation only. This is a reasonable assumption when working with converters whose duty cycles are near 50%, however, when the duty cycle becomes narrow this estimate may no longer be valid and considerably more loss may result.

$$P_{fe} = k \times f^{\alpha} \times B_{AC}{}^{\beta} \tag{7}$$

The principle drivers in this equation are the material and its respective geometry (k, α, β), the peak AC flux density (B_{AC}) and the excitation frequency (f). The frequency is simply the switching frequency of the converter while the constant k, can be computed based on the effective core volume (V_e) and a specific material constant (k_{fe}).

$$k = k_{fe} \times V_e \tag{8}$$

The AC flux density (B_{AC}) is related to the conventional inductance specifications by the following relationship:

$$B_{AC} = \frac{L}{A_e \times N} \frac{\Delta I}{2} \tag{9}$$

Where L is the inductance, A_e, is the effective cross sectional area that the flux takes through the core and N is the number of turns.

Some inductor manufactures use the inductor ΔI as a figure of merit for this loss, since all of the other terms are a constant for a given component. They may provide a plot of core loss versus ΔI for various frequencies where ΔI can be calculated as:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{L} \frac{D}{f s} \tag{10}$$

I_{MAX} has a direct impact on the saturation level. A good rule of thumb is to add 15% of head room to the maximum steady state peak value to provide some room for transients.

$$I_{MAX} = 1.15 \times \left(I_{OUT} + \frac{\Delta I}{2} \right) \tag{11}$$

For example for a 10A design has the following:

I_{OUT}	10A
I_{LRMS}	10A
ΔI	4A
I_{MAX}	13.8A

Armed with this data one can now approach the inductor data sheet to select a part with a “saturation” limit above 13.8A and current “heating” limit above 10A. Furthermore, total losses can be estimated based on the datasheet DCR value (I_{LRMS} ^{2}DCR) and the core loss curves for a given frequency and ΔI.

INPUT CAPACITANCE

Due to the non-zero impedance of the power planes of the input voltage rail, it is necessary to add some local capacitance near the UCD7242 to ensure that the voltage at this node is quiet and stable. The primary things to consider are:

1. The radiated fields generated by the di/dt and dv/dt from this node
2. RMS currents capability needed in the capacitors
3. The AC voltage present and respective susceptibility of any device connected to this node

$$I_{CINRMS} = \sqrt{I_{OUT}^2 \times D \times (1 - D) + \frac{\Delta I^2}{12} \times D} \tag{12}$$

As a point of reference if ΔI=0.4 I_{OUT} this places the worst case I_{CINRMS} at approximately 5A. This corresponds to a duty cycle of approximately 50%. Other duty cycles can result in a significantly lower RMS current.

A good input capacitor would be a 22µF X5R ceramic capacitor. Equally important as selecting the proper capacitor is placing and routing that capacitor. It is crucial that the decoupling be placed as close as possible to both the power pin (V_{IN}) and ground (PGND). It is important to recognize that each power stage should have its own local decoupling. One 22µF capacitor should be placed across each V_{IN} and PGND pair. The proximity of the capacitance to these pins will reduce the radiated fields mentioned above.

OUTPUT CAPACITANCE

The goal of the output capacitor bank is to keep the output voltage within regulation limits during steady state and transient conditions.

The total AC RMS current flowing through the capacitor bank can be calculated as:

$$I_{COUTRMS} = \frac{\Delta I}{\sqrt{12}} \tag{13}$$

For a single type of output capacitor the output ripple voltage wave form can be approximated by the following equation:

$$V_{OUT}(t) = I_C(t) \times esr + \frac{1}{C}\int_0^t I_C(\tau) \times d\tau \tag{14}$$

Where:

$$I_C(t) = \begin{cases} \dfrac{\Delta I \times f_s}{D} \times t - \dfrac{\Delta I}{2} & t < \dfrac{D}{f_s} \\ \dfrac{\Delta I \times f_s}{1 - D} \times \left(t - \dfrac{D}{f_s}\right) + \dfrac{\Delta I}{2} & \text{otherwise} \end{cases} \tag{15}$$

After substitution and simplification yields

$$V_{OUT}(t) = \begin{cases} esr \times \left(\dfrac{\Delta I \times f_s}{D} \times t - \dfrac{\Delta I}{2}\right) + \dfrac{1}{C} \times \left(\dfrac{t \times \Delta I \times (f_s \times t - D)}{2 \times D} - \dfrac{\Delta I \times (1 - 2 \times D)}{12 \times f_s}\right) & t < \dfrac{D}{f_s} \\ esr \times \left(\dfrac{\Delta I \times f_s}{1 - D} \times \left(t - \dfrac{D}{f_s}\right) + \dfrac{\Delta I}{2}\right) + \dfrac{1}{C} \times \left(\dfrac{\Delta I \times (f_s \times t - 1) \times (D - f_s \times t)}{2 \times (1 - D) \times f_s} - \dfrac{\Delta I \times (1 - 2 \times D)}{12 \times f_s}\right) & \text{otherwise} \end{cases} \tag{16}$$

The term in this equation multiplied by the esr gives the ripple voltage component due to esr and the term multiplied by 1/C gives the ripple voltage component due to the change in charge on the capacitor plates. In the case were the esr component dominates the peak to peak output voltage can be approximated as:

$$V_{PPesr} \neq \Delta I \times esr \quad (17)$$ (17)

When the charge term dominates the peak to peak voltage ripple becomes:

$$V_{PPQ} \approx \frac{\Delta I}{8 \times C \times f_s} \quad (18)$$

It is tempting to simply add these two results together for the case where the voltage ripple is significantly influenced by both the capacitance and the esr. However, this will yield an overly pessimistic result, in that it does not account for the phase difference between these terms.

Using the ripple voltage equations and the RMS current equation should give a design that safely meets the steady state output requirements. However, additional capacitance is often needed to meet transient requirements and the specific local decoupling requirements of any IC that is being powered off of this voltage. This is not just a function of the capacitor bank but also the dynamics of the control loop. See the *UCD9240 Compensation Cookbook* for additional details.

DECOUPLING

It is necessary that V_{GG} and BP3 have their own local capacitance as physically close as possible to these pins. The V_{GG} capacitor should be connected as close as possible to pin 5 and PGND with a 4.7µF ceramic capacitor. The BP3 capacitor should be connected as close as possible to pin 22 and AGND with a 1µF ceramic capacitor.

The UCD7242 also supports the ability to operate from input voltages down to 2.2V. In these cases an additional supply rail must be connected to V_{GG} and VGG_DIS must be shorted to V_{GG}. Potential external bias supply generators for low V_{IN} operation: *TPS63000, TPS61220*. The amount of current required for this supply is dependant on the V_{GG} voltage, the switching frequency and the number of active channels used in the UCD7242. When both sides are active, use Figure 11: *V_{GG} Supply Current with 2 Rails Operating* for current draw estimates. If only one side is active, use Figure 10: *V_{GG} Supply Current with 1 Rail Operating and 1 Rail Off*.

CURRENT SENSE

An appropriate resistor must be connected to the current sense output pins to convert the I_{MON} current to a voltage. In the case of the UCD9XXX digital controllers, these parts have a full scale current monitor range of 0V to 2V. It is desirable to maximize this range to make full use of the current monitoring resolution inside the controller. In order to ensure that current sensing will occur all the way to I_{MAX}=10A a 1.8V target is chosen. In this case a resistor 9.09kΩ would work.

$$R_{MON} = \frac{V_{MON}}{I_{MAX} \times 20 \frac{\mu A}{A}} \quad (19)$$

In some applications it may be necessary to filter the I_{MON} signal. The UCD7242 I_{MON} pin is a current source output, so a capacitor to ground in parallel with the current-to-voltage conversion resistor is all that is required. As a rule of thumb, placing the corner frequency of the filter at 20% of the switching frequency should be sufficient.

For example, if the switching frequency is 500kHz or higher the ripple frequency will be easily rejected with a corner frequency of approximately 100kHz. With a 100kHz pole point, the filter time constant is 1.6µs. A fast current transient should be detected within 4.8µs.

$$C_{MON} = \frac{1}{2 \times \pi \times R_{MON} \times 20\% \times f_s} \quad (20)$$

20A Power Stage

It is possible to configure the UCD7242 to supply 20A by tying the outputs of two power stages together. When doing this it is required that the PWM pulse widths of the two PWM input signals be identical. The best way to do this is to drive PWM-A and PWM-B from the same signal. This ensures that balanced volt seconds will be applied to the external SW pins.

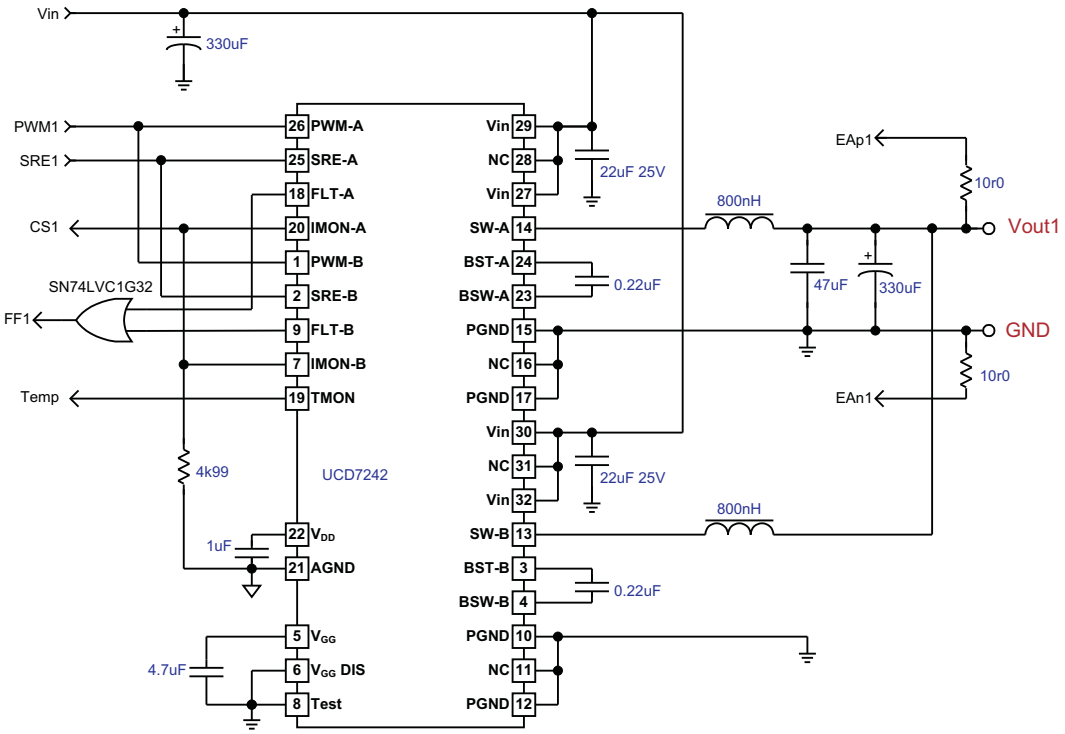


Figure 18. 20A Design

Layout Recommendations

The primary thermal cooling path is from the V_{IN}, GND, and the SW “stripes” on the bottom of the package. Wide copper traces should connect to these nodes. 1-ounce copper should be the minimum thickness of the top layer; however, 2-ounce copper is better. Multiple thermal vias should be placed near the GND stripes that connect to a PCB ground plane. There is room to place multiple 10-mil (0.25mm) diameter vias next to the V_{IN} and GND stripes under the package.

For input bypassing, the 22µF input ceramic capacitors should be connected as close as possible to the V_{IN} and GND stripes. If possible, the input caps should be placed directly under the UCD7242 using multiple 10-mil vias to bring the V_{IN} and GND connections to the back side of the board. Minimizing trace inductance in the bypass path is extremely important to reduce the amplitude of ringing on the switching node.

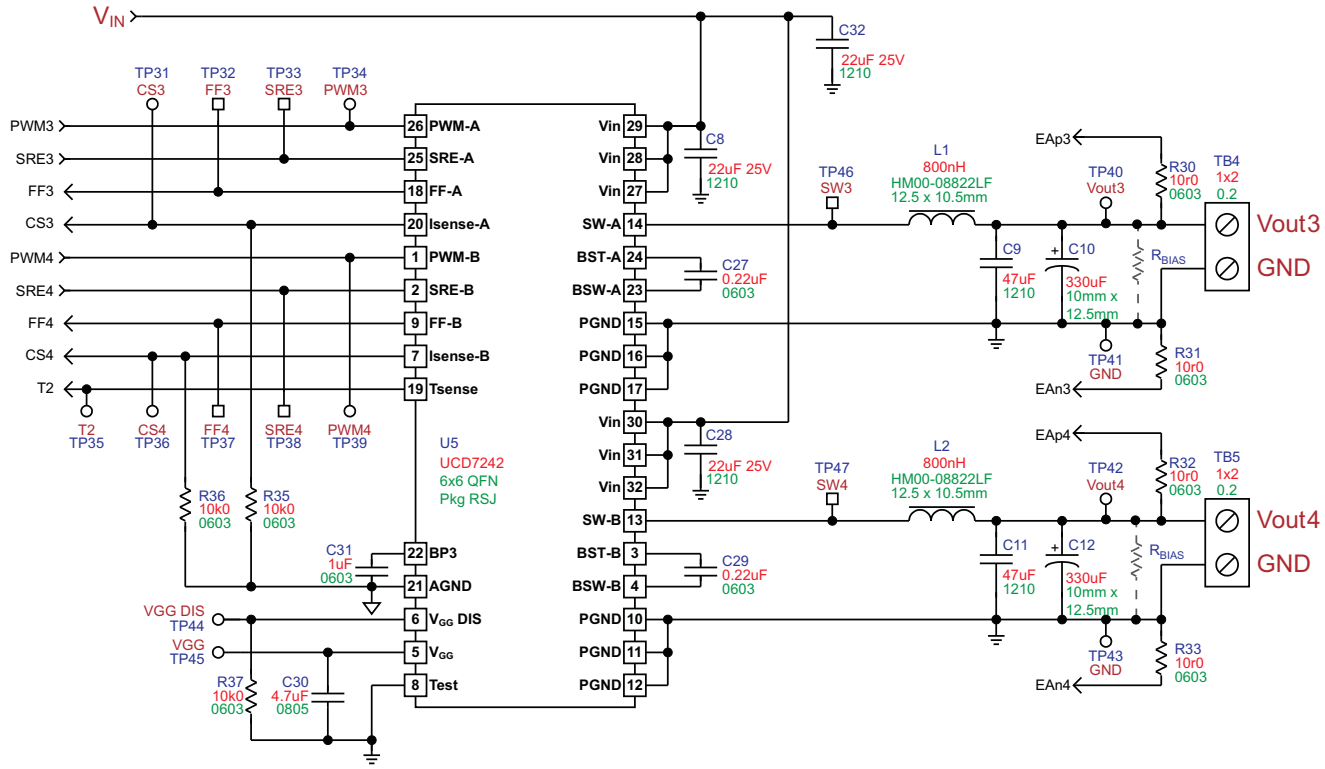


Figure 19. Schematic Fragment from 4-Output EVM

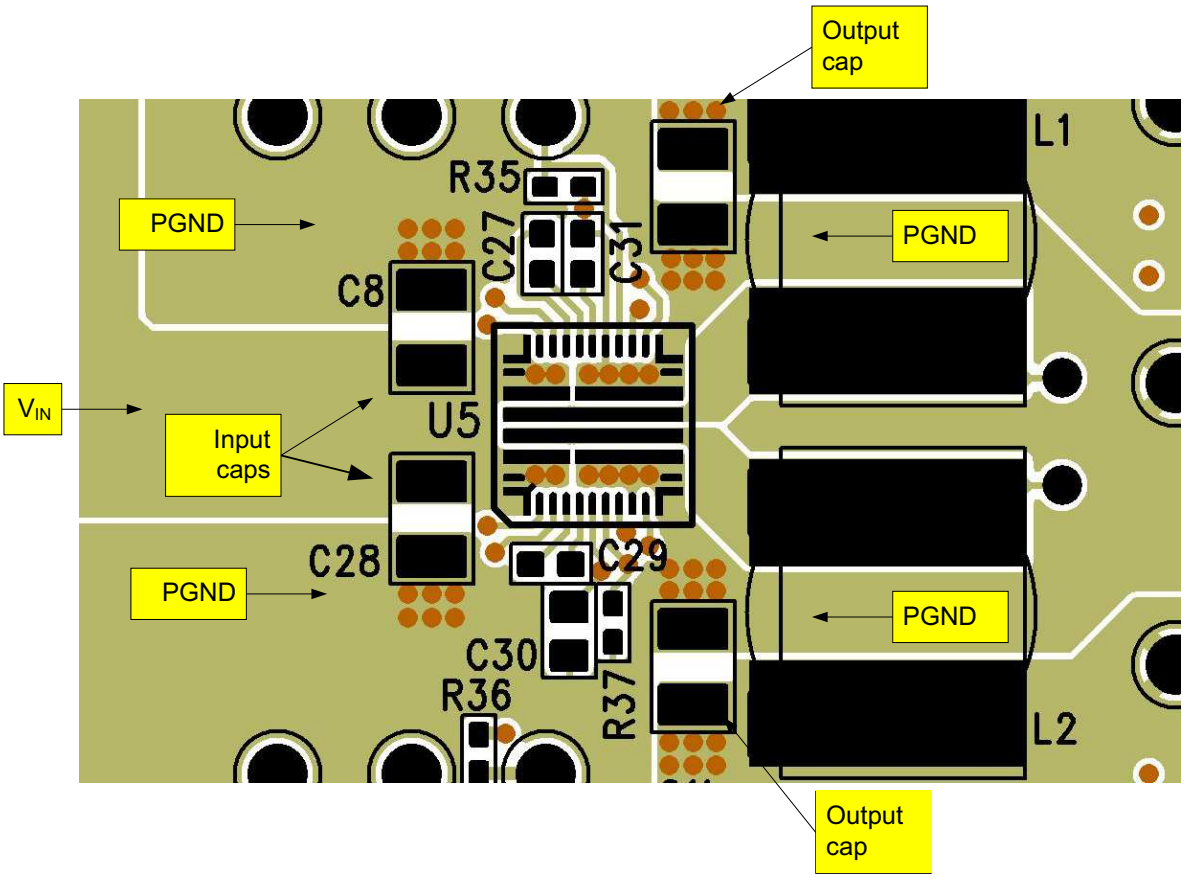
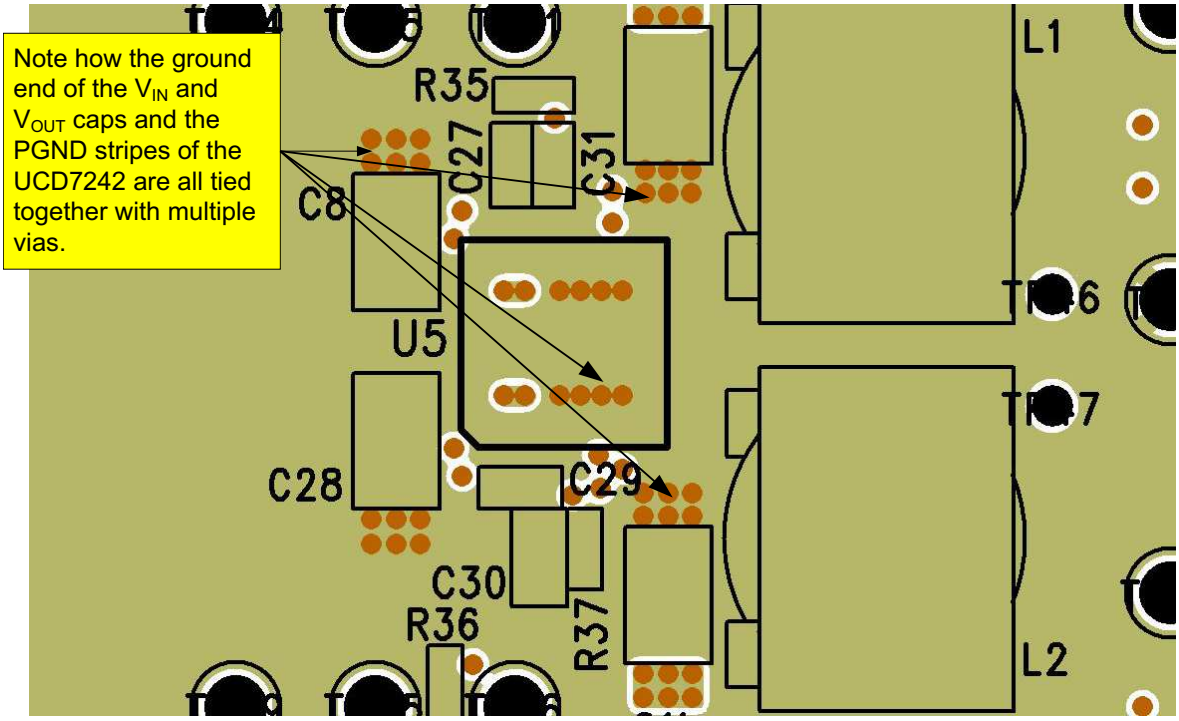


Figure 20. Top Layer



Note: This is the primary heat dispersal layer as well as the major return-current path.

Figure 21. Layer 2 - Power GND Plane

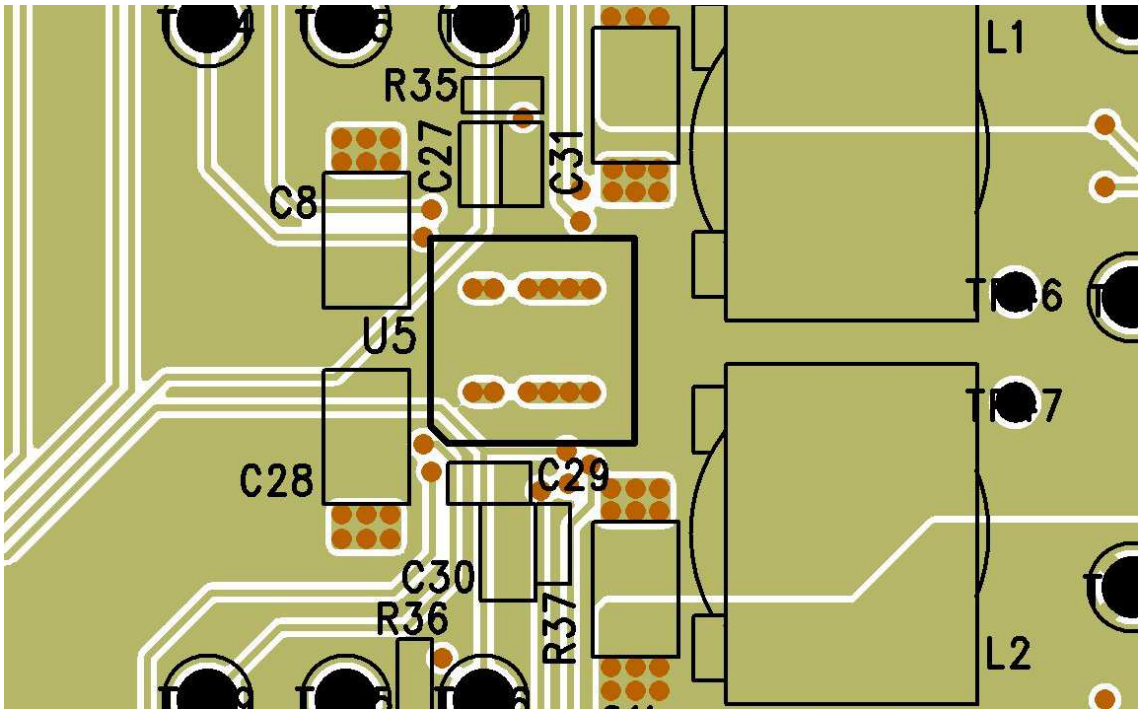


Figure 22. Layer 3

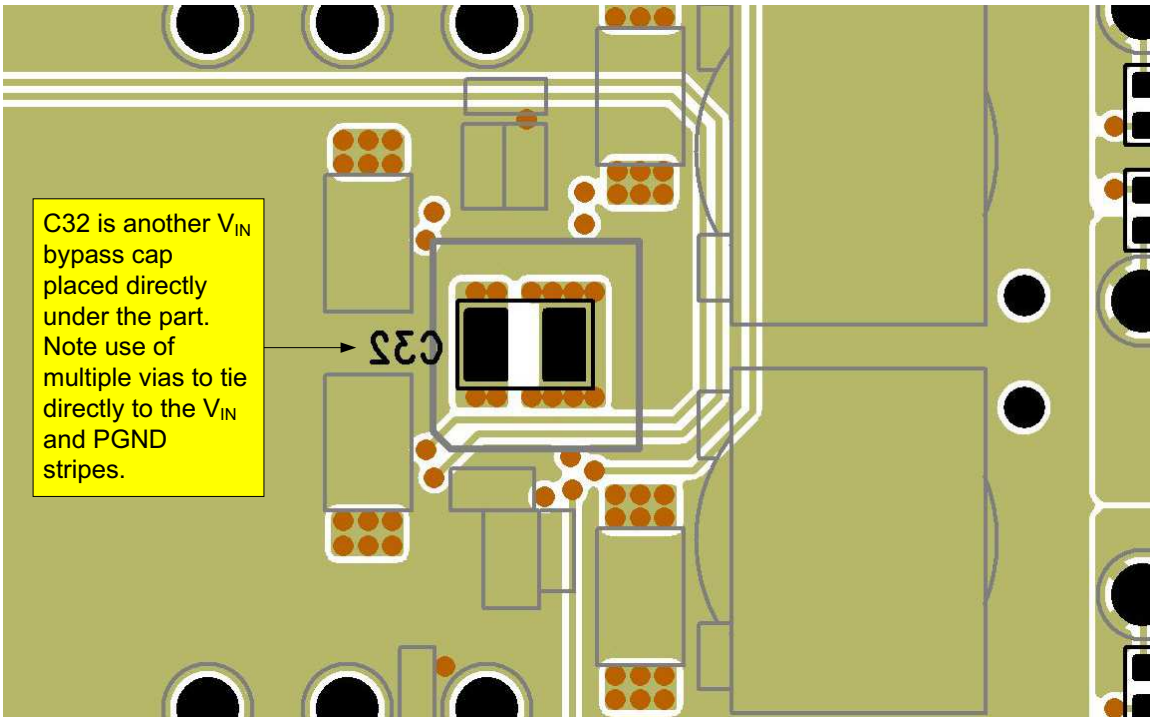


Figure 23. Bottom Layer (X-ray View)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCD7242MRSJREP	ACTIVE	VQFN-HR	RSJ	32	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	UCD7242 EP	Samples
V62/14601-01XE	ACTIVE	VQFN-HR	RSJ	32	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	UCD7242 EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

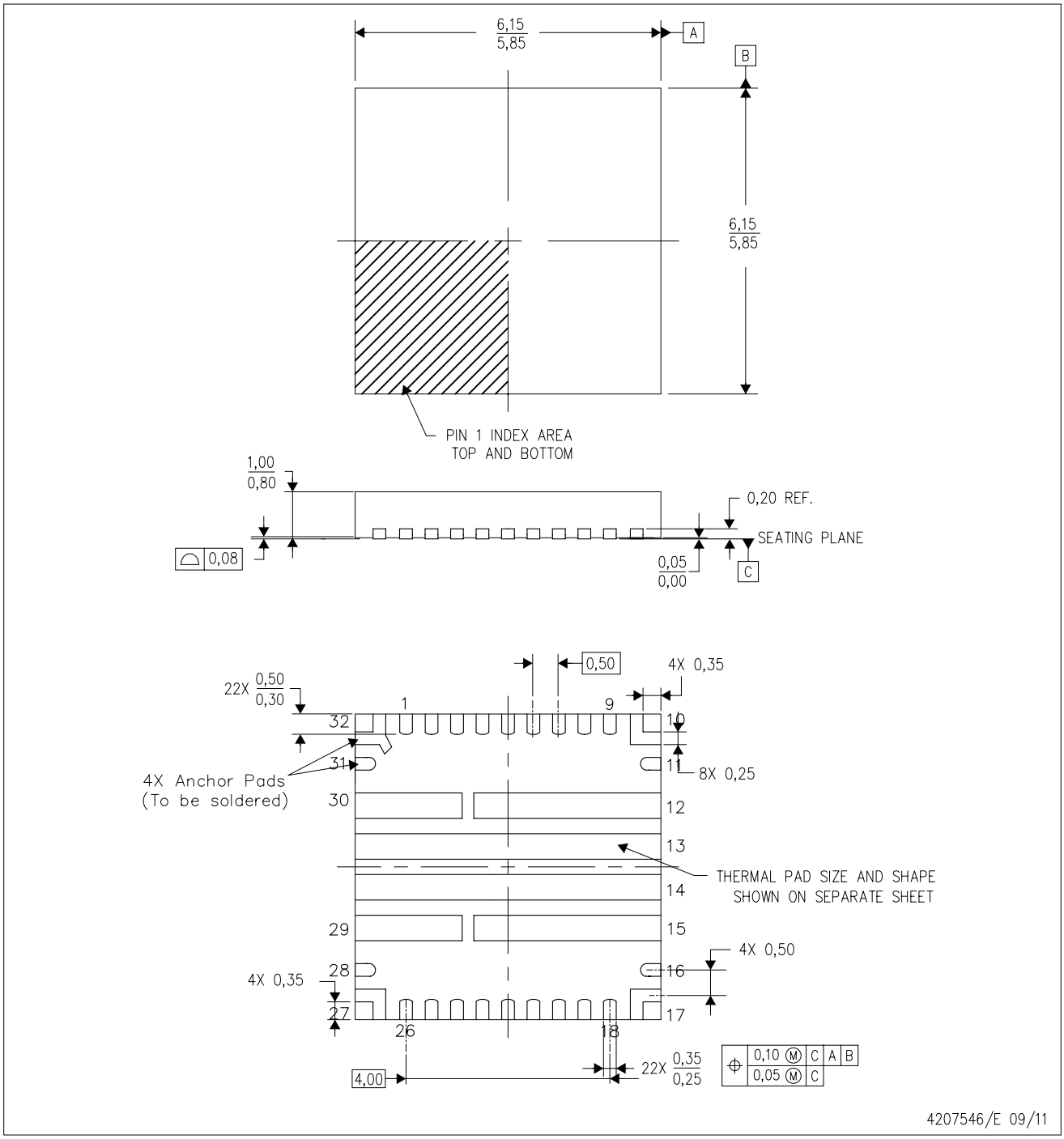
OTHER QUALIFIED VERSIONS OF UCD7242-EP :

- Catalog: UCD7242

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

RSJ (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

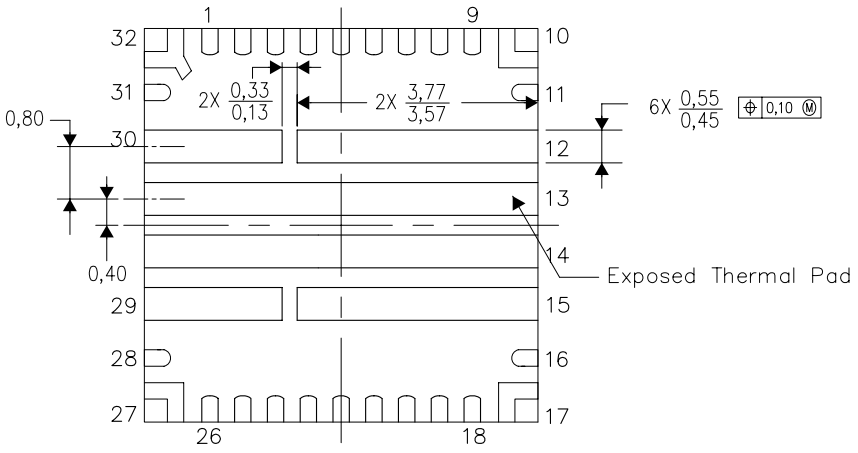
RSJ (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



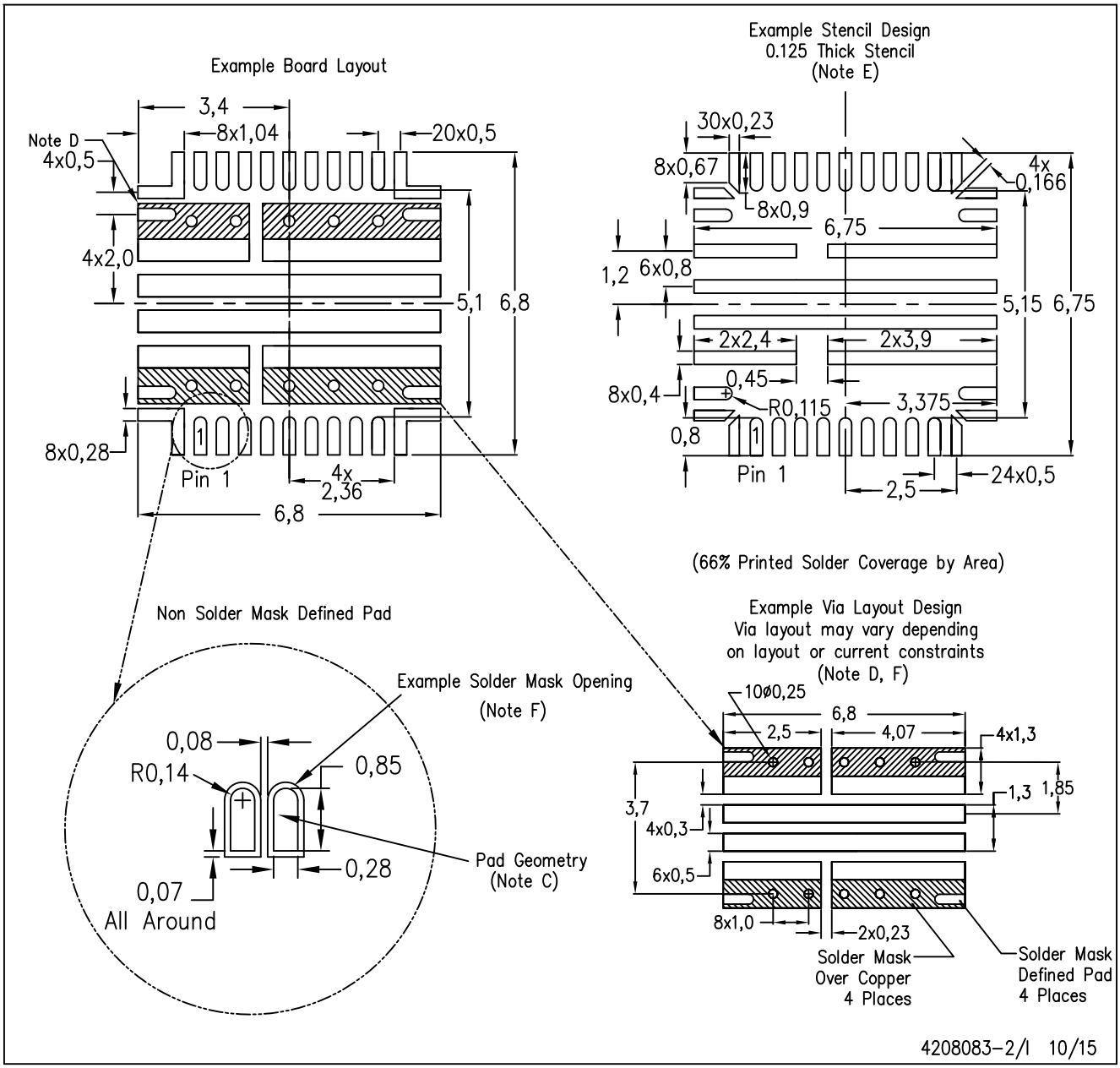
Bottom View

Exposed Thermal Pad Dimensions

4208082/F 09/11

NOTE: All linear dimensions are in millimeters

RSJ (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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