

P/N: TS8FSDMAR62ISI TS16FSDMAR62ISI Industrial Grade SD card

Description

Transcend's Industrial Temp SD cards combine the advantages of large storage capacity and industrial range (-40°~85°C) operating temperature flexibility, making them the best solution for tough industrial environments where performance and reliability are essential.

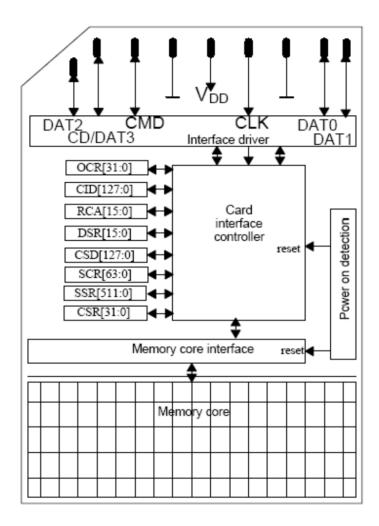
Features

- RoHS compliant product
- Compatible with SD Specification Ver. 3.01
- Supports Speed Class Specification up to Class 10
- Manufactured with SLC NAND Flash chips for extra long life and stability
- Support S.M.A.R.T. Function
- Operating Temperature: -40 ~ 85°C
- Mechanical Write Protection Switch
- Built-in ECC and Wear leveling
- Support ESD IEC 61000-4-2

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Architecture

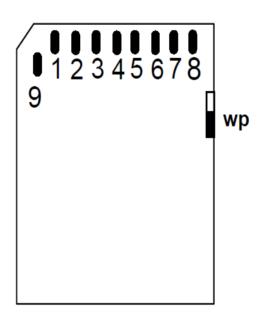


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Pin Definition

	SD Mode		SPI Mode		
Pin No.	Name	Description	Name	Description	
1	CD/DAT3	Card Detect/Data Line [Bit3]	CS	Reserved	
2	CMD	Command/Response	DI	Chip Select	
3	V _{SS1}	Supply voltage ground	V _{SS}	Data In	
4	V_{DD}	Supply voltage	VDD	Supply voltage	
5	CLK	Clock	SCLK	Clock	
6	V_{SS2}	Supply voltage ground	V_{SS2}	Supply voltage ground	
7	DAT0	Data Line [Bit0]	DO	Data out	
8	DAT1	Data Line [Bit1]	RSV	Reserved	
9	DAT2	Data Line [Bit2]	RSV	Reserved	



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Specifications

Physical Specification		
Form Factor		SD
SD specification		SD3.01
	Length	32.00 ± 0.1
Dimensions (mm)	Width	24.00 ± 0.1
	Height	2.10 ± 0.15



Bus Mode/ Power Consumption					
		Value(Max.)			
	Read	100mA			
Default Mode (25MHz)	Write	100mA			
(====)	ldle	0.5mA			
High Ones describe	Read	200mA			
High Speed mode (50MHz)	Write	200mA			
(00///12)	ldle	0.5mA			

Note: Power consumption is referred to Section 6.6.3 of the SDA Physical Layer Specification, Version 3.01

Environmental Specifications				
Operating Temperature	- 40°C to 85°C			
Storage Temperature	- 40°C to 85°C			
Durability	10.000 mating cycles			
Drop test	1.5m free fall			
Regulator	CE/FCC/BSMI			



Product Description

1.Features

1.1 Lock Function

Support for password protected locking and unlocking of SD devices. It uses the LOCK/UNLOCK command(CMD42) which is available in SD command sets.

1.2 Built-in ECC Engine

In event of errors, the combined data allow the recovery of the original data. The number of errors that can be recovered depends on the algorithm used.

1.3 Wear-leveling

This function means the data are no longer tied to a single physical area, which can extend Card's life expectancy.

1.4 S.M.A.R.T. function

Transcend Industrial SD Card supports S.M.A.R.T. command (ACMD13) that allows the user to read the health information of the SD. Transcend also define some innovated S.M.A.R.T. features which allows the user to evaluate the status of the SD in a much more efficient way.

Identifier	Length	Description		
Min Erase Count-L/H	4 Bytes	Min Erase Count-Low Byte /High Byte		
Max Erase Count-L/H	4 Bytes	Max Erase Count-Low Byte /High Byte		
Abnormal Power Off Count	2 Bytes	Abnormal Power Off Count		
Health Status (Remain Life in %)	1 Byte	(erase_count - avg_erase_count) / erase_count		
Total Erase Count	4 Bytes	Total Erase Count		
Average Erase Count-L/H	2 Bytes	Average Erase Count-Low Byte /High Byte		
RTBB count	2 Bytes	Bad block after SD card used		
Spare block count	1 Byte	Spare block count		



2.Bus Topology

The SD Memory Card system defines two alternative communication protocols:SD and SPI. The host system can choose either one of modes. The card detects which mode is request by host when the reset command is received and expects all further communication to be in the same communication mode.

2.1 SD Bus

For more details, refer to Section 3.5.1 of the SDA Physical Layer Specification, Version 3.01.

2.2 SPI Bus

For more details, refer to Section 3.5.2 of the SDA Physical Layer Specification, Version 3.01.

3.SD card Register information

3.1 OCR register

The OCR register stores the VDD voltage profile of the card, refer to Section 5.1 of the SDA Physical Layer Specification, Version 3.01 for more information.

3.2 CID register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

Name	Field	Width	CID-slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product revision	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
reserved	-	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
not used, always '1'	-	1	[0:0]

• MID

An 8-bit binary number that identifies the card manufacturer. The MID number is controlled, defined, and allocated to a SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

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• OID

A 2-character ASCII string that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined, and allocated to a SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

PNM

The product name is a string, 5 ASCII characters long. PNM can be customized by Transcend

• PRV

The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an \hat{Y} . \hat{w} revision number. The \hat{Y} is the most significant nibble and \hat{w} is the least significant nibble.

As an example, the PRV binary value field for product revision 6.1 will be: 0110 0010

PSN

The Serial Number is 32 bits of binary number. PSN Number can be customized by Transcend

MDT

The manufacturing date composed of two hexadecimal digits, one is 8 bit representing the year(y) and the other is four bits representing the month(m).

The $\hat{\mathbf{w}}$ field [11:8] is the month code. 1 = January.

The \overline{y} field [19:12] is the year code. 0 = 2000.

As an example, the binary value of the Date field for production date April 1666 will be: 00000001 0100.

MDT can be customized by Transcend

• CRC

CRC7 checksum (7 bits).

3.3 CSD register

The following sections describe the CSD fields and the relevant data types for the standard and High Capacity SD Memory Card. CSD Version 1.0 is applied Capacity SD Memory Card and CSD Version is applied to 2.0 is applied to only the High Capacity SD Memory Card. The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enables host, which refers to these fields, to keep compatibility to CSD Version 1.0. The Cell Type field is coded as follows: R = readable, W(1) = writable once, W = multiple writable.

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3.3.1 CSD Register Structure

CSD_STRUCTURE	CSD Structure version	Card capacity
0	CSD Version1.0	Standard Capacity
1	CSD Version2.0	High Capacity and Extended Capacity
2-3	reserved	

3.3.2 CSD Register Structure (CSD Version 1.0)

Name	Field	Width	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	R	[127:126]
reserved	-	6	R	[125:120]
data read access-time-1	TAAC	8	R	[119:112]
data read access-time-2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]
max. data transfer rate	TRAN_SPEED	8	R	[103:96]
card command classes	ccc	12	R	[95:84]
max. read data block length	READ_BL_LEN	4	R	[83:80]
partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]
write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]
read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]
DSR implemented	DSR_IMP	1	R	[76:76]
reserved	-	2	R	[75:74]
device size	C_SIZE	12	R	[73:62]
max. read current @VDD min	VDD_R_CURR_MIN	3	R	[61:59]
max. read current @VDD max	VDD_R_CURR_MAX	3	R	[58:56]
max. write current @VDD min	VDD_W_CURR_MIN	3	R	[55:53]
max. write current @VDD max	VDD_W_CURR_MAX	3	R	[52:50]



Name	Field	Width	Cell Type	CSD-slice
device size multiplier	C_SIZE_MULT	3	R	[49:47]
erase single block enable	ERASE_BLK_EN	1	R	[46:46]
erase sector size	SECTOR_SIZE	7	R	[45:39]
write protect group size	WP_GRP_SIZE	7	R	[38:32]
write protect group enable	WP_GRP_ENABLE	1	R	[31:31]
reserved for MultiMediaCard compatibili	ty	2	R	[30:29]
write speed factor	R2W_FACTOR	3	R	[28:26]
max. write data block length	WRITE_BL_LEN	4	R	[25:22]
partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]
reserved	-	5	R	[20:16]
File format group	FILE_FORMAT_GRP	1	R/W(1)	[15:15]
copy flag (OTP)	COPY	1	R/W(1)	[14:14]
permanent write protection	PERM_WRITE_PROTECT	1	R/W(1)	[13:13]
temporary write protection	TMP_WRITE_PROTECT	1	R/W	[12:12]
File format	FILE_FORMAT	2	R/W(1)	[11:10]
reserved		2	R/W	[9:8]
CRC	CRC	7	R/W	[7:1]
not used, always'1'	-	1	-	[0:0]

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3.3.3 CSD Register (CSD Version 2.0)

Name	Field	Width	Value	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	01b	R	[127:126]
reserved	-	6	00 0000Ь	R	[125:120]
data read access-time	(TAAC)	8	0Eh	R	[119:112]
data read access-time in CLk cycles (NSAC*100)	(NSAC)	8	00h	R	[111:104]
max. data transfer rate	(TRAN_SPEED)	8	32h or 5Ah	R	[103:96]
card command classes	CCC	12	01x110110101b	R	[95:84]
max. read data block length	(READ_BL_LEN)	4	9	R	[83:80]
partial blocks for read allowed	(READ_BL_PARTIAL)	1	0	R	[79:79]
write block misalignment	(WRITE BLK MISALIGN)	1	0	R	[78:78]
read block misalignment	(READ_BLK_MISALIGN)	1	0	R	[77:77]
DSR implemented	DSR_IMP	1	x	R	[76:76]
reserved	-	6	00 0000ь	R	[75:70]
device size	C_SIZE	22	00 xxxxh	R	[69:48]
reserved	-	1	0	R	[47:47]
erase single block enable	(ERASE BLK EN)	1	1	R	[46:46]
erase sector size	(SECTOR_SIZE)	7	7Fh	R	[45:39]
write protect group size	(WP_GRP_SIZE)	7	0000000ь	R	[38:32]
write protect group enable	(WP GRP ENABLE)	1	0	R	[31:31]
reserved		2	00b	R	[30:29]
write speed factor	(R2W_FACTOR)	3	010b	R	[28:26]
max. write data block length	(WRITE BL LEN)	4	9	R	[25:22]
partial blocks for write allowed	(WRITE_BL_PARTIAL)	1	0	R	[21:21]
reserved	-	5	00000b	R	[20:16]
File format group	(FILE FORMAT GRP)	1	0	R	[15:15]
copy flag (OTP)	COPY	1	x	R/W(1)	[14:14]
permanent write protection	PERM_WRITE_PROTECT	1	x	R/W(1)	[13:13]
temporary write protection	TMP WRITE PROTECT	1	x	R/W	[12:12]
File format	(FILE_FORMAT)	2	00b	R	[11:10]
reserved	-	2	00b	R	[9:8]
CRC	CRC	7	xxxxxxxb	R/W	[7:1]
not used, always'1'	-	1	1	-	[0:0]

3.4 RCA register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. Refer to Section 5.4 in the SDA Physical Layer Specification, Version 3.01 for more information.

3.5 SCR register

In addition to the CSD register, there is another configuration register named SD CARD configuration Register, SCR provide information on the SD memory card's special feature that were configured into the given card.Refer to Section 5.6 in the SDA Physical Layer Specification, Version 3.01 for more information.

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3.6 SSR register
The SD status contains status bits that are related to the SD memory card proprietary features and may be used for future application-specific usage. The SD Status structure is described in Section 4.10.2 in the SDA Physical Layer Specification, Version 3.01.
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