# SY89228U

## 1GHz Precision, LVPECL ÷3, ÷5 Clock Divider with Fail-Safe Input and Internal Termination

Precision Edge®

## General Description

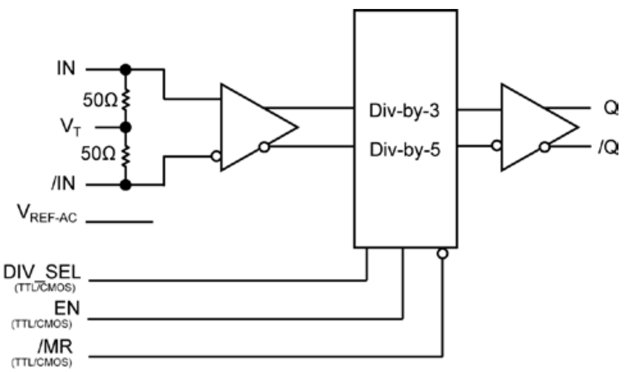
The SY89228U is a precision, low jitter 1GHz ÷3, ÷5 clock divider with an LVPECL output. A unique Fail-Safe Input (FSI) protection prevents metastable output conditions when the input clock voltage swing drops significantly below 100mV or input is removed.

The differential input includes Micrel's unique, 3-pin internal termination architecture that allows the input to interface to any differential signal (AC- or DC-coupled) as small as 100mV (200mV$_{PP}$) without any level shifting or termination resistor networks in the signal path. The outputs are 800mV, 100K-compatible LVPECL with fast rise/fall times guaranteed to be less than 270ps.

The SY89228U operates from a 2.5V ±5% or 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY89228U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at: www.micrel.com.

## Block Diagram




United States Patent No. RE44,134

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## Features

- Accepts a high-speed input and provides a precision ÷3 and ÷5 sub-rate, LVPECL output
- Fail-Safe Input
  – Prevents oscillations when input is invalid
- Guaranteed AC performance over temperature and supply voltage:
  – DC-to >1.0GHz throughput
  – < 1500ps Propagation Delay (In-to-Q)
  – < 270ps Rise/Fall times
- Ultra-low jitter design:
  – <1ps$_{RMS}$ random jitter
  – <1ps$_{RMS}$ cycle-to-cycle jitter
  – <10ps$_{PP}$ total jitter (clock)
  – <0.7ps$_{RMS}$ MUX crosstalk induced jitter
- Unique patented internal termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- Wide input voltage range VCC to GND
- 800mV LVPECL output
- 46% to 54% Duty Cycle(÷ 3)
- 47% to 53% Duty Cycle(÷ 5)
- 2.5V ±5% or 3.3V ±10% supply voltage
- -40°C to +85°C industrial temperature range
- Available in 16-pin (3mm x 3mm) QFN package

## Applications

- Fail-safe clock protection

## Markets

- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

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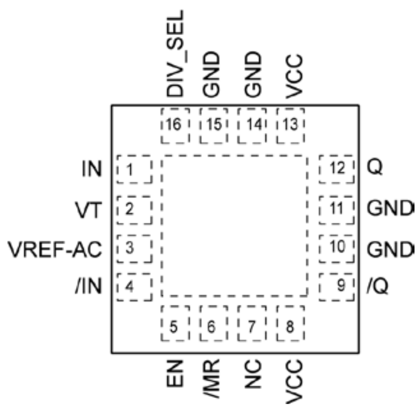
## Ordering Information[1]

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|---|---|---|---|---|
| SY89228UMG | QFN-16 | Industrial | 228U with Pb-Free bar-line Indicator | NiPdAu Pb-Free |
| SY89228UMGTR[2] | QFN-16 | Industrial | 228U with Pb-Free bar-line Indicator | NiPdAu Pb-Free |

**Notes:**
1. Contact factory for die availability. Dice are guaranteed at $T_A$ = 25°C, DC Electricals Only.
2. Tape and Reel.

## Pin Configuration




**16-Pin QFN**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## Pin Description

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1, 4 | IN, /IN | Differential Input: This input pair is the differential signal input to the device, which accepts AC- or DC-coupled signal as small as 100mV. The input internally terminates to a VT pin through 50Ω and has level shifting resistors of 3.72 kΩ to VCC. This allows a wide input voltage range from VCC to GND. See Figure 3a, Simplified Differential Input Stage for details. Note that this input will default to a valid (either HIGH or LOW) state if left open. See "Input Interface Applications" subsection. |
| 2 | VT | Input Termination Center-Tap: Each side of the differential input pair terminates to the VT pin. The VT pin provides a center-tap for the input (IN, /IN) to a termination network for maximum interface flexibility. See "Input Interface Applications" subsection for more details. |
| 3 | VREF-AC | Reference Voltage: This output biases to $V_{CC}$–1.2V. It is used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the VT pin. Bypass with 0.01µF low ESR capacitor to VCC. Due to limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. Maximum sink/source current is ±0.5mA. See "Input Interface Applications" subsection. |
| 5 | EN | Single-ended Input: This TTL/CMOS-compatible input disables and enables the output. It is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. When disabled, Q goes LOW and /Q goes HIGH. EN being synchronous, outputs will be enabled/disabled after a rising and a falling edge of the input clock. $V_{TH} = V_{CC}/2$. |
| 6 | /MR | Single-ended Input: This TTL/CMOS-compatible input, when pulled LOW, asynchronously sets Q output LOW and /Q output HIGH. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. $V_{TH} = V_{CC}/2$. |
| 7 | NC | No Connect |
| 8, 13 | VCC | Positive Power Supply: Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to the $V_{CC}$ pins as possible. |
| 12, 9 | Q, /Q | Differential Output: The LVPECL output swing is typically 800mV and is terminated with 50Ω to $V_{CC}$-2V. See the "Truth Table" below for the logic function. |
| 10, 11, 14,15 | GND, Exposed Pad | Ground: Ground and exposed pad must be connected to a ground plane that is the same potential as the ground pins. |
| 16 | DIV_SEL | Single-ended Input: This TTL/CMOS-compatible input selects divide-by-3 when pulled LOW and divide-by-5 when pulled HIGH. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. $V_{TH} = V_{CC}/2$. |

## Truth Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **DIV_SEL** | **EN** | **/MR** | **Q** | **/Q** |
| X | X | 0 | 0 | 1 |
| 0 | 1 | 1 | ÷3 | ÷3 |
| 1 | 1 | 1 | ÷5 | ÷5 |
| X | 0 | 1 | 0 | 1 |


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## Absolute Maximum Ratings[1]

Supply Voltage ($V_{CC}$) ..........................–0.5V to +4.0V
Input Voltage ($V_{IN}$) .................................–0.5V to $V_{CC}$
LVPECL Output Current ($I_{OUT}$)..................................
Continuous ................................................ 50mA
Surge....................................................... 100mA
Current ($V_T$)
Source or sink current on $V_T$ pin…………±100mA
Input Current
Source or sink current on (IN, /IN) ........... ±50mA
Current ($V_{REF-AC}$)
Source/Sink Current on $V_{REF-AC}$[4]............ ±0.5mA
Maximum Operating Junction Temperature…..125°C
Lead Temperature (soldering, 20 sec.) ..........+260°C
Storage Temperature ($T_s$)..................–65°C to 150°C

## Operating Ratings[2]

Supply Voltage ($V_{CC}$).................. +2.375V to +2.625V
.....................................................+3.0V to +3.6V
Ambient Temperature ($T_A$)................ –40°C to +85°C
Package Thermal Resistance [3]
QFN ($\theta_{JA}$)
Still-Air .................................................... 75°C/W
QFN ($\psi_{JB}$)
Junction-to-Board…………………………33°C/W

## DC Electrical Characteristics[5]

$T_A$ = –40°C to +85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply | | 2.375<br>3.0 | 2.5<br>3.3 | 2.625<br>3.6 | V<br>V |
| $I_{CC}$ | Power Supply Current | No load, max $V_{CC}$ | | 40 | 55 | mA |
| $R_{IN}$ | Input Resistance (IN-to-$V_T$) | | 45 | 50 | 55 | Ω |
| $R_{DIFF\_IN}$ | Differential Input Resistance (IN-to-/IN) | | 90 | 100 | 110 | Ω |
| $V_{IH}$ | Input High Voltage (IN, /IN) | | 1.2 | | $V_{CC}$ | V |
| $V_{IL}$ | Input Low Voltage (IN, /IN) | | 0 | | $V_{IH}$–0.1 | V |
| $V_{IN}$ | Input Voltage Swing (IN, /IN) | See Figure 2a. Note 6. | 0.1 | | $V_{CC}$ | V |
| $V_{DIFF\_IN}$ | Differential Input Voltage Swing \|IN-/IN\| | See Figure 2b. | 0.2 | | | V |
| $V_{IN\_FSI}$ | Input Voltage Threshold that Triggers FSI | | | 30 | 100 | mV |
| $V_{REF-AC}$ | Output Reference Voltage | | $V_{CC}$–1.3 | $V_{CC}$–1.2 | $V_{CC}$–1.1 | V |
| $V_{T\_IN}$ | Voltage from Input to $V_T$ | | | | 1.8 | V |

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. $\theta_{JA}$ and $\psi_{JB}$ values are determined for a 4-layer board in still air unless otherwise stated.
4. Due to limited drive capability use for input of the same package only.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. $V_{IN}$ (max) is specified when $V_T$ is floating.

## LVPECL Outputs DC Electrical Characteristics[7]

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $R_L$ = 50Ω to $V_{CC}$-2V; $T_A$ = –40°C to + 85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage<br>Q, /Q | | $V_{CC}$-1.145 | | $V_{CC}$-0.895 | V |
| $V_{OL}$ | Output LOW Voltage<br>Q, /Q | | $V_{CC}$-1.945 | | $V_{CC}$-1.695 | V |
| $V_{OUT}$ | Output Voltage Swing<br>Q, /Q | See Figure 2a. | 550 | 800 | 950 | mV |
| $V_{DIFF\_OUT}$ | Differential Output Voltage Swing<br>Q, /Q | See Figure 2b. | 1100 | 1600 | | mV |

## LVTTL/CMOS DC Electrical Characteristics[7]

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $T_A$ = –40°C to + 85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V |
| $I_{IH}$ | Input HIGH Current | | -125 | | 30 | µA |
| $I_{IL}$ | Input LOW Current | | -300 | | | µA |

**Note:**

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC Electrical Characteristics[8]

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $R_L$ = 50Ω to $V_{CC}$-2V; $T_A$ = –40°C to + 85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Input Operating Frequency | $V_{OUT}$ ≥ 200mV | 1.0 | 1.5 | | GHz |
| tw | Minimum Pulse Width | IN, /IN | 400 | | | ps |
| $t_{pd}$ | Differential Propagation Delay In-to-Q | 100mV < $V_{IN}$ ≤ 200mV, Note 9 | 900 | 1150 | 1500 | ps |
| | In-to-Q | 200mV < $V_{IN}$ ≤ 800mV, Note 9 | 800 | 1050 | 1400 | ps |
| | /MR(H-L)-to-Q | | 350 | 570 | 850 | ps |
| $t_{RR}$ | Reset Recovery Time | /MR(L-H)-to-IN | 300 | | | ps |
| $t_S$ EN | Set-up Time EN-to-IN | Note 10 | 300 | | | ps |
| $t_H$ EN | Hold Time IN-to-EN | Note 10 | 800 | | | ps |
| $t_{skew}$ | Part-to-Part Skew | Note 10 | | | 450 | ps |
| $t_{JITTER}$ | Clock Random Jitter | Note 11 | | | 1 | $ps_{RMS}$ |
| | Cycle-to-Cycle Jitter | Note 12 | | | 1 | $ps_{RMS}$ |
| | Total Jitter | Note 13 | | | 10 | $ps_{PP}$ |
| $t_r$, $t_f$ | Output Rise/Fall Time (20% to 80%) | At full output swing. | 100 | | 270 | ps |
| | Output Duty Cycle(÷ **3)** | Duty Cycle(input): 50%; f ≤1GHz; Note 14 | 46 | | 54 | % |
| | Output Duty Cycle(÷ **5)** | Duty Cycle(input): 50%; f ≤1GHz; Note 14 | 47 | | 53 | % |

**Notes:**

8. High-frequency AC-parameters are guaranteed by design and characterization.
9. The propagation delay is function of the rise and fall times at IN. Input $t_r$ / $t_f$ ≤ 300ps (20% to 80%). See “Typical Operating Characteristics” for details.
10. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold do not apply.
11. Random Jitter is measured with a K28.7 character pattern, measured at <$f_{MAX}$.
12. Cycle-to-Cycle Jitter definition: the variation of periods between adjacent cycles, $T_n – T_{n-1}$ where T is the time between rising edges of the output signal.
13. Total Jitter definition: with an ideal clock input of frequency <$f_{MAX}$, no more than one output edge in $10^{12}$ output edges will deviate by more than the specified peak-to-peak jitter value.
14. For Input Duty Cycle different from 50%, see “Output Duty Cycle Equation” in “Functional Description” subsection.

## Functional Description

### Fail-Safe Input (FSI)

The input includes a special failsafe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below 100m$V_{PK}$ (200m$V_{PP}$), typically 30m$V_{PK}$. Maximum frequency of the SY89228U is limited by the FSI function. Refer to Figure 1b.

### Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing, the FSI function will eliminate a metastable condition and guarantee a stable output signal. No ringing and no undetermined state will occur at the output under these conditions.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal as it nears the FSI threshold (typically, 30mV). Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. See "Typical Operating Characteristics" for detailed information.

### Output Duty Cycle Equation

For a non 50% input, derate the spec by:

For Divide by 3:

$$(0.5 - \frac{1 + \frac{X}{100}}{3}) \text{ x100, in \%}$$

For Divide by 5:

$$(0.5 - \frac{2 + \frac{X}{100}}{5}) \text{ x100, in \%}$$

X = input Duty Cycle, in %

Example: if a 45% input duty cycle is applied or X=45, in divide by 3 mode, the spec would expand by 1.67% to 44.3%-55.7%

### Enable (EN)

EN is a synchronous TTL/CMOS-compatible input that enables/disables the outputs based on the input to this pin. Internal 25kΩ pull-up resistor defaults the input to logic HIGH if left open. Input switching threshold is $V_{CC}$/2.

The Enable function operates as follows:

1. The enable/disable function is synchronous so that the clock outputs will be enabled or disabled following a rising and a falling edge of the input clock when switching from EN = LOW to EN = HIGH.

   However, when switching from EN = HIGH to EN = LOW, the clock outputs will be disabled following an input clock rising edge and an output clock falling edge.
2. The enable/disable function always guarantees the full pulse width at the output before the clock outputs are disabled, non-depending on the divider ratio.

Refer to Figure 1c for examples.

### Divider Operation

The divider operation uses both the rising and falling edge of the input clock. For divide by 3, the falling edge of the second input clock cycle will determine the falling edge of the output. For divide by 5, the falling edge of the third input clock cycle. Refer to Figure 1d.


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## Timing Diagrams

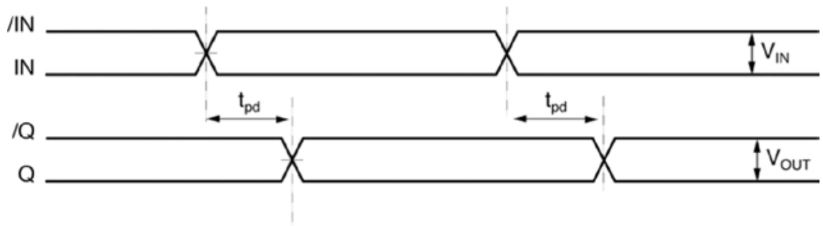


**Figure 1a. Propagation Delay**

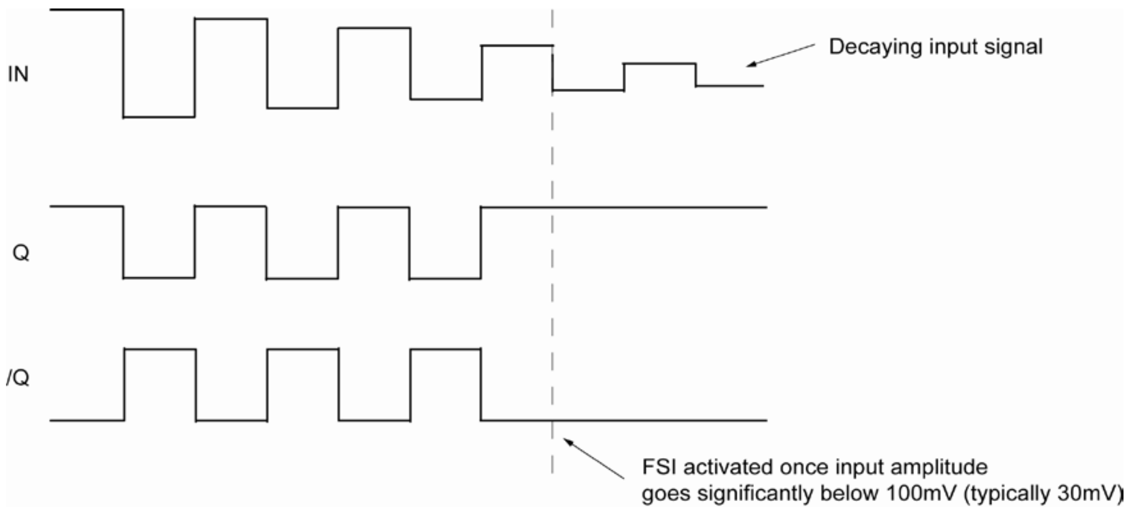


**Figure 1b. Fail-Safe Feature**


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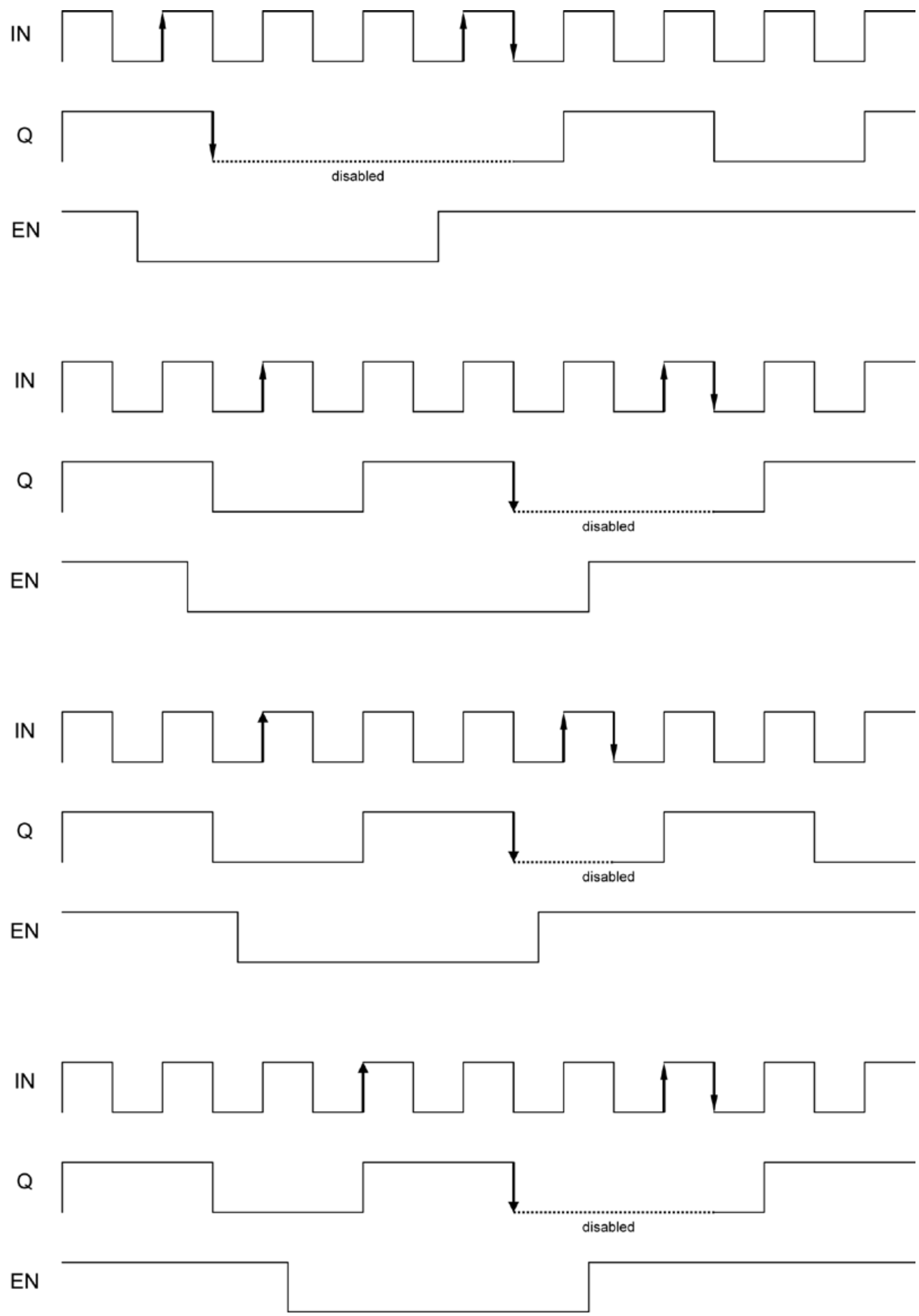


**Figure 1c. Enable Output Timing Diagram Examples (divide by 3)**


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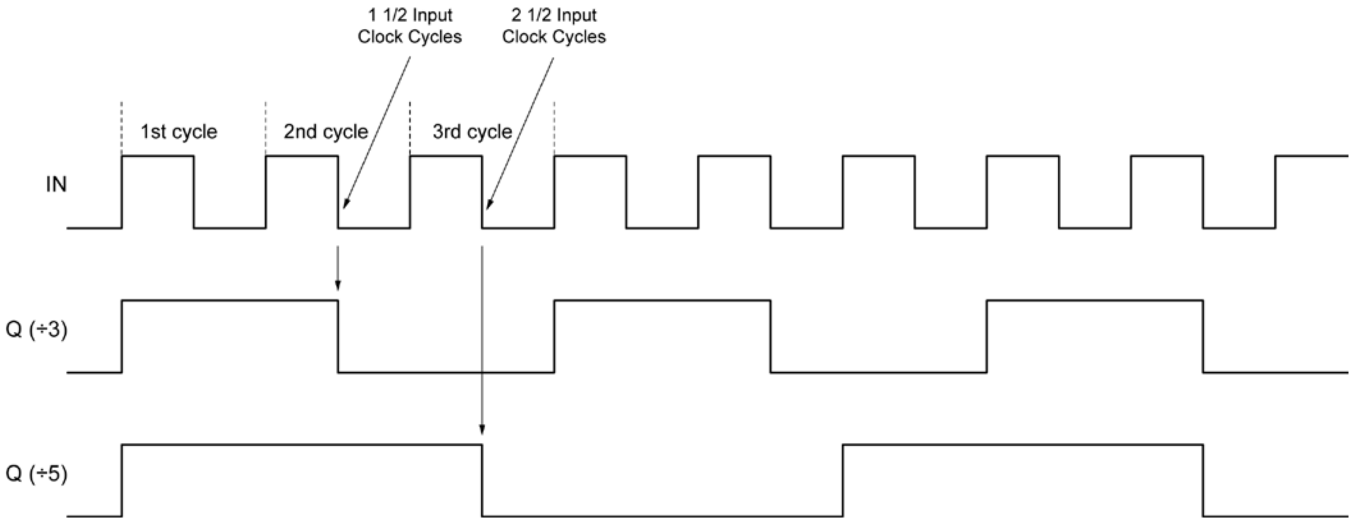


**Figure 1d. Divider Operation Timing Diagram**


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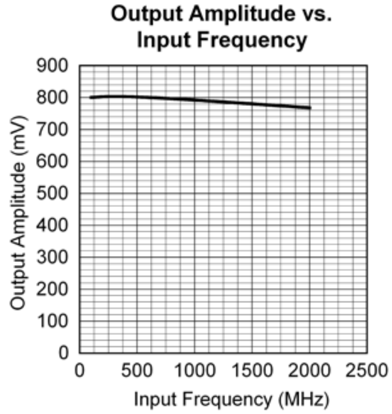
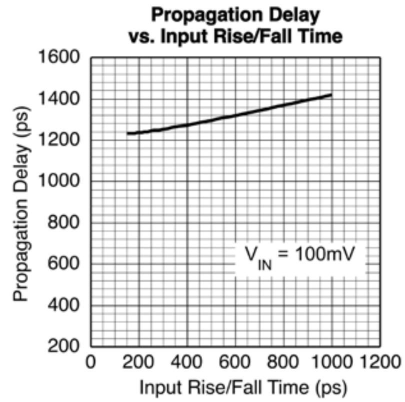
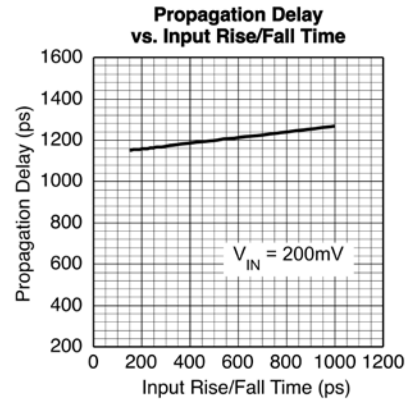
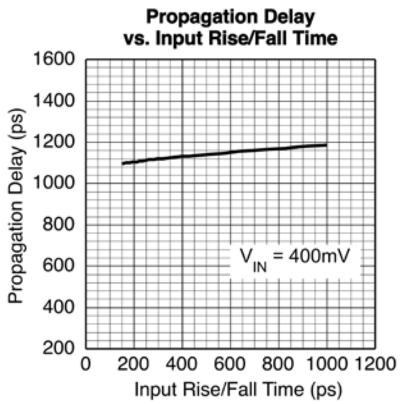
## Typical Operating Characteristics

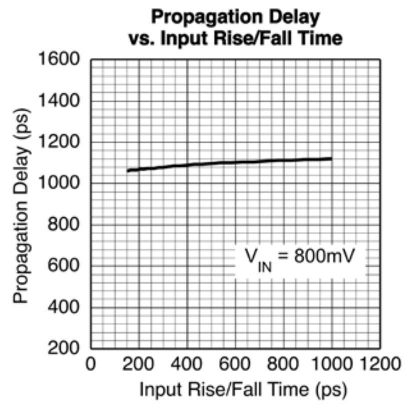
$V_{CC}$ = 3.3V, GND = 0V, $V_{IN}$ = 200mV, $t_r$ / $t_f$ ≤ 300ps, $R_L$ = 50Ω to $V_{CC}$–2V; $T_A$ = 25°C, unless otherwise stated.



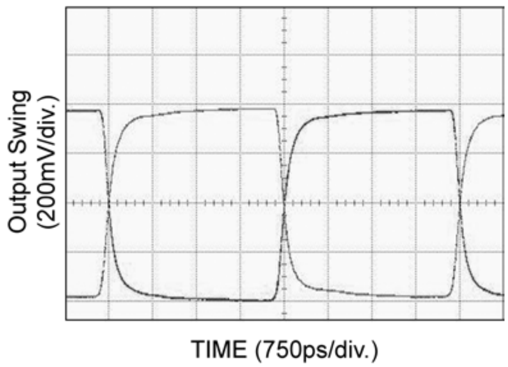



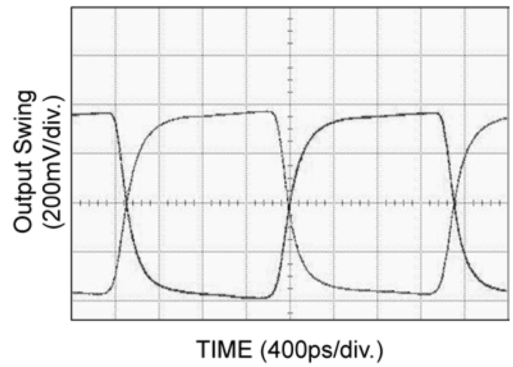
## Functional Characteristics

$V_{CC}$ = 3.3V, GND = 0V, $V_{IN}$ = 100mV, Q = Divide by 3, $t_r/t_f$ ≤ 300ps, $R_L$ = 50Ω to $V_{CC}$-2V; $T_A$ = 25°C, unless otherwise stated.

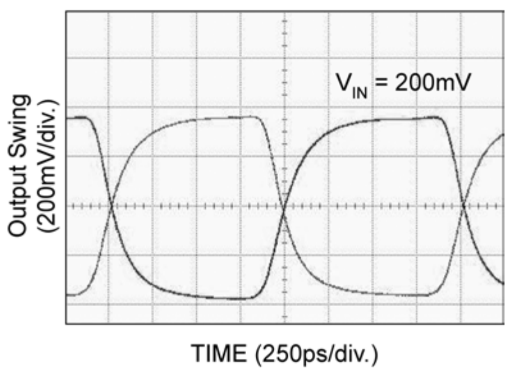
**500MHz Input Clock**




**1GHz Input Clock**




**1.5GHz Input Clock**



## Single-Ended and Differential Swings

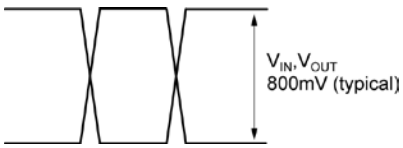



**Figure 2a. Single-Ended Voltage Swing**

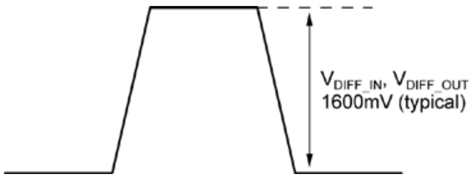



**Figure 2b. Differential Voltage Swing**

## Input and Output Stages

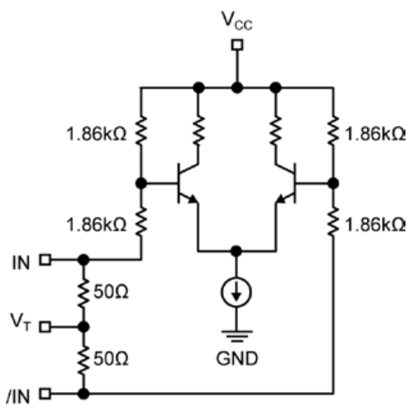



**Figure 3a. Simplified Differential Input Stage**

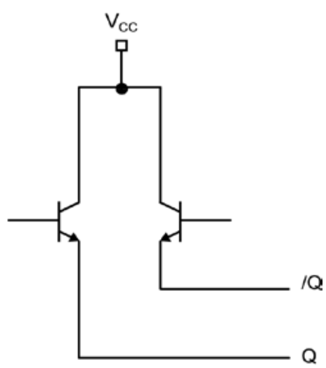



**Figure 3b. Simplified Differential Output Stage**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## Input Interface Applications

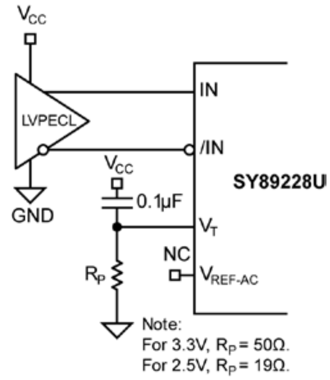



**Figure 4a. LVPECL Interface (DC-Coupled)**

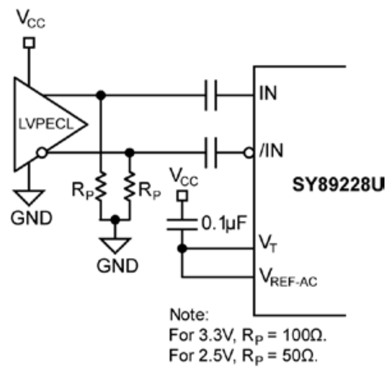
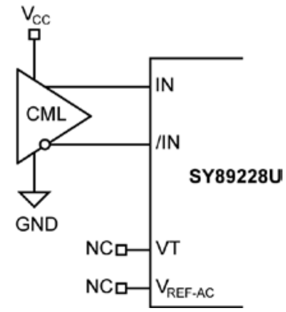



**Figure 4b. LVPECL Interface (AC-Coupled)**




**Option: may connect $V_T$ to $V_{CC}$**

**Figure 4c. CML Interface (DC-Coupled)**

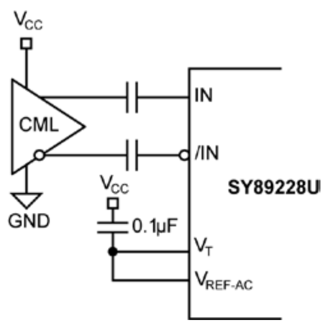



**Figure 4d. CML Interface (AC-Coupled)**

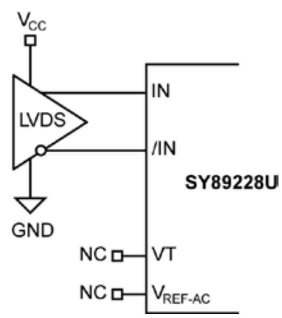



**Figure 4e. LVDS Interface (DC-Coupled)**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## PECL Output Interface Applications

PECL has high input impedance, very low output impedance (open emitter), and a small signal swing which results in low EMI. PECL is ideal for driving 50Ω- and 100Ω-controlled impedance transmission lines. There are several techniques for terminating the PECL output: parallel termination-thevenin equivalent, parallel termination (3-resistor), and AC-coupled termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.

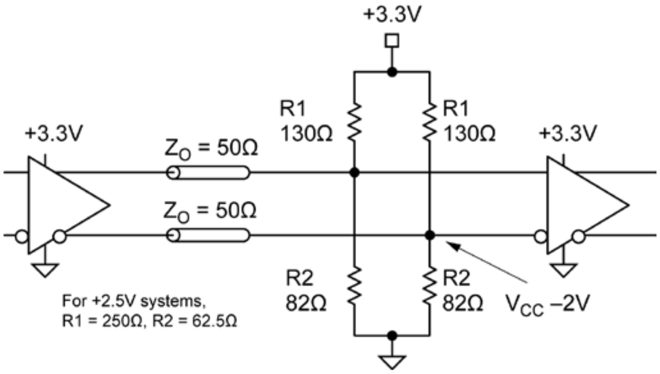
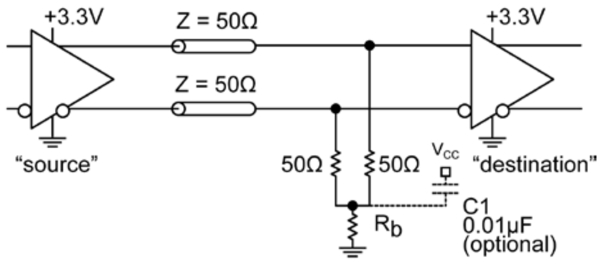



**Figure 5a. Parallel Termination-Thevenin Equivalent**



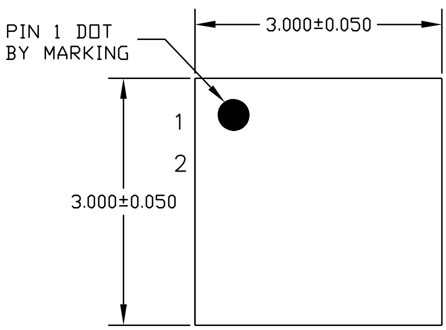

Notes:
1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. Rb resistor sets the DC bias voltage, equal to $V_{CC}$ – 2V.
4. For 2.5V systems, $R_b$ = 19Ω. For 3.3V systems, $R_b$ = 50Ω.

**Figure 5b. Parallel Termination (3-Resistor)**

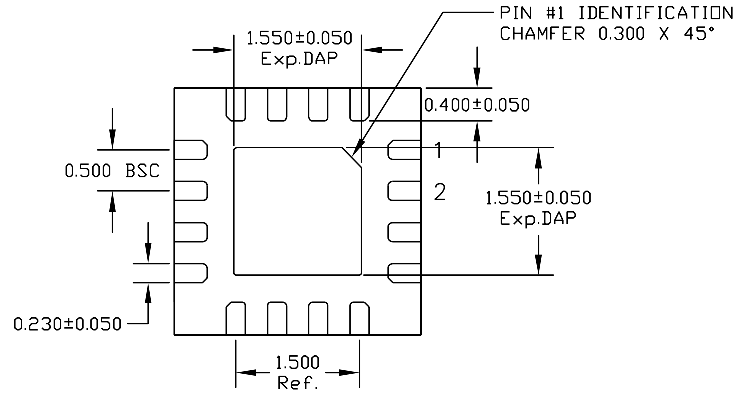
## Related Product and Support Documentation

| Part Number | Function | Datasheet Link |
|---|---|---|
| SY89229U | 1GHz Precision, LVDS ÷3, ÷5 Clock Divider with Fail Safe Input and Internal Termination | http://www.micrel.com/_PDF/HBW/sy89229u.pdf |
| SY89230U | 3.2GHz Precision, LVPECL ÷3, ÷5 Clock Divider | http://www.micrel.com/_PDF/HBW/sy89230u.pdf |
| SY89231U | 3.2GHz Precision, LVDS ÷3, ÷5 Clock Divider | http://www.micrel.com/_PDF/HBW/sy89231u.pdf |

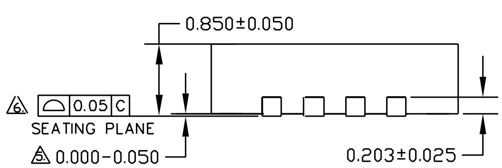
# Package Information




TOP VIEW




BOTTOM VIEW




SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. APPLIED ONLY FOR TERMINALS.
6. APPLIED FOR EXPOSED PAD AND TERMINALS.

**16-Pin QFN**

**Packages Notes:**

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packed before shipment.
3. Exposed pad must be soldered to a ground for proper thermal management.

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