

# UG150: Si5381/82-E-EVB User's Guide

The Si5381/82E-E-EB is used for evaluating the Ultra-Low Phase Noise Quad/Dual PLL. The Si5381/82 employs fourth-generation DSPLL technology to enable clock generation for LTE/ JESD204B applications which require the highest level of jitter performance. The Si5381/82E-E-EB has four independent input clocks and a total of 12 outputs with 4 PLLs. The Si5381/82E-E-EB also has four independent input clocks and a total of 12 outputs with 2 PLLs. The Si5381/82E-E-EB can be easily controlled and configured using Silicon Labs' Clock Builder Pro<sup>™</sup> (CBPro<sup>™</sup>) software tool.

The device revision is distinguished by a white 1 inch x 0.187 inch label with the text "Si5381/82E-E-EB" installed in the lower left hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)

#### EVB FEATURES

- Powered from USB port or external power supply
- Internal 48.0231 MHz crystal provides holdover mode of operation on the Si5381/82
- CBPro GUI programmable VDDO supplies allow each of the ten primary outputs to have its own supply voltage selectable from 3.3, 2.5, or 1.8 V
- CBPro GUI-controlled voltage, current, and power measurements of VDDA and all VDDO supplies
- Status LEDs for power supplies and control/status signals of Si5381/82
- SMA connectors for input clocks, output clocks and optional external timing reference clock



## 1. Si5381/82 Functional Block Diagram

Below is a functional block diagram of the Si5381/82E-E-EB. This EB can be connected to a PC via the main USB connector for programming, control, and monitoring. See 2. Quick Start and Jumper Defaults or 5.1 Installing ClockBuilderPro (CBPro) Desktop Software for more information.

**Note:** All Si5381/82 schematics, BOMs, User's Guides, and software can be found online at the following link: http://www.silabs.com/si538x-4x-evb

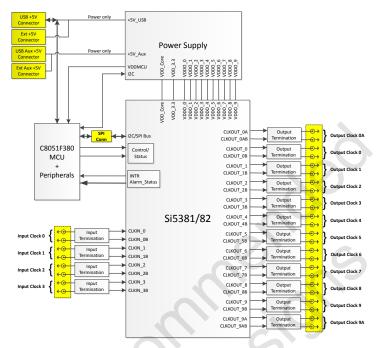


Figure 1.1. Functional Block Diagram of Si5381/82E-E-EB

# 2. Quick Start and Jumper Defaults

Perform the following steps to quick-start the ClockBuilderPro software.

- 1. Install ClockBuilderPro desktop software. http://www.silabs.com/CBPro
- 2. Connect a USB cable from the Si5381/82E-E-EB to the PC where the software was installed.
- 3. Leave the jumpers as installed from the factory, and launch the ClockBuilderPro software.
- 4. You can use ClockBuilderPro to create, download, and verify a frequency plan on the Si5381/82E-E-EB.
- 5. For the Si5381/82 data sheet, go to: http://www.silabs.com/si538x-4x-evb and search for Si5381/82 data sheet.

The following table lists the Si5381/82E-E-EB jumper defaults.

Table 2.1. Si5381/82E-E-EVB Jumper Defaults*	
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Location	Туре	I = Installed O = Open	Location	Туре	I = Installed O = Open
JP1	2 pin	0	JP23	2 pin	0
JP2	2 pin	0	JP24	3 pin	all open
JP3	2 pin	0	JP25	2 pin	0
JP4	2 pin	I	JP26	3 pin	all open
JP5	2 pin	0	JP27	2 pin	0
JP6	2 pin	0	JP28	3 pin	all open
JP7	2 pin	1	JP29	2 pin	0
JP8	2 pin	0	JP30	3 pin	all open
JP9	2 pin	0	JP31	2 pin	0
JP13	2 pin	0	JP33	2 pin	0
JP14	2 pin		JP34	3 pin	all open
JP15	3 pin	1 to 2	JP35	2 pin	0
JP16	3 pin	1 to 2	JP36	3 pin	all open
JP17	2 pin	0	JP39	2 pin	0
JP18	3 pin	all open	JP40	2 pin	0
JP19	2 pin	0	JP41	2 pin	0
JP20	3 pin	all open			
JP21	2 pin	0			
JP22	3 pin	all open	J36	5x2 Hdr	All 5 installed

## 3. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D11	INTRB	Blue	DUT Interrupt Active
D21	READY	Green	MCU Ready
D22	3P3V	Blue	DUT +3.3 V is present
D24	BUSY	Green	MCU Busy
D25	INTR	Red	MCU Interrupt active
D26	VDD DUT	Blue	DUT VDD voltage present
D27	5VUSBMAIN	Blue	Main USB +5 V present

### Table 3.1. Si5381/82E-E-EVB Status LEDs

D27, D22, and D26 are illuminated when USB +5 V, Si5381/82 +3.3 V, and Si5381/82 Output +5 V supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity. D11 and D12 are status indicators from the DUT.

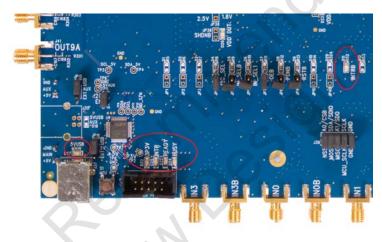
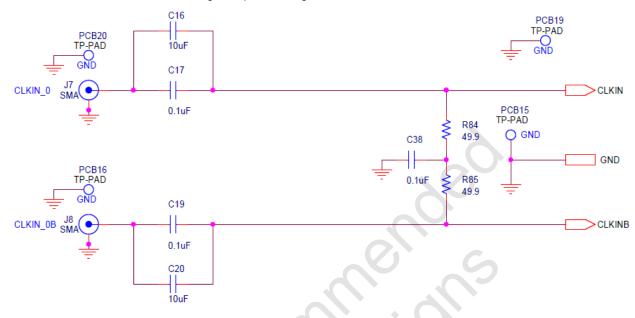


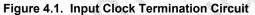
Figure 3.1. Status LEDs

## 4. Clock Input and Output Circuits

#### 4.1 Clock Input Circuits (INx/INxB and FB\_IN/FB\_INB)

The Si5381/82E-E-EB has eight SMA connectors (IN0/IN0B–IN2/IN2B and IN3(FB\_IN)/IN3B(FB\_INB)) for receiving external clock signals. All input clocks are terminated as shown in the figure below. Note input clocks are ac coupled and 50  $\Omega$  terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, refer to the Si5381/82 Data Sheet.





#### 4.2 Clock Output Circuits (OUTx/OUTxB)

Each of the twenty-four output drivers (12 differential pairs) is ac coupled to its respective SMA connector. The output clock termination circuit is shown in the figure below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5381/82E-E-EB provides pads for optional output termination resistors and/or low frequency capacitors. Note that components with schematic "NI" designation are not normally populated on the Si5381/82E-E-EB, and provide locations on the PCB for optional dc/ac terminations by the end user.

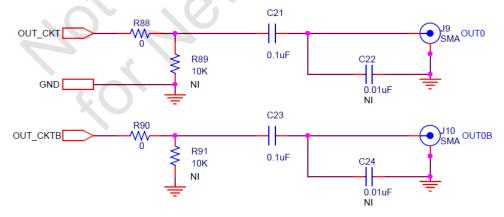


Figure 4.2. Output Clock Termination Circuit

## 5. Using the Si5381/82E-E-EVB and Installing ClockBuilderPro (CBPro) Desktop Software

#### 5.1 Installing ClockBuilderPro (CBPro) Desktop Software

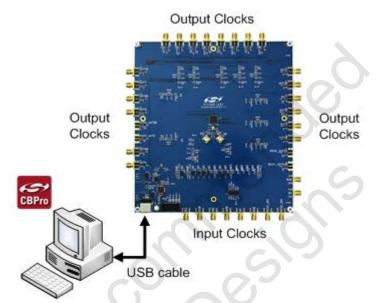
To install the CBPro software on any Windows 7 (or above) PC:

Go to http://www.silabs.com/cbpro and download the ClockBuilderPro software.

Installation instructions, release notes, and a user's guide for ClockBuilderPro can be found at the download link shown above. Please follow the instructions as indicated.

### 5.2 Connecting the EVB to Your Host PC

Once ClockBuilderPro software in installed, connect to the EVB with a USB cable as shown below.





#### 5.3 Additional Power Supplies

The Si5381/82E-E-EB comes preconfigured with jumpers installed on JP15 and JP16 (pins 1-2 in both cases) in order to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain +5 V power to all EVB power solely through the J37 USB connector. This setup is the default EVB configuration and is sufficient to configure the device and run multiple clock outputs simultaneously.

In some cases when enabling all outputs or at high output frequencies, the EVB requires more power than a single USB connection can provide. This may result in intermittent device behavior or undesired increases in jitter/phase-noise. This condition may be checked using the EVB GUI, which is described further below. Selecting the "**All Voltages**" tab of the GUI and clicking on the "**Read All**" button produces a display similar to this one:



Figure 5.2. EVB GUI - Power Supply Check

Verify that the "**RAIL\_5V**" measurement shows the EVB voltage > 4.7 V. An EVB voltage lower than this level may cause the issues described above.

In this case, J33 can be used to provide power to the output drivers separately from the main Si5381/82 device supplies. To make this change, move jumper JP15 to connect pins 2-3 "EXT". Connect J33 to an external 5 V, 0.5 A or higher power source. Make sure that the polarity of the +5 V and GND connections are correct. Verify that the RAIL\_5V voltage is 4.7 V or higher. The EVB should be powered by the USB connector when turning this auxiliary 5 V supply on or off.

See the figure below for the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.

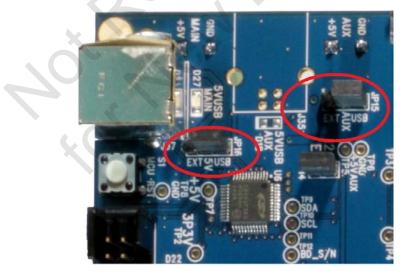


Figure 5.3. JP15-JP16 Standard Jumper Shunt Installation

#### 5.4 Overview of ClockBuilderPro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro.

The ClockBuilderPro installer will install two main applications.

#### Application 1:

ClockBuilder Pro	0		
Work With a Design	Quick Links		
Create New Design	Clock Generators & Jitter Attenuators Knowledge Base Custom Part Number Lookup ClockBuilder Go IOS App		
ex Open Sample Design	Applications Documentation		
Evaluation Board Detected SI5381 Rev D EVB Open Default Plan EVB GUE	10/40/2005 Line Card White Paper Clock Generators for Cloud Data Centers White Paper Optimizing SiS24x litter Performance App Note Selecting the Right Clocks for Timing Synchronization Applications App Note		
	ClockBuilder Pro Documentation		
	CBPto Overview CBPto Tools & Support for In-System Programming Includes walk-tooghas of hepenery-on-the-fly, full configuration, and partial configuration programming senarios. CILLISer's Guide Release Notes + Knowledge Base		
e.			



Use the CBPro Wizard to do the following:

- · Create a new design.
- Review or edit an existing design.
- · Export: Create in-system programming files.

#### **Application 2:**

Info DU	T SPI C	OUT Registe	er Editor	Regulators	All Voltage	s GPIO	Status Registers	
					Voltage	Current	Power	
	VDD	1.80V		On	1.781 V	311 mA	554 mW	Read
	VDDA	3.30V		On	3.305 V	132 mA	436 mW	Read
	VDDOD	2.50V		On	2.467 V	16 mA	39 mW	Read
1	VDDO1	2.50V		Dn	2.474 V	16 mA	40 mW	Read
	VDDO2	1.80V		Off	o v	0 mA	0 mW	Read
	VDDO3	2.50V		On	2.495 V	16 mA	40 mW	Read
	VDDO4	1.80V		Off	o v	0 mA	0 mW	Read
	VDDOS	1.80V		Off	0 V	0 mA	0 mW	Read
	VDDO6	2.50V		Dn	2.479 V	18 mA	45 mW	Read
	VDD07	2.50V		On	2.486 V	15 mA	37 mW	Read
	VDDO8	2.50V		On	2.490 V	15 mA	37 mW	Read
	VDDO9	2.50V		Dn	2.484 V	16 mA	40 mW	Read
All Out		Select V	oltage		Total	555 m/	1.268 W	Read

Figure 5.5. EVB GUI

Use the EVB GUI to do the following:

- Download configuration to EVB's DUT (Si5381/82).
- · Control the EVB's regulators.
- Monitor voltage, current, power on the EVB.

#### 5.5 Common ClockBuilderPro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5381/82E-E-EB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Silicon Labs-created Default Configuration
- · Workflow Scenario #2: Modifying the Default Silicon Labs-created Device Configuration
- Workflow Scenario #3: Testing a User-created Device Configuration

Each is described in more detail in the following sections.

#### 5.6 Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration

Verify that the PC and EVB are connected, then launch ClockBuilder Pro by clicking on this icon on your PC's desktop:



Figure 5.6. ClockBuilder Pro Icon

CBPro automatically detects the EVB and device type. When the EVB has been detected, click on the "Open Default Plan" button.

SILICON LABS	ClockBuilder Pro We Make Timing Simp
Work With a Desig	ŋn
Create New [	Design
🖶 Open Design	Project File
ex Open Sample	e Design
1111	Open Default Plan EVB GUI

Figure 5.7. CBPro-Open Default Plan Button

Once you open the default plan, a popup will appear.

0	Write Design	to EVB?		
U			h vour desian. W	ould you like to write
	your design to			
	· ·			
		Yes	No	

Figure 5.8. CBPro—Write Design Dialog

Select "Yes" to write the default plan to the Si5381/82 device mounted on your EVB. This ensures the device on the EVB is configured with the latest parameters from Silicon Labs.

Writing Si5381E D	esign to EVB		
Address 0x0305			

Figure 5.9. CBPro—Write Progress Window

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown in the figure below.

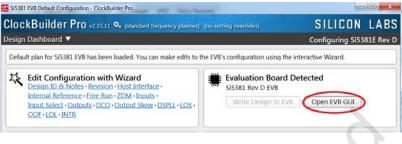


Figure 5.10. CBPro—Open EVB GUI Button

The EVB GUI window will appear on the desktop. Note all power supplies on the "Regulators" tab will be set to the values defined in the device's default CBPro project, as shown in the figure below.

	-	Voltage	Current	Power	
VDD	1.80V	1.781 V	311 mA	554 mW	Rea
VDDA	3.30V	3.305 V	132 mA	436 mW	Rea
VDDOO	2.50V	2.467 V	16 mA	39 mW	Rea
VDD01	2.50V	2.474 V	16 mA	40 mW	Rea
VDDO2	1.80V	n ov	0 mA	0 mW	Rea
VDDO3	2.50V	2.495 V	16 mA	40 mW	Rea
VDDO4	1.80V	r ov	0 mA	0 mW	Rea
VDDO5	1.80V	r ov	0 mA	0 mW	Rea
VDDOG	2.50V	2.479 V	18 mA	45 mW	Rea
VDD07	2.50V	2.486 V	15 mA	37 mW	Rea
VDDOS	2.50V On	2.490 V	15 mA	37 mW	Rea
VDDO9	2.50V 💽 On	2.484 V	16 mA	40 mW	Rea
All Output	- Select Voltage	Total	555 mA	1.268 W	Read
Supplies			are Design Esti		1.11

Figure 5.11. EVB GUI—Regulators

#### 5.6.1 Verify Free-Run Mode Operation

Assuming no external clocks have yet been connected to the INPUT CLOCK differential SMA connectors, labeled "INx/INxB" and located around the perimeter of the EVB, the DUT should now be operating in free-run mode and locked to the internal crystal.

You can run a quick check to determine if the device is powered up, generating output clocks, and consuming power by clicking on the "**Read All**" button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

**Note:** Turning  $V_{DD}$  or  $V_{DDA}$  "Off" will power-down and reset the DUT. Once both of these supplies are turned "On" again, you must reload the desired frequency plan back into the device memory by selecting the "**Write Design to EVB**" button on the CBPro home screen:

ClockBuilder Pro v2.15.11 🍫 (standard frequency planner)	(no setting overrides) SILICON LAB
Design Dashboard 🔻	Configuring Si5381E Rev
You have made edits to the EVB design. You can also save your new Design to Project File" link.	configuration to a project file for future use by clicking the "Save
Edit Configuration with Wizard Design ID & Notes - Revision - Host Interface -	: Evaluation Board Detected

Figure 5.12. CBPro—Write Design Button

Failure to do the step above will cause the device to read in the preprogrammed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks, running in free-run mode from the crystal, using external instrumentation connected to the output clock SMA connectors, labeled OUTx/OUTs. To verify plan inputs, go to the appropriate configuration page or click on "**Frequency Plan Valid**" to see the design report.

esign Dashboard 🔻	Configuring Si5381E Rev
You have made edits to the EVB design. You can also save your new co Design to Project File" link.	onfiguration to a project file for future use by clicking the "Save
Edit Configuration with Wizard Design ID & Notes - Revision - Host Interface - Internal Reference - Free Run - ZDM - Inputs - Input Select - Outputs - DCO - Output Skew - DSPLI - LOS - QOF - LOL - INTR	Evaluation Board Detected Si5381 Rev D EVB Write Design to EVB Open EVB GUI
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time.	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can viewe design report (text) of create a draft datasheet addendum (PDF) for your design.	Documentation Technical documentation is currently restricted for this product. Please contact your <u>Silicon Labs sales</u> representative to request access to documentation.
Silicon Labs Cloud Services You can create a custom part number for your design, which can be used to order factory pre-programmed devices. Or request a phase noise report for this design.	Ask for Help Have a question about your design? Click here to get assistance

Figure 5.13. CBPro—Design Report Button and Link

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

ign Report		
		 A
art:	SI5381E Rev D	mi l
	5381EVB1	13
reated By:	ClockBuilder Pro v2.15.11 [2017-07-14]	
imestamp:	2017-07-17 11:00:00 GMT-05:00	
esign Rule	Check	
	*****	
Errors:		
No errors		
Warnings:		
- No warnin	gs.	
	512	
Design		
and the section of the		
Host Interf		
	r Supply: VDD (Core)	
SPI Mode		
I2C Addr	ess Range: 104d to 107d / 0x68 to 0x6B (selected via A0/A1 pins)	
Internal Re	ference:	
	MHz [ 48 + 231/10000 MHz ] (XTAL - Crystal)	
	the territory and the territory	
Inputs:		
1NU: Un	used	
	.72 NHz [ 30 + 18/25 NHz ]	
	andard	
	PLL A, B, C, D	
IN2: Un		
IN3: Un		
Outputs:		
	5.52 MHz [ 155 + 13/25 MHz ]	
	abled, LVDS 2.5 V	
	PLL A	
OUT0: Un		
	6.25 MHz [ 156 + 1/4 MHz ]	
	100/64 1	
	abled, LVDS 2.5 V	
	PLL C	
		51/
OUT2: Un		

Figure 5.14. CBPro—Design Report

#### 5.6.2 Verify Locked Mode Operation

Now, assuming that you connect the input clocks to the EVB as shown in the Design Report above, the DUT on your EVB will be running in "locked" mode.

## 5.7 Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the configuration using the CBPro Wizard, click on the appropriate category. The category may also be selected from a dropdown list by clicking on the "**Design Dashboard**" button above this section.

ClockBuilder Pro v2.15.11 💁	SILICON LABS
Design Dashboard	Configuring Si5381E Rev I
You have made edits to the EVB design. You can also save your new cor Design to Project File" link.	figuration to a project file for future use by clicking the "Save
Edit Configuration with Wizard     Design JD. & Notes - Revision - Host Interface -     Internal Reference - Free Run - ZDM - Inputs -     Input Select - Quitputs - DCO - Output Skew - DSPLL - LOS -     OOF - LOL - INTR	Evaluation Board Detected Si5381 Rev D EVB Write Design to EVB Open EVB GUI
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time.	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a <u>design report (text)</u> or create a <u>draft datasheet addendum (PDP)</u> for your design.	Documentation Technical documentation is currently restricted for this product. Please contact your <u>Silicon Labs sales</u> representative to request access to documentation.
Silicon Labs Cloud Services You can create a custom part number for your design, which can be used to order factory pre-programmed devices. Or request a phase noise report for this design.	Ask for Help     Have a question about your design? Click here to get assistance.
Frequency Plan Valid 😡 Design OK 😗 Pd: 1.254 W, Tj: 97 °C	Home Close

Figure 5.15. CBPro—Edit Settings Links and Pulldown

You will now be taken to the Wizard's step-by-step menu pages to allow you to change any of the default plan's operating configurations.

	er Pro v2.15.11 🗞	SILICON L
tep 1 of 16 - De	esign ID & Notes	Configuring Si5381E
Design ID The device has 8 r	egisters, DESIGN_ID0 through DESIGN_ID7, that can be used to sto	re a design/configuration/revision identifier.
Design ID:	5381EVB1 (optional; max 8 characters)	
	The string you enter here is stored as ASCII bytes in registers DI	SIGN_ID0 through DESIGN_ID7.
Padding Mode:	NULL Padded If you do not enter the full 8 characters, the remaining byte character).	s of DESIGN_IDx will be padded with 0x00 bytes (aka NULL
	O Space Padded If you do not enter the full 8 characters, the remaining byte character).	s of DESIGN_IDx will be padded with 0x20 bytes (space
	u want here. The text is stored in your project file and included in d rord wrapped in reports, you can use newlines to start a new parag	
Enter anything you		

Figure 5.16. CBPro—Design ID and Notes Edit Page

As you edit the settings, you may notice the "Frequency Plan Valid" link in the lower left corner updating. You can click on this link to bring up the design report to confirm that the information is correct. When you are finished editing each page, you may click on the "> Next" or "< Back" buttons to move from page to page. When you are done making all your desired changes, you can click on "Write to EVB" to reconfigure your device. The Design Write status window will appear each time you write to the EVB.

	riting Si5381E Design to EVB	
ress 0v0305	ddress 0x0305	

Figure 5.17. CBPro—Design Write Progress Window

When you have verified your design settings, you may save the design project. Click on the "**Finish**" button to return to the home page and then click on the "**Save Design to Project File**" link. You can use the windows file browser to reach the correct location and enter a filename for this new project.

#### 5.8 Workflow Scenario #3: Testing a User-Created Device Configuration

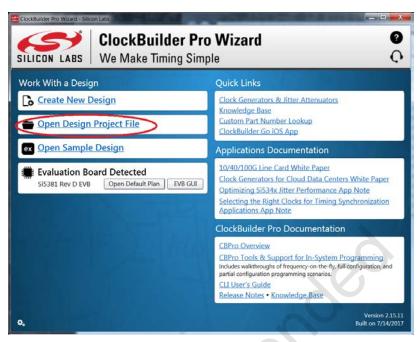


Figure 5.18. CBPro—Open Design Project Link

Using the windows file browser popup, locate your CBPro design file (\*.slabtimeproj or \*.sitproj file).

Organize   New folder		*
Favorites E Desktop	Network System Folder	
Downloads     Dropbox (Silicon Labs)     Recent Places	EVB - Shortcut Shortcut 1.79 KB	
Calibraries	nashasho - Shortcut Shortcut	
3 Documents 4 Music	■ 1.70 KB Si538x-4x	
E Videos	Shortcut 184 KB	
Computer	SIS381E-RevO-Project Silicon Labs Timing Project File 12.1 KB	
File name: \$i5381E-R	vD-Project Silicon Labs Timing	Proje

Figure 5.19. CBPro—Windows File Browser

Select "Yes" when the WRITE DESIGN to EVB popup appears:

141.14-	Design to E	100			
			h your design	Would we	u like to write
	esian to the E		n your design	would ye	A like to little
6					

Figure 5.20. CBPro—Write Design Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

#### 5.9 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting "Export" as shown below:



Figure 5.21. CBPro—Export Design Programming File

You can now write your device's complete configuration to file formats suitable for in-system programming.

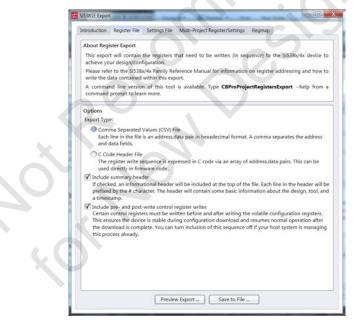


Figure 5.22. CBPro—Export Configuration Window

## 6. Writing A New Frequency Plan or Device Configuration to Non-volatile Memory (OTP)

The Si5381/82 device loads the Non-Volatile Memory (OTP) on either a powerup or a hard reset, overwriting any previous volatile register changes. This allows the device to begin functioning as desired on powerup/hard-reset without manual intervention. To restart the device while preserving volatile changes and without loading the OTP, use soft-reset through the registers or EVB-GUI.

**Note:** Writing to the device non-volatile memory (OTP) is NOT the same as writing a configuration into the Si5381/82 using ClockBuilderPro on the Si5381/82E-E-EB. Writing a configuration into the EVB from ClockBuilderPro is done using Si5381/82 RAM space and can be done virtually an unlimited number of times. Writing to OTP is limited as described below.

Refer to the Si5381/82 Family Reference Manual and device datasheet for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

Not New Design

## 7. Serial Device Communications (Si5381/82 <-> MCU)

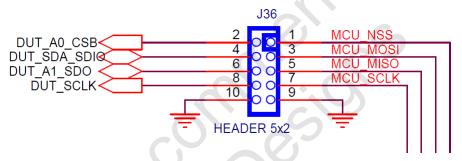
#### 7.1 Onboard SPI Support

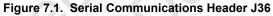
The MCU on-board the Si5381/82E-E-EB communicates with the Si5381/82 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5381/82 device is the SPI slave. The Si5381/82 device can also support a 2-wire I<sup>2</sup>C serial interface, although the Si5381/82E-E-EB does NOT support the I<sup>2</sup>C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I<sup>2</sup>C.

## 7.2 External I<sup>2</sup>C Support

I<sup>2</sup>C can be supported if driven from an external I<sup>2</sup>C controller. The serial interface signals between the MCU and Si5381/82 pass through shunts loaded on header J36. These jumper shunts must be installed in J36 for normal EVB operation using SPI with CBPro. If testing of I<sup>2</sup>C operation via external controller is desired, the shunts in J36 can be removed thereby isolating the on-board MCU from the Si5381/82 device. The shunt at J4 (I2C\_SEL) must also be removed to select I<sup>2</sup>C as Si5381/82 interface type. An external I<sup>2</sup>C controller connected to the Si5381/82 side of J36 can then communicate to the Si5381/82 device. (For more information on I<sup>2</sup>C signal protocol, refer to the Si5381/82 Data Sheet.)

The figure below illustrates the J36 header schematic. J36 even numbered pins (2, 4, 6, etc.) connect to the Si5381/82 device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J36 and J4,  $I^2C$  operation should use J36 pin 4 (DUT\_SDA\_SDIO) as the  $I^2C$  SDA and J36 pin 8 (DUT\_SCLK) as the  $I^2C$  SCLK. Please note the external  $I^2C$  controller will need to supply its own  $I^2C$  signal pull-up resistors.



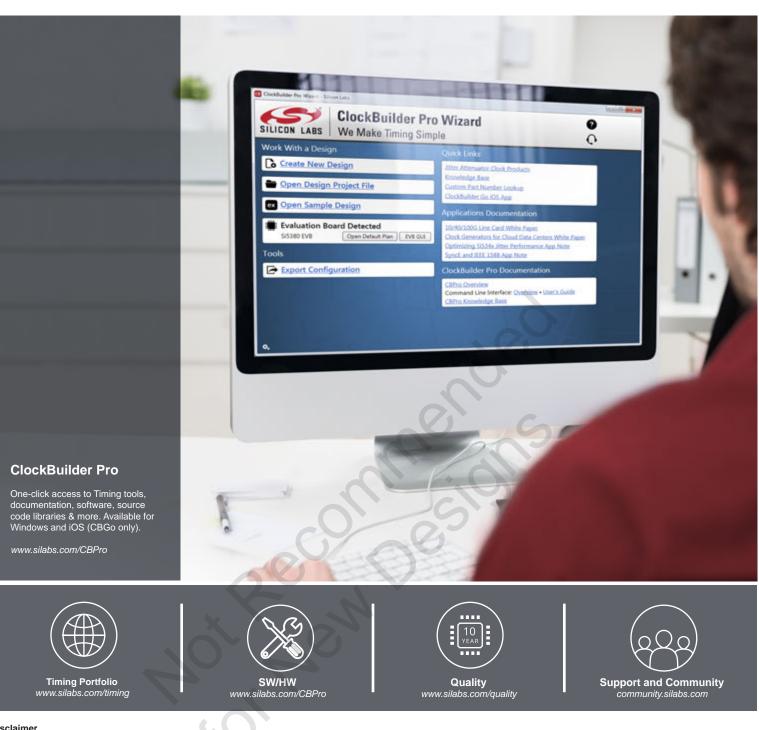


## 8. Si5381/82-E-EB Schematic and Bill of Materials (BOM)

The Si5381/82-E-EB Schematic and Bill of Materials (BOM) can be found online at: http://www.silabs.com/si538x-4x-evb

Note: Please be aware the Si5381/82-E-EB schematic is in OrCad Capture *hierarchical format* and not in a typical "flat" schematic format.

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