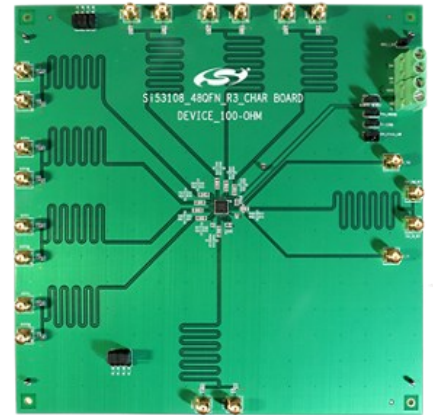


Si53108 PCI Express Zero-Delay/Fanout Buffer Evaluation Kit

Si53108-EK

Evaluation boards are available for [PCIe clock generators](#), [clock buffers](#), and [zero-delay buffers](#). The EVB allows you to measure jitter performance, power consumption, and signal integrity. The boards feature SMA connectors for robust low jitter signal integrity measurements.

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Features

Each evaluation kit includes one evaluation board and is designed to verify:

- Performance and compliancy of PCI Express
- Measure device power consumption
- Connect to prototype systems that have SMA connectors, supporting robust, low jitter signal integrity measurements for system validation
- Output enable (OE) pins for power management
- Spread spectrum control pins for easy EMI control
- Tweaks, verify, and understand I²C edge rate and skew controls for PCIe clocks

Additional Resources

Si53108-EVB User's Guide

[Read Now](#) ↗

Si53108 Data Sheet

[Read Now](#) ↗

AN871: Driving Long PCIe Clock Lines

[Read Now](#) ↗

AN874: Cascading Two Si53112 Buffers

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