

# NXB0108

Dual supply translating transceiver; auto direction sensing;  
3-state

Rev. 2 — 3 November 2021

Product data sheet

## 1. General description

The NXB0108 is an 8-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 8-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ( $V_{CC(A)}$  and  $V_{CC(B)}$ ).  $V_{CC(A)}$  can be supplied at any voltage between 1.2 V and 3.6 V and  $V_{CC(B)}$  can be supplied at any voltage between 1.65 V and 5.5 V, making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V).

Pins An and OE are referenced to  $V_{CC(A)}$  and pins Bn are referenced to  $V_{CC(B)}$ . A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$ : 1.2 V to 3.6 V and  $V_{CC(B)}$ : 1.65 V to 5.5 V
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
  - HBM: ANSI/ESDA/Jedec JS-001 Class 2 exceeds 2500 V for A port
  - HBM: ANSI/ESDA/Jedec JS-001 Class 3B exceeds 15000 V for B port
  - CDM: ANSI/ESDA/Jedec JS-002 Class C3 exceeds 1500 V
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NXB0108PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
NXB0108BQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body $2.5 \times 4.5 \times 0.85$ mm	SOT764-1

### 4. Functional diagram

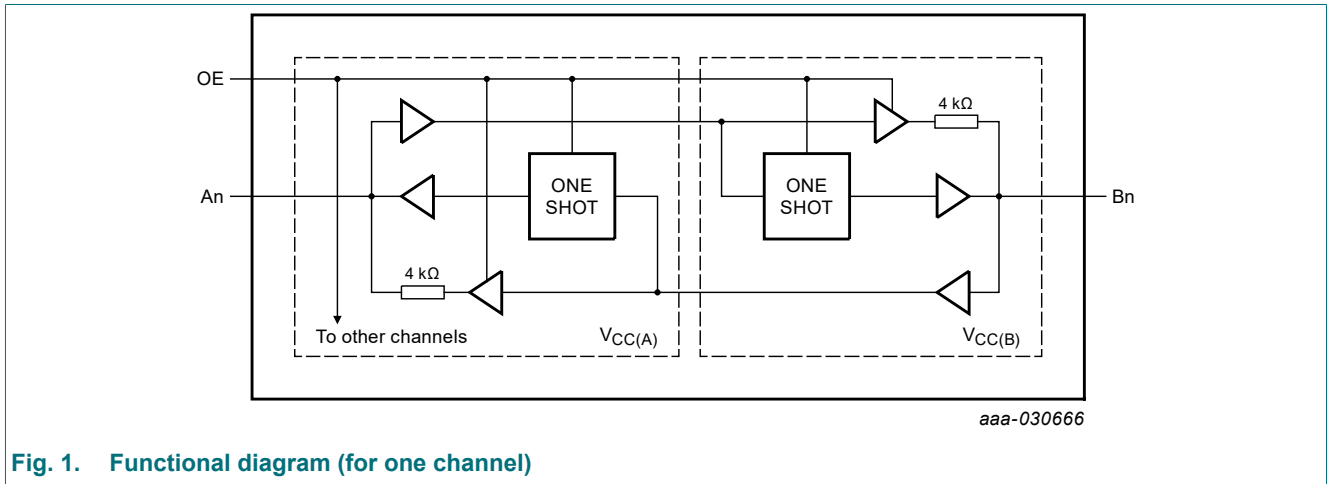


Fig. 1. Functional diagram (for one channel)

### 5. Pinning information

#### 5.1. Pinning

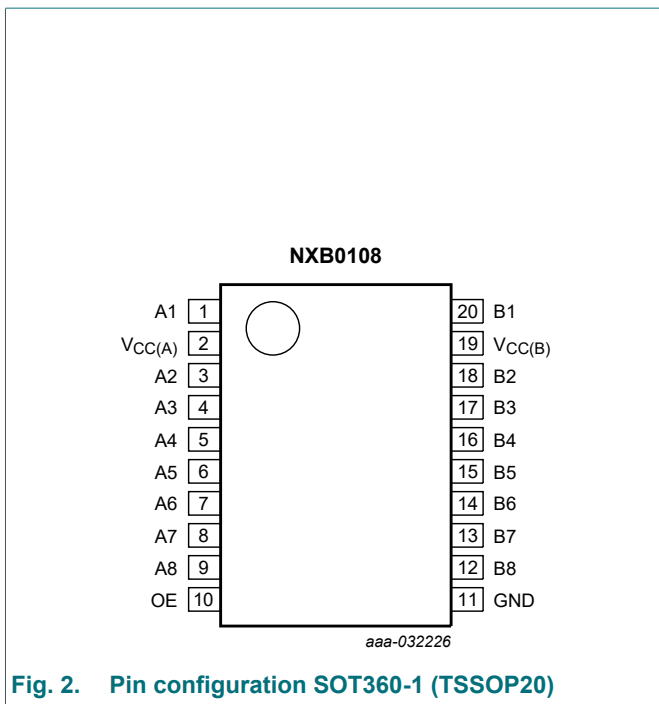


Fig. 2. Pin configuration SOT360-1 (TSSOP20)

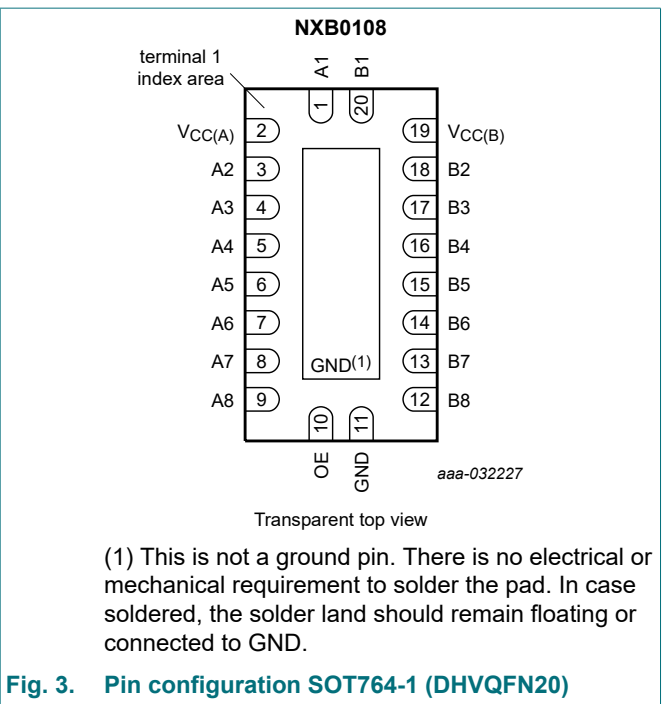


Fig. 3. Pin configuration SOT764-1 (DHVQFN20)

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A1, A2, A3, A4, A5, A6, A7, A8	1, 3, 4, 5, 6, 7, 8, 9	data input or output (referenced to $V_{CC(A)}$ )
$V_{CC(A)}$	2	supply voltage A
OE	10	output enable input (active HIGH; referenced to $V_{CC(A)}$ )
GND	11	ground (0 V)
B1, B2, B3, B4, B5, B6, B7, B8	20, 18, 17, 16, 15, 14, 13, 12	data input or output (referenced to $V_{CC(B)}$ )
$V_{CC(B)}$	19	supply voltage B

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage		Input	Input/output	
$V_{CC(A)}$	$V_{CC(B)}$	OE	An	Bn
1.2 V to $V_{CC(B)}$	1.65 V to 5.5 V	L	Z	Z
1.2 V to $V_{CC(B)}$	1.65 V to 5.5 V	H	input or output	output or input
GND[1]	GND[1]	X	Z	Z

[1] When either  $V_{CC(A)}$  or  $V_{CC(B)}$  is at GND level, the device goes into power-down mode.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	+6.5	V
$V_I$	input voltage		-0.5	+6.5	V
$V_O$	output voltage	Active mode	-0.5	$V_{CCO} + 0.5$	V
		Power-down or 3-state mode	-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	$V_O = 0$ V to $V_{CCO}$	-	±50	mA
$I_{CC}$	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	-	500	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{CCO}$  is the supply voltage associated with the output.

[3]  $V_{CCO} + 0.5$  V should not exceed 6.5 V.

[4] For SOT360-1 (TSSOP20) package:  $P_{tot}$  derates linearly with 10.0 mW/K above 100 °C.  
For SOT764-1 (DHVQFN20) package:  $P_{tot}$  derates linearly with 12.9 mW/K above 111 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions [1] [2]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.2	3.6	V
$V_{CC(B)}$	supply voltage B		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	Power-down or 3-state mode; $V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$			
		A port	0	3.6	V
		B port	0	5.5	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	40	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at  $V_{CCI}$  or both at GND.

[2]  $V_{CC(A)}$  must be less than or equal to  $V_{CC(B)}$ .

## 9. Static characteristics

Table 6. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ °C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH}$	HIGH-level output voltage	A port; $V_{CC(A)} = 1.2\text{ V}; I_O = -20\text{ }\mu\text{A}$	-	1.1	-	V
$V_{OL}$	LOW-level output voltage	A port; $V_{CC(A)} = 1.2\text{ V}; I_O = 20\text{ }\mu\text{A}$	-	0.09	-	V
$I_I$	input leakage current	OE input; $V_I = 0\text{ V to }3.6\text{ V}; V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0\text{ V to }V_{CCO}; V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	[1]	-	$\pm 1$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0\text{ V to }3.6\text{ V}; V_{CC(A)} = 0\text{ V};$ $V_{CC(B)} = 0\text{ V to }5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
		B port; $V_I$ or $V_O = 0\text{ V to }5.5\text{ V}; V_{CC(B)} = 0\text{ V};$ $V_{CC(A)} = 0\text{ V to }3.6\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	OE input; $V_{CC(A)} = 1.2\text{ V to }3.6\text{ V}; V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	5	-	pF
$C_{I/O}$	input/output capacitance	A port; $V_{CC(A)} = 1.2\text{ V to }3.6\text{ V}; V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	5	-	pF
		B port; $V_{CC(A)} = 1.2\text{ V to }3.6\text{ V}; V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	8	-	pF

[1]  $V_{CCO}$  is the supply voltage associated with the output.

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Table 7. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

$V_{CC(A)}$	$V_{CC(B)}$								Unit
	1.8 V		2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.2 V	10	10	10	10	10	20	10	1050	nA
1.5 V	10	10	10	10	10	10	10	650	nA
1.8 V	10	10	10	10	10	10	10	350	nA
2.5 V	-	-	10	10	10	10	10	40	nA
3.3 V	-	-	-	-	10	10	10	10	nA

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	A or B port and OE input [1]					
		$V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
$V_{IL}$	LOW-level input voltage	A or B port and OE input [1]					
		$V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	$0.35V_{CCI}$	-	$0.35V_{CCI}$	V
$V_{OH}$	HIGH-level output voltage	A or B port; $I_O = -20\text{ }\mu\text{A}$ [2]					
		A port; $V_{CC(A)} = 1.4\text{ V to }3.6\text{ V}$	$V_{CCO} - 0.4$	-	$V_{CCO} - 0.4$	-	V
		B port; $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	$V_{CCO} - 0.4$	-	$V_{CCO} - 0.4$	-	V
$V_{OL}$	LOW-level output voltage	A or B port; $I_O = 20\text{ }\mu\text{A}$ [2]					
		A port; $V_{CC(A)} = 1.4\text{ V to }3.6\text{ V}$	-	0.4	-	0.4	V
		B port; $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	0.4	-	0.4	V
$I_I$	input leakage current	OE input; $V_I = 0\text{ V to }3.6\text{ V};$ $V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	$\pm 2$	-	$\pm 5$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0\text{ V or }V_{CCO};$ [2] $V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	$\pm 2$	-	$\pm 10$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0\text{ V to }3.6\text{ V};$ $V_{CC(A)} = 0\text{ V}; V_{CC(B)} = 0\text{ V to }5.5\text{ V}$	-	$\pm 2$	-	$\pm 10$	$\mu\text{A}$
		B port; $V_I$ or $V_O = 0\text{ V to }5.5\text{ V};$ $V_{CC(B)} = 0\text{ V}; V_{CC(A)} = 0\text{ V to }3.6\text{ V}$	-	$\pm 2$	-	$\pm 10$	$\mu\text{A}$

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Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>CC</sub>	supply current	V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A [1]					
		I <sub>CC(A)</sub>					
		OE = LOW; V <sub>CC(A)</sub> = 1.4 V to 3.6 V; V <sub>CC(B)</sub> = 1.65 V to 5.5 V	-	5	-	15	μA
		OE = HIGH; V <sub>CC(A)</sub> = 1.4 V to 3.6 V; V <sub>CC(B)</sub> = 1.65 V to 5.5 V	-	5	-	20	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	2	-	15	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 5.5 V	-	-2	-	-15	μA
		I <sub>CC(B)</sub>					
		OE = LOW; V <sub>CC(A)</sub> = 1.4 V to 3.6 V; V <sub>CC(B)</sub> = 1.65 V to 5.5 V	-	5	-	20	μA
		OE = HIGH; V <sub>CC(A)</sub> = 1.4 V to 3.6 V; V <sub>CC(B)</sub> = 1.65 V to 5.5 V	-	13	-	65	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	-2	-	-15	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 5.5 V	-	2	-	15	μA
		I <sub>CC(A)</sub> + I <sub>CC(B)</sub>					
		V <sub>CC(A)</sub> = 1.4 V to 3.6 V; V <sub>CC(B)</sub> = 1.65 V to 5.5 V	-	15	-	70	μA

[1] V<sub>CCI</sub> is the supply voltage associated with the input.

[2] V<sub>CCO</sub> is the supply voltage associated with the output.

## 10. Dynamic characteristics

**Table 9. Typical dynamic characteristics for temperature 25 °C [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6; for waveforms see Fig. 4 and Fig. 5.

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>				Unit
			1.8 V	2.5 V	3.3 V	5.0 V	
<b>V<sub>CC(A)</sub> = 1.2 V; T<sub>amb</sub> = 25 °C</b>							
t <sub>pd</sub>	propagation delay	A to B	6.9	5.6	5.1	4.9	ns
		B to A	7.1	5.8	5.0	5.1	ns
t <sub>en</sub>	enable time	OE to A, B	500	500	500	500	ns
t <sub>dis</sub>	disable time	OE to A; no external load [2]	14.5	14.5	14.5	14.5	ns
		OE to B; no external load [2]	12.2	10.1	9.3	8.7	ns
		OE to A; see Fig. 5	87	87	87	87	ns
		OE to B; see Fig. 5	98	71	101	68	ns
t <sub>t</sub>	transition time	A port	4.2	4.2	4.2	4.2	ns
		B port	2.7	2.0	1.7	1.5	ns
t <sub>sk(o)</sub>	output skew time	between channels [3]	1.4	0.7	0.6	0.5	ns
t <sub>W</sub>	pulse width	data inputs	13	13	13	13	ns
f <sub>data</sub>	data rate		60	60	60	60	Mbps

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.

[2] These values are guaranteed by design.

[3] Skew between any two outputs of the same package switching in the same direction.

**Table 10. Dynamic characteristics for temperature range -40 °C to +85 °C [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6; for waveforms see Fig. 4 and Fig. 5.

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 1.5 V ± 0.1 V</b>											
t <sub>pd</sub>	propagation delay	A to B	1.4	11.4	1.2	8.0	1.1	6.7	0.8	6.2	ns
		B to A	0.9	10.8	0.7	8.3	0.4	7.8	0.3	7.2	ns
t <sub>en</sub>	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	µs
t <sub>dis</sub>	disable time	OE to A; no external load [2]	3.7	18.0	3.7	18.0	3.7	18.0	3.7	18.0	ns
		OE to B; no external load [2]	3.7	19.5	3.5	15.0	3.0	13.0	1.7	11.5	ns
		OE to A; see Fig. 5	-	100	-	100	-	100	-	100	ns
		OE to B; see Fig. 5	-	150	-	105	-	150	-	105	ns
t <sub>t</sub>	transition time	A port	0.8	6.5	0.8	6.3	0.8	6.3	0.8	6.3	ns
		B port	1.0	7.3	0.7	4.9	0.7	4.6	0.6	4.6	ns
t <sub>sk(o)</sub>	output skew time	between channels [3]	-	2.6	-	1.9	-	1.6	-	1.3	ns
t <sub>W</sub>	pulse width	data inputs	20	-	20	-	20	-	20	-	ns
f <sub>data</sub>	data rate		-	50	-	50	-	50	-	50	Mbps

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Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			$1.8\text{ V} \pm 0.15\text{ V}$		$2.5\text{ V} \pm 0.2\text{ V}$		$3.3\text{ V} \pm 0.3\text{ V}$		$5.0\text{ V} \pm 0.5\text{ V}$		
			Min	Max	Min	Max	Min	Max	Min	Max	
<b><math>V_{CC(A)} = 1.8\text{ V} \pm 0.15\text{ V}</math></b>											
$t_{pd}$	propagation delay	A to B	1.6	10.8	1.4	7.9	1.3	6.2	1.2	5.3	ns
		B to A	1.5	9.2	1.3	7.2	0.8	6.3	0.5	5.8	ns
$t_{en}$	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	$\mu\text{s}$
$t_{dis}$	disable time	OE to A; no external load [2]	2.9	13.0	2.9	13.0	2.9	13.0	2.9	13.0	ns
		OE to B; no external load [2]	4.0	18.0	3.0	13.0	2.5	11.5	1.5	9.5	ns
		OE to A; see Fig. 5	-	120	-	120	-	120	-	120	ns
		OE to B; see Fig. 5	-	150	-	105	-	150	-	105	ns
$t_t$	transition time	A port	0.7	5.1	0.7	5.0	1.0	5.0	0.7	5.0	ns
		B port	1.0	7.3	0.7	5.0	0.7	3.9	0.6	3.8	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	0.8	-	0.7	-	0.6	-	0.6	ns
$t_W$	pulse width	data inputs	19	-	17	-	17	-	17	-	ns
$f_{data}$	data rate		-	52	-	60	-	60	-	60	Mbps
<b><math>V_{CC(A)} = 2.5\text{ V} \pm 0.2\text{ V}</math></b>											
$t_{pd}$	propagation delay	A to B	-	-	1.1	7.5	1.0	5.2	0.9	4.2	ns
		B to A	-	-	1.0	5.6	0.6	5.0	0.3	4.2	ns
$t_{en}$	enable time	OE to A, B	-	-	-	1.0	-	1.0	-	1.0	$\mu\text{s}$
$t_{dis}$	disable time	OE to A; no external load [2]	-	-	2.5	8.0	2.5	8.0	2.5	8.0	ns
		OE to B; no external load [2]	-	-	2.0	11.5	2.8	9.5	1.2	8.0	ns
		OE to A; see Fig. 5	-	-	-	85	-	85	-	85	ns
		OE to B; see Fig. 5	-	-	-	105	-	150	-	100	ns
$t_t$	transition time	A port	-	-	0.8	3.6	0.6	3.6	0.5	3.5	ns
		B port	-	-	0.6	4.9	0.7	3.9	0.6	3.2	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	0.4	-	0.3	-	0.3	ns
$t_W$	pulse width	data inputs	-	-	13	-	10	-	10	-	ns
$f_{data}$	data rate		-	-	-	80	-	100	-	100	Mbps



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Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V $\pm$ 0.15 V		2.5 V $\pm$ 0.2 V		3.3 V $\pm$ 0.3 V		5.0 V $\pm$ 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)} = 3.3 \text{ V} \pm 0.3 \text{ V}$											
$t_{pd}$	propagation delay	A to B	-	-	-	-	0.9	4.8	0.8	3.9	ns
		B to A	-	-	-	-	0.5	4.3	0.2	3.7	ns
$t_{en}$	enable time	OE to A, B	-	-	-	-	-	1.0	-	1.0	$\mu\text{s}$
$t_{dis}$	disable time	OE to A; no external load [2]	-	-	-	-	2.1	6.5	2.0	6.5	ns
		OE to B; no external load [2]	-	-	-	-	1.0	8.5	1.7	7.0	ns
		OE to A; see Fig. 5	-	-	-	-	-	125	-	125	ns
		OE to B; see Fig. 5	-	-	-	-	-	150	-	100	ns
$t_t$	transition time	A port	-	-	-	-	0.5	3.0	0.5	3.0	ns
		B port	-	-	-	-	0.7	3.9	0.6	3.2	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	-	-	0.4	-	0.3	ns
$t_W$	pulse width	data inputs	-	-	-	-	9.0	-	9.0	-	ns
$f_{data}$	data rate		-	-	-	-	-	110	-	110	Mbps

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

$t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

$t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

$t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[2] These values are guaranteed by design.

[3] Skew between any two outputs of the same package switching in the same direction.

**Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6; for waveforms see Fig. 4 and Fig. 5.

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V $\pm$ 0.15 V		2.5 V $\pm$ 0.2 V		3.3 V $\pm$ 0.3 V		5.0 V $\pm$ 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)} = 1.5 \text{ V} \pm 0.1 \text{ V}$											
$t_{pd}$	propagation delay	A to B	1.4	11.9	1.2	9.0	1.1	7.3	0.8	6.5	ns
		B to A	0.9	10.9	0.7	8.8	0.4	7.9	0.3	7.7	ns
$t_{en}$	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	$\mu\text{s}$
$t_{dis}$	disable time	OE to A; no external load [2]	3.7	19.0	3.7	19.0	3.7	19.0	3.7	19.0	ns
		OE to B; no external load [2]	3.7	22.0	3.5	16.0	3.0	14.0	1.7	12.5	ns
		OE to A; see Fig. 5	-	105	-	105	-	105	-	105	ns
		OE to B; see Fig. 5	-	155	-	110	-	155	-	105	ns
$t_t$	transition time	A port	0.8	8.1	0.8	7.9	0.8	7.9	0.8	7.9	ns
		B port	1.0	9.1	0.7	6.1	0.7	5.8	0.6	5.8	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	2.6	-	1.9	-	1.6	-	1.3	ns
$t_W$	pulse width	data inputs	25	-	25	-	25	-	25	-	ns
$f_{data}$	data rate		-	40	-	40	-	40	-	40	Mbps

## Dual supply translating transceiver; auto direction sensing; 3-state

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			$1.8\text{ V} \pm 0.15\text{ V}$		$2.5\text{ V} \pm 0.2\text{ V}$		$3.3\text{ V} \pm 0.3\text{ V}$		$5.0\text{ V} \pm 0.5\text{ V}$		
			Min	Max	Min	Max	Min	Max	Min	Max	
<b><math>V_{CC(A)} = 1.8\text{ V} \pm 0.15\text{ V}</math></b>											
$t_{pd}$	propagation delay	A to B	1.6	11.1	1.4	8.1	1.3	6.5	1.2	5.5	ns
		B to A	1.5	9.6	1.2	7.8	0.8	6.6	0.5	6.3	ns
$t_{en}$	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	$\mu\text{s}$
$t_{dis}$	disable time	OE to A; no external load [2]	2.9	14.0	2.9	14.0	2.9	14.0	2.9	14.0	ns
		OE to B; no external load [2]	4.0	20.5	3.0	14.5	2.5	12.5	1.5	10.5	ns
		OE to A; see Fig. 5	-	125	-	125	-	125	-	125	ns
		OE to B; see Fig. 5	-	150	-	105	-	150	-	105	ns
$t_t$	transition time	A port	0.8	6.4	0.7	6.3	1.0	6.3	0.7	6.3	ns
		B port	1.0	9.1	0.7	6.3	0.7	4.9	0.6	4.8	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	0.8	-	0.7	-	0.6	-	0.6	ns
$t_W$	pulse width	data inputs	22	-	18	-	18	-	18	-	ns
$f_{data}$	data rate		-	45	-	55	-	55	-	55	Mbps
<b><math>V_{CC(A)} = 2.5\text{ V} \pm 0.2\text{ V}</math></b>											
$t_{pd}$	propagation delay	A to B	-	-	1.1	7.6	1.0	5.8	0.9	4.4	ns
		B to A	-	-	1.0	7.1	0.6	5.1	0.3	4.8	ns
$t_{en}$	enable time	OE to A, B	-	-	-	1.0	-	1.0	-	1.0	$\mu\text{s}$
$t_{dis}$	disable time	OE to A; no external load [2]	-	-	2.5	9.0	2.5	9.0	2.5	9.0	ns
		OE to B; no external load [2]	-	-	2.0	13.0	2.8	10.5	1.2	8.5	ns
		OE to A; see Fig. 5	-	-	-	85	-	85	-	85	ns
		OE to B; see Fig. 5	-	-	-	105	-	150	-	100	ns
$t_t$	transition time	A port	-	-	0.8	4.5	0.6	4.5	0.5	4.4	ns
		B port	-	-	0.6	6.1	0.7	4.9	0.6	4.0	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	0.4	-	0.3	-	0.3	ns
$t_W$	pulse width	data inputs	-	-	13	-	13	-	13	-	ns
$f_{data}$	data rate		-	-	-	75	-	80	-	80	Mbps

Dual supply translating transceiver; auto direction sensing; 3-state

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 3.3 V ± 0.3 V</b>											
t <sub>pd</sub>	propagation delay	A to B	-	-	-	-	0.9	5.3	0.8	4.2	ns
		B to A	-	-	-	-	0.5	4.4	0.2	4.0	ns
t <sub>en</sub>	enable time	OE to A, B	-	-	-	-	-	1.0	-	1.0	µs
t <sub>dis</sub>	disable time	OE to A; no external load [2]	-	-	-	-	2.1	7.0	2.0	7.0	ns
		OE to B; no external load [2]	-	-	-	-	1.0	9.5	1.7	7.5	ns
		OE to A; see Fig. 5	-	-	-	-	-	125	-	125	ns
		OE to B; see Fig. 5	-	-	-	-	-	150	-	100	ns
t <sub>t</sub>	transition time	A port	-	-	-	-	0.5	3.8	0.5	3.8	ns
		B port	-	-	-	-	0.7	4.9	0.6	4.0	ns
t <sub>sk(o)</sub>	output skew time	between channels [3]	-	-	-	-	-	0.4	-	0.3	ns
t <sub>W</sub>	pulse width	data inputs	-	-	-	-	10	-	10	-	ns
f <sub>data</sub>	data rate		-	-	-	-	-	100	-	100	Mbps

- [1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.  
t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>
- [2] These values are guaranteed by design.
- [3] Skew between any two outputs of the same package switching in the same direction.

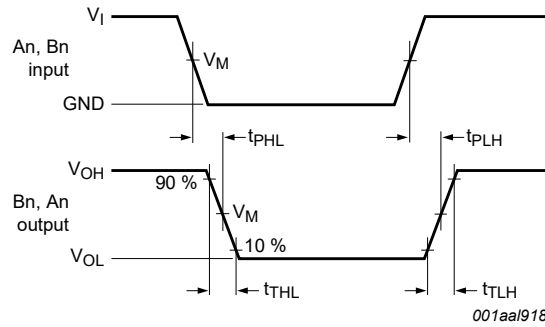
Table 12. Typical power dissipation capacitance [1] [2]

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	V <sub>CC(A)</sub>								Unit
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V		
			V <sub>CC(B)</sub>								
1.8 V	5.0 V	1.8 V	1.8 V	2.5 V	5.0 V	3.3 V to 5.0 V					
<b>T<sub>amb</sub> = 25 °C</b>											
C <sub>PD</sub>	power dissipation capacitance	outputs enabled; OE = V <sub>CC(A)</sub>									
		A port: (direction A to B)	7.0	6.5	7.2	7.6	7.6	7.0	8.0	pF	
		A port: (direction B to A)	9.6	10.0	9.8	10.1	10.5	10.3	10.8	pF	
		B port: (direction A to B)	23.3	28.7	23.1	23.1	23.7	25.9	25.9	pF	
		B port: (direction B to A)	17.8	25.5	17.1	16.8	17.4	21.0	20.5	pF	
		outputs disabled; OE = GND									
		A port: (direction A to B)	0.2	0.2	0.2	0.3	0.3	0.3	0.3	pF	
		A port: (direction B to A)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF	
B port: (direction A to B)	0.01	0.02	0.01	0.01	0.01	0.01	0.01	pF			
B port: (direction B to A)	0.2	0.3	0.2	0.2	0.3	0.3	0.3	pF			

- [1] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in µW). P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:  
f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz;  
C<sub>L</sub> = load capacitance in pF; V<sub>CC</sub> = supply voltage in V;  
N = number of inputs switching; Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.
- [2] f<sub>i</sub> = 10 MHz; V<sub>i</sub> = GND to V<sub>CC</sub>; t<sub>r</sub> = t<sub>f</sub> = 1 ns; C<sub>L</sub> = 0 pF; R<sub>L</sub> = ∞ Ω.

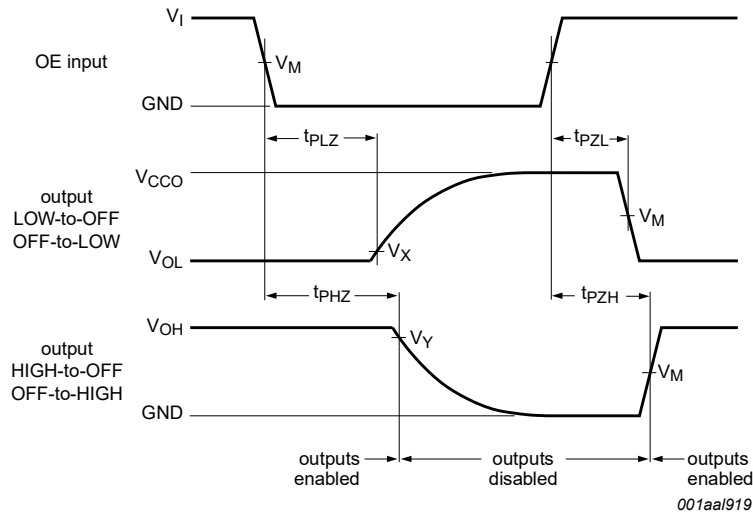
10.1. Waveforms and test circuit



Measurement points are given in Table 13.

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 4. The data input (An, Bn) to data output (Bn, An) propagation delay times



Measurement points are given in Table 13.

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

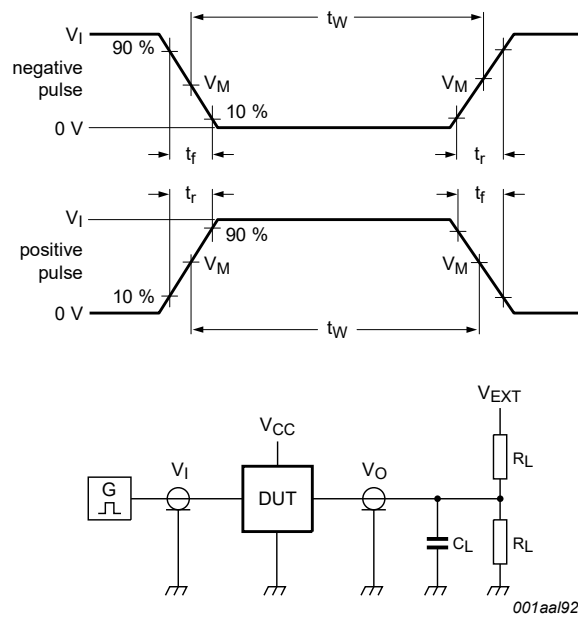
Fig. 5. 3-state enable and disable times

Table 13. Measurement points [1]

Supply voltage	Input	Output		
$V_{CCO}$	$V_M$	$V_M$	$V_X$	$V_Y$
1.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1 V$	$V_{OH} - 0.1 V$
$1.5 V \pm 0.1 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1 V$	$V_{OH} - 0.1 V$
$1.8 V \pm 0.15 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
$2.5 V \pm 0.2 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
$3.3 V \pm 0.3 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
$5.0 V \pm 0.5 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

[1]  $V_{CCI}$  is the supply voltage associated with the input and  $V_{CCO}$  is the supply voltage associated with the output.

Dual supply translating transceiver; auto direction sensing; 3-state



Test data is given in [Table 14](#).

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz; Z<sub>O</sub> = 50 Ω; dV/dt ≥ 1.0 V/ns.

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

V<sub>EXT</sub> = External voltage for measuring switching times.

**Fig. 6. Test circuit for measuring switching times**

**Table 14. Test data**

Supply voltage		Input		Load		V <sub>EXT</sub>		
V <sub>CC(A)</sub>	V <sub>CC(B)</sub>	V <sub>I</sub> [1]	Δt/ΔV	C <sub>L</sub>	R <sub>L</sub> [2]	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub> [3]
1.2 V to 3.6 V	1.65 V to 5.5 V	V <sub>CC1</sub>	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	2V <sub>CC0</sub>

[1] V<sub>CC1</sub> is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R<sub>L</sub> = 1 MΩ; for measuring enable and disable times, R<sub>L</sub> = 50 kΩ.

[3] V<sub>CC0</sub> is the supply voltage associated with the output.

## 11. Application information

### 11.1. Applications

Voltage level-translation applications. The NXB0108 can be used to interface between devices or systems operating at different supply voltages. See Fig. 7 for a typical operating circuit using the NXB0108.

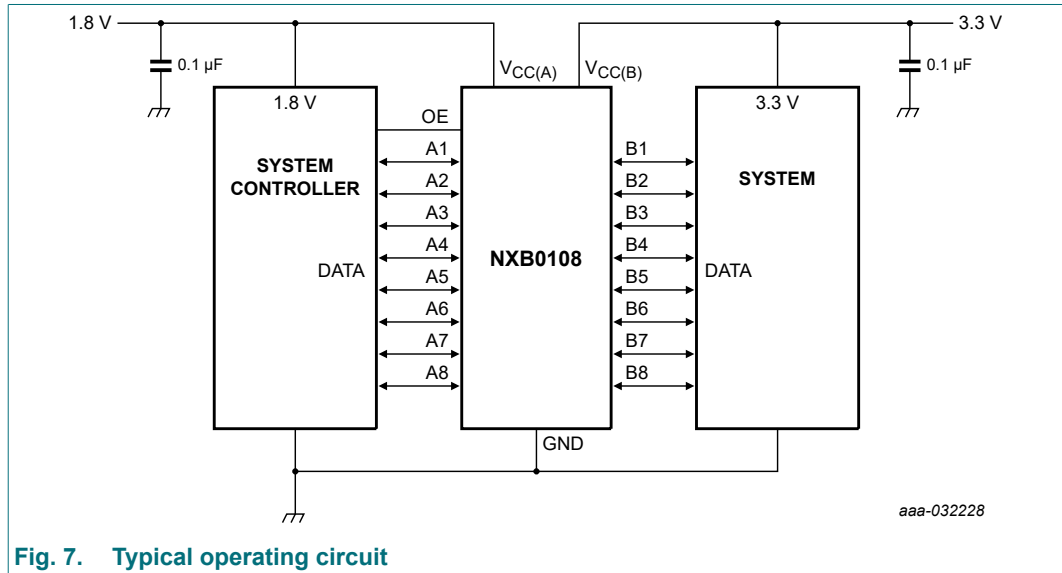


Fig. 7. Typical operating circuit

### 11.2. Architecture

The architecture of the NXB0108 is shown in Fig. 8. The device does not require an extra input signal to control the direction of data flow from A to B or from B to A. In a static state, the output drivers of the NXB0108 can maintain a defined output level, but the output architecture is designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing in the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shots turn on the PMOS transistors (T1, T3) for a short duration, accelerating the low-to-high transition. Similarly, during a falling edge, the one shots turn on the NMOS transistors (T2, T4) for a short duration, accelerating the high-to-low transition. During output transitions the typical output impedance is 70  $\Omega$  at  $V_{CCO} = 1.2$  V to 1.8 V, 50  $\Omega$  at  $V_{CCO} = 1.8$  V to 3.3 V and 40  $\Omega$  at  $V_{CCO} = 3.3$  V to 5.0 V.

Dual supply translating transceiver; auto direction sensing; 3-state

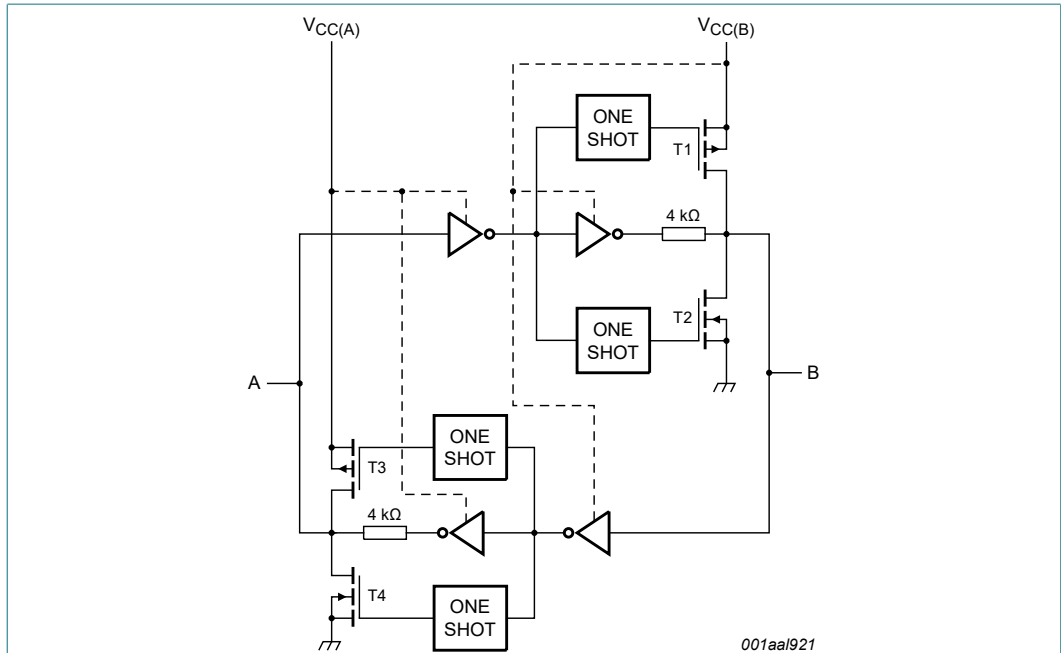
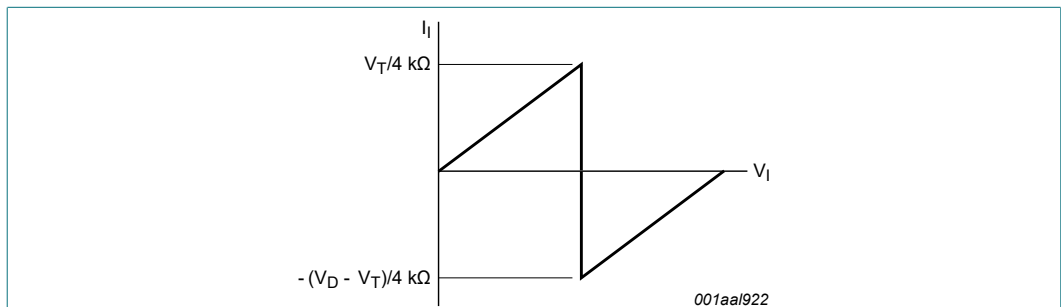


Fig. 8. Architecture of NXB0108 I/O cell (one channel)

11.3. Input driver requirements

For correct operation, the device driving the data I/Os of the NXB0108 must have a minimum drive capability of  $\pm 2$  mA. See Fig. 9 for a plot of typical input current versus input voltage.



$V_T$ : input threshold voltage of the NXB0108 (typically  $V_{CC1} / 2$ ).  
 $V_D$ : supply voltage of the external driver.

Fig. 9. Typical input current versus input voltage graph

11.4. Power up

During operation  $V_{CC(A)}$  must never be higher than  $V_{CC(B)}$ , however during power-up  $V_{CC(A)} \geq V_{CC(B)}$  does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NXB0108 includes circuitry that disables all output ports when either  $V_{CC(A)}$  or  $V_{CC(B)}$  is switched off.

### 11.5. Enable and disable

An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time ( $t_{dis}$  with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### 11.6. Pull-up or pull-down resistors on I/O lines

As mentioned previously the NXB0108 is designed with low static drive strength to drive capacitive loads of up to 70 pF. To avoid output contention issues, any pull-up or pull-down resistors used must be kept higher than 50 k $\Omega$ . For this reason the NXB0108 is not recommended for use in open drain driver applications such as 1-Wire or I<sup>2</sup>C. For these applications, the NXS0108 level translator is recommended.



## 12. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

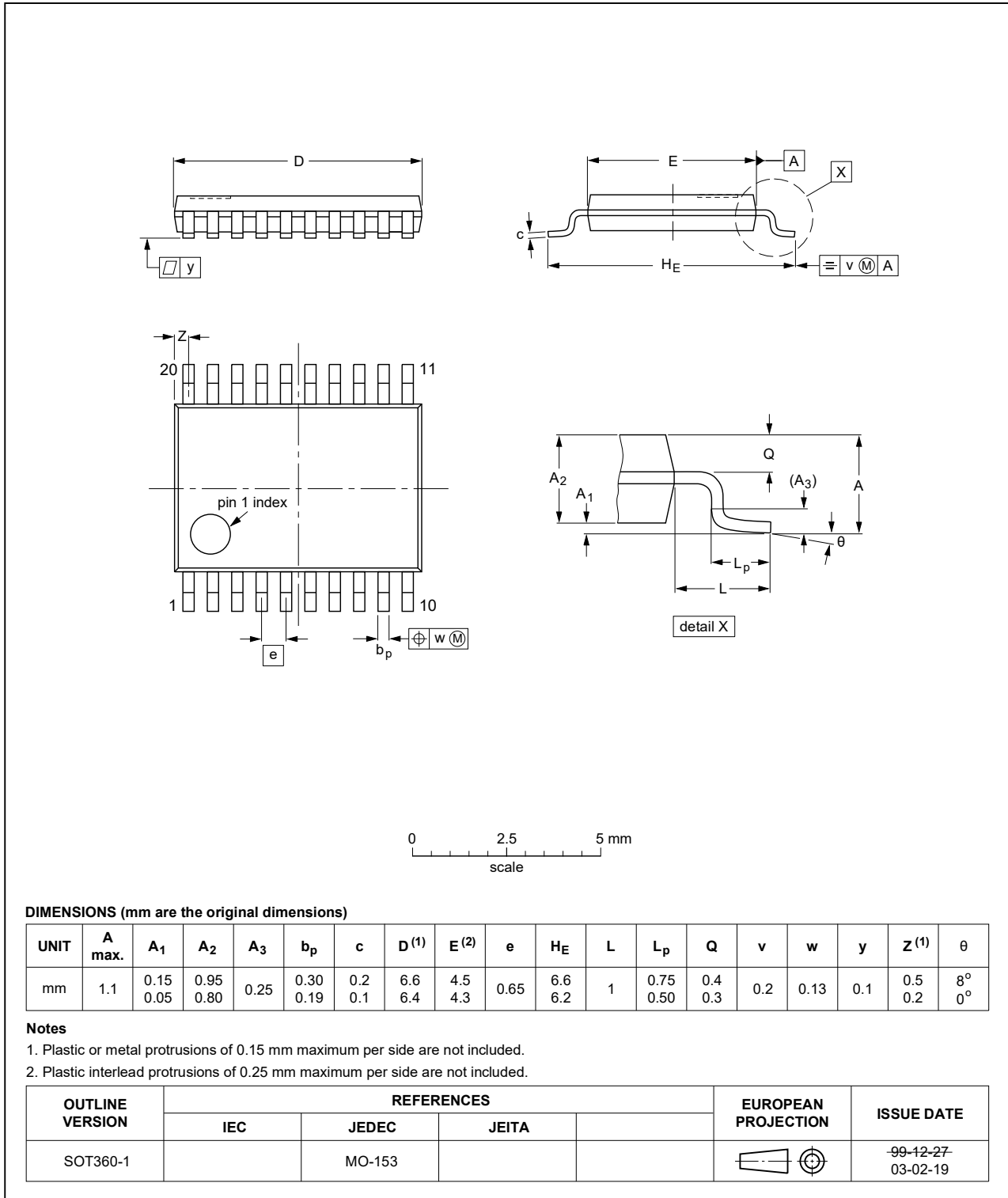


Fig. 10. Package outline SOT360-1 (TSSOP20)

Dual supply translating transceiver; auto direction sensing; 3-state

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

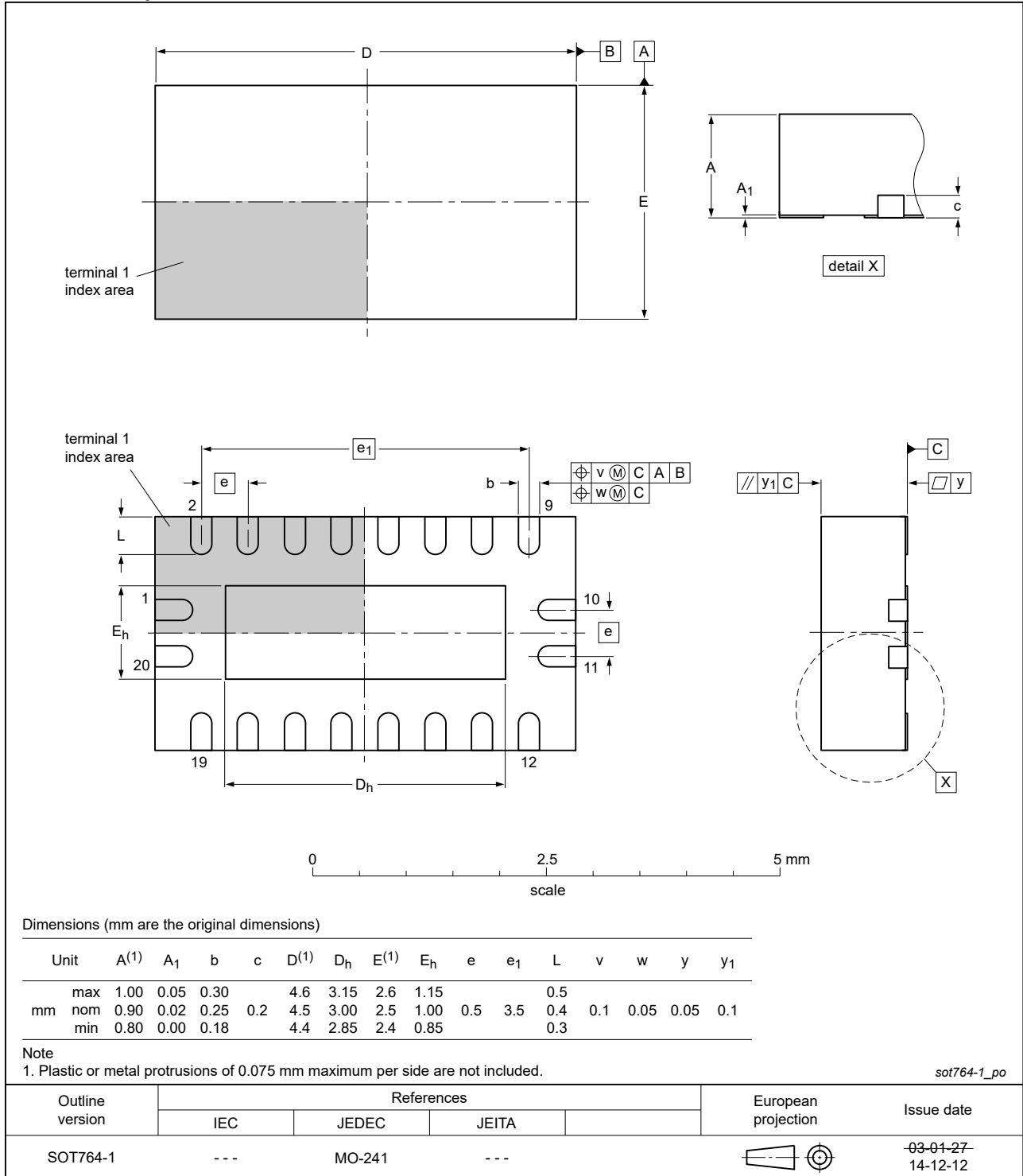


Fig. 11. Package outline SOT764-1 (DHVQFN20)

## 13. Abbreviations

**Table 15. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	Electro Static Discharge
HBM	Human Body Model
MM	Machine Model

## 14. Revision history

**Table 16. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXB0108 v.2	20211103	Product data sheet	-	NXB0108 v.1
Modifications:	• <a href="#">Fig. 1</a> updated			
NXB0108 v.1	20200903	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 3 November 2021