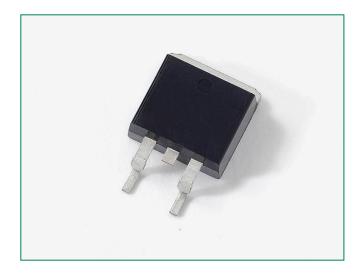


NGD18N45CLB - 18 A, 450 V, N-Channel Ignition IGBT, DPAK





18 Amps, 450 Volts $V_{cr}(on) \le 2.1 \text{ V } @$ $I_{c} = 10 \text{ A, } V_{GE} \ge 4.5 \text{ V}$

Maximum Ratings (T₁ = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V _{CES}	500	V _{DC}
Gate-Gate Voltage	V _{CER}	500	V _{DC}
Gate-Emitter Voltage	V _{GE}	18	V _{DC}
Collector Current-Continuous @T _c = 25°C - Pulsed	I _c	18 50	A _{DC}
ESD (Human Body Model) R = 1500 Ω , C = 100 pF	ESD	8.0	kV
ESD (Machine Model) R = 0 Ω, C = 200 pF	ESD	400	V
Total Power Dissipation @T _c = 25°C Derate above 25°C	P _D	115 0.77	W W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

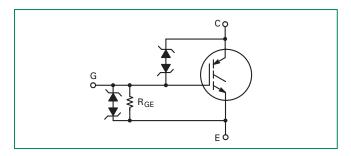
Description

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over-Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

Features

- Ideal for Coil-on-Plug Applications
- DPAK Package Offers Smaller Footprint for Increased **Board Space**
- Gate-Emitter ESD Protection
- Temperature Compensated Gate-Collector Voltage Clamp Limits Stress Applied to Load
- Low Threshold Voltage Interfaces Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Emitter Ballasting for Short-Circuit Capability
- This is a Pb-Free Device

Functional Diagram



Additional Information









Samples



Unclamped Collector-To-Emitter Avalanche Characteristics (Note 2)					
	Symbol	Value	Unit		
Single Pulse Collector-to-Emitter Avalanche Energy					
$V_{CC} = 50 \text{ V}, V_{GE} = 5.0 \text{ V}, P_k I_L = 26.0 \text{ A}, R_G = 1000 \Omega, L = 1.0 \text{ mH}, Starting T_J = 25^{\circ}\text{C}$		338			
$V_{CC} = 50 \text{ V, } V_{GE} = 5.0 \text{ V, } P_k I_L = 10.0 \text{ A, } R_G = 1000 \Omega, L = 8.4 \text{ mH, Starting } T_J = 25^{\circ}\text{C}$	_	420			
$V_{CC} = 50 \text{ V}, V_{GE} = 5.0 \text{ V}, P_k I_L = 15.4 \text{ A}, R_G = 1000 \Omega, L = 2.0 \text{ mH}, Starting T_J = 150°C$	E _{AS}	237	mJ		
$V_{CC} = 50 \text{ V}, V_{GE} = 5.0 \text{ V}, P_k I_L = 5.7 \text{ A}, R_G = 1000 \Omega, L = 15.2 \text{ mH}, Starting T_J = 150 °C$		247			

Thermal Characteristics

	Symbol	Value	Unit
Thermal Resistance, Junction to Case	R _{eJc}	1.3	°C/W
Thermal Resistance, Junction to Ambient DPAK (Note 1)	$R_{\theta_{JA}}$	95	C/VV
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L	275	°C

Maximum Short-Circuit Times

Rating	Symbol	Value	Unit
Short Circuit Withstand Time – Test 1 (See Figure 17, 3 Pulses with 10 ms Period, Ta = 105°C)	t _{sc1-1}	1000	μS
Short Circuit Withstand Time – Test 1 (See Figure 17, 3 Pulses with 10 ms Period, Ta = 150°C)	t _{sc1-2}	800	μS
Short Circuit Withstand Time – Test 2 (See Figure 18, 3 Pulses with 10 ms Period, Ta = 105°C)	t _{sc2-1}	5	ms
Short Circuit Withstand Time – Test 2 (See Figure 18, 3 Pulses with 10 ms Period, Ta = 150°C)	t _{sc2-2}	1	ms



Electrical Characteristics - OFF (Note 2)

Characteristic	Symbol	Test Conditions	Temperature	Min	Тур	Max	Unit										
Collector-Emitter	D) /	I _C = 2.0 mA	$T_{J} = -40^{\circ}\text{C to } 150^{\circ}\text{C}$	430	455	470	\/										
Clamp Voltage	BV _{CES}	I _c = 10 mA	$T_{J} = -40^{\circ}\text{C to } 150^{\circ}\text{C}$	440	475	500	V _{DC}										
			T _J = 25°C	-	0.5	20											
Zero Gate Voltage	:500	$V_{CE} = 350 \text{ V}$ $V_{GE} = 0 \text{ V}$	T _J = 150°C	-	75	250	μA _{DC}										
Collector Current	iECS		T _J = -40°C	-	0.2	10											
		$V_{CE} = 15 V$ $V_{GE} = 0 V$	T _J = 25°C	-	-	2.0											
			T _J = 25°C	-	0.7	1.0											
Reverse Collector–Emitter Leakage Current	l _{CES}	V _{CE} = −24 V	T _J = 150°C	-	12	25	mA										
														T _J = -40°C	-	0.1	1.0
			T _J = 25°C	24	27	30											
Reverse Collector-Emitter Clamp Voltage	BV _{CES(R)}	I _c = -75 mA	T _J = 150°C	26	29	33	V_{DC}										
			T _J = -40°C	23	26	29											
Gate-Emitter Clamp Voltage	BV _{GES}	I _G = 5.0 mA	$T_J = -40$ °C to 150°C	11	13	15	V _{DC}										
Gate-Emitter Leakage Current	I _{GES}	$V_{GE} = \pm 10 \text{ V}$	$T_J = -40$ °C to 150°C	384	590	700	μA _{DC}										
Gate-Emitter Resistor	R _{GE}	-	$T_J = -40$ °C to 150°C	10	16	26	kΩ										

^{1.} When surface mounted to an FR4 board using the minimum recommended pad size.



Electrical Characteristics - ON (Note 2)

Characteristic	Symbol	Test Conditions	Temperature	Min	Тур	Max	Unit
			T _J = 25°C	1.1	1.56	1.9	
Gate Threshold Voltage	V _{GE (th)}	$I_{c} = 1.0 \text{ mA},$ $V_{GE} = V_{CE}$	T _J = 150°C	0.75	1.08	1.4	V _{DC}
			T _J = -40°C	1.2	1.75	2.1	
Threshold Temperature Coefficient (Negative)	_	-	_	-	3.5	_	mV/∘C
		$V_{CE} = 4.5 \text{ V},$ $I_{C} = 7 \text{ A}$	$T_J = -40^{\circ}\text{C to } 150^{\circ}\text{C}$	1.10	1.84	2.30	
		$V_{CE} = 4.0 \text{ V},$ $I_{C} = 7 \text{ A}$	$T_J = -40^{\circ}\text{C to } 150^{\circ}\text{C}$	1.15	1.89	2.35	
		$V_{CE} = 3.7 \text{ V},$ $I_{C} = 7 \text{ A}$	$T_J = -40^{\circ}\text{C to } 150^{\circ}\text{C}$	1.20	1.93	2.50	
Collector-to-Emitter On-Voltage	V _{CE (on)}	$V_{CE} = 4.5 \text{ V},$ $I_{C} = 10 \text{ A}$	$T_J = -40^{\circ}\text{C to } 150^{\circ}\text{C}$	1.45	2.07	2.65	V _{DC}
		$V_{CE} = 4.0 \text{ V},$ $I_{C} = 10 \text{ A}$	$T_J = -40^{\circ}\text{C to } 150^{\circ}\text{C}$	1.50	2.13	2.80	
		$V_{CE} = 3.7 \text{ V},$ $I_{C} = 10 \text{ A}$	$T_J = -40^{\circ}\text{C to } 150^{\circ}\text{C}$	1.55	2.19	2.85	
		$V_{CE} = 4.5 \text{ V},$ $I_{C} = 10 \text{ mA}$	$T_J = -40^{\circ}\text{C to } 150^{\circ}\text{C}$	-	0.65	1.00	
Forward Transconductance	gfs	$V_{CE} = 5.0 \text{ V},$ $I_{C} = 6.0 \text{ A}$	$T_J = -40^{\circ}\text{C to } 150^{\circ}\text{C}$	6.0	14	25	Mhos



Dynamic Characteristics

Characteristic	Symbol	Test Conditions	Temperature	Min	Тур	Max	Unit
Input Capacitance	C _{ISS}	V = 25 V	T 4000	400	780	1000	
Output Capacitance	C _{oss}	$V_{CC} = 25 V$ $V_{GE} = 0 V$	$T_{J} = -40^{\circ}C$ to $150^{\circ}C$	50	72	100	pF
Transfer Capacitance	C _{RSS}	f = 1.0 MHz	130 C	4.0	6	10	

Switching Characteristics (Note 2)

Characteristic	Symbol	Test Conditions	Temperature	Min	Тур	Max	Unit
Turn-Off Delay Time	t _{d (off)}	$V_{CC} = 300 \text{ V}$ $V_{GE} = 0 \text{ V}$ $R_{G} = 1.0 \text{ k}\Omega$ $R_{L} = 46 \Omega$	T _J = 25°C	1.0	2.9	12	
Fall Time	t _f	$V_{CC} = 300 \text{ V}$ $V_{GE} = 5 \text{ V}$ $R_{G} = 1.0 \text{ k}\Omega$ $R_{L} = 46 \Omega$	T _J = 25°C	1.0	2.5	7.0	w\$00
Turn-On Delay Time	t _{d (on)}	$V_{CC} = 14 \text{ V},$ $V_{GE} = 5 \text{ V}$ $R_{G} = 1.0 \text{ k}\Omega$ $R_{L} = 1 \Omega$	T _J = 25°C	0.1	0.42	1.4	μSec
Rise Time	t _r	$V_{CC} = 14 \text{ V},$ $V_{GE} = 5 \text{ V}$ $R_{G} = 1.0 \text{ k}\Omega$ $R_{L} = 1 \Omega$	T _J = 25°C	1.0	2.5	9.0	

^{2.} Electrical Characteristics at temperature other than 25°C, Dynamic and Switching characteristics are not subject to production testing. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



Typical Electrical Characteristics (unless otherwise noted)

Figure 1. Output Characteristics

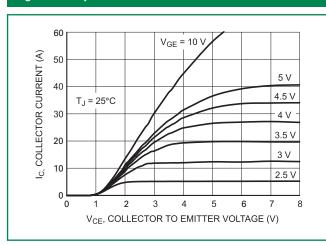


Figure 3. Output Characteristics

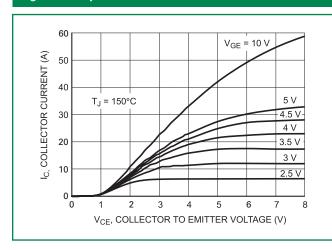


Figure 5. Collector-to-Emitter Saturation Voltage vs. Junction Temp

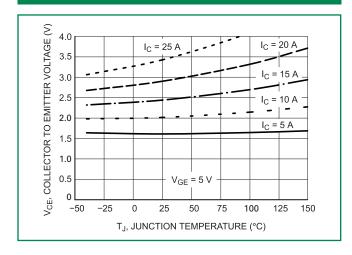


Figure 2. Output Characteristics

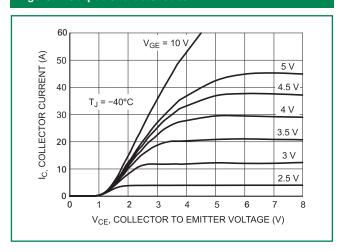


Figure 4. Transfer Characteristics

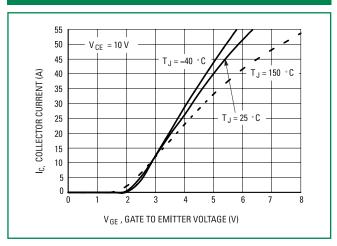
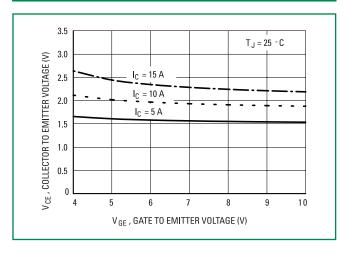


Figure 6. Collector-to-Emitter Voltage versus Gate-to-Emitter



© 2018 Littelfuse, Inc.

Specifications are subject to change without notice.

Revised: 02/15/18



Figure 7. Collector-to-Emitter Voltage vs Gate-to-Emitter Voltage

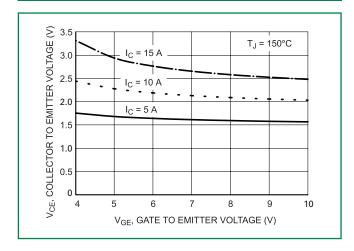


Figure 8. Capacitance Variation

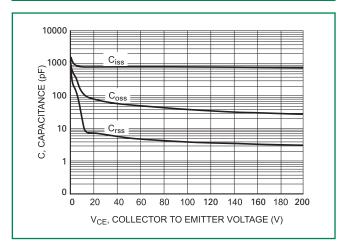


Figure 9. Gate Threshold Voltage vs. Junction Temperature

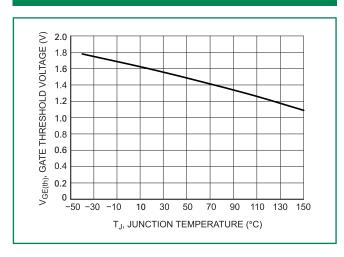


Figure 10. Minimum Open Secondary Latch Current vs.Inductance

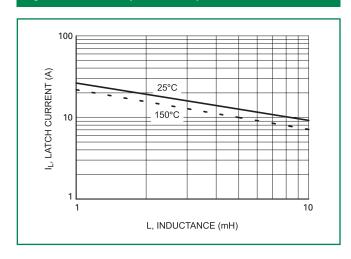


Figure 11. Typical Open Secondary Latch Current vs. Inductance

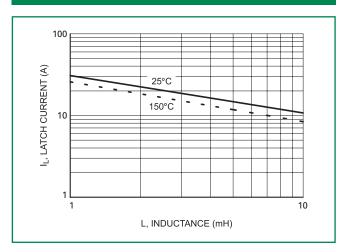
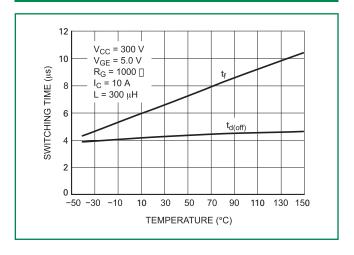


Figure 12. Inductive Switching Fall Time vs. Temperature



© 2018 Littelfuse, Inc.

Specifications are subject to change without notice.

Revised: 02/15/18



Figure 13. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at T_a = 25°C)

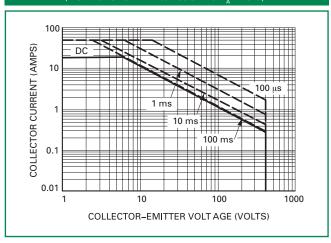


Figure 14. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at $T_A = 125$ °C)

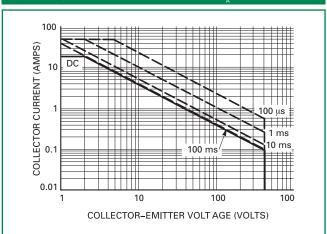


Figure 15. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at T_c = 25°C)

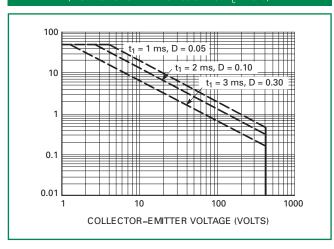


Figure 16. Pulse Train Safe Operating Area
(Mounted on an Infinite Heatsink at T_c = 25°C)

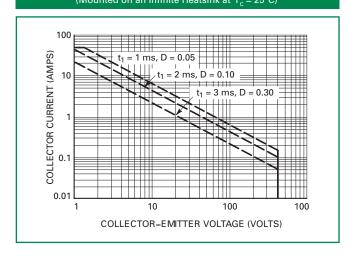


Figure 17. Circuit Configuration for Short Circuit Test #1

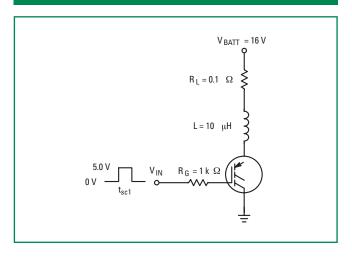


Figure 18. Circuit Configuration for Short Circuit Test #2

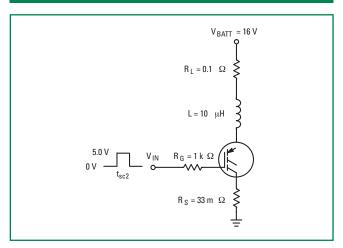
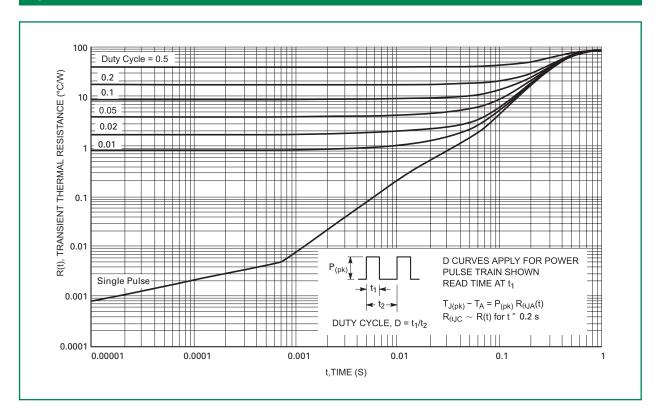
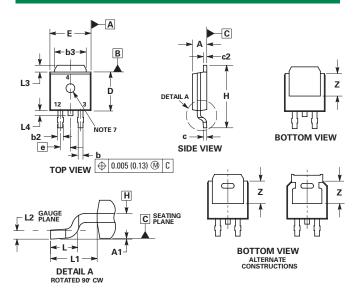




Figure 19. Transient Thermal Resistance (Non-normalized Junction-to-Ambient mounted on minimum pad area)



Dimensions

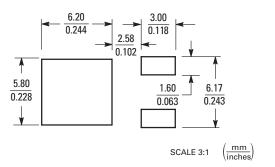


D:	Incl	hes	Millim	neters
Dim	Min	Max	Min	Max
А	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
С	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
Е	0.250	0.265	6.35	6.73
е	0.090	BSC	2.29 BSC	
Н	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

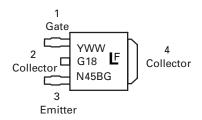
NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: INCH.
- 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- 5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- 7. OPTIONAL MOLD FEATURE

Soldering Footrpint



Part Marking System



G18N45BG = Device Code

Y=	Year
WW	= Work Week
G	= Pb-Free Device

ORDERING INFORMATION

Device	Package	Shipping†
NGD18N45CLBT4G	DPAK (Pb-Free)	2,500 / Tape & Reel

Disclaimer Notice - Information furnished is believed to be accurate and reliable. However, users should independently evaluate the suitability of and test each product selected for their own applications. Littlefluse products are not designed for, and may not be used in, all applications. Read complete Disclaimer Notice at: www.littlefluse.com/disclaimer-electronics.