

Features

December 2005

- Full duplex transcoder with four encode channels and four decode channels
- 32 kb/s, 24 kb/s and 16 kb/s ADPCM coding complying with ITU-T (previously CCITT) G.726 (without 40 kb/s), and ANSI T1.303-1989
- Low power operation, 25 mW typical
- Asynchronous 4.096 MHz master clock operation
- SSI and ST-BUS interface options
- Transparent PCM bypass
- Transparent ADPCM bypass
- Linear PCM code
- No microprocessor control required
- Simple interface to Codec devices
- Pin selectable μ -Law or A-Law operation
- Pin selectable ITU-T or signed magnitude PCM coding
- Single 5 volt power supply

Applications

- Pair gain
- Voice mail systems
- Wireless telephony systems

Ordering Information

MT9126AE	28 Pin PDIP	Tubes
MT9126AS	28 Pin SOIC	Tubes
MT9126ASR	28 Pin SOIC	Tape & Reel
MT9126AE1	28 Pin PDIP*	Tubes
MT9126AS1	28 Pin SOIC*	Tubes
MT9126ASR1	28 Pin SOIC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

Description

The Quad ADPCM Transcoder is a low power, CMOS device capable of four encode and four decode functions per frame. Four 64 kbit/s PCM octets are compressed into four 32, 24 or 16 kbit/s ADPCM words, and four 32, 24 or 16 kbit/s ADPCM words are expanded into four 64 kbit/s PCM octets. The 32, 24 and 16 kbit/s ADPCM transcoding algorithms utilized conform to ITU-T Recommendation G.726 (excluding 40 kbit/s), and ANSI T1.303 - 1989.

Switching, on-the-fly, between 32 kbit/s and 24 kbit/s ADPCM, is possible by controlling the appropriate mode select (MS1 - MS6) control pins. All optional functions of the device are pin selectable allowing a simple interface to industry standard codecs, digital phone devices and Layer 1 transceivers. Linear coded PCM is provided to facilitate external DSP functions.

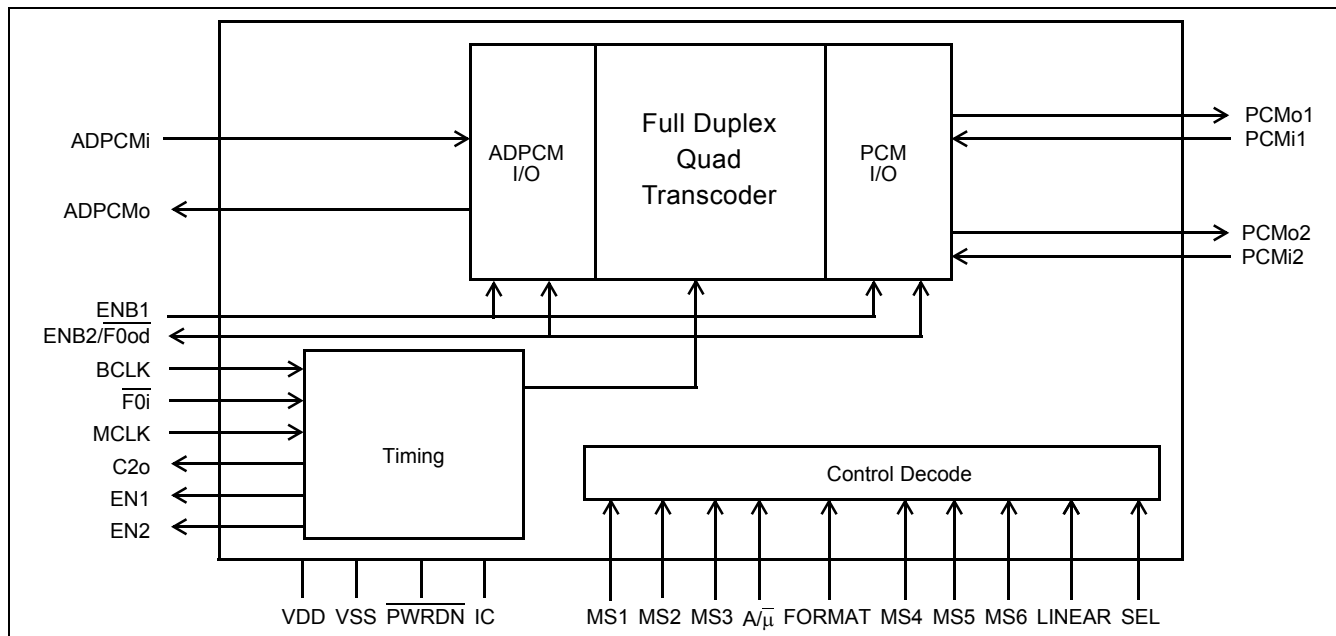


Figure 1 - Functional Block Diagram

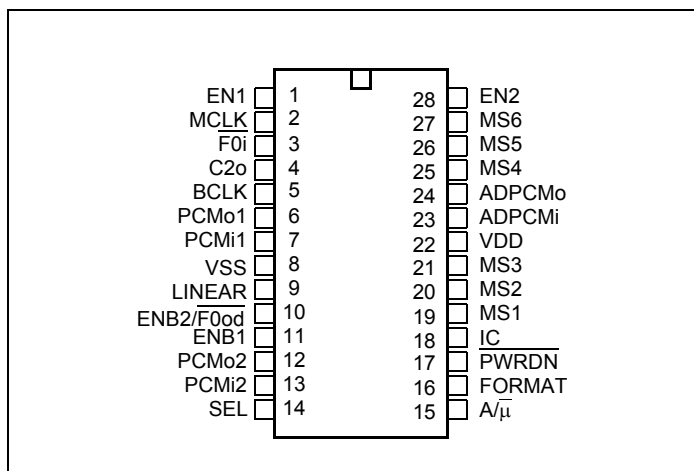


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	EN1	Enable Strobe 1 (Output). This 8 bit wide, active high strobe is active during the B1 PCM channel in ST-BUS mode. Becomes a single bit, high true pulse when LINEAR=1. In SSI mode this output is high impedance.
2	MCLK	Master Clock (input). This is a 4.096 MHz (minimum) input clock utilized by the transcoder function; it must be supplied in both ST-BUS and SSI modes of operation. In ST-BUS mode the $\overline{C4}$ ST-BUS clock is applied to this pin. This synchronous clock is also used to control the data I/O flow on the PCM and ADPCM input/output pins according to ST-BUS requirements. In SSI mode this master clock input is derived from an external source and may be asynchronous with respect to the 8 kHz frame. MCLK rates greater than 4.096 MHz are acceptable in this mode since the data I/O rate is governed by BCLK.
3	$\overline{F0i}$	Frame Pulse (Input). Frame synchronization pulse input for ST-BUS operation. SSI operation is enabled by connecting this pin to V_{SS} .
4	C2o	2.048 MHz Clock (Output). This ST-BUS mode bit clock output is the MCLK ($\overline{C4}$) input divided by two, inverted, and synchronized to $\overline{F0i}$. This output is high-impedance during SSI operation.
5	BCLK	Bit Clock (Input). 128 kHz to 4096 kHz bit clock input for both PCM and ADPCM ports; used in SSI mode only. The falling edge of this clock latches data into ADPCMi, PCMi1 and PCMi2. The rising edge clocks data out on ADPCMo, PCMo1 and PCMo2. This input must be tied to V_{SS} for ST-BUS operation.
6	PCMo1	Serial PCM Stream 1 (Output). 128 kbit/s to 4096 kbit/s serial companded/linear PCM output stream. Data are clocked out by rising edge of BCLK in SSI mode. Clocked out by MCLK divided by two in ST-BUS mode. See Figure 14.
7	PCMi1	Serial PCM Stream 1 (Input). 128 kbit/s to 4096 kbit/s serial companded/linear PCM input stream. Data are clocked in on falling edge of BCLK in SSI mode. Clocked in at the 3/4 bit position of MCLK in ST-BUS mode. See Figure 14.
8	V_{SS}	Digital Ground. Nominally 0 volts.

Pin Description

Pin #	Name	Description
9	LINEAR	Linear PCM Select (Input). When tied to V_{DD} the PCM I/O ports (PCM1,PCM2) are 16-bit linear PCM. Linear PCM operates only at a bit rate of 2048 kbit/s. Companded PCM is selected when this pin is tied to V_{SS} . See Figures 5 & 8.
10	ENB2/ $\overline{F0od}$	PCM B-Channel Enable Strobe 2 (Input) / Delayed Frame Pulse (Output). SSI operation: ENB2 (Input). An 8-bit wide enable strobe input defining B2 channel (AD)PCM data. A valid 8-bit strobe must be present at this input for SSI operation. See Figures 4 & 6. ST-BUS operation: $\overline{F0od}$ (Output). This pin is a delayed frame strobe output. When LINEAR=0, this becomes a delayed frame pulse output occurring 64 $\overline{C4}$ clock cycles after $\overline{F0i}$ and when LINEAR = 1 at 128 $\overline{C4}$ clock cycles after $\overline{F0i}$. See Figures 7, 8, 9 & 14.
11	ENB1	PCM B-Channel Enable Strobe 1 (Input). SSI operation: An 8-bit wide enable strobe input defining B1 channel (AD)PCM data. A valid 8-bit strobe must be present at this input for SSI operation. ST-BUS operation: When tied to V_{SS} transparent bypass of the ST-BUS D- and C-channels is enabled. When tied to V_{DD} the ST-BUS D-channel and C-channel output timeslots are forced to a high-impedance state.
12	PCMo2	Serial PCM Stream 2 (Output). 128 kbit/s to 4096 kbit/s serial companded/linear PCM output stream. Clocked out by rising edge of BCLK in SSI mode. Clocked out by MCLK divided by two in ST-BUS mode. See Figure 14.
13	PCMi2	Serial PCM Stream 2 (Input). 128 kbit/s to 4096 kbit/s serial companded/linear PCM input stream. Data bits are clocked in on falling edge of BCLK in SSI mode. Clocked in at the 3/4 bit position of MCLK in ST-BUS mode. See Figure 14.
14	SEL	SELECT (Input). PCM bypass mode: When SEL=0 the PCM1 port is selected for PCM bypass operation and when SEL=1 the PCM2 port is selected for PCM bypass operation. See Figures 6 & 9. 16 kbit/s transcoding mode: SSI Operation - in 16 kbit/s transcoding mode, the ADPCM words are assigned to the I/O timeslot defined by ENB2 when SEL=1 and by ENB1 when SEL=0. See Figure 4. ST-BUS operation- in 16 kbit/s transcoding mode, the ADPCM words are assigned to the B2 timeslot when SEL=1 and to the B1 timeslot when SEL=0. See Figure 9.
15	$A/\overline{\mu}$	A-Law/$\overline{\mu}$-Law Select (Input). This input pin selects $\overline{\mu}$ -Law companding when set to logic 0, and A-Law companding when set to logic 1. This control is for all channels. This input is ignored in Linear mode during which it may be tied to V_{SS} or V_{DD} .
16	FORMAT	FORMAT Select (Input). Selects ITU-T PCM coding when high and Sign-Magnitude PCM coding when low. This control is for all channels. This input is ignored in Linear mode during which it may be tied to V_{SS} or V_{DD} .
17	\overline{PWRDN}	Power-down (Input). An active low reset forcing the device into a low power mode where all outputs are high-impedance and device operation is halted.

Pin Description

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18	IC	Internal Connection (Input). Tie to V_{SS} for normal operation.																																				
19	MS1	Mode Selects 1, 2 and 3 (Inputs). Mode selects for all four encoders. <table border="1"> <thead> <tr> <th>MS3</th> <th>MS2</th> <th>MS1</th> <th>MODE</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>32 kbit/s ADPCM</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>24 kbit/s ADPCM</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>16 kbit/s ADPCM in EN1/ENB1 when SEL=0 in EN2/ENB2 when SEL=1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>ADPCM Bypass for 32 kbit/s and 24 kbit/s</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>ADPCM Bypass for 16 kbit/s</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>PCM Bypass (64 kbit/s) to PCM1 if SEL=0, PCM2 if SEL=1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Algorithm reset (ITU-T optional reset)</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>ADPCM_o disable</td> </tr> </tbody> </table>	MS3	MS2	MS1	MODE	0	0	0	32 kbit/s ADPCM	0	0	1	24 kbit/s ADPCM	0	1	0	16 kbit/s ADPCM in EN1/ENB1 when SEL=0 in EN2/ENB2 when SEL=1	0	1	1	ADPCM Bypass for 32 kbit/s and 24 kbit/s	1	0	0	ADPCM Bypass for 16 kbit/s	1	0	1	PCM Bypass (64 kbit/s) to PCM1 if SEL=0, PCM2 if SEL=1	1	1	0	Algorithm reset (ITU-T optional reset)	1	1	1	ADPCM _o disable
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22	V_{DD}	Positive Power Supply. Nominally 5 volts +/-10%																																				
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25	MS4	Mode Selects 4, 5 and 6 (Inputs). Mode selects for all four decoders. <table border="1"> <thead> <tr> <th>MS6</th> <th>MS5</th> <th>MS4</th> <th>MODE</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>32 kbit/s ADPCM</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>24 kbit/s ADPCM</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>16 kbit/s ADPCM in EN1/ENB1 when SEL=0 in EN2/ENB2 when SEL=1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>ADPCM Bypass for 32 kbit/s and 24 kbit/s</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>ADPCM Bypass for 16 kbit/s</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>PCM Bypass (64 kbit/s) to PCM1 if SEL=0, PCM2 if SEL=1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Algorithm reset (ITU-T optional reset)</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>PCM_o1/2 disable</td> </tr> </tbody> </table>	MS6	MS5	MS4	MODE	0	0	0	32 kbit/s ADPCM	0	0	1	24 kbit/s ADPCM	0	1	0	16 kbit/s ADPCM in EN1/ENB1 when SEL=0 in EN2/ENB2 when SEL=1	0	1	1	ADPCM Bypass for 32 kbit/s and 24 kbit/s	1	0	0	ADPCM Bypass for 16 kbit/s	1	0	1	PCM Bypass (64 kbit/s) to PCM1 if SEL=0, PCM2 if SEL=1	1	1	0	Algorithm reset (ITU-T optional reset)	1	1	1	PCM _o 1/2 disable
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28	EN2	Enable Strobe 2 (Output). This 8 bit wide, active high strobe is active during the B2 PCM channel in ST-BUS mode. Forced to high impedance when LINEAR=1.																																				

Notes:

All unused inputs should be connected to logic low or high unless otherwise stated. All outputs should be left open circuit when not used.

All inputs have TTL compatible logic levels except for MCLK which has CMOS compatible logic levels and \overline{PWRDN} which has Schmitt trigger compatible logic levels.

All outputs are CMOS with CMOS logic levels (See DC Electrical Characteristics).

Functional Description

The Quad-channel ADPCM Transcoder is a low power, CMOS device capable of four encode and four decode operations per frame. Four 64 kbit/s channels (PCM octets) are compressed into four 32, 24 or 16 kbit/s ADPCM channels (ADPCM words), and four 32, 24 or 16 kbit/s ADPCM channels (ADPCM words) are expanded into four 64 kbit/s PCM channels (PCM octets). The ADPCM transcoding algorithm utilized conforms to ITU-T recommendation G.726 (excluding 40 kb/s), and ANSI T1.303 - 1989. Switching on-the-fly between 32 and 24 kbit/s transcoding is possible by toggling the appropriate mode select pins (supports T1 robbed-bit signalling).

All functions supported by the device are pin selectable. The four encode functions comprise a common group controlled via Mode Select pins MS1, MS2 and MS3. Similarly, the four decode functions form a second group commonly controlled via Mode Select pins MS4, MS5 and MS6. All other pin controls are common to the entire transcoder.

The device requires 25 mWatts (MCLK= 4.096 MHz) typically for four channel transcode operation. A minimum master clock frequency of 4.096 MHz is required for the circuit to complete four encode channels and four decode channels per frame. For SSI operation a master clock frequency greater than 4.096 MHz and asynchronous, relative to the 8 kHz frame, is allowed.

The PCM and ADPCM serial busses support both ST-BUS and Synchronous Serial Interface (SSI) operation. This allows serial data clock rates from 128 kHz to 4096 kHz, as well as compatibility with Zarlink's standard Serial Telecom BUS (ST-BUS). For ST-BUS operation, on chip channel counters provide channel enable outputs as well as a 2048 kHz bit clock output which may be used by down-stream devices utilizing the SSI bus interface.

Linear coded PCM is also supported. In this mode the encoders compress, four 14-bit, two's complement (S,S,S,12,...,1,0), uniform PCM channels into four 4, 3 or 2 bit ADPCM channels. Similarly, the decoder expands four 4, 3 or 2 bit ADPCM channels into four 16-bit, two's complement (S,14,...,1,0), uniform PCM channels. The data rate for both ST-BUS and SSI operation in this mode is 2048 kbit/s.

Serial (AD)PCM Data I/O

Serial data transfer to/from the Quad ADPCM transcoder is provided through one ADPCM and two PCM ports (ADPCMi, ADPCMo, PCMi1, PCMo1, PCMi2, PCMo2). Data is transferred through these ports according to either ST-BUS or SSI requirements. The device determines the mode of operation by monitoring the signal applied to the $\overline{F0i}$ pin. When a valid ST-BUS frame pulse (244 nSec low going pulse) is applied to the $\overline{F0i}$ pin the transcoder will assume ST-BUS operation. If $\overline{F0i}$ is tied continuously to V_{SS} the transcoder will assume SSI operation. Pin functionality in each of these modes is described in the following sub-sections.

ST-BUS Mode

During ST-BUS operation the C2o, EN1, EN2 and $\overline{F0od}$ outputs become active and all serial timing is derived from the MCLK ($\overline{C4}$) and $\overline{F0i}$ inputs while the BCLK input is tied to V_{SS} . (See Figures 7, 8 & 9.)

Basic Rate "D" and "C" Channels

In ST-BUS mode, when ENB1 is brought low, transparent transport of the ST-BUS "Basic Rate D- and C-channels" is supported through the PCMi1 and PCMo1 pins. This allows a microprocessor controlled device, connected to the PCMi/o1 pins, to access the "D" and "C" channels of a transmission device connected to the ADPCMi/o pins. When ENB1 is brought high, the "D" and "C" channel outputs are tristated. Basic Rate "D" and "C" channels are not supported in LINEAR mode.(See Figure 7.)

SSI Mode

During SSI operation the BCLK, ENB1 and ENB2/ $\overline{F0od}$ inputs become active. The C2o, EN1, and EN2 outputs are forced to a high-impedance state except during LINEAR operation during which the EN1 output remains active. (See Figures 4, 5 & 6.)

The SSI port is a serial data interface, including data input and data output pins, a variable rate bit clock input and two input strobes providing enables for data transfers. There are three SSI I/O ports on the Quad ADPCM; the PCMi/o1 PCM port, the PCMi/o2 PCM port, and the ADPCMi/o port. The two PCM ports may transport 8-bit companded PCM or 16-bit linear PCM. The alignment of the channels is determined by the two input strobe signals ENB1 and ENB2/ $\overline{F0od}$. The bit clock (BCLK) and input strobes (ENB1 and ENB2/ $\overline{F0od}$) are common for all three of the serial I/O ports. BCLK can be any frequency between 128 kHz and 4096 kHz synchronized to the input strobes. BCLK may be discontinuous outside of the strobe boundaries except when LINEAR=1. In LINEAR mode, BCLK must be 2048 kHz and continuous for 64 cycles after the ENB1 rising edge and for the duration of ENB2/ $\overline{F0od}$.

Mode Select Operation (MS1, MS2, MS3, MS4, MS5, MS6)

Mode Select pins MS1, MS2 and MS3 program different bit rate ADPCM coding, bypass, algorithmic reset and disable modes for all four encoder functions simultaneously. When 24 kbit/s ADPCM mode is selected bit 4 is unused while in 16 kb/s ADPCM mode all ADPCM channels are packed contiguously into one 8-bit octet. Mode Select pins MS4, MS5 and MS6 operate in the same manner for the four decode functions. The mode selects must be set up according to the timing constraints illustrated in Figures 16 and 17.

32 kbit/s ADPCM Mode

In 32 kbit/s ADPCM mode, the 8-bit PCM octets of the B1, B2, B3 and B4 channels (PCMi1 and PCMi2) are compressed into four 4-bit ADPCM words on ADPCMo. Conversely, the 4-bit ADPCM words of the B1, B2, B3 and B4 channels from ADPCMi are expanded into four 8-bit PCM octets on PCMo1 and PCMo2. The 8-bit PCM octets (A-Law or μ -Law) are transferred most significant bit first starting with b7 and ending with b0. ADPCM words are transferred most significant bit first starting with I1 and ending with I4 (See Figures 4 & 7). Reference ITU-T G.726 for I-bit definitions.

24 kbit/s ADPCM Mode

In 24 kbit/s mode PCM octets are transcoded into 3-bit words rather than the 4-bit words utilized in 32 kbit/s ADPCM. This is useful in situations where lower bandwidth transmission is required. Dynamic operation of the mode select control pins will allow switching from 32 kbit/s mode to 24 kbit/s mode on a frame by frame basis. The 8 bit PCM octets (A-Law or μ -Law) are transferred most significant bit first starting with b7 and ending with b0. ADPCM words are transferred most significant bit first starting with I1 and ending with I3 (I4 becomes don't care). (See Figures 4 & 7.)

16 kbit/s ADPCM Mode

When SEL is set to 0, the 8-bit PCM octets of the B1, B2, B3 and B4 channels (PCMi1 and PCMi2) are compressed into four 2-bit ADPCM words on ADPCMo during the ENB1 timeslot in SSI mode and during the B1 timeslot in ST-BUS mode. Similarly, the four 2-bit ADPCM words on ADPCMi are expanded into four 8-bit PCM octets (on PCMo1 and PCMo2) during the ENB1/B1 timeslot. (See Figures 4 & 7.)

When SEL is set to 1, The same conversion takes place as described when SEL = 0 except that the ENB2/B2 timeslots are utilized.

A-Law or μ -Law 8-bit PCM are received and transmitted most significant bit first starting with b7 and ending with b0. ADPCM data are most significant bit first starting with I1 and ending with I2.

ADPCM BYPASS (32 and 24 kbit/s)

In ADPCM bypass mode the B1 and B2 channel ADPCM words are bypassed (with a two-frame delay) to/from the ADPCM port and placed into the most significant nibbles of the PCM1/2 port octets. Note that the SEL pin performs no function for these two modes (See Figures 6 & 9). LINEAR, FORMAT and $A/\overline{\mu}$ pins are ignored in bypass mode.

In 32 kb/s ADPCM bypass mode, Bits 1 to 4 of the B1, B2, B3 and B4 channels from PCMi1 and PCMi2 are transparently passed, with a two frame delay, to the same channels on ADPCMo. In the same manner, the B1, B2, B3 and B4 channels from ADPCMi are transparently passed, with a two frame delay, to the same channels on PCMo1 and PCMo2 pins. Bits 5 to 8 are don't care. This feature allows two voice terminals, which utilize ADPCM

transcoding, to communicate through a system without incurring unnecessary transcode conversions. This arrangement allows byte-wide or nibble-wide transport through a switching matrix.

24 kb/s ADPCM bypass mode is the same as 32 kb/s mode bypass excepting that only bits 1 to 3 are bypassed and bits 4 to 8 are don't care.

ADPCM BYPASS (16 kbit/s)

When SEL is set to 0, only bits 1 and 2 of the B1, B2, B3 and B4 PCM octets (on PCMi1 and PCMi2) are bypassed, with a two frame delay, to the same channels on ADPCM_o during the ENB1 timeslot in SSI mode and during the B1 timeslot in ST-BUS mode. Similarly, the four 2-bit ADPCM words on ADPCM_i are transparently bypassed, with a two frame delay, to PCMo1 and PCMo2 during the ENB1 or B1 timeslot. Bits 3-8 are don't care. (See Figures 6 & 9.)

When SEL is set to 1, the same bypass occurs as described when SEL = 0 except that the ENB2 or B2 timeslots are utilized.

LINEAR, FORMAT and $A\bar{\mu}$ pins are ignored in bypass mode.

PCM BYPASS

When SEL is set to 0, the B1 and B2 PCM channels on PCMi1 are transparently passed, with a two-frame delay, to the same channels on the ADPCM_o. Similarly, the two 8-bit words which are on ADPCM_i are transparently passed, with a two-frame delay, to channels B1 and B2 of PCMo1 while PCMo2 is set to a high-impedance state. (See Figures 6 & 9.)

When SEL is set to 1, the B3 and B4 channels on PCMi2 are transparently passed, with a two frame delay, to the same channels on ADPCM_o. Similarly, the two 8-bit words which are on ADPCM_i are transparently passed, with a two-frame delay, to channels B3 and B4 of PCMo2. In this case PCMo1 is always high-impedance if ENB1 = 0. If ENB1 = 1 during ST-BUS operation then the D and C channels are active on PCMo1.

LINEAR, FORMAT and $A\bar{\mu}$ pins are ignored in bypass mode.

Algorithm Reset Mode

While an algorithmic reset is asserted the device will incrementally converge its internal variables to the 'Optional reset values' stated in G.726. Algorithmic reset requires that the master clock (MCLK) and frame pulse (ENB1/2 or \overline{FOi}) remain active and that the reset condition be valid for at least four frames. Note that this is not a power down mode; see PWRDN for this function.

ADPCM_o & PCMo1/2 Disable

When the encoders are programmed for ADPCM_o disable (MS1 to MS3 set to 1) the ADPCM_o output is set to a high impedance state and the internal encode function remains active. Therefore convergence is maintained. The decode processing function and data I/O remain active.

When the decoders are programmed for PCMo1/2 disable (MS4 to MS6 set to 1) the PCMo1/2 outputs are high impedance during the B Channel timeslots and also, during ST-BUS operation, the D and C channel timeslots according to the state of ENB1. Therefore convergence is maintained. The encode processing function and data I/O remain active.

Whenever any combination of the encoders or decoders are set to the disable mode the following outputs remain active. A) ST-BUS mode: ENB2/ \overline{FOod} , EN1, EN2 and C2o. Also the "D" and "C" channels from PCMo1 and ADPCM_o remain active if ENB1 is set to 0. If ENB1 is brought high then PCMo1 and ADPCM_o are fully tri-stated. B) SSI mode: When used in the 16-bit linear mode, only the EN1 output remains active. For complete chip power down see PWRDN.

Other Pin Controls

16 Bit Linear PCM

Setting the LINEAR pin to logic one causes the device to change to 16-bit linear (uniform) PCM transmission on the PCMi/o1 and PCMi/o2 ports. The data rate for both ST-BUS and SSI operation in this mode is 2048 kbit/s and all decode and encode functions are affected by this pin. In SSI mode, the input channel strobes ENB1 and ENB2/ $\overline{F0od}$ remain active for 8 cycles of BCLK for an ADPCM transfer. The EN1 output is high for one BCLK period at the end of the frame (i.e., during the 256th BCLK period). In ST-BUS mode, the output strobes EN1 and ENB2/ $\overline{F0od}$ are adjusted to accommodate the required PCM I/O streams. The EN1 output becomes a single bit high true pulse during the last clock period of the frame (i.e., the 256th bit period) while ENB2/ $\overline{F0od}$ becomes a delayed, low true frame-pulse ($\overline{F0od}$) output occurring during the 64th bit period after the EN1 rising edge.

Linear PCM on PCMi1 and PCMi2, are received as 14-bit, two's complement data with three bits of sign extension in the most significant positions (i.e., S,S,S,12,...1,0) for a total of 16 bits. The linear PCM data transmitted from PCMo1 and PCMo2 are 16-bit, two's complement data with one sign bit in the most significant position (i.e., S,14,13,...1,0)

32 and 24 kbit/s ADPCM mode

In 32 kbit/s and 24 kbit/s linear mode, the 16-bit uniform PCM dual-octets of the B1, B2, B3 and B4 channels (from PCMi1 and PCMi2) are compressed into four 4-bit words on ADPCM_o. The four 4-bit ADPCM words of the B1, B2, B3 and B4 channels from ADPCM_i are expanded into four 16-bit uniform PCM dual-octets on PCMo1 and PCMo2. 16-bit uniform PCM are received and transmitted most significant bit first starting with b15 and ending with b0. ADPCM data are transferred most significant bit first starting with I1 and ending with I4 for 32 kbit/s and ending with I3 for 24 kbit/s operation (i.e., I4 is don't care).(See Figures 5 & 8.)

16 kbit/s ADPCM mode

When SEL is set to 0, the four, 2-bit ADPCM words are transmitted/received on ADPCM_o/i during the ENB1 timeslot in SSI mode and during the B1 timeslot in ST-BUS mode. When SEL is set to 1, the four, 2-bit ADPCM words are transmitted/received on ADPCM_o/i during the ENB2 timeslot in SSI mode and during the B2 timeslot in ST-BUS mode. (See Figures 5 & 8.)

PCM Law Control ($A/\overline{\mu}$, FORMAT)

The PCM companding/coding law invoked by the transcoder is controlled via the $A/\overline{\mu}$ and FORMAT pins. ITU-T G.711 companding curves, μ -Law and A-Law, are selected by the $A/\overline{\mu}$ pin (0= μ -Law; 1=A-Law). Per sample, digital code assignment can conform to ITU-T G.711 (when FORMAT=1) or to Sign-Magnitude coding (when FORMAT=0). Table 1 illustrates these choices.

PCM Code	FORMAT		
	Sign-Magnitude $A/\overline{\mu} = 0 \text{ or } 1$	0	1
		ITU-T (G.711)	
		$(A/\overline{\mu} = 0)$	$(A/\overline{\mu} = 1)$
+ Full Scale	1111 1111	1000 0000	1010 1010
+ Zero	1000 0000	1111 1111	1101 0101
- Zero	0000 0000	0111 1111	0101 0101
- Full Scale	0111 1111	0000 0000	0010 1010

Table 1 - Companded PCM

Power Down

Setting the $\overline{\text{PWRDN}}$ pin low will asynchronously cause all internal operation to halt and the device to go to a power down condition where no internal clocks are running. Output pins C2o, EN1, EN2, PCMo1, PCMo2 and ADPCMo and I/O pin $\overline{\text{F0od/ENB2}}$ are forced to a high-impedance state. Following the reset (i.e., $\overline{\text{PWRDN}}$ pin brought high) and assuming that clocks are applied to the MCLK and BCLK pins, the internal clocks will still not begin to operate until the first frame alignment is detected on the ENB1 pin for SSI mode or on the $\overline{\text{F0i}}$ pin for ST-BUS mode. The C2o clock and EN1, EN2 pins will not start operation until a valid frame pulse is applied to the $\overline{\text{F0i}}$ pin. If the $\overline{\text{F0i}}$ pin remains low for longer than 2 cycles of MCLK then the C2o pin will stop toggling and will stay low. If the $\overline{\text{F0i}}$ pin is held high then the C2o pin will continue to operate. In ST-BUS mode the EN1 and EN2 pins will stop toggling if the frame pulse ($\overline{\text{F0i}}$) is not applied every frame.

Master Clock (MCLK)

A minimum 4096 kHz master clock is required for execution of the transcoding algorithm. The algorithm requires 512 cycles of MCLK during one frame for proper operation. For SSI operation this input, at the MCLK pin, may be asynchronous with the 8 kHz frame provided that the lowest frequency and deviation due to clock jitter still meets the strobe period requirement of a minimum of $512 t_{\text{C4P}} - 25\%t_{\text{C4P}}$ (see Figure 3). For example, a system producing large jitter values can be accommodated by running an over-speed MCLK that will ensure a minimum 512 MCLK cycles per frame is obtained. The minimum MCLK period is 61 nSec, which translates to a maximum frequency of 16.384 MHz. Extra MCLK cycles ($>512/\text{frame}$) are acceptable since the transcoder is aligned by the appropriate strobe signals each frame.

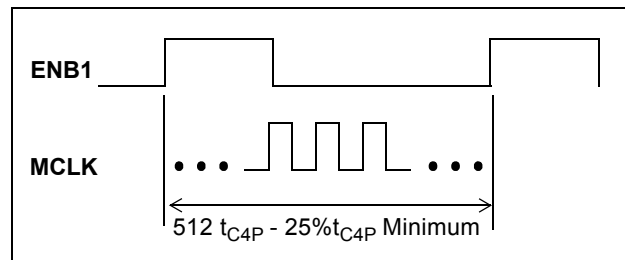


Figure 3 - MCLK Minimum Requirement

Bit Clock (BCLK)

For SSI operation the bit rate, for both ADPCM and PCM ports, is determined by the clock input at BCLK. BCLK must be eight periods in duration and synchronous with the 8 kHz frame inputs at ENB1 and ENB2. Data is sampled at PCMi1/2 and at ADPCMi concurrent with the falling edge of BCLK. Data is available at PCMo1/2 and ADPCMo concurrent with the rising edge of BCLK. BCLK may be any rate between 128 kHz and 4096 kHz. For ST-BUS operation BCLK is ignored (tie to V_{SS}) and the bit rate is internally set to 2048 kbit/s.

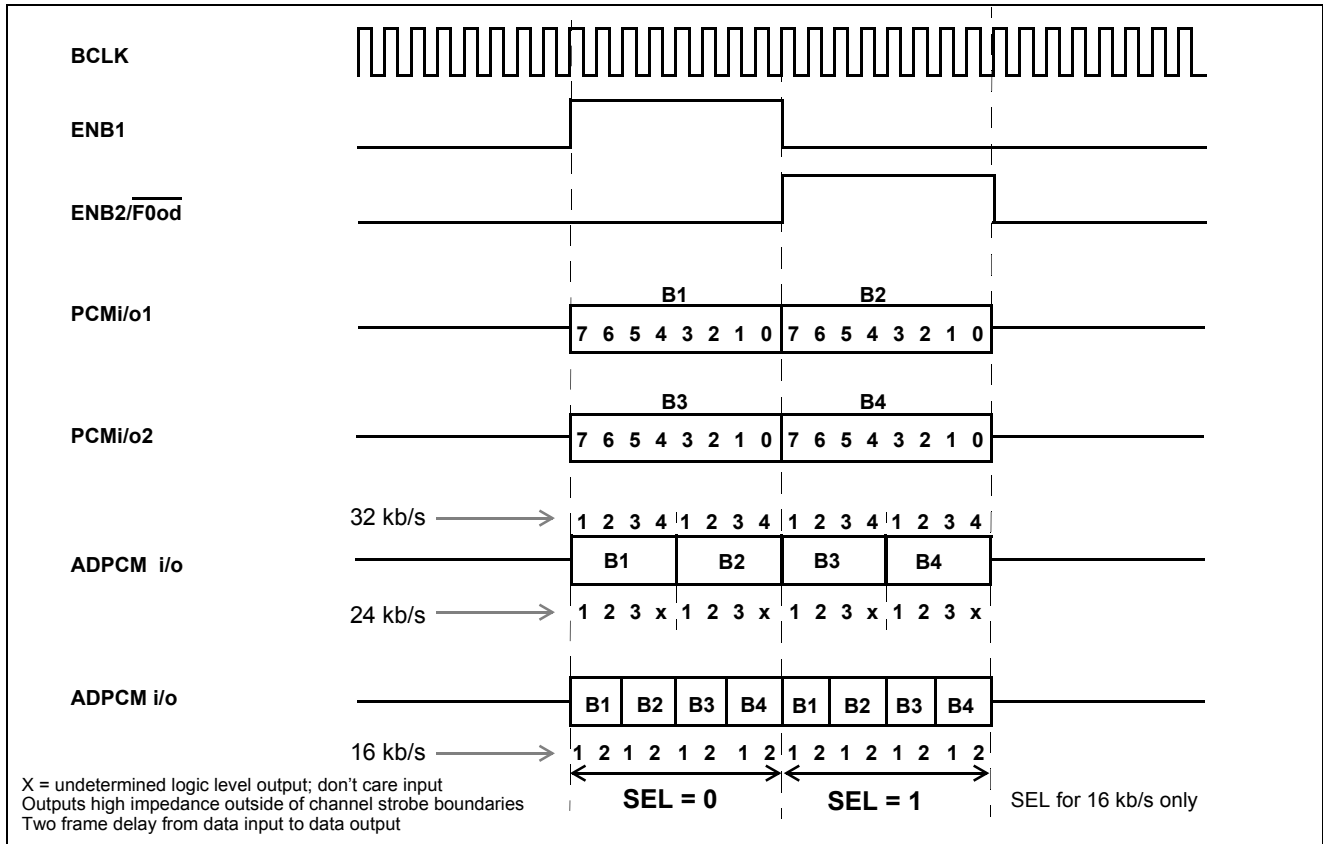


Figure 4 - SSI 8-Bit Companded PCM Relative Timing

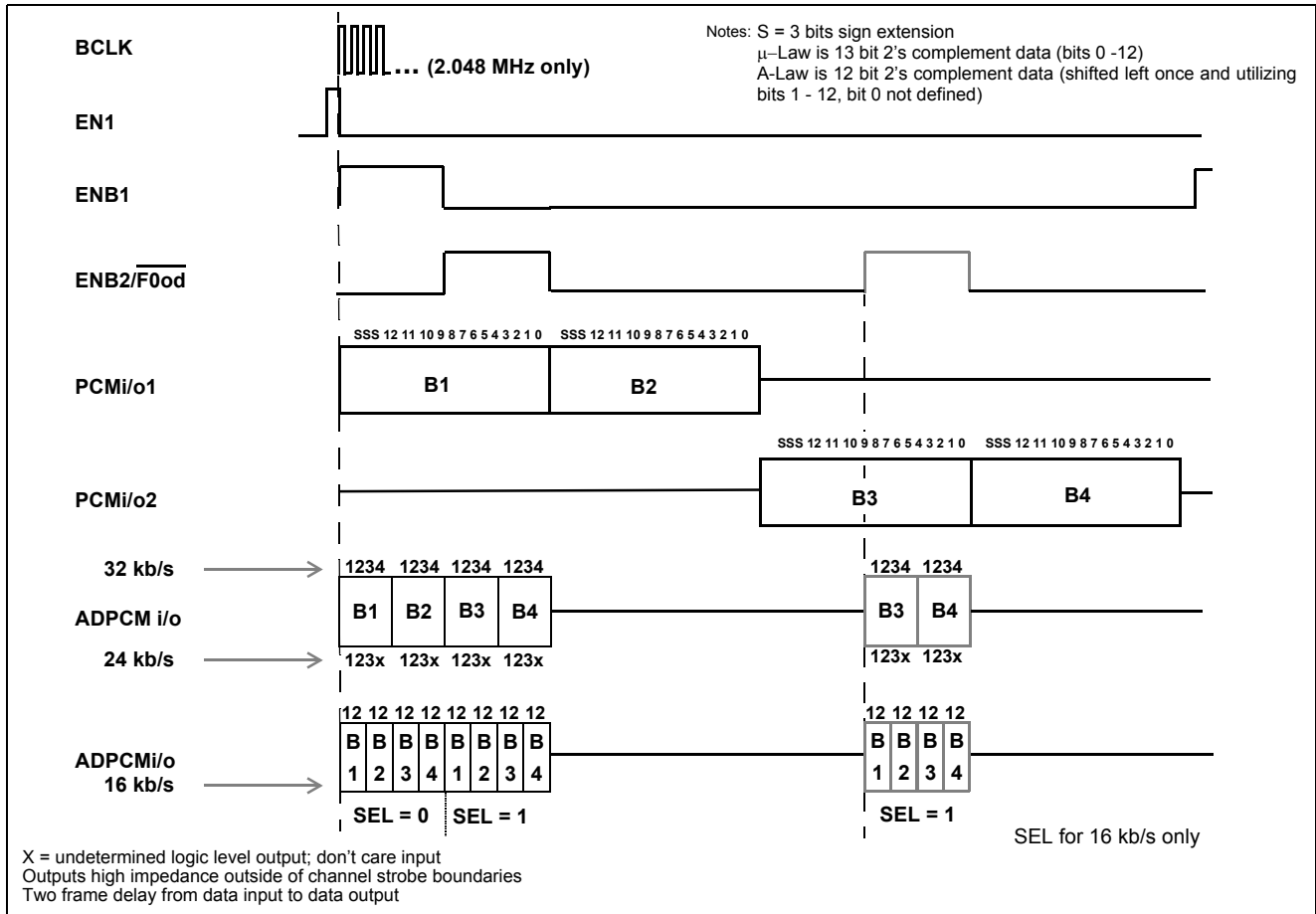


Figure 5 - SSI 16-Bit Linear PCM Relative Timing

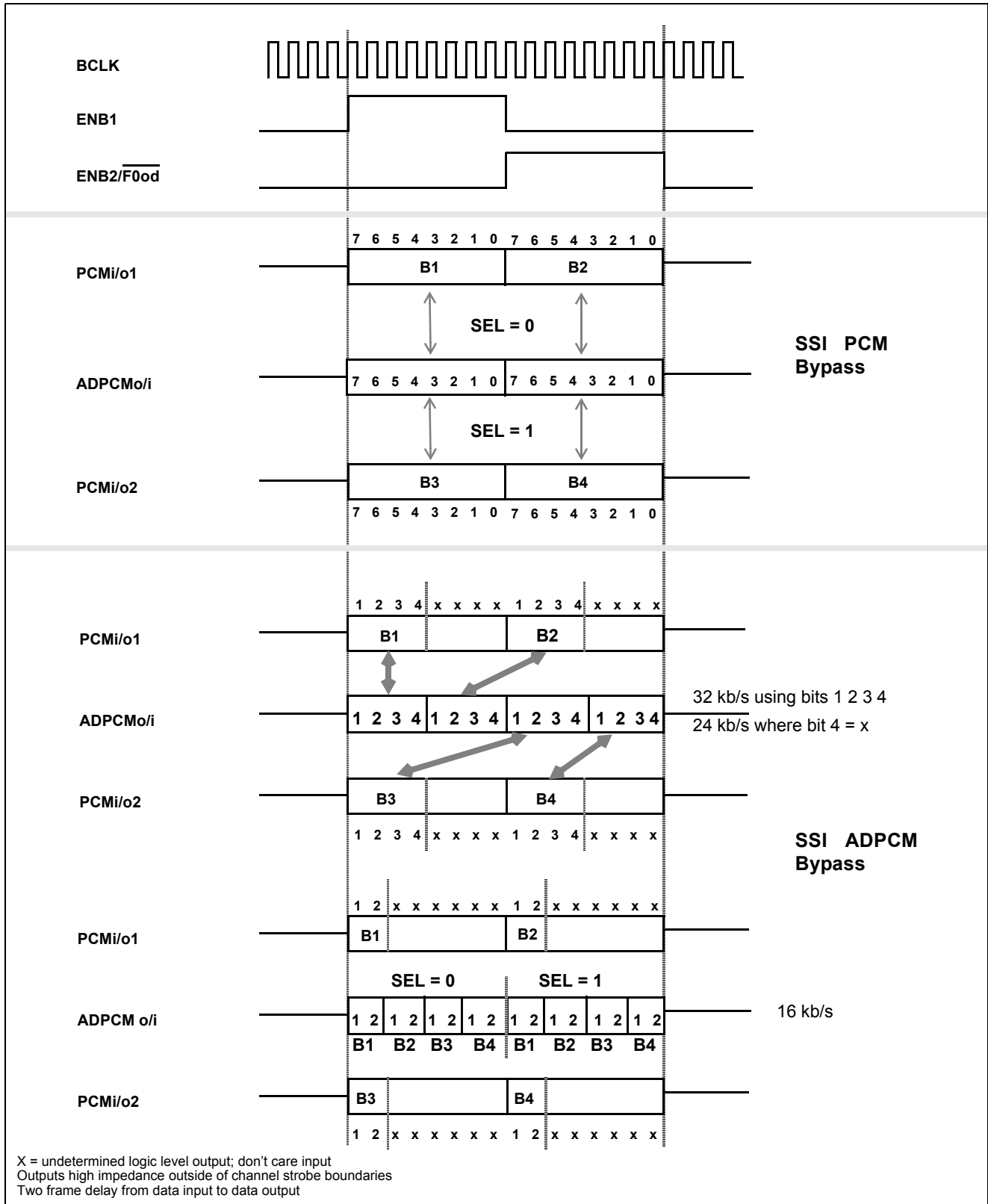


Figure 6 - SSI PCM and ADPCM Bypass Relative Timing

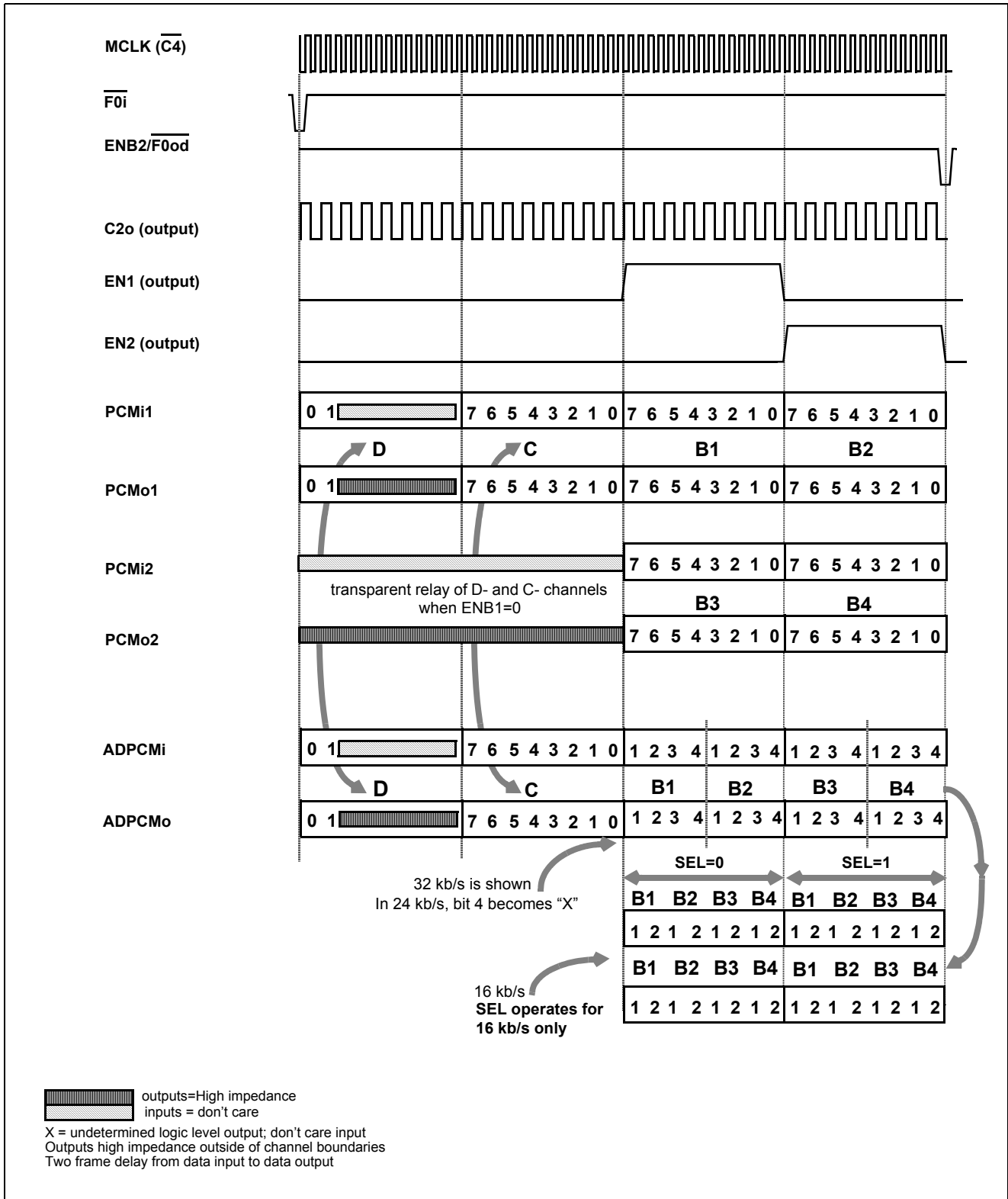


Figure 7 - ST-BUS 8-bit Companded PCM Relative Timing

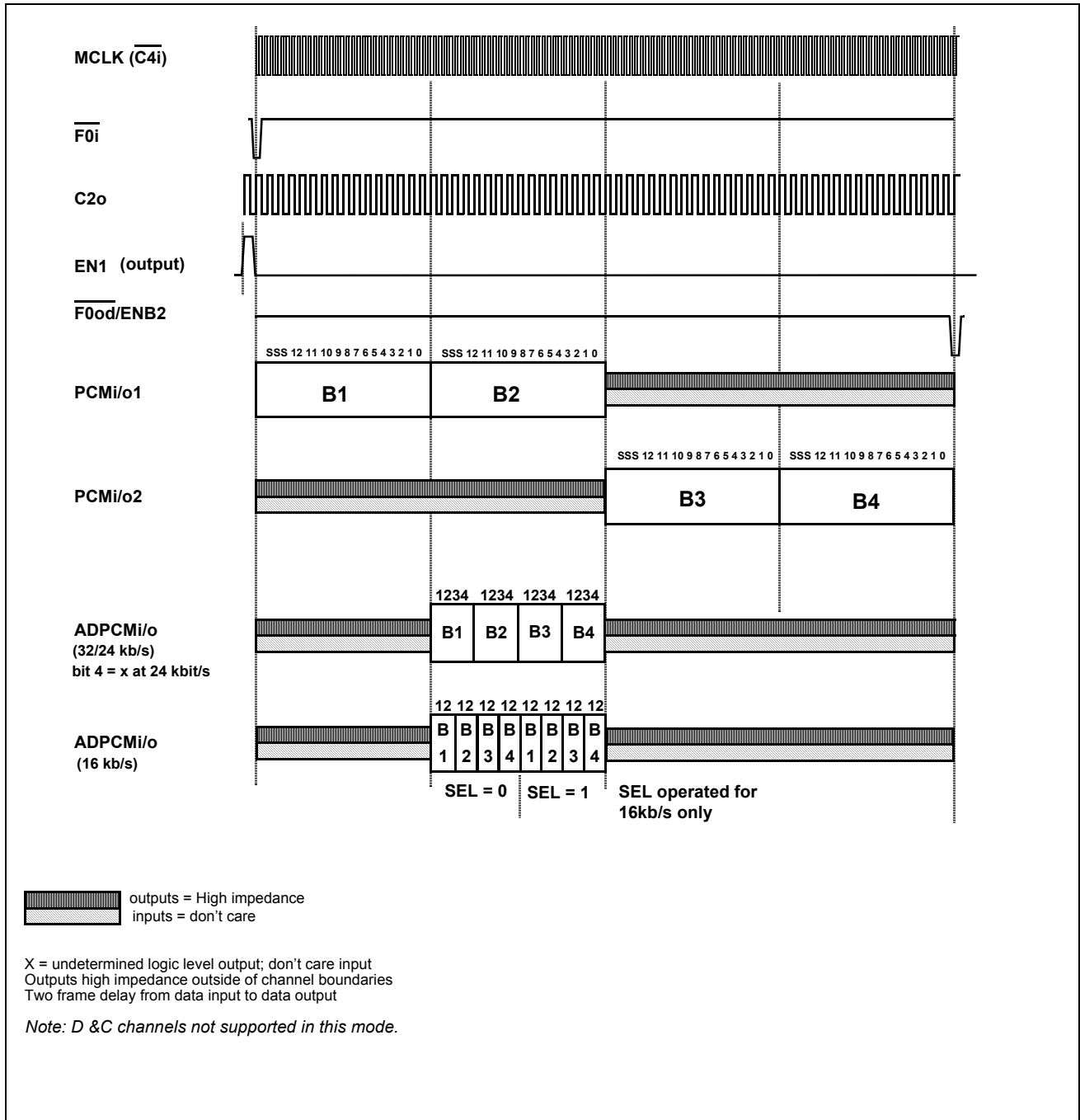


Figure 8 - ST-BUS 16-bit Linear PCM Relative Timing

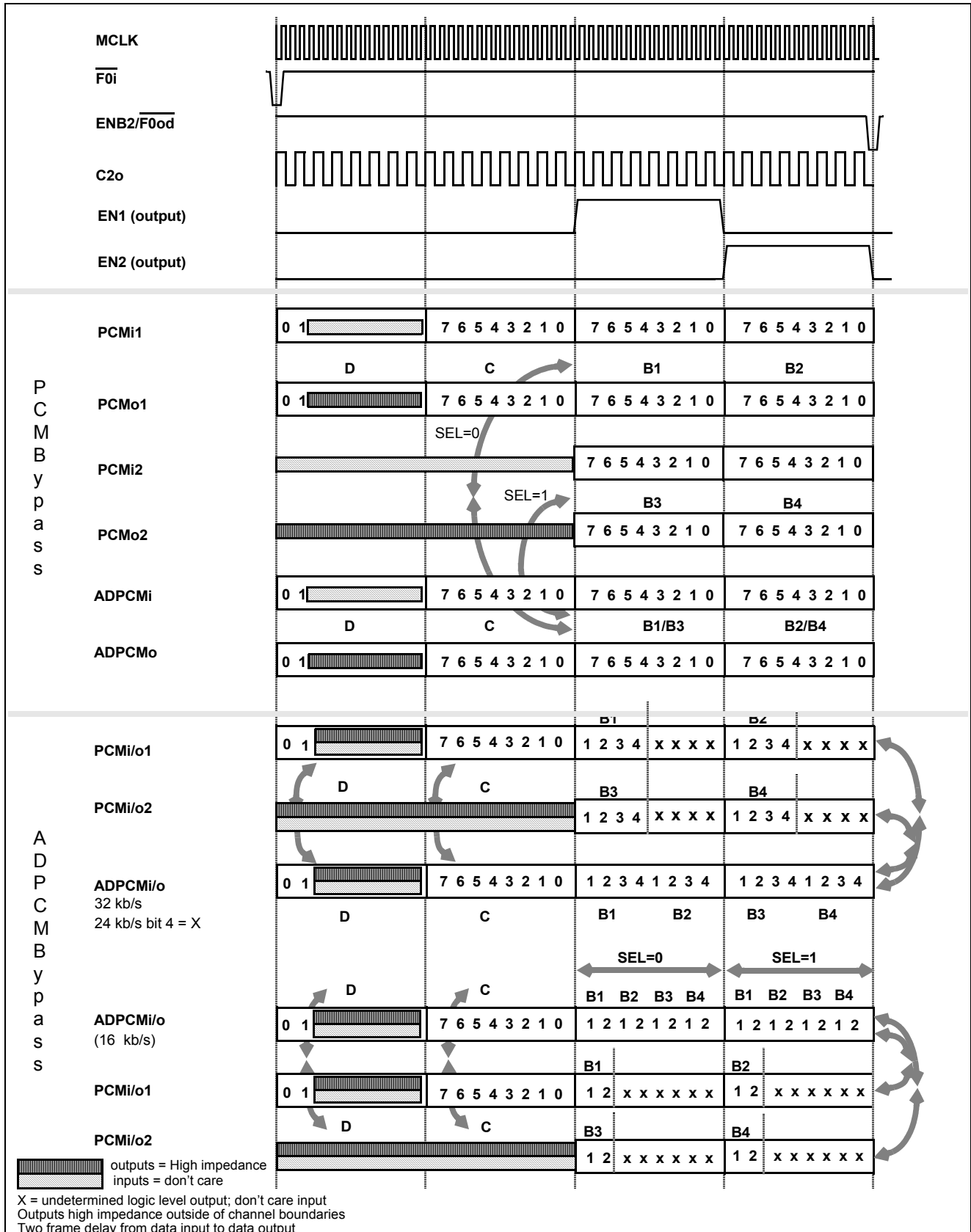


Figure 9 - ST-BUS PCM and ADPCM Bypass Relative Timing

Processing Delay Through the Device

In order to accommodate variable rate PCM and ADPCM interfaces, the serial input and output streams require a complete frame to load internal shift registers. Internal frame alignment of the encoding/decoding functions are taken from either of the $\overline{F0i}$ or ENB1 & ENB2 input strobes depending upon the device operating mode (i.e., ST-BUS or SSI). The encoding/decoding of all channels then takes one frame to complete before the output buffers are loaded. This results in a two frame transcoding delay. The two frame delay also applies to the D and C channels and to the PCM and ADPCM bypass functions. (See Figure 10.)

Note: When changing the relative positions of the ENB1 and ENB2 strobes, precaution must be taken to ensure that two conditions are met. They are:

1. There must be at least 512 master clock cycles between consecutive rising edges of ENB1. This condition also holds true for ENB2.
2. The ENB1 strobe must alternate with the ENB2 strobe.

Violation of these requirements may cause noise on the output channels.

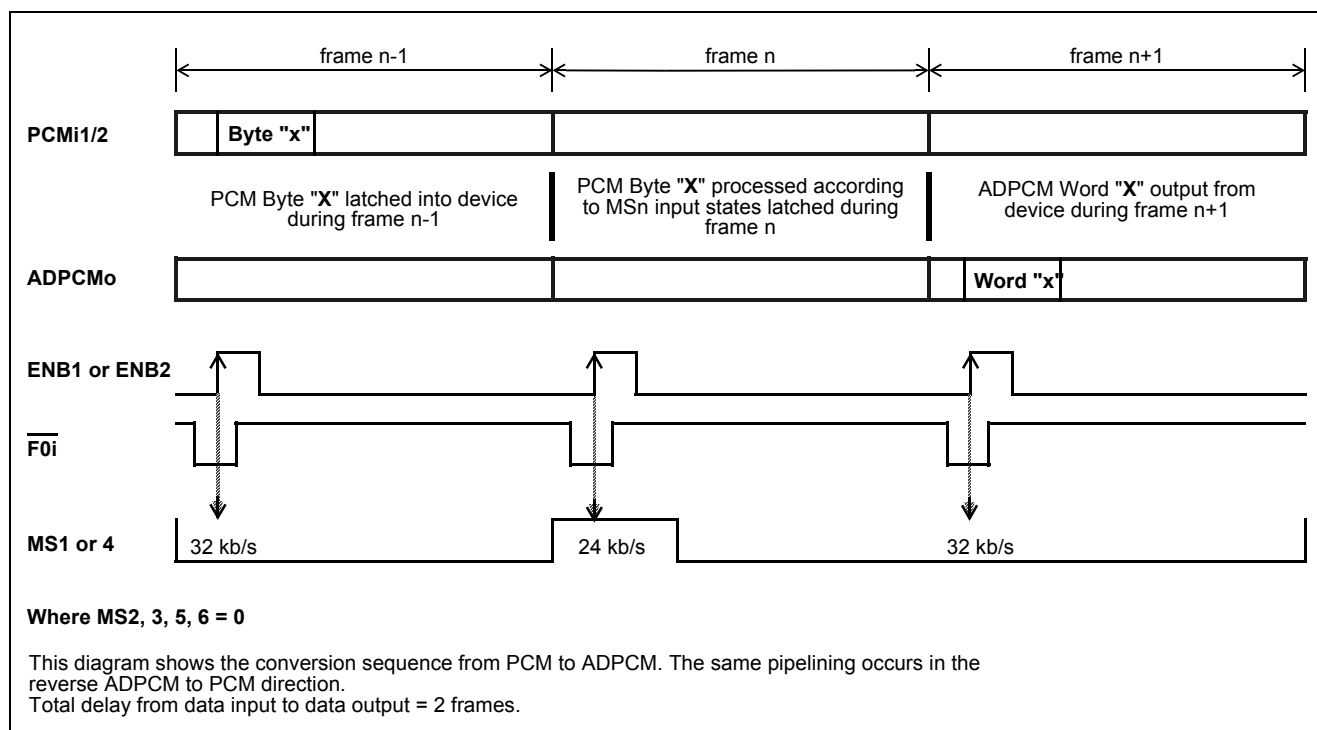


Figure 10 - Data Throughput

Applications

Figure 11 depicts an ISDN line card utilizing the MT8910 'U' interface transceiver and MT9126 ADPCM transcoder. This central office application implements the network end of a Pair-Gain system. Figure 12 shows Zarlink devices used to construct the remote Pair-Gain loop terminator.

Figure 13 depicts an ADPCM to linear PCM converter for applications where further, value added, functions are being performed via digital signal processor. Access to linear coded PCM reduces the overhead of the DSP by removing the need for a companded to linear conversion. The linear PCM capability of the ADPCM transcoder in conjunction with the frame alignment signal EN1 allows direct connection to the serial port of both Motorola and Texas Instruments Digital Signal Processors. Daisy-chaining via the delayed frame strobe output ensures that the ADPCM array is distributed over the complete 2048 kbit bandwidth. If the DSP has a second serial port then access

to the processed PCM can be had directly. For processors with only one serial port the MT8920 connected to the DSP parallel port will provide serial access by parallel to serial conversion. The same daisy-chained arrangement of Quad ADPCM transcoders will provide a general system resource for PCM-ADPCM conversion by setting the device to non-linear operation.

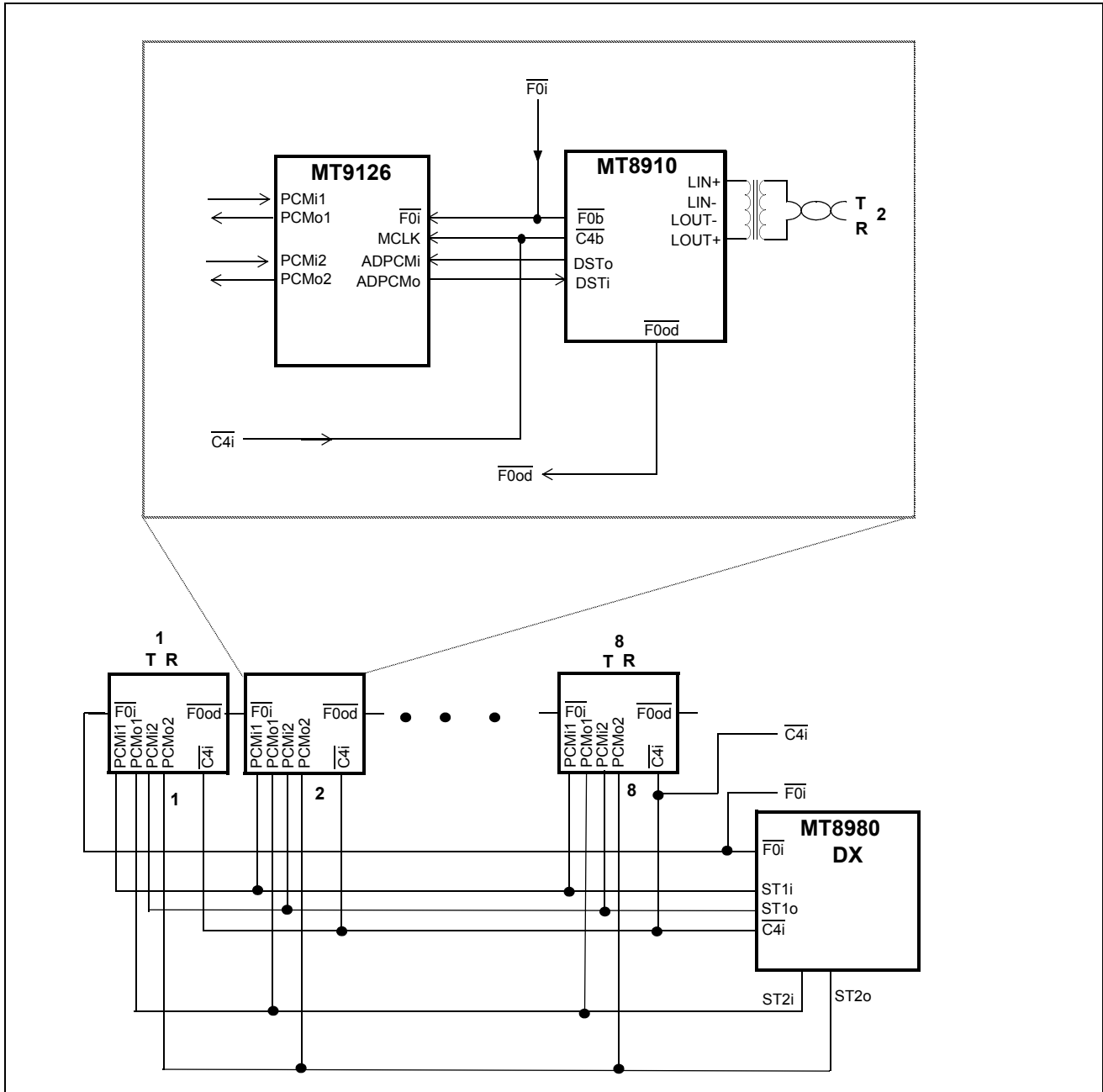


Figure 11 - ISDN Line Card with 32 kbit/s ADPCM

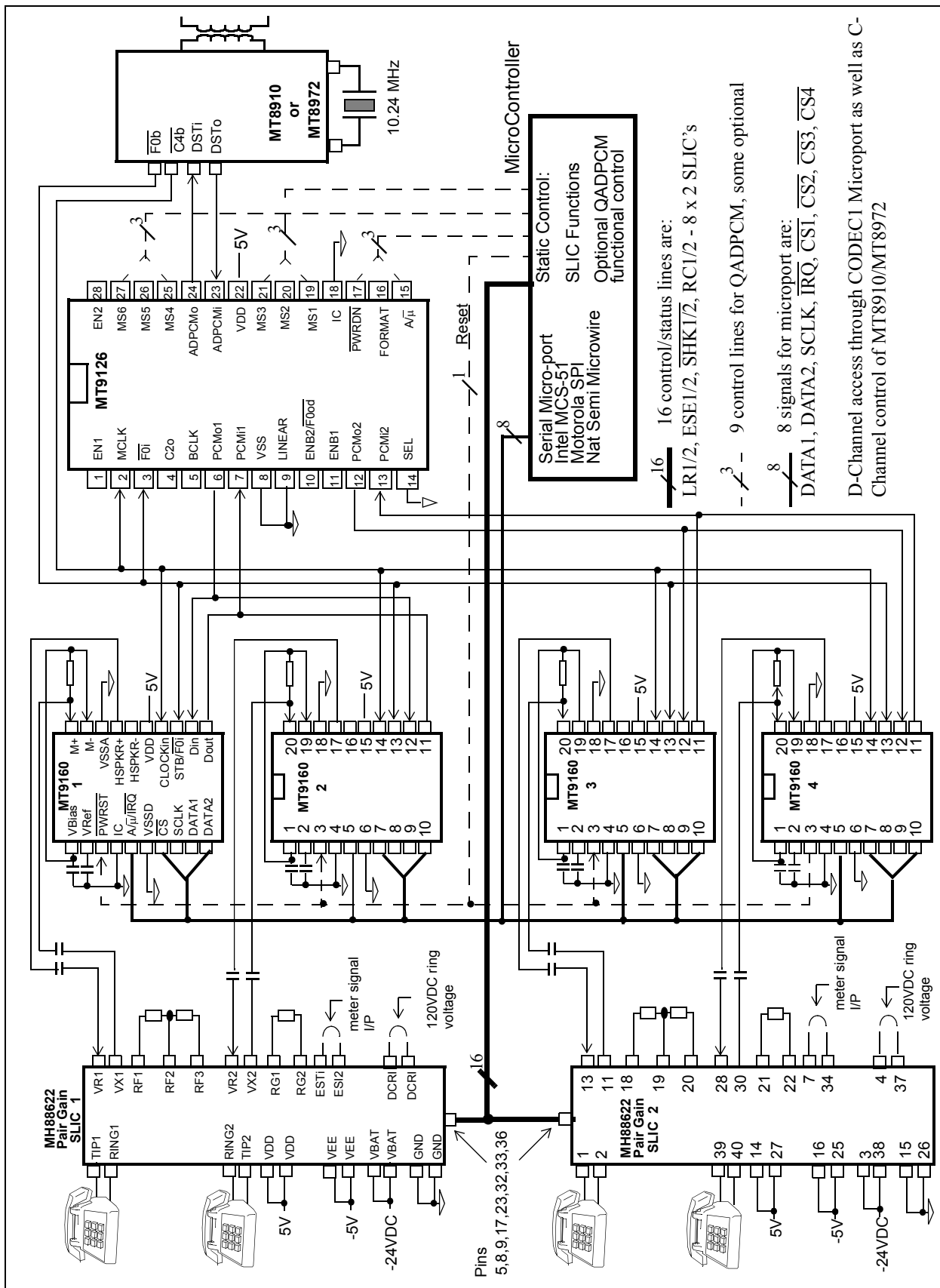


Figure 12 - Pair Gain Remote Terminal Utilizing Zarlink Components

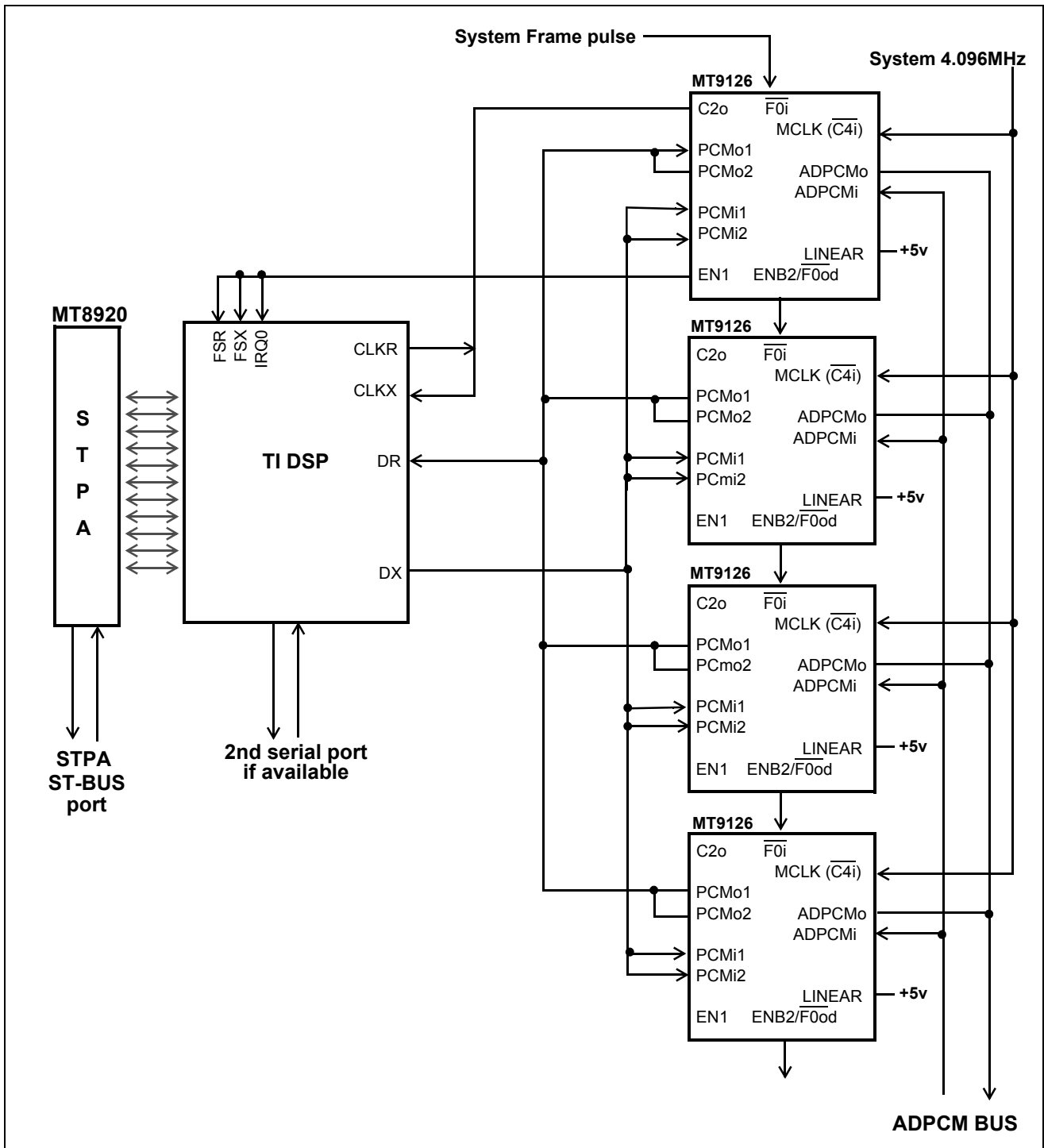


Figure 13 - ST-BUS to DSP Platform

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	$V_{DD}-V_{SS}$	-0.3	7.0	V
2	Voltage on any I/O pin	$V_i V_o$	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	Continuous Current on any I/O pin	$I_i I_o$		± 20	mA
4	Storage Temperature	T_{ST}	-65	150	°C
5	Package Power Dissipation	P_D		500	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
2	TTL Input High Voltage		2.4		V_{DD}	V	400 mV noise margin
3	TTL Input Low Voltage		V_{SS}		0.4	V	400 mV noise margin
4	CMOS Input High Voltage		4.5		V_{DD}	V	
5	CMOS Input Low Voltage		V_{SS}		0.5	V	
6	Operating Temperature	T_A	-40		+85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions	
1		Supply Current	I_{CC} I_{DD}		5	100	μA mA	$\overline{PWRDN} = 0$ $PWRDN = 1$, clocks active	
2		Input HIGH voltage (TTL)	V_{IH}	2.0			V		
3		Input LOW voltage (TTL)	V_{IL}			0.8	V		
4	M C L K	Input HIGH voltage (CMOS)	V_{IHC}	3.5			V		
5		Input LOW voltage (CMOS)	V_{ILC}			1.5	V		
6		Input leakage current	I_{IH}/I_{IL}		0.1	10	μA	$V_{IN}=V_{SS}$ to V_{DD}	
7		High level output voltage	V_{OH}	2.4			V	$I_{OL}=5.0$ mA	
8		Low level output voltage	V_{OL}				0.4	V	$I_{OL}=5.0$ mA
9		High impedance leakage	I_{OZ}		1	10	μA	$V_{IN}=V_{SS}$ to V_{DD}	
10		Output capacitance	C_o		10		pF		
11		Input capacitance	C_i		8		pF		
12	P W R D N	Positive Threshold Voltage Hysteresis Negative Threshold Voltage	V^+ V_H V^-	3.7	1.0	1.3	V V V		

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* DC Electrical Characteristics are over recommended temperature and supply voltage.

AC Electrical Characteristics[†] - Serial PCM/ADPCM Interfaces (see Figure 14)Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ. [†]	Max.	Units	Test Conditions
1	BCLK Clock High	t_{BCH}	80			ns	
2	BCLK Clock Low	t_{BCL}	80			ns	
3	BCLK Period	t_{BCP}	200		7900	ns	
4	Data Output Delay (excluding first bit)	t_{DD}		60		ns	$C_L=150pF//R_L=1K$
5	Output Active to High Z	t_{AHZ}		60		ns	$C_L=150pF//R_L=1K$
6	Strobe Signal Setup	t_{SSS}	80		$t_{BCL}-80$	ns	
7	Strobe Signal Hold	t_{SSH}	80		$t_{BCL}-80$	ns	
8	Data Input Setup	t_{DIS}	50			ns	
9	Data Input Hold	t_{DIH}	50			ns	
10	Strobe to Data Delay (first bit)	t_{SD}		60		ns	$C_L=150pF//R_L=1K$
11	\overline{FOi} Setup	t_{FOiS}	50	122	150	ns	
12	\overline{FOi} Hold	t_{FOiH}	50	122	150	ns	
13	MCLK ($\overline{C4i}$) duty cycle	$t_H/t_L \times 100$	40	50	60	%	
14	\overline{FOod} Delay	t_{DFD}			60	ns	$C_L=150pF//R_L=1K$
15	\overline{FOod} Pulse Width	t_{DFW}		244		ns	$C_L=150pF//R_L=1K$
16	MCLK ($\overline{C4i}$) period	t_{C4P}	61		244.2	ns	
17	Data Output delay	t_{DSD}			95	ns	$C_L=150pF//R_L=1K$
18	Data in Hold time	t_{DSH}	50			ns	
19	Data in Setup time	t_{DSS}	50			ns	

[†] Timing is over recommended temperature & power supply voltages.[‡] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

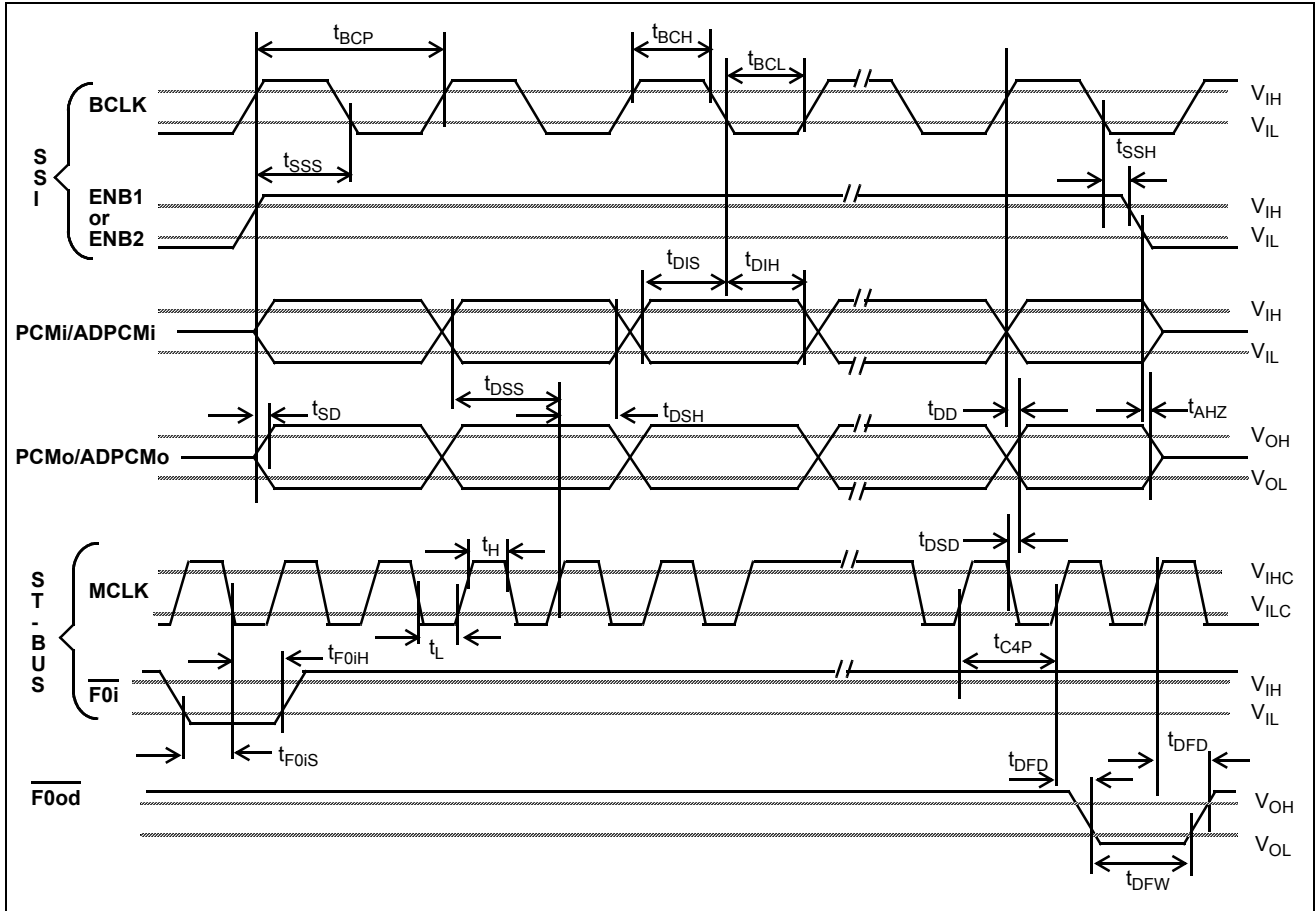


Figure 14 - Serial Port Timing

AC Electrical Characteristics† - ST-BUS C2o Conversion

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.†	Max.	Units	Test Conditions
1	Delay MCLK falling to C2o rising	t_{D1}		100		ns	150pF//1K Load
2	Delay MCLK falling to Enable	t_{D2}		100		ns	150pF//1K Load

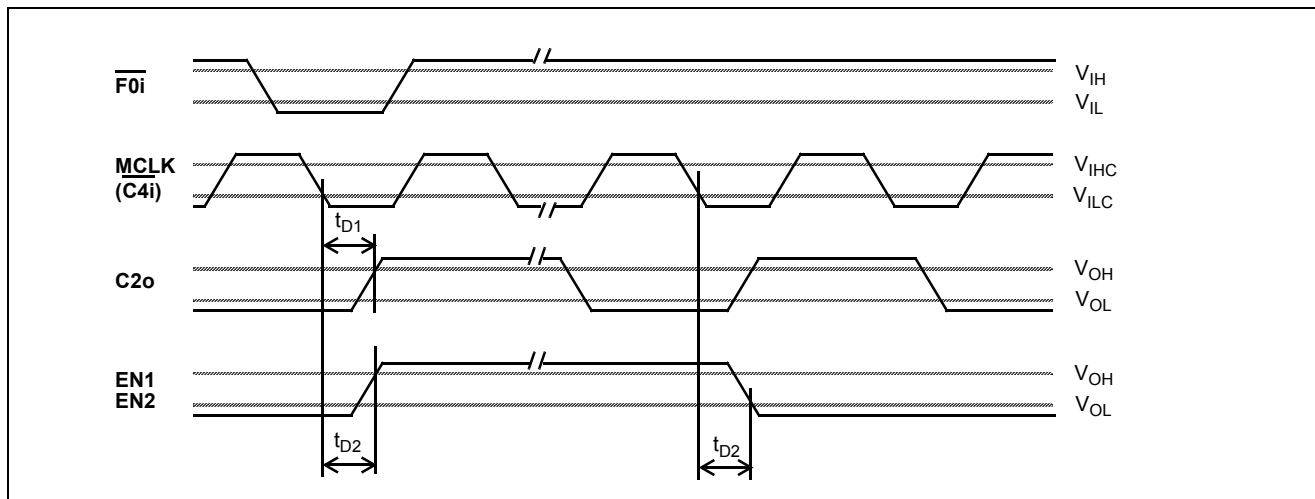


Figure 15 - ST-BUS Timing for External Signal Generation

AC Electrical Characteristics† - Mode Select Timing (see Figures 16 & 17)

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.†	Max.	Units	Test Conditions
1	Mode Select Setup	t_{SU}	500			ns	MCLK=4096 kHz
2	Mode Select Hold	t_{HOLD}	500			ns	

† Timing is over recommended temperature & power supply voltages.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

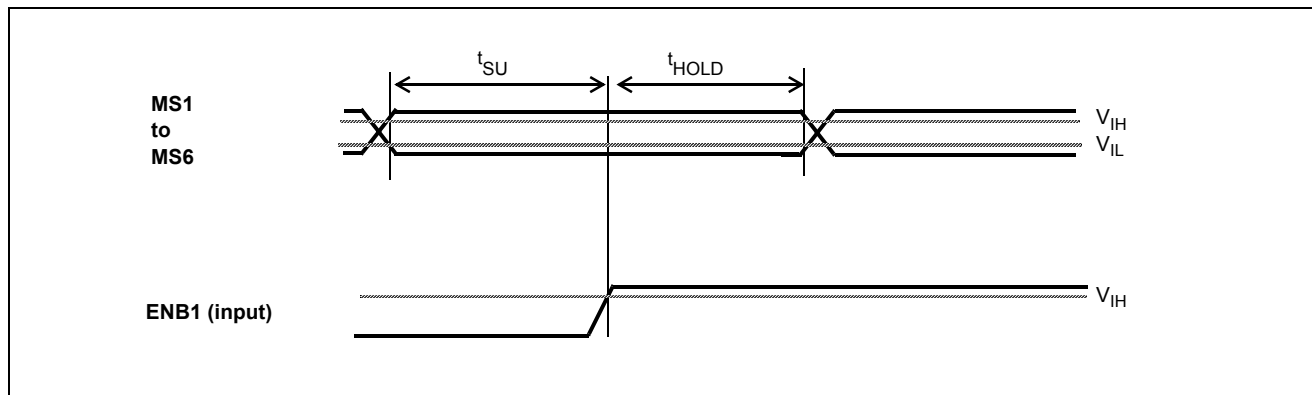


Figure 16 - SSI Mode Select Set-up and Hold Timing

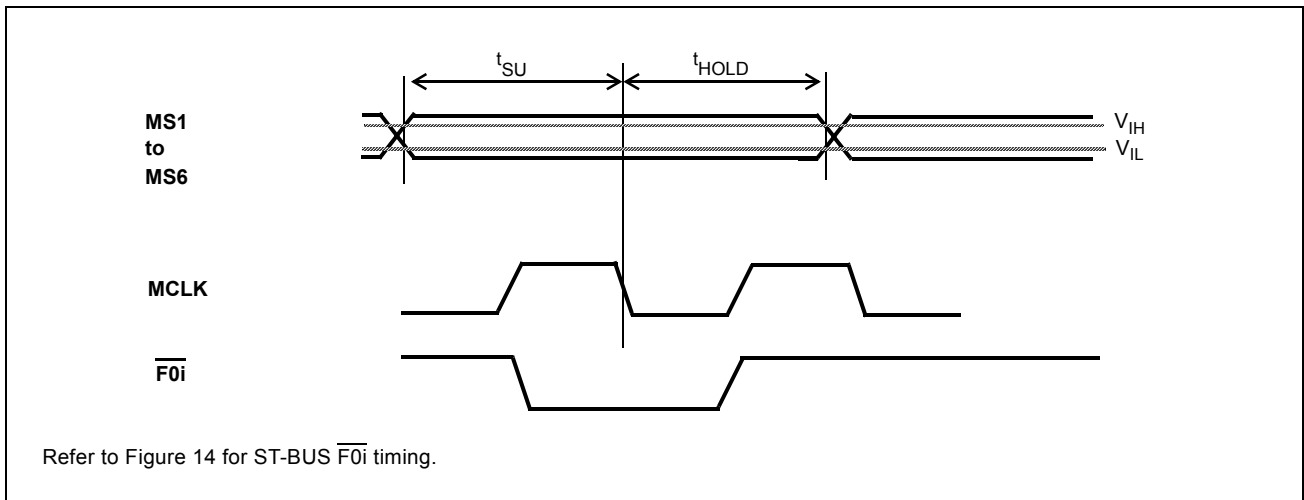
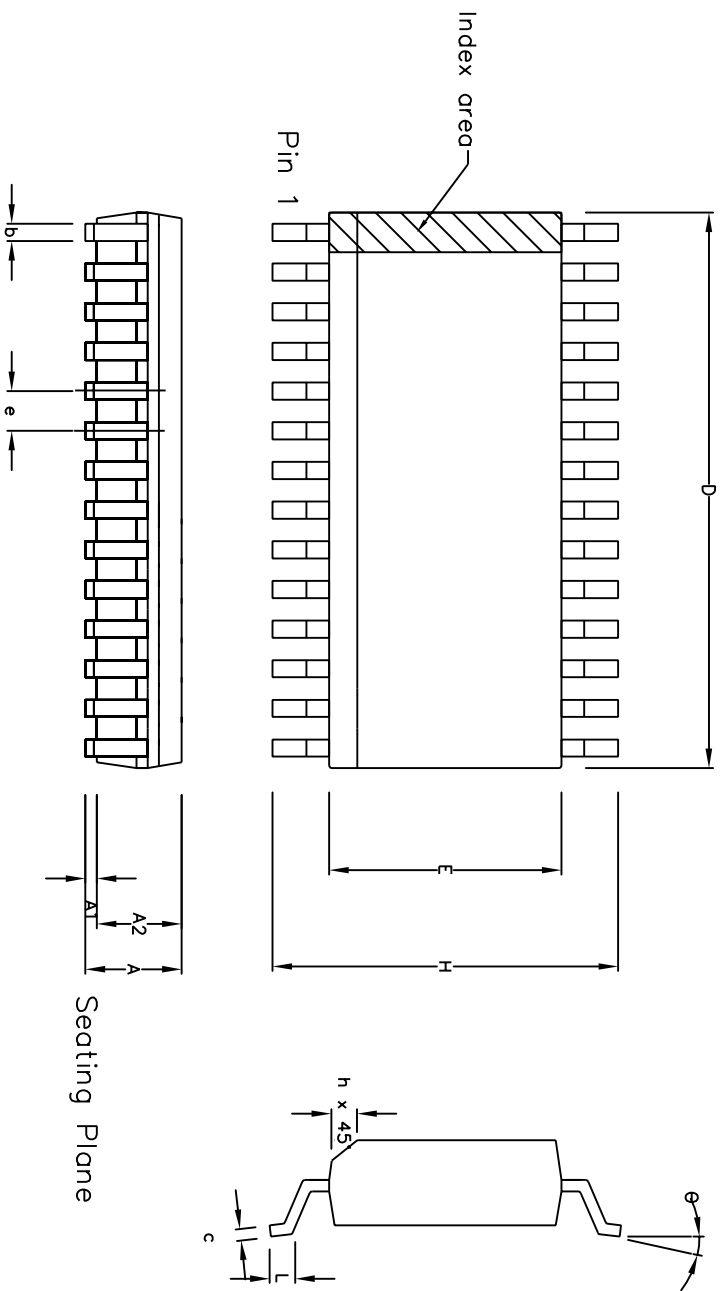


Figure 17 - ST-BUS Mode Select Set-up and Hold Timing



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches		
	MIN	Nominal	MAX	MIN	Nominal	MAX
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
A2	2.25		2.35	0.089		0.092
D	17.70		18.10	0.697		0.713
H	10.00		10.65	0.394		0.419
E	7.40		7.60	0.291		0.299
L	0.40		1.27	0.016		0.050
e	1.27 BSC.			0.050 BSC.		
b	0.33		0.51	0.013		0.020
c	0.23		0.32	0.009		0.013
θ	0°		8°	0°		8°
h	0.25		0.75	0.010		0.029
Pin features						
28						
N						
Conforms to JEDEC MS-013AE Iss. C						

- Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
 2. Controlling dimension are in millimeters.
 3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
 4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
 5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

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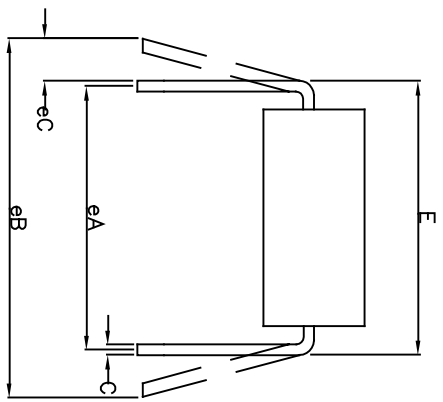
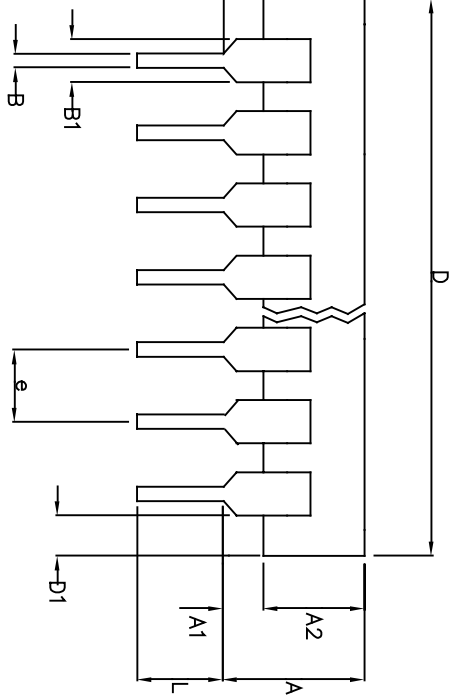
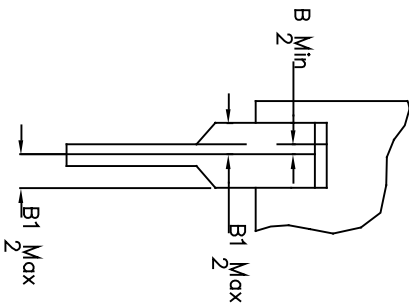
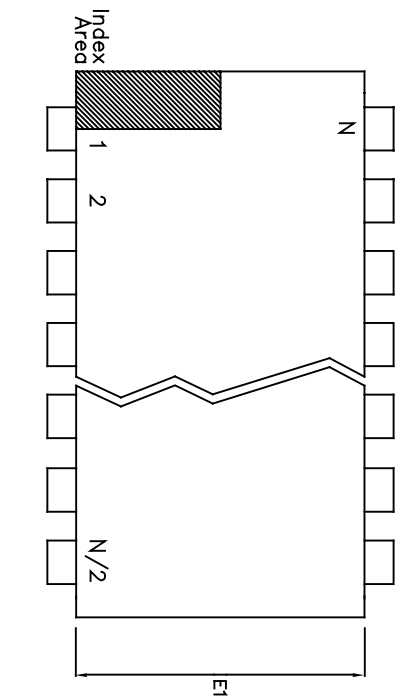
Previous package codes

MP / S

Package Code DC

Package Outline for
28 lead SOIC
(0.300" Body Width)

GPD000017



	Min	Max	Min	Max
	mm	mm	Inches	Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	35.05	39.75	1.380	1.565
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54	BSC	0.100	BSC
eA	15.24	BSC	0.600	BSC
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N		28		28

Conforms to Jedec MS-011AB ISS.B

Controlling Dimensions are in inches
 Dimension A, A1 and L are measured with the package seated in the Seating Plane
 Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
 Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
 Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

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1	2	3	4
7010	203532	213102	CDCA
20Apr95	25Nov97	15Jul02	02Dec05



Previous package codes

DP / E

Package Code DA

Package Outline for 28 lead 600mils PDIP

GPD00072



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