MT8816
ISO-CMOS 8 x 16 Analog Switch Array

Data Sheet

Features

September 2011

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5 V to 13.2 V
- 12Vpp analog signal capability
- R_{ON} 65 Ω max. @ V_{DD} = 12 V, 25°C
- ΔR_{ON} ≤10 Ω @ V_{DD} = 12 V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Separate analog and digital reference supplies
- Low power consumption ISO-CMOS technology

Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment/instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Ordering Information

MT8816AP1	44 Pin PLCC*	Tubes
MT8816APR1	44 Pin PLCC*	Tape & Reel
MT8816AE1	40 Pin PDIP*	Tubes
MT8816AF1	44 Pin TQFP*	Trays

* Pb Free Matte Tin

-40°C to +85°C

Description

The Zarlink MT8816 is fabricated in Zarlink's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8 x 16 array of crosspoint switches along with a 7 to 128 line decoder and latch circuits. Any one of the 128 switches can be addressed by selecting the appropriate seven address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. V_{SS} is the ground reference of the digital inputs. The range of the analog signal is from V_{DD} to V_{EE}. Chip Select (CS) allows the crosspoint array to be cascaded for matrix expansion.

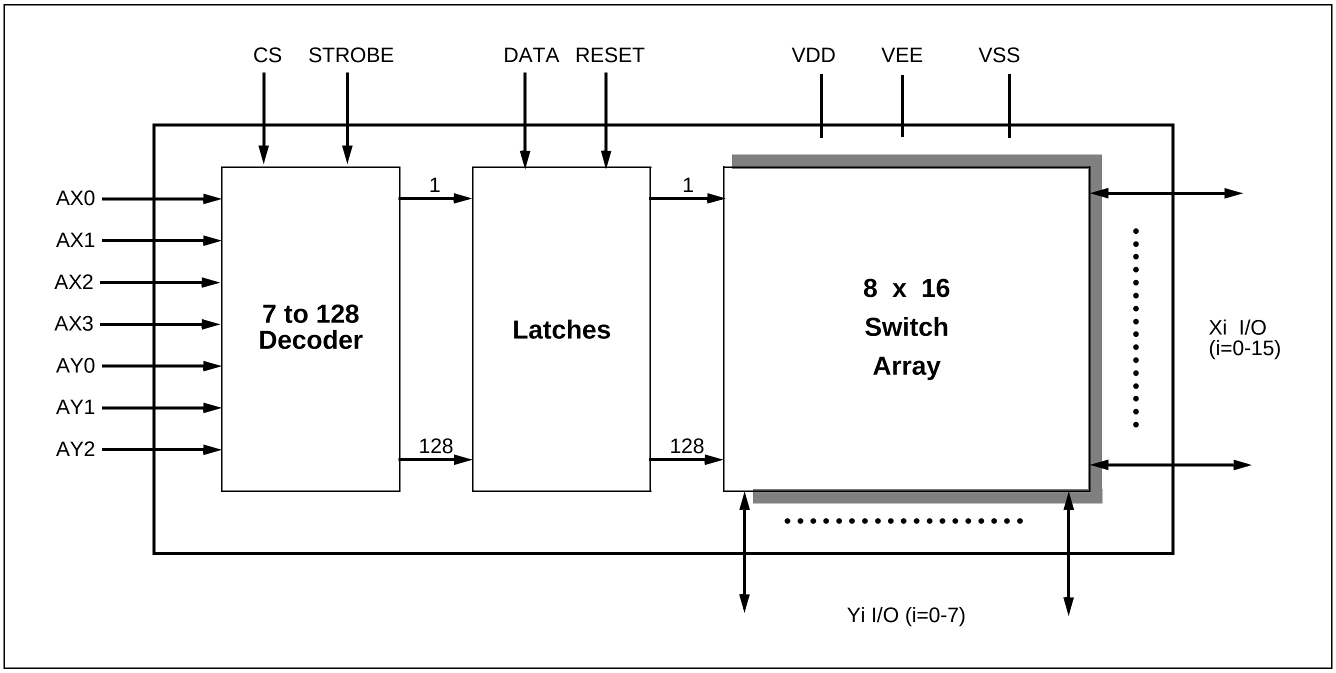


Figure 1 - Functional Block Diagram

Change Summary

Changes from the January 2010 issue to the September 2011 issue.

Page	Item	Change
1	Ordering Information	Removed leaded packages as per PCN notice.

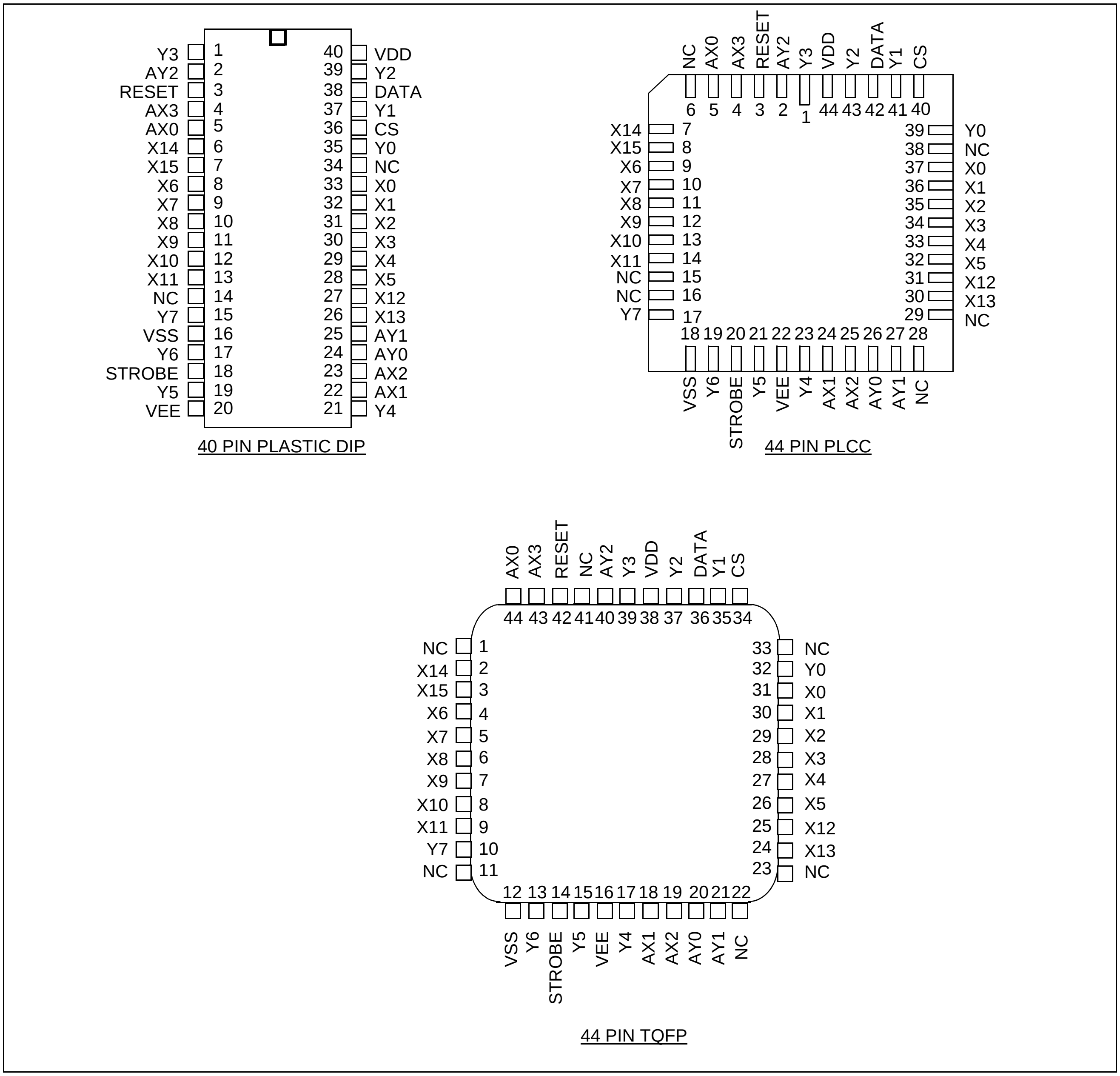


Figure 2 - Pin Connections

Pin Description

Pin #			Name	Description
TQFP	PDIP	PLCC		
39	1	1	Y3	**Y3 Analog (Input/Output):** this is connected to the Y3 column of the switch array.
40	2	2	AY2	**Y2 Address Line (Input)**.
42	3	3	RESET	**Master RESET (Input):** this is used to turn off all switches regardless of the condition of CS. Active High.
43,44	4,5	4,5	AX3,AX0	**X3 and X0 Address Lines (Inputs)**.
2, 3	6,7	7,8	X14, X15	**X14 and X15 Analog (Inputs/Outputs):** these are connected to the X14 and X15 rows of the switch array.
4-9	8-13	9-14	X6-X11	**X6-X11 Analog (Inputs/Outputs):** these are connected to the X6-X11 rows of the switch array.
41,1,11	14	6,15,16	NC	**No Connection**
10	15	17	Y7	**Y7 Analog (Input/Output):** this is connected to the Y7 column of the switch array.
12	16	18	V_{SS}	**Digital Ground Reference.**
13	17	19	Y6	**Y6 Analog (Input/Output):** this is connected to the Y6 column of the switch array.
14	18	20	STROBE	**STROBE (Input)**: enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
15	19	21	Y5	**Y5 Analog (Input/Output):** this is connected to the Y5 column of the switch array.
16	20	22	V_{EE}	**Negative Power Supply.**
17	21	23	Y4	**Y4 Analog (Input/Output):** this is connected to the Y4 column of the switch array.
18,19	22, 23	24,25	AX1,AX2	**X1 and X2 Address Lines (Inputs)**.
20,21	24, 25	26,27	AY0,AY1	**Y0 and Y1 Address Lines (Inputs)**.
24,25	26, 27	30,31	X13, X12	**X13 and X12 Analog (Inputs/Outputs):** these are connected to the X13 and X12 rows of the switch array.
26-31	28 - 33	32-37	X5-X0	**X5-X0 Analog (Inputs/Outputs):** these are connected to the X5-X0 rows of the switch array.
22,23,33	34	28,29, 38	NC	**No Connection.**
32	35	39	Y0	**Y0 Analog (Input/Output)**: this is connected to the Y0 column of the switch array.
34	36	40	CS	**Chip Select (Input)**: this is used to select the device. Active High.

Pin Description (continued)

Pin #			Name	Description
TQFP	PDIP	PLCC		
35	37	41	Y1	**Y1 Analog (Input/Output)**: this is connected to the Y1 column of the switch array.
36	38	42	DATA	**DATA (Input)**: a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
37	39	43	Y2	**Y2 Analog (Input/Output)**: this is connected to the Y2 column of the switch array.
38	40	44	V_{DD}	**Positive Power Supply.**

Functional Description

The MT8816 is an analog switch matrix with an array size of 8 x 16. The switch array is arranged such that there are 8 columns by 16 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 128 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the CS (Chip Select) and STROBE inputs are high and are latched on the falling edge of STROBE. A logical “1” written into a memory cell turns the corresponding crosspoint switch on and a logical “0” turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical “1” on the RESET input will asynchronously return all memory locations to logical “0” turning off all crosspoint switches regardless of whether CS is high or low. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the MT8816 to enable switching of negative analog signals. The range for digital signals is from V_{DD} to V_{SS} while the range for analog signals is from V_{DD} to V_{EE}. V_{SS} and V_{EE} pins can be tied together if a single voltage reference is needed.

Address Decode

The seven address inputs along with the STROBE and CS (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low and CS must go high while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

Applications

Figure 3 shows a typical Operating Circuit of a video surveillance system using analog crosspoint switches which allow multiple video sources switched to multiple output devices, e.g., video monitor, video recorder etc.

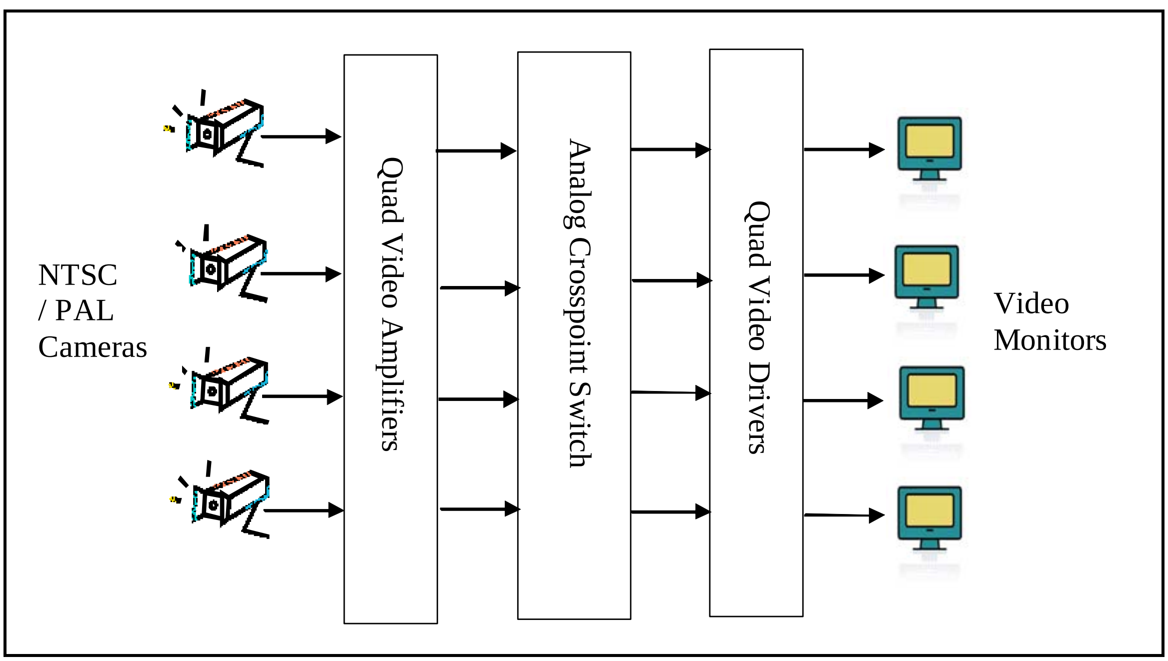


Figure 3 - Typical Video Surveillance System

Figure 4 illustrates the major components of a video surveillance system. In the center is the MT8816, a 16 x 8 analog cross-point IC. At the left are 16 video input buffers CLC2005 from Cadeka Microcircuits. At the right hand side are 8 video output buffers CLC2005 and each buffer is capable of driving a 75 ohm video load directly. BNC connectors are provided for all video inputs and video outputs.

A FT245R USB FIFO from Future Technology Devices International (FTDI) provides a standard USB interface for a PC. Through this USB connection the PC controls the switching of the video signals.

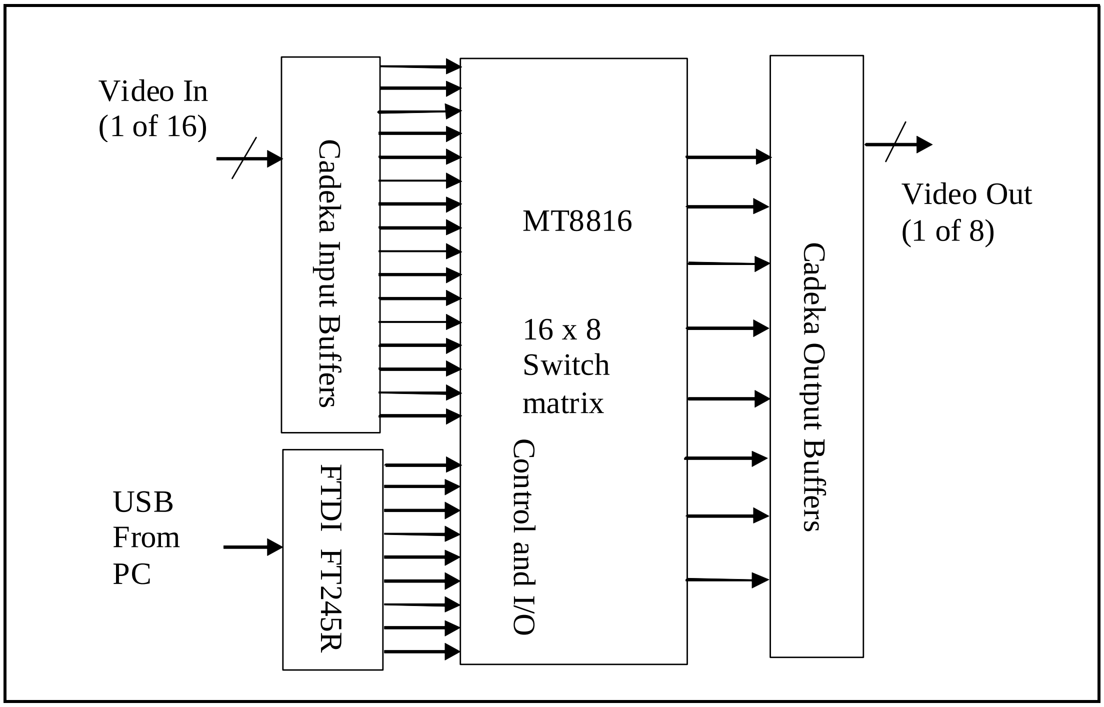


Figure 4 - Functional Block Diagram for a 16 x 8 Video Surveillance System using MT8816

Absolute Maximum Ratings*- Voltages are with respect to V_{EE} unless otherwise stated.

	Parameter		Symbol	Min.	Max.	Units
1	Supply Voltage		V_{DD} V_{SS}	-0.3 -0.3	16.0 V_{DD}+0.3	V V
2	Analog Input Voltage		V_{INA}	-0.3	V_{DD}+0.3	V
3	Digital Input Voltage		V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T_S	-65	+150	°C
6	Package Power Dissipation	PLASTIC DIP	P_D		0.6	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{EE} unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Operating Temperature	T_O	-40	25	85	°C	
2	Supply Voltage	V_{DD} V_{SS}	4.5 V_{EE}		13.2 V_{DD}-4.5	V V	
3	Analog Input Voltage	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics†- Voltages are with respect to V_{EE} = V_{SS} = 0 V, V_{DD} =12 V unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	µA	All digital inputs at V_{IN}=V_{SS} or V_{DD}
				0.4	1.5	mA	All digital inputs at V_{IN}=2.4V + V_{SS}; V_{SS}=7.0 V
				5	15	mA	All digital inputs at V_{IN}=3.4 V
2	Off-state Leakage Current (See G.9 in Appendix)	I_{OFF}		±1	±500	nA	$\lvert V_{Xi} - V_{Yj}\rvert = V_{DD} - V_{EE}$ See Appendix, Fig. A.1
3	Input Logic “0” level	V_{IL}			0.8+V_{SS}	V	V_{SS}=7.5V; V_{EE}=0 V
4	Input Logic “1” level	V_{IH}	2.0+V_{SS}			V	V_{SS}=6.5V; V_{EE}=0 V
5	Input Logic “1” level	V_{IH}	3.3			V	
6	Input Leakage (digital pins)	I_{LEAK}		0.1	10	µA	All digital inputs at V_{IN} = V_{SS} or V_{DD}

† DC Electrical Characteristics are over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym.	25°C		70°C		85°C		Units	Test Conditions
			Typ.	Max.	Typ.	Max.	Typ.	Max.		
1	On-state Resistance V_{DD}=12V V_{DD}=10V V_{DD}= 5V (See G.1, G.2, G.3 in Appendix)	R_{ON}	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	V_{SS}=V_{EE}=0 V,V_{DC}=V_{DD}/2, IV_{Xi}-V_{Yj}I = 0.4 V See Appendix, Fig. A.2
2	Difference in on-state resistance between two switches (See G.4 in Appendix)	ΔR_{ON}	5	10		10		10	Ω	V_{DD}=12V, V_{SS}=V_{EE}=0, V_{DC}=V_{DD}/2, IV_{Xi}-V_{Yj}I = 0.4 V See Appendix, Fig. A.2

AC Electrical Characteristics† - Crosspoint Performance-Voltages are with respect to V_{DD}= 5 V, V_{SS}= 0 V, V_{EE}= -7 V, unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f=1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f=1 MHz
3	Frequency Response Channel "ON" 20LOG(V_{OUT}/V_{Xi})=-3 dB	F_{3dB}		45		MHz	Switch is "ON"; V_{INA} = 2Vpp sinewave; R_L = 1 kΩ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; V_{INA} = 2Vpp sinewave f= 1 kHz; R_L=1 kΩ
5	Feedthrough Channel "OFF" Feed.=20LOG (V_{OUT}/V_{Xi}) (See G.8 in Appendix)	FDT		-95		dB	All Switches "OFF"; V_{INA}= 2Vpp sinewave f= 1 kHz; R_L= 1 kΩ. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi-Yi and Xj-Yj. Xtalk=20LOG (V_{Yj}/V_{Xi}). (See G.7 in Appendix).	X_{talk}		-45		dB	V_{INA}=2Vpp sinewave f= 10 MHz; R_L = 75 Ω.
				-90		dB	V_{INA}=2Vpp sinewave f= 10 kHz; R_L = 600 Ω.
				-85		dB	V_{INA}=2Vpp sinewave f= 10 kHz; R_L = 1 kΩ.
				-80		dB	V_{INA}=2Vpp sinewave f= 1 kHz; R_L = 10 kΩ. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	R_L=1 kΩ; C_L=50 pF

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5 dB better.

AC Electrical Characteristics† - Control and I/O Timings- Voltages are with respect to V_{DD} = 5 V, V_{SS} = 0 V, V_{EE} = -7V, unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Control Input crosstalk to switch (for CS, DATA, STROBE, Address)	CX_{talk}		30		mVpp	V_{IN}=3 V squarewave; R_{IN}=1 kΩ, R_L=10 kΩ. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f=1 MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to STROBE	t_{DS}	10			ns	R_L= 1 kΩ, C_L=50 pF ¿
5	Hold Time DATA to STROBE	t_{DH}	10			ns	R_L= 1 kΩ, C_L=50 pF ¿
6	Setup Time Address to STROBE	t_{AS}	10			ns	R_L= 1 kΩ, C_L= 50pF ¿
7	Hold Time Address to STROBE	t_{AH}	10			ns	R_L= 1 kΩ, C_L=50 pF ¿
8	Setup Time CS to STROBE	t_{CSS}	10			ns	R_L= 1 kΩ, C_L=50 pF ¿
9	Hold Time CS to STROBE	t_{CSH}	10			ns	R_L= 1 kΩ, C_L=50 pF ¿
10	STROBE Pulse Width	t_{SPW}	20			ns	R_L= 1 kΩ, C_L=50 pF ¿
11	RESET Pulse Width	t_{RPW}	40			ns	R_L= 1 kΩ, C_L=50 pF ¿
12	STROBE to Switch Status Delay	t_S		40	100	ns	R_L= 1 kΩ, C_L=50 pF ¿
13	DATA to Switch Status Delay	t_D		50	100	ns	R_L= 1 kΩ, C_L=50 pF ¿
14	RESET to Switch Status Delay	t_R		35	100	ns	R_L= 1 kΩ, C_L=50 pF ¿

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5 ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
¿ Refer to Appendix, Fig. A.7 for test circuit.

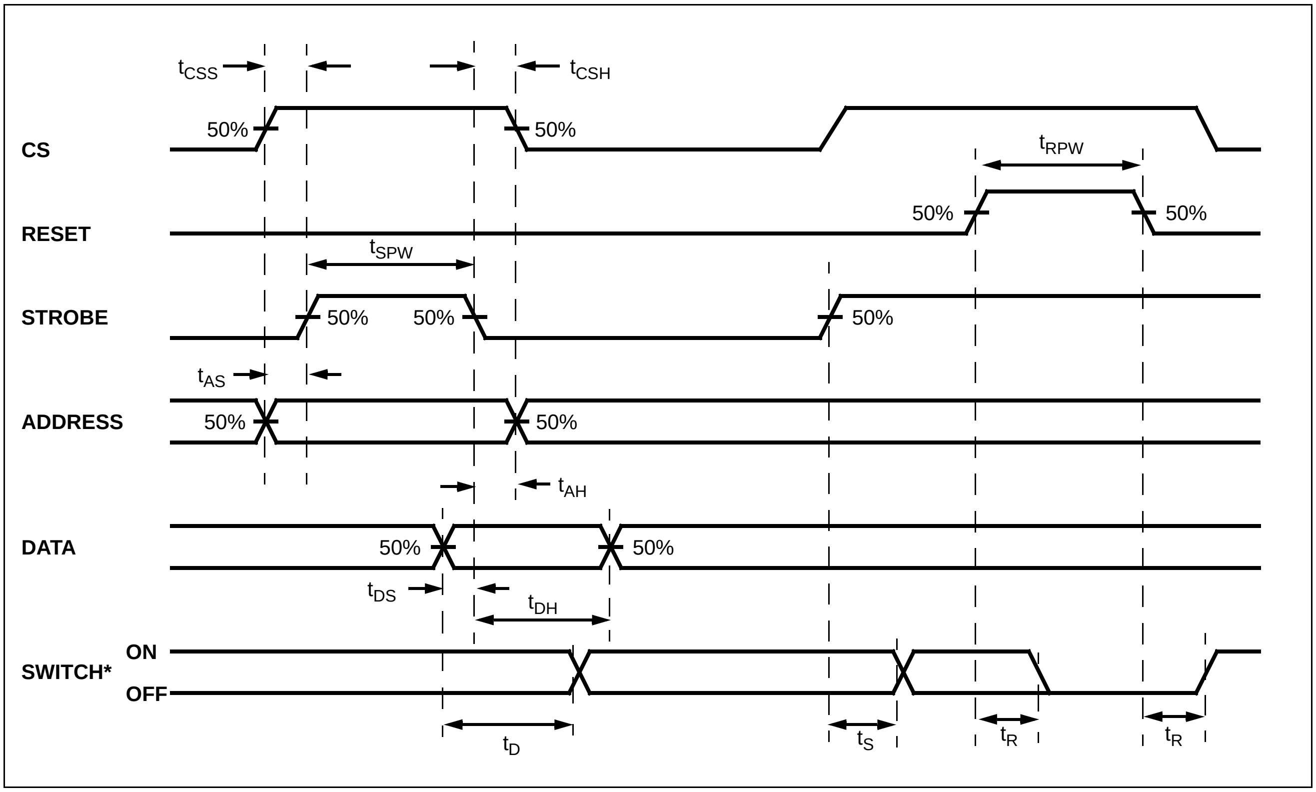


Figure 5 - Control Memory Timing Diagram

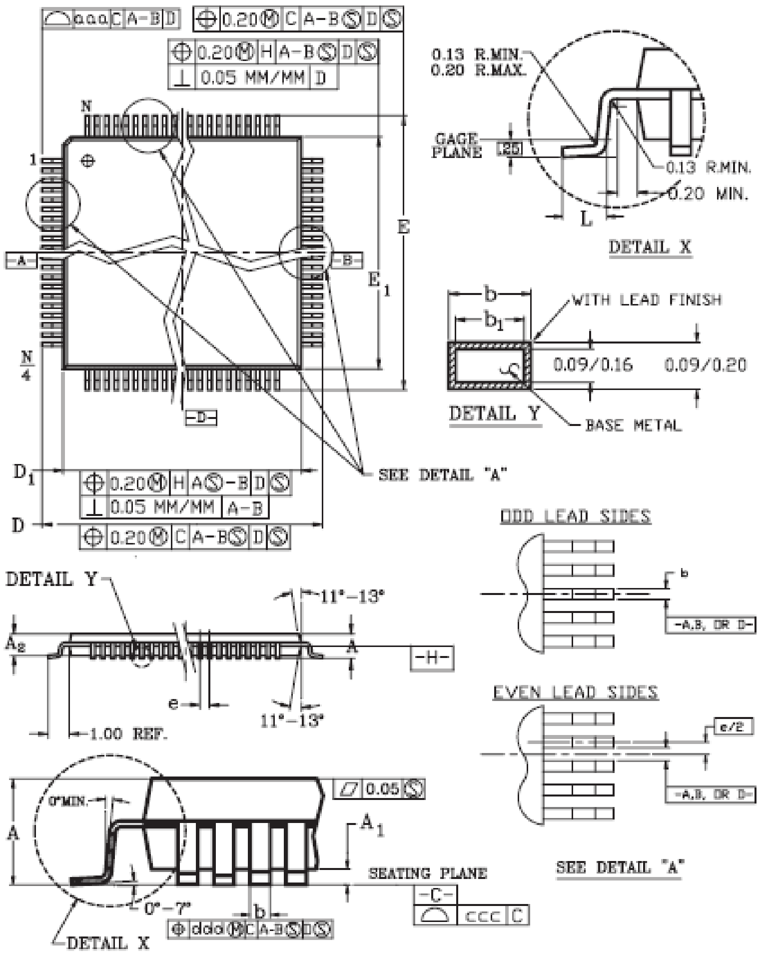
* See Appendix, Fig. A.7 for switching waveform

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection*
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	X12-Y0
1	1	1	0	0	0	0	X13-Y0
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	X14-Y0
1	1	1	1	0	0	0	X15-Y0
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	0 ↓ 0	X0-Y1 ↓ ↓ X15-Y1
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	0 ↓ 0	X0-Y2 ↓ ↓ X15-Y2
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	0 ↓ 0	X0-Y3 ↓ ↓ X15-Y3
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 0	0 ↓ 0	1 ↓ 1	X0-Y4 ↓ ↓ X15-Y4
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	1 ↓ 1	X0-Y5 ↓ ↓ X15-Y5
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	1 ↓ 1	X0-Y6 ↓ ↓ X15-Y6
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	1 ↓ 1	X0-Y7 ↓ ↓ X15-Y7

Table 1 - Address Decode Truth Table

* Switch connections are not in ascending order

44 Pin TQFP



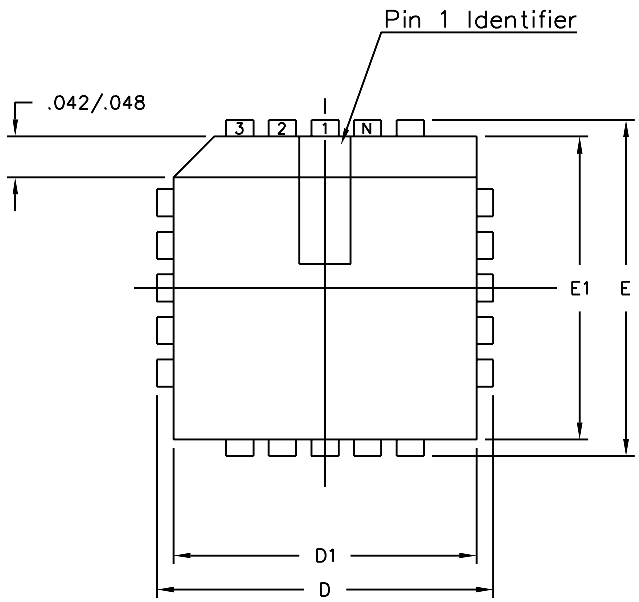
Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
D	12 BSC		
D1	10 BSC		
E	12 BSC		
E1	10 BSC		
L	0.45	0.60	0.75
N	44		
e	0.80 BSC		
b	0.30	0.37	0.45
b1	0.30	0.35	0.40
ccc	0.10		
ddd	0.20		
aaa	0.20		

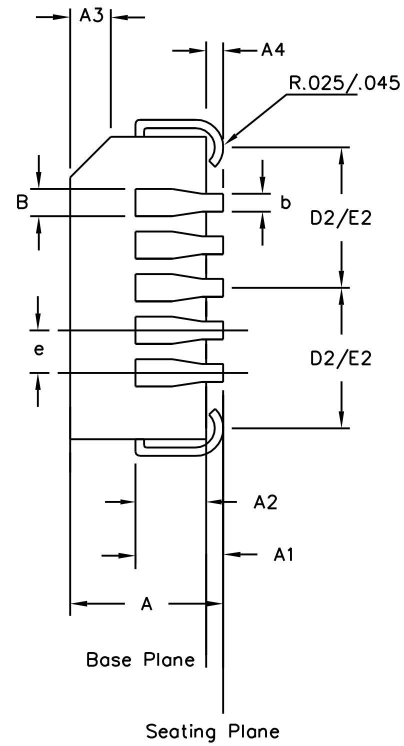
JEDEC #: MS-026 (C) ACB

Notes:
1. All dimensions and toleerances conform to ANSI Y14.5-1982.
2. Datum plane -H- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.
3. Dimensions "D1" and "E1" do not include mold protrusion. Allowable protrusion is 0.254mm per side. Dimensions "D1" and "E1" include mold mismatch and are determined at Datum plane -H- .
4. Dimension "B" does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Dambar can not be located on the lower radius or the foot.
5. Controlling dimensions: Millimeter.
6. Dimensions "D" and "E" are measured from both innermost and outermost points.
7. Deviation from lead-tip true position shall be within ±0.076mm for pitch >0.5mm and within ±0.04 for pitch ≤0.5mm.
8. Lead coplanarity shall be within: (Refer to 06-500)
   1- 0.10mm for devices with lead pitch of 0.65-0.80mm.
   2- 0.076mm for devices with lead pitch of 0.50mm.
   Coplanarity is measured per specification 06-500.
9. Half span (center of package to lead tip) shall be 15.30 ± 0.165mm (.602"±.0065").
10. "N" is the total number of terminals.
11. The top of package is smaller than the bottom of the package by 0.15mm.
12. This outline conforms to Jedec publication 95 registration MS-026
13. The 160 lead is a compliant depopulation of the 176 lead MS-026 variation BGA.

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207470	213094	
DATE	15Aug94	10Sep99	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

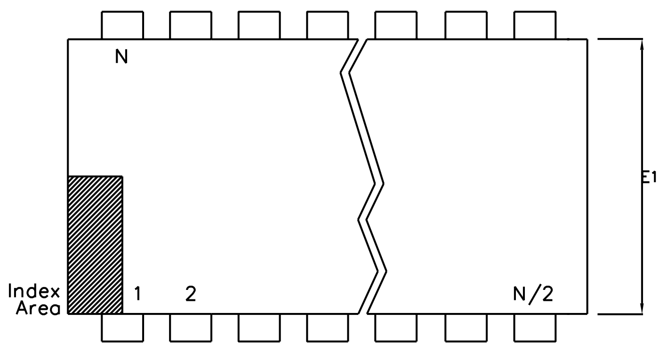
Previous package codes

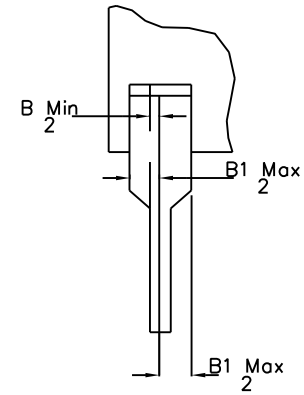
HP / P

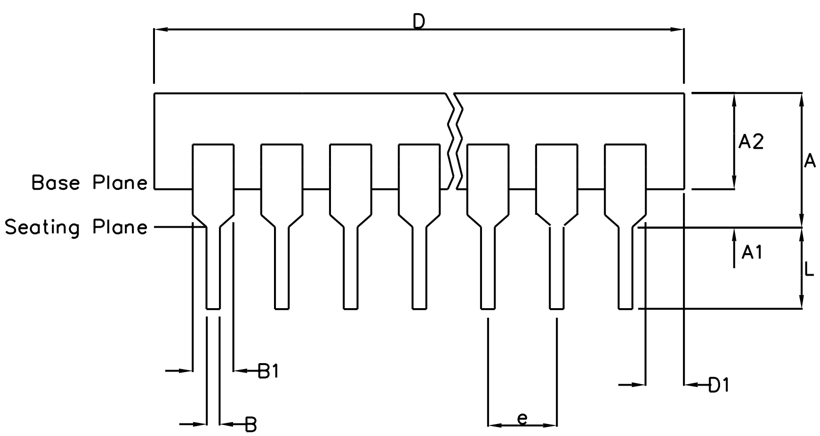
Package Code QA

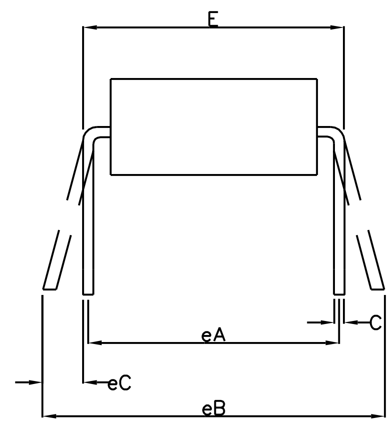
Package Outline for 44 lead PLCC

GPD00003









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	50.29	53.21	1.980	2.095
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	40		40	
Conforms to Jedec MS-011AC ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

ISSUE	1	2	3	
ACN	7010	203533	213103	
DATE	20Apr95	25Nov97	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
DP / E

Package Code DA

Package Outline for 40 lead PDIP

GPD00073

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