TwinDie™ 1.2V DDR4 SDRAM

MT40A4G4 – 128 Meg x 4 x 16 Banks x 2 Ranks
MT40A2G8 – 64 Meg x 8 x 16 Banks x 2 Ranks

Description

The 16Gb (TwinDie™) DDR4 SDRAM uses Micron's 8Gb DDR4 SDRAM die (essentially two ranks of the 8Gb DDR4 SDRAM). Refer to Micron's 8Gb DDR4 SDRAM data sheet for the specifications not included in this document. Specifications for base part number MT40A2G4 correlate to TwinDie manufacturing part number MT40A4G4; specifications for base part number MT40A1G8 correlate to TwinDie manufacturing part number MT40A2G8.

Features

- Uses 8Gb Micron die
- Two ranks (includes dual CS#, ODT, and CKE balls)
- Each rank has 4 groups of 4 internal banks for concurrent operation
- $V_{DD} = V_{DDQ}$ = 1.2V (1.14–1.26V)
- 1.2V V_{DDQ}-terminated I/O
- JEDEC-standard ball-out
- Low-profile package
- T_C of 0°C to 95°C
  - 0°C to 85°C: 8192 refresh cycles in 64ms
  - 85°C to 95°C: 8192 refresh cycles in 32ms

Options	Marking
• Configuration	
– 128 Meg x 4 x 16 banks x 2 ranks	4G4
– 64 Meg x 8 x 16 banks x 2 ranks	2G8
• FBGA package (Pb-free)	
– 78-ball FBGA (9.5mm x 13mm x 1.2mm) Die Rev :A	FSE
– 78-ball FBGA (8.0mm x 12mm x 1.2mm) Die Rev :B	NRE
• Timing – cycle time[1]	
– 0.750ns @ CL = 18 (DDR4-2666)	-075E
– 0.833ns @ CL = 16 (DDR4-2400)	-083E
– 0.833ns @ CL = 17 (DDR4-2400)	-083
– 0.937ns @ CL = 15 (DDR4-2133)	-093E
– 0.937ns @ CL = 16 (DDR4-2133)	-093
• Self refresh	
– Standard	None
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ 95°C)	None
• Revision	:A
	:B

Note: 1. CL = CAS (READ) latency.

Table 1: Key Timing Parameters

Speed Grade[1]	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-075E	2666	18-18-18	13.50	13.50	13.50
-075	2666	19-19-19	14.25	14.25	14.25
-083E	2400	16-16-16	13.32	13.32	13.32
-083	2400	17-17-17	14.16 (13.75)	14.16 (13.75)	14.16 (13.75)
-093E	2133	15-15-15	14.06 (13.50)	14.06 (13.50)	14.06 (13.50)
-093	2133	16-16-16	15.00	15.00	15.00

Note: 1. Refer to the Speed Bin Tables for additional details.

Table 2: Addressing

Parameter	4096 Meg x 4	2048 Meg x 8
Configuration	128 Meg x 4 x 16 banks x 2 ranks	64 Meg x 8 x 16 banks x 2 ranks
Bank group address	BG[1:0]	BG[1:0]
Bank count per group	4	4
Bank address in bank group	BA[1:0]	BA[1:0]
Row address	128K A[16:0]	64K A[15:0]
Column address	1K A[9:0]	1K A[9:0]

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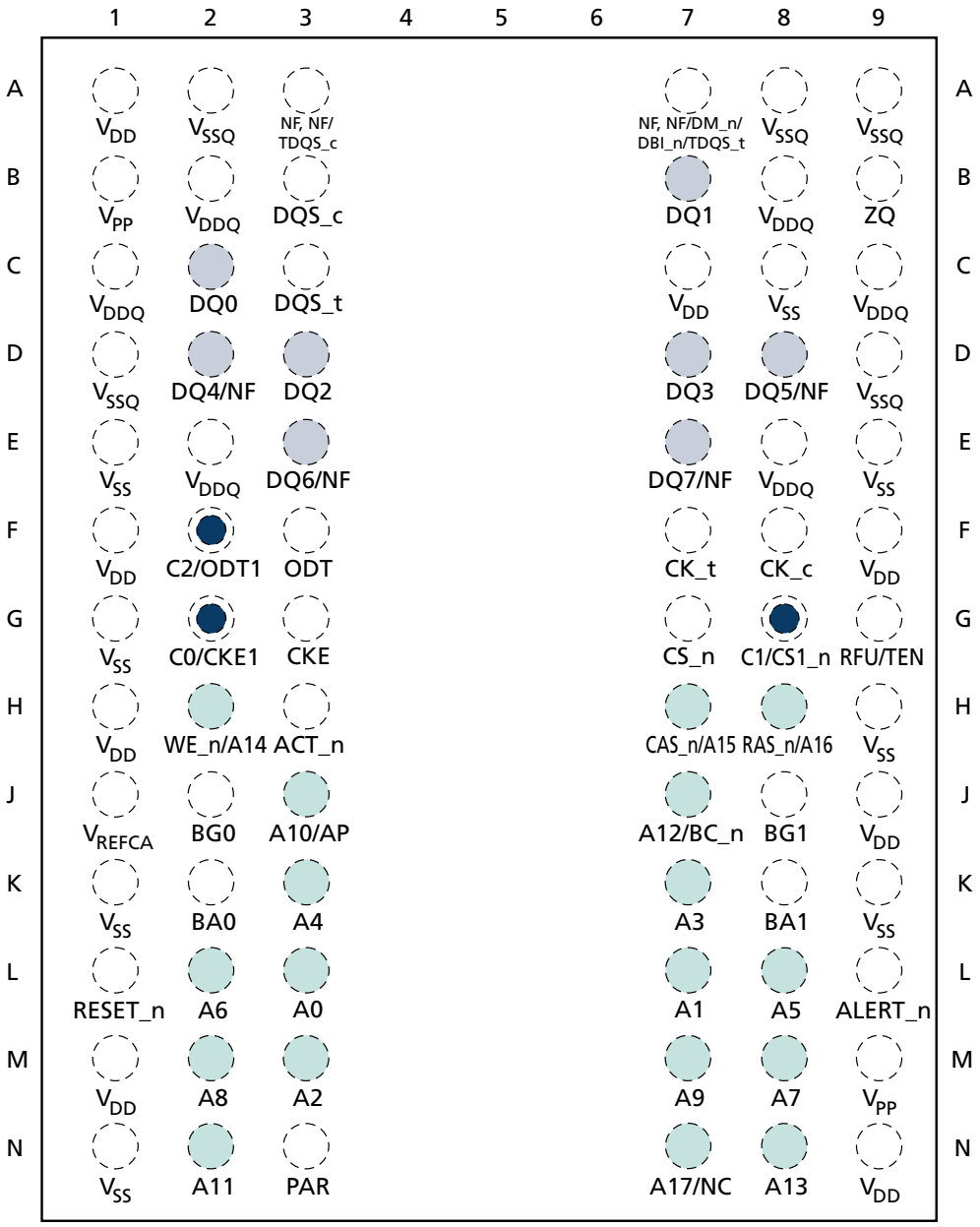
Ball Assignments and Descriptions

Figure 1: 78-Ball FBGA Ball Assignments (Top View)



Notes:
1. See the FBGA 78-Ball Descriptions table.
2. Dark balls (with ring) designate balls that are specific to controlling the second die of the TwinDie package when compared to a monolithic package.
3. A comma "," separates the configuration; a slash "/" defines a selectable function. For example: Ball A7 = NF, NF/DM_n/DBI_n/TDQS_t where NF applies to the x4 configuration only. NF/DM_n/DBI_n/TDQS_t applies to the x8 configuration only and is selectable between NF, DM_n, DBI_n, or TDQS_t via MRS.

Table 3: FBGA 78-Ball Descriptions

Symbol	Type	Description
A[17:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, RAS_n/A16, have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb and 16Gb parts, and A17 is only used on some 16Gb parts.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation (HIGH = auto precharge; LOW = no auto precharge). A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst-chopped). See the Command Truth Table.
ACT_n	Input	**Command input:** ACT_n indicates an ACTIVATE command. When ACT_n (along with CS_n) is LOW, the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as row address inputs for the ACTIVATE command. When ACT_n is HIGH (along with CS_n LOW), the input pins RAS_n/ A16, CAS_n/A15, and WE_n/A14 are treated as normal commands that use the RAS_n, CAS_n, and WE_n signals. See the Command Truth Table.
BA[1:0]	Input	**Bank address inputs:** Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
BG[1:0]	Input	**Bank group address inputs:** Define the bank group to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations.
C0/CKE1, C1/CS1_n, C2/ODT1	Input	**Stack address inputs:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations (these pins are not used in the x16 configuration). DDR4 will support a traditional dual-die package (DDP), which uses these three signals for control of the second die (CS1_n, CKE1, ODT1). DDR4 is not expected to support a traditional quad-die package (QDP). For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave) type of configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT.
CK_t, CK_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.

Table 3: FBGA 78-Ball Descriptions (Continued)

Symbol	Type	Description
CKE	Input	**Clock enable:** CKE HIGH activates, and CKE LOW deactivates, the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during self refresh.
CS_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
DM_nS	Input	**Input data mask:** DM_n is an input mask signal for write data. Input data is masked when DM is sampled LOW coincident with that input data during a write access. DM is sampled on both edges of DQS. DM is not supported on x4 configurations. LDM_n is associated with DQ[7:0]. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Mask (DM) section.
ODT	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for the x4 and x8 configurations (when the TDQS function is enabled via mode register). The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PAR	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled, the parity signal covers all command and address inputs, including RAS_n/A16, CAS_n/A15, WE_n/A14, A[17:0], A10/AP, A12/BC_n, BA[1:0], BG[1:0], C0/A18, C1/A19, C2/A20. Control pins NOT covered by the parity signal are CS_n, CKE, and ODT. Unused address pins that are density- and configuration-specific should be treated internally as 0s by the DRAM parity logic.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	**Command inputs:** RAS_n/A16 , CAS_n/A15, and WE_n/A14 (along with CS_n and ACT_n) define the command and/or address being entered. See the ACT_n description in this table.
RESET_n	Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD}; that is, 960 mV for DC HIGH and 240 mV for DC LOW.
TEN	Input	**Connectivity test mode:** TEN is active when HIGH and inactive when LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD} (960mV for DC HIGH and 240mV for DC LOW).

Table 3: FBGA 78-Ball Descriptions (Continued)

Symbol	Type	Description
DQ	I/O	**Data input/output:** Bidirectional data bus. DQ represents DQ[3:0], and DQ[7:0] for the x4, and x8, respectively. If write CRC is enabled via mode register, the write CRC code is added at the end of data burst. Any one or all of DQ0, DQ1, DQ2, and DQ3 may be used to monitor the internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH, training times change when enabled. During this mode, R_{TT} value should be set to High-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DBI_n	I/O	**DBI input/output:** Data bus inversion. DBI_n is an input/output signal used for data bus inversion in the x8 configuration. DBI_n is associated with DQ[7:0]. The DBI feature is not supported on x4 configurations. DBI can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Bus Inversion (DBI) section.
DQS_t, DQS_c	I/O	**Data strobe:** Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0] respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	**Alert output:** This signal allows the DRAM to indicate to the system's memory controller that a specific alert or event has occurred. Alerts will include the command/address parity error and the CRC data error when either of these functions is enabled in the mode register.
TDQS_t, TDQS_c	Output	**Termination data strobe:** TDQS_t and TDQS_c are used by x8 DRAMs only. When enabled via the mode register, the DRAM will enable the same R_{TT} termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin will provide the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for the x4 configuration. The DM function is supported only in x8 configuration.
V_{DD}	Supply	**Power supply:** 1.2V ±0.060V.
V_{DDQ}	Supply	**DQ power supply:** 1.2V ±0.060V.
V_{PP}	Supply	**DRAM activating power supply:** 2.5V -0.125V / +0.250V.
V_{REFCA}	Supply	Reference voltage for control, command, and address pins.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	DQ ground.
ZQ	Reference	**Reference ball for ZQ calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}. Note that this ball is shared by two DRAM devices. As a result, ZQ calibration operations need to be carried out separately so that correct values are achieved.
RFU	–	Reserved for future use.
NC	–	**No connect:** No internal electrical connection is present.
NF	–	**No function:** May have internal connection present, but has no function.

Functional Description

The TwinDie DDR4 SDRAM is a high-speed, CMOS dynamic random access memory device internally configured as two 16-bank DDR4 SDRAM devices.

Although each die is tested individually within the dual-die package, some TwinDie test results may vary from a like-die tested within a monolithic die package.

The DDR4 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR4 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR4 SDRAM and edge-aligned to the data strobes.

Read and write accesses to the DDR4 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Operation begins with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits (including CS*n*#, BA*n*, and A*n*) registered coincident with the READ or WRITE command are used to select the rank, bank, and starting column location for the burst access.

This data sheet provides a general description, package dimensions, and the package ballout. Refer to the Micron monolithic DDR4 data sheet for complete information regarding individual die initialization, register definition, command descriptions, and die operation.

Industrial Temperature

The industrial temperature (IT) option, if offered, requires that the case temperature not exceed –40°C or 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance, I_{DD} values, some I_{DD} specifications and the input/output impedance must be derated when T_C is < 0°C or > 95°C. See the DDR4 monolithic data sheet for details.

Functional Block Diagrams

Figure 2: Functional Block Diagram (128 Meg x 4 x 16 Banks x 2 Ranks)

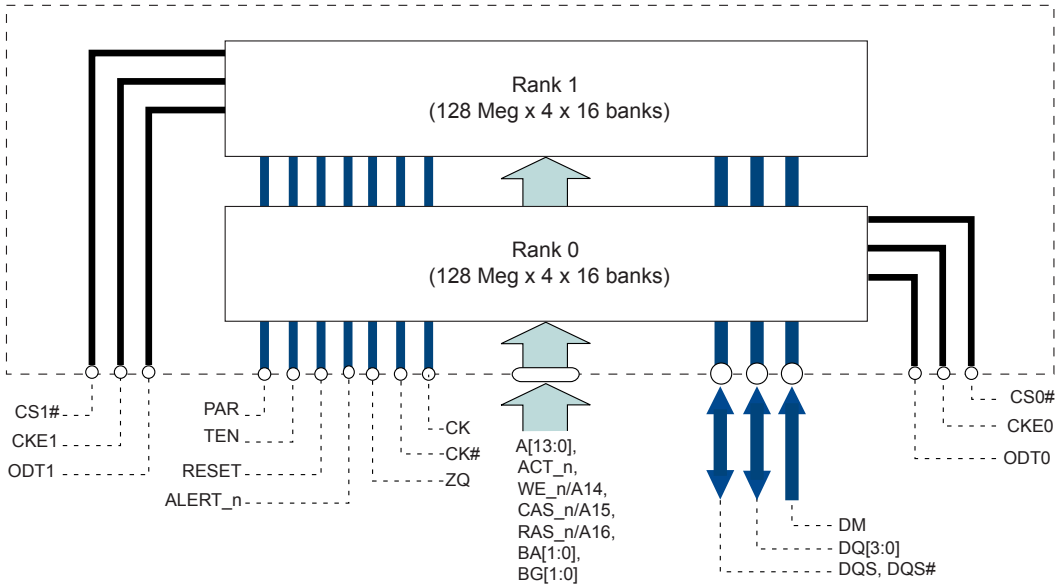
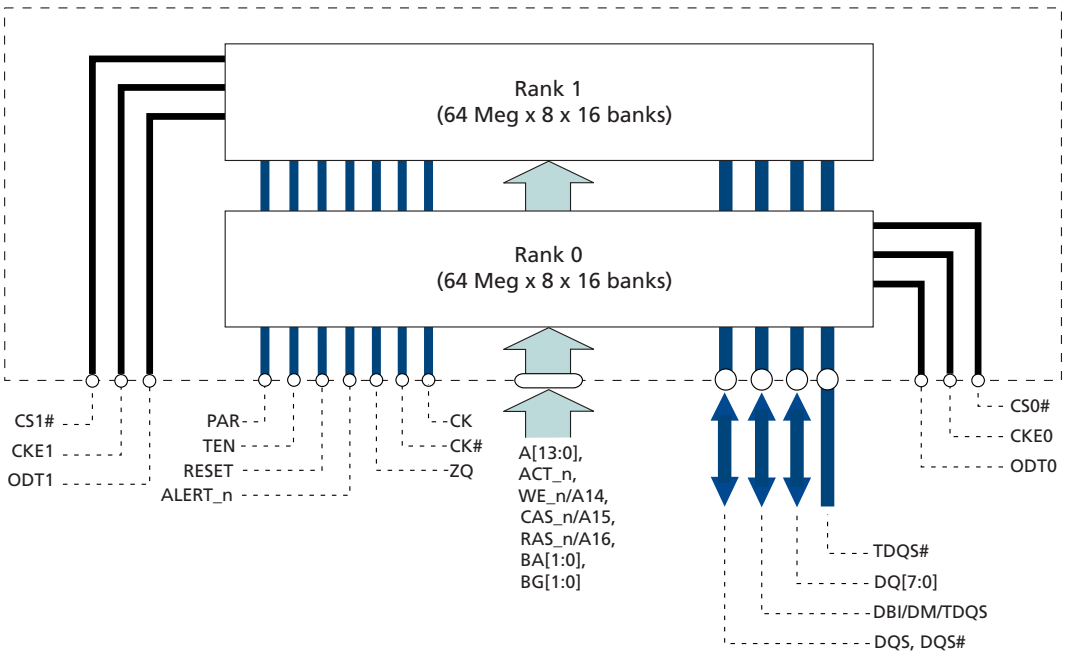


Figure 3: Functional Block Diagram (64 Meg x 8 x 16 Banks x 2 Ranks)



Electrical Specifications – Leakages

Table 4: Input and Output Leakages

Symbol	Parameter	Min	Max	Units	Notes
I_{IN}	Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.1V (All other pins not under test = 0V)	–4	4	µA	1
I_{VREFCA}	V_{REF} supply leakage current (All other pins not under test = 0V)	–4	4	µA	2
I_{ZQ}	Input leakage on ZQ pin	–100	20	µA	
I_{TEN}	Input leakage on TEN pin	–12	20	µA	
I_{OZpd}	Output leakage: V_{OUT} = V_{DDQ}	–	20	µA	3
I_{OZpu}	Output leakage: V_{OUT} = V_{SSQ}	–100	–	µA	3, 4

Notes:
1. Any input 0V < V_{IN} < 1.1V
2. V_{REFCA} = V_{DD}/2, V_{DD} at valid level.
3. DQ are disabled.
4. ODT is disabled with the ODT input HIGH.

Temperature and Thermal Impedance

It is imperative that the DDR4 SDRAM device's temperature specifications, shown in the following table, be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances listed in Table 6 (page 11) apply to the current die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications," prior to using the values listed in the thermal impedance table. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the die size reduction.

The DDR4 SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

Table 5: Thermal Characteristics

Notes 1–3 apply to entire table

Parameter	Symbol	Value	Units	Notes
Operating temperature	T_C	0 to 85	°C	
		0 to 95	°C	4

Notes:
1. MAX operating case temperature T_C is measured in the center of the package, as shown below.
2. A thermal solution must be designed to ensure that the device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate. The use of self refresh temperature (SRT) or automatic self refresh (ASR), if available, must be enabled.

Figure 4: Temperature Test Point Location

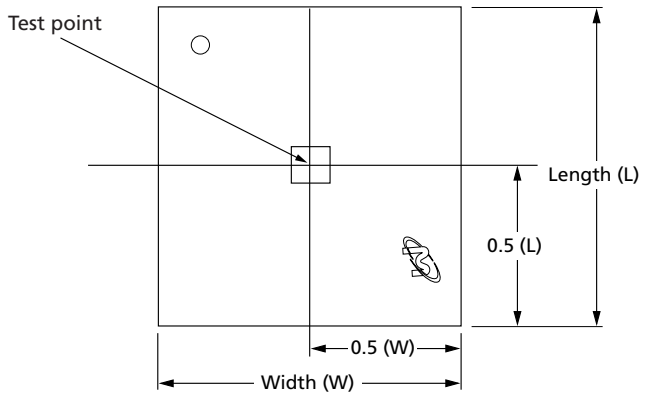
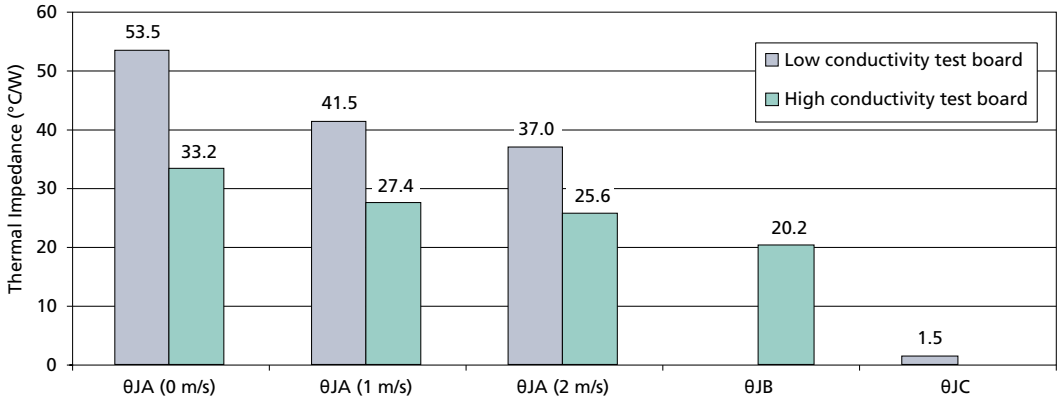


Table 6: Thermal Impedance

Package		Substrate	Θ JA (°C/W) Airflow = 0m/s	Θ JA (°C/W) Airflow = 1m/s	Θ JA (°C/W) Airflow = 2m/s	Θ JB (°C/W)	Θ JC (°C/W)	Notes
78-ball	Rev A "FSE"	Low conductivity	47.9	36.2	32.0	NA	1.6	1
		High conductivity	28.3	23.0	21.3	10.6	NA	
78-ball	Rev B "NRE"	Low conductivity	53.5	41.5	37.0	NA	1.5	1
		High conductivity	33.2	27.4	25.6	20.2	NA	

Note:
1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

Figure 5: Thermal Impedance



Note: 1. All simulations are conducted per JEDEC standards.

Electrical Characteristics – AC and DC Output Measurement Levels

Single-Ended Outputs

Table 7: Single-Ended Output Levels

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
DC output high measurement level (for IV curve linearity)	$V_{OH(DC)}$	1.1 × V_{DDQ}	V
DC output mid measurement level (for IV curve linearity)	$V_{OM(DC)}$	0.8 × V_{DDQ}	V
DC output low measurement level (for IV curve linearity)	$V_{OL(DC)}$	0.5 × V_{DDQ}	V
AC output high measurement level (for output slew rate)	$V_{OH(AC)}$	(0.7 + 0.15) × V_{DDQ}	V
AC output low measurement level (for output slew rate)	$V_{OL(AC)}$	(0.7 - 0.15) × V_{DDQ}	V

Note: 1. The swing of ±0.15 × V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of 50Ω to V_{TT} = V_{DDQ}.

Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals.

Table 8: Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]/\Delta TR_{se}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]/\Delta TF_{se}$

Figure 6: Single-ended Output Slew Rate Definition

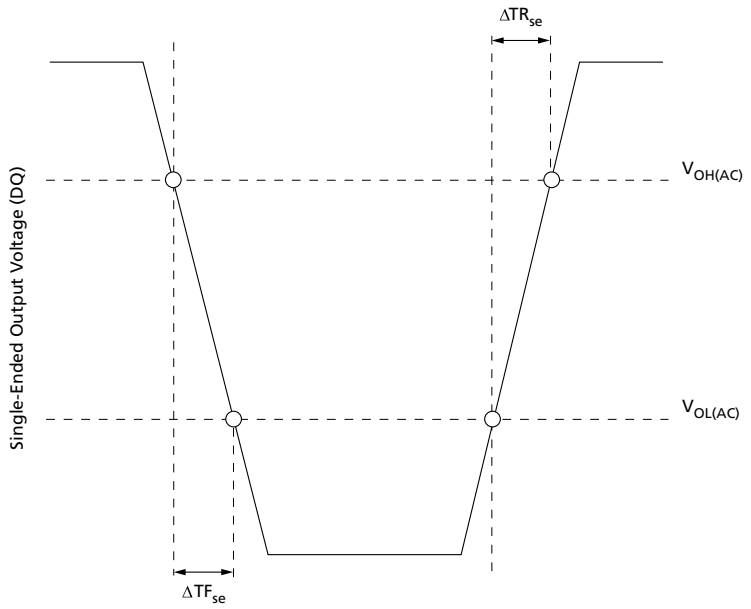


Table 9: Single-Ended Output Slew Rate

For $R_{ON} = R_{ZQ}/7$

Parameter	Symbol	DDR4-1333 / 1866 / 2133 / 2400 /2666		Unit
		Min	Max	
Single-ended output slew rate	SRQ_{se}	2	7	V/ns

Notes:
1. SR = slew rate; Q = query output; se = single-ended signals
2. In two cases a maximum slew rate of 12V/ns applies for a single DQ signal within a byte lane:
   - Case 1 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from HIGH-to-LOW or LOW-to-HIGH) while all remaining DQ signals in the same byte lane are static (they stay at either HIGH or LOW).
   - Case 2 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from HIGH-to-LOW or LOW-to-HIGH) while all remaining DQ signals in the same byte lane are switching into the opposite direction (from LOW-to-HIGH or HIGH-to-LOW, respectively). For the remaining DQ signal switching into the opposite direction, the standard maximum limit of 7 V/ns applies.

Differential Outputs

Table 10: Differential Output Levels

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
AC differential output high measurement level (for output slew rate)	$V_{OH,diff(AC)}$	$0.3 \times V_{DDQ}$	V
AC differential output low measurement level (for output slew rate)	$V_{OL,diff(AC)}$	$-0.3 \times V_{DDQ}$	V

Note:
1. The swing of $\pm 0.3 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$ at each differential output.

Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL,diff(AC)}$ and $V_{OH,diff(AC)}$ for differential signals.

Table 11: Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}]/\Delta TR_{diff}$
Differential output slew rate for falling edge	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}]/\Delta TF_{diff}$

Figure 7: Differential Output Slew Rate Definition

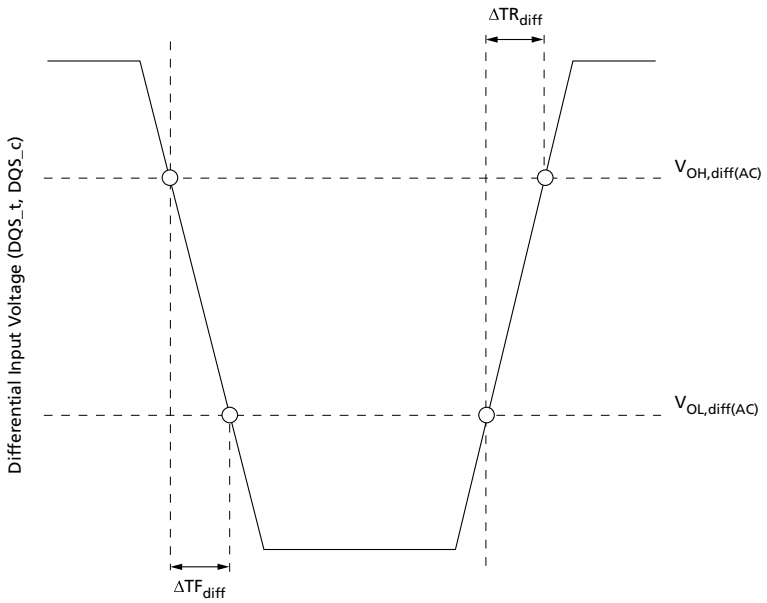


Table 12: Differential Output Slew Rate

For $R_{ON} = R_{ZQ}/7$

Parameter	Symbol	DDR4-1333 / 1866 / 2133 / 2400 / 2666		Unit
		Min	Max	
Differential output slew rate	SRQ_{diff}	4	14	V/ns

Note: 1. SR = slew rate; Q = query output; diff = differential signals.

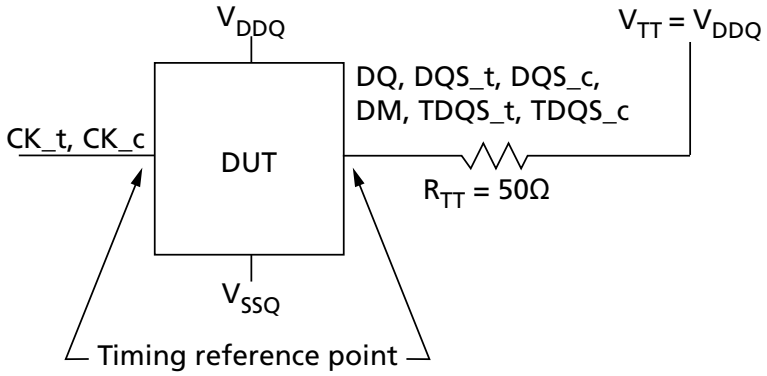
Reference Load for AC Timing and Output Slew Rate

The effective reference load of 50Ω to $V_{TT} = V_{DDQ}$ and driver impedance of $R_{ZQ}/7$ for each output was used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

R_{ON} nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing paraeter values of the device. The maximum DC high level of output signal = 1.0 × V_{DDQ}, the minimum DC low level of output signal = { 34 /(34 + 50) } × V_{DDQ} = 0.4 × V_{DDQ}

The nominal reference level of an output signal can be approximated by the following: The center of maximum DC high and minimum DC low = { (1 + 0.4) / 2 } × V_{DDQ} = 0.7 × V_{DDQ}. The actual reference level of output signal might vary with driver R_{ON} and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye.

Figure 8: Reference Load For AC Timing and Output Slew Rate



Electrical Specifications – I_{CDD} Parameters

Table 13: DDR4 I_{CDD} Specifications and Conditions (Rev. A)

Note 1 applies to the entire table

Combined Symbol	Individual Die Status	Bus Width	DDR4-2133	DDR4-2400	DDR4-2666	Units
I_{CDD0}	$I_{CDD0} = I_{DD0} + I_{DD2P} + 3$	x4, x8	83	93	TBD	mA
I_{CPP0}	$I_{CPP0} = I_{PP0} + I_{PP3N}$	x4, x8	6	6	TBD	mA
I_{CDD1}	$I_{CDD1} = I_{DD1} + I_{DD2P} + 3$	x4, x8	98	108	TBD	mA
I_{CDD2N}	$I_{CDD2N} = I_{DD2N} + I_{DD2P}$	x4, x8	70	80	TBD	mA
I_{CDD2NT}	$I_{CDD2NT} = I_{DD2NT} + I_{DD2P}$	x4, x8	80	90	TBD	mA
I_{CDD2P}	$I_{CDD2P} = I_{DD2P} + I_{DD2P}$	x4, x8	50	60	TBD	mA
I_{CDD2Q}	$I_{CDD2Q} = I_{DD2Q} + I_{DD2P}$	x4, x8	70	75	TBD	mA
I_{CDD3N}	$I_{CDD3N} = I_{DD3N} + I_{DD2P}$	x4, x8	80	85	TBD	mA
I_{CPP3N}	$I_{CPP3N} = I_{PP3N} + I_{PP3N}$	x4, x8	6	6	TBD	mA
I_{CDD3P}	$I_{CDD3P} = I_{DD3P} + I_{DD2P}$	x4, x8	60	70	TBD	mA
I_{CDD4R}	$I_{CDD4R} = I_{DD4R} + I_{DD2P} + 3$	x4	163	178	TBD	mA
		x8	178	183	TBD	
I_{CDD4W}	$I_{CDD4W} = I_{DD4W} + I_{DD2P} + 3$	x4	163	178	TBD	mA
		x8	178	193	TBD	
I_{CDD5R}	$I_{CDD5R} = I_{DD5R} + I_{DD2P}$	x4, x8	89	94	TBD	mA
I_{CPP5R}	$I_{CPP5R} = I_{PP5R} + I_{PP3N}$	x4, x8	8	8	TBD	mA
I_{CDD6N}	$I_{CDD6N} = I_{DD6N} + I_{DD6N}$	x4, x8	60	60	TBD	mA
I_{CDD6E}	$I_{CDD6E} = I_{DD6E} + I_{DD6E}$	x4, x8	70	70	TBD	mA
I_{CDD6R}[2]	$I_{CDD6R} = I_{DD6R} + I_{DD6R}$	x4, x8	50	50	TBD	mA
I_{CDD6A} (25°C)[2]	$I_{CDD6A} = I_{DD6A} + I_{DD6A}$	x4, x8	40	40	TBD	mA
I_{CDD6A} (45°C)[2]	$I_{CDD6A} = I_{DD6A} + I_{DD6A}$	x4, x8	50	50	TBD	mA
I_{CDD6A} (75°C)[2]	$I_{CDD6A} = I_{DD6A} + I_{DD6A}$	x4, x8	70	70	TBD	mA

Table 13: DDR4 I_{CDD} Specifications and Conditions (Rev. A) (Continued)

Note 1 applies to the entire table

Combined Symbol	Individual Die Status	Bus Width	DDR4-2133	DDR4-2400	DDR4-2666	Units
I_{CDD7}	I_{CDD7} = $I_{DD7} + I_{DD2P} + 3$	x4	213	223	TBD	mA
		x8	228	238	TBD	
I_{CPP7}	I_{CPP7} = $I_{PP7} + I_{PP3N}$	x4, x8	18	18	TBD	mA
I_{CDD8}	$I_{CDD8} = I_{DD8} + I_{DD8}$	x4, x8	40	40	TBD	mA

Notes:
1. I_{CDD} values reflect the combined current of both individual die. I_{DDx} represents individual die values.
2. I_{CDD6R} and I_{CDD6A} values are typical.

Table 14: DDR4 I_{CDD} Specifications and Conditions (Rev. B)

Note 1 applies to the entire table

Combined Symbol	Individual Die Status	Bus Width	DDR4-2133	DDR4-2400	DDR4-2666	Units
I_{CDD0}	$I_{CDD0} = I_{DD0} + I_{DD2P} + 3$	x4	68	71	TBD	mA
		x8	73	76	TBD	
I_{CPP0}	$I_{CPP0} = I_{PP0} + I_{PP3N}$	x4, x8	6	6	TBD	mA
I_{CDD1}	$I_{CDD1} = I_{DD1} + I_{DD2P} + 3$	x4	80	83	TBD	mA
		x8	85	88	TBD	
I_{CDD2N}	$I_{CDD2N} = I_{DD2N} + I_{DD2P}$	x4, x8	58	59	TBD	mA
I_{CDD2NT}	$I_{CDD2NT} = I_{DD2NT} + I_{DD2P}$	x4, x8	70	75	TBD	mA
I_{CDD2P}	$I_{CDD2P} = I_{DD2P} + I_{DD2P}$	x4, x8	50	50	TBD	mA
I_{CDD2Q}	$I_{CDD2Q} = I_{DD2Q} + I_{DD2P}$	x4, x8	55	55	TBD	mA
I_{CDD3N}	$I_{CDD3N} = I_{DD3N} + I_{DD2P}$	x4, x8	65	68	TBD	mA
I_{CPP3N}	$I_{CPP3N} = I_{PP3N} + I_{PP3N}$	x4, x8	6	6	TBD	mA
I_{CDD3P}	$I_{CDD3P} = I_{DD3P} + I_{DD2P}$	x4, x8	55	57	TBD	mA
		x8	60	62	TBD	
I_{CDD4R}	$I_{CDD4R} = I_{DD4R} + I_{DD2P} + 3$	x4	138	138	TBD	mA
		x8	153	163	TBD	
I_{CDD4W}	$I_{CDD4W} = I_{DD4W} + I_{DD2P} + 3$	x4	133	141	TBD	mA
		x8	143	151	TBD	
I_{CDD5R}	$I_{CDD5R} = I_{DD5R} + I_{DD2P}$	x4, x8	75	78	TBD	mA
I_{CPP5R}	$I_{CPP5R} = I_{PP5R} + I_{PP3N}$	x4, x8	8	8	TBD	mA
I_{CDD6N}	$I_{CDD6N} = I_{DD6N} + I_{DD6N}$	x4, x8	60	60	TBD	mA
I_{CDD6E}	$I_{CDD6E} = I_{DD6E} + I_{DD6E}$	x4, x8	70	70	TBD	mA
I_{CDD6R}[2]	$I_{CDD6R} = I_{DD6R} + I_{DD6R}$	x4, x8	40	40	TBD	mA
I_{CDD6A} (25°C)[2]	$I_{CDD6A} = I_{DD6A} + I_{DD6A}$	x4, x8	16	16	TBD	mA
I_{CDD6A} (45°C)[2]	$I_{CDD6A} = I_{DD6A} + I_{DD6A}$	x4, x8	40	40	TBD	mA

Table 14: DDR4 I_{CDD} Specifications and Conditions (Rev. B) (Continued)

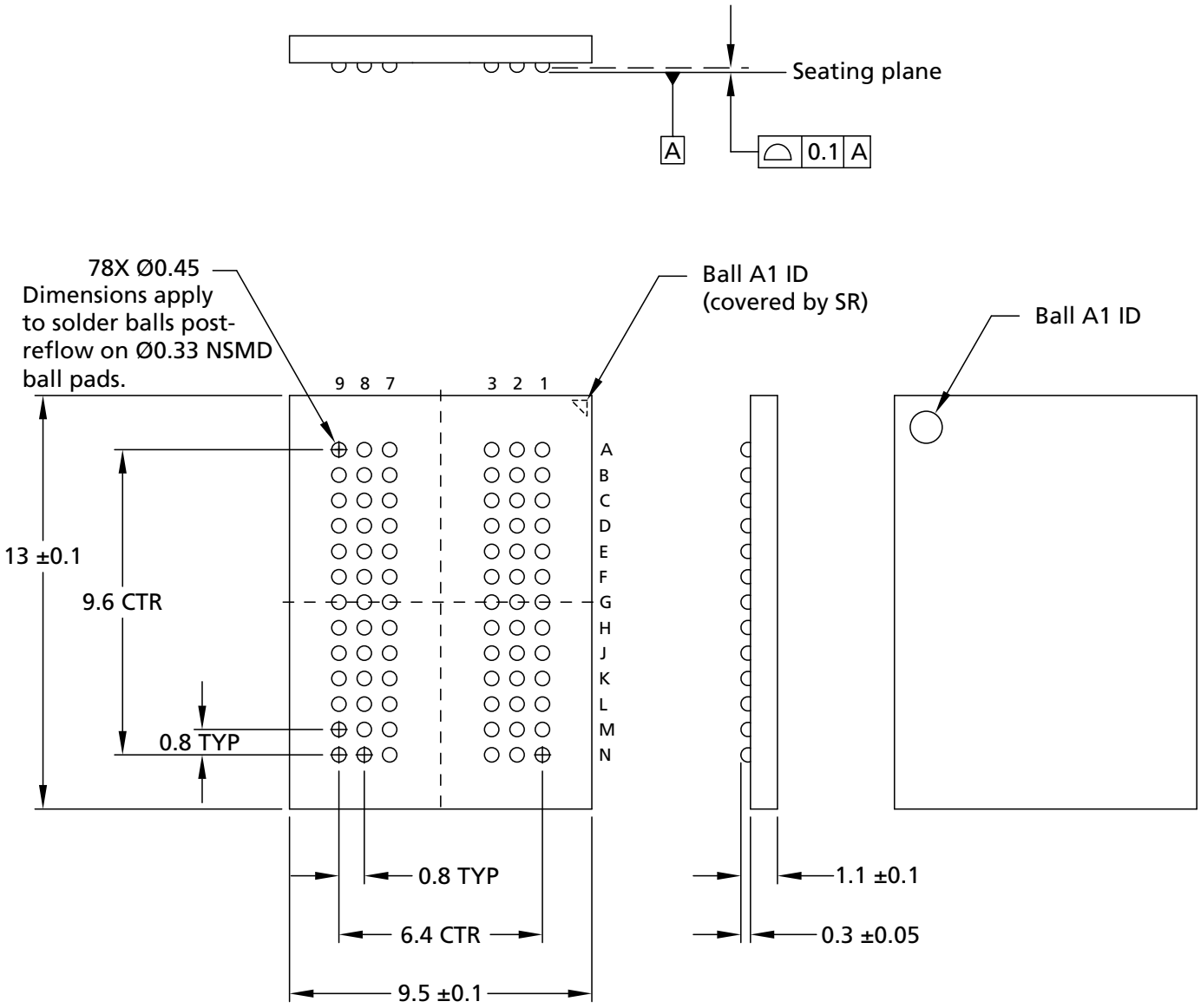
Note 1 applies to the entire table

Combined Symbol	Individual Die Status	Bus Width	DDR4-2133	DDR4-2400	DDR4-2666	Units
I_{CDD6A} (75°C)[2]	I_{CDD6A} = I_{DD6A} + I_{DD6A}	x4, x8	60	60	TBD	mA
I_{CDD7}	I_{CDD7} = I_{DD7} + I_{DD2P} + 3	x4	188	193	TBD	mA
		x8	198	203	TBD	
I_{CPP7}	I_{CPP7} = I_{PP7} + I_{PP3N}	x4, x8	18	18	TBD	mA
I_{CDD8}	I_{CDD8} = I_{DD8} + I_{DD8}	x4, x8	50	50	TBD	mA

Notes:
1. I_{CDD} values reflect the combined current of both individual die. I_{DDx} represents individual die values.
2. I_{CDD6R} and I_{CDD6A} values are typical.

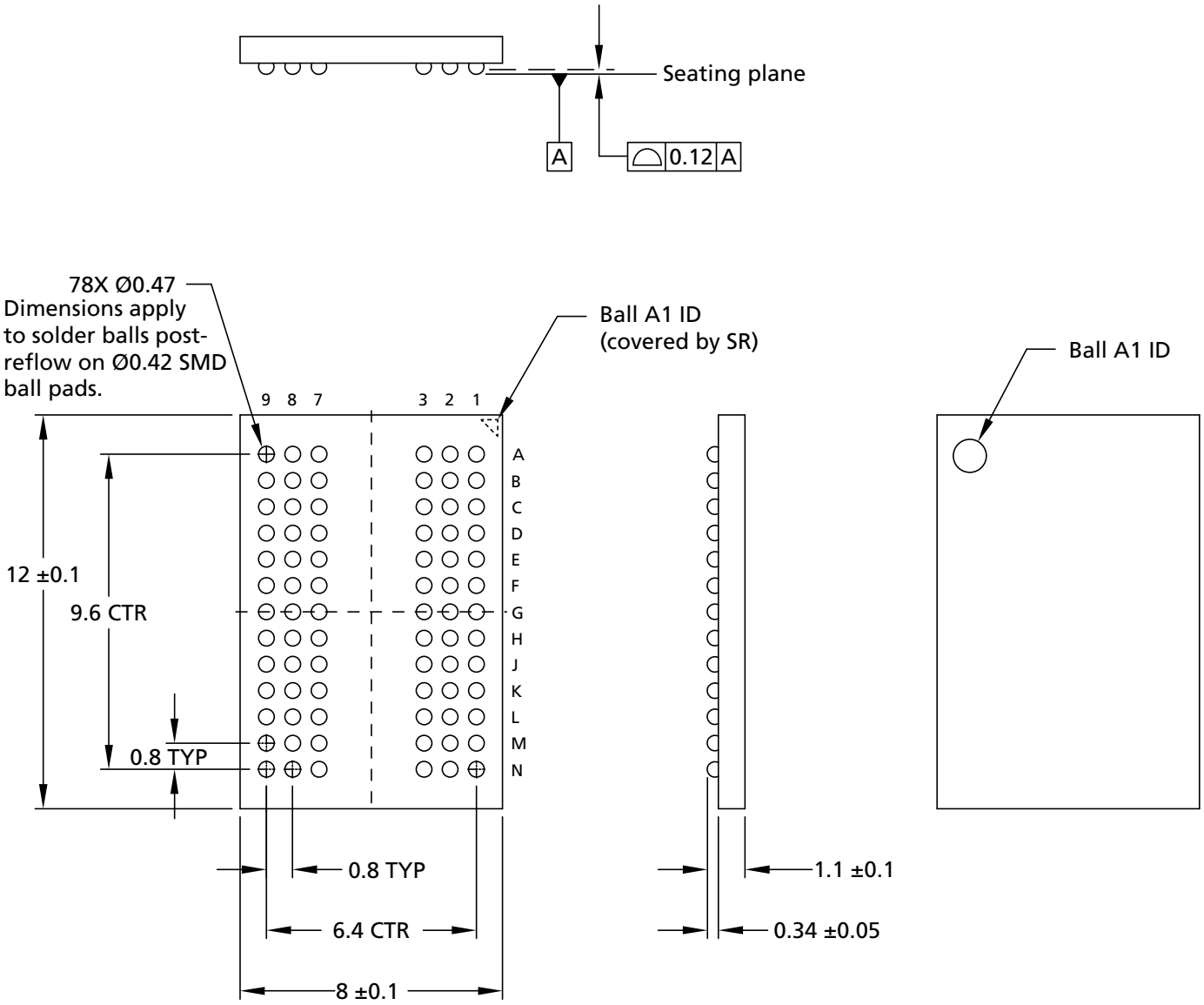
Package Dimensions

Figure 9: 78-Ball FBGA Die Rev. A (package code FSE)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 10: 78-Ball FBGA Die Rev. B (package code NRE)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).