BLAZAR BE3-BURST Accelerator Engine
Intelligent In Memory Computing

PRODUCT BRIEF

BANDWIDTH ENGINE (BE) INTRODUCTION

The **BLAZAR Family of Accelerator Engines** support high bandwidth, fast random memory access rates and *embedded **I**n **M**emory **F**unctions (**IMF**)* that solve critical memory access challenges for memory bottlenecked applications like network search, statistics, buffering, security, firewall, 8k video, anomaly detect, genomics, ML random forest of trees, graph/tree/list walking, traffic monitoring.

The ***Bandwidth Engine 3 BURST (BE3-BURST)*** combines the high speed serial memory with in memory ***Bandwidth* functions** called BURST. These are sequential read and write for Data Movement that nearly doubles the memory access bandwidth.

Applications benefits…

- FPGA Acceleration for Xilinx and Intel
- Replaces up to 8 QDR/RLDRAM memory devices
- Memory architecture allows up to 32 simultaneous accesses
- Lowers latency up to 4x and increases available access rates 6x by avoiding memory bottlenecks
- Accelerates FPGA application by providing fast, efficient, single function calls for burst, multi-read or multi-Write operations
- ***Bandwidth IMFs - BURST***
  - ***Sequential read and write functions for Data Movement nearly doubles bandwidth.***
  - ***BE3 includes all of the BE2 Burst IMF and additional functions.***
- The devices support application acceleration for aggregate throughput rates ranging from 70Gb/s to over 810Gb/s per device
- Facilitates a "Software Define-Hardware Acceleration" system architecture

KEY FEATURES / PRODUCT OPTIONS

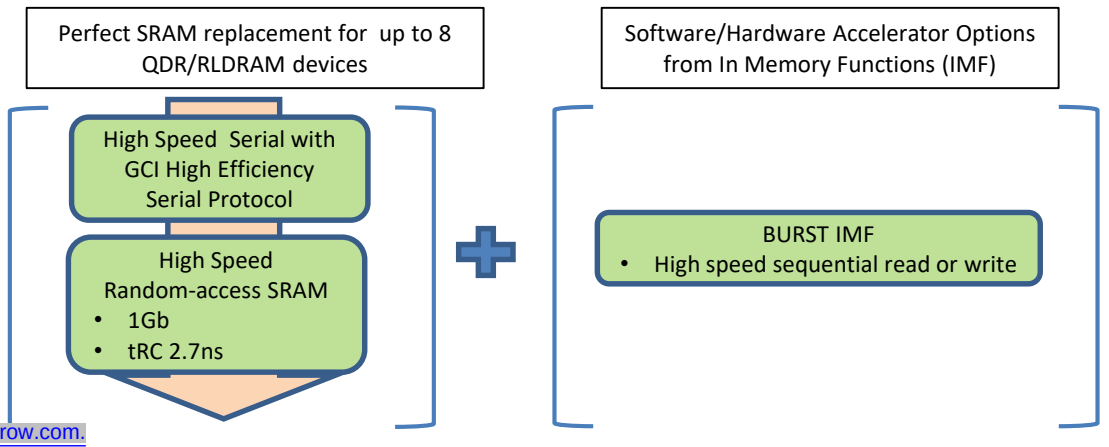
- High Bandwidth, low pin count serial interface
  - Highly efficient reliable transport command and data protocol optimized for 90% efficiency
  - Eases board layout and signal integrity, no trace length matching required, operates over connectors
- 1Gb SRAM (16M x 72b)
- High access rate SRAM class memory
  - Up to 6.5 Billion transactions/sec
- High cycle rate memory
  - 2.7ns tRC
- Low latency: 40ns external (pin to pin)
- **In Memory Bandwidth Functions**
  - BURST sequential read and write functions for Data Movement nearly doubles bandwidth
  - Burst length: 1, 2, 4, 8 x 72b
  - Reduction of I/O up to 7X
- Highest Single Chip Bandwidth – up to 717 Gbps throughput

APPLICATIONS FOCUS

- High bandwidth data access application where low latency and Movement of Data is a critical requirement.
- Applications needed large SRAMs.
- FPGA Acceleration for Xilinx and Intel

MoSys ACCELERATOR ENGINE Elements

MoSys Engines have a Unique Memory Architecture that can replace SRAM/RLDRAM memories and embeds In Memory Functions (IMF) that execute many times faster. A single embedded function can replace several traditional memory accesses.



MoSys Bandwidth Engine BURST (BE3) Architecture

Fixed In Memory BANDWIDTH Functions - BURST

The BURST Functions are focused on DATA MOVEMENT. They accelerate getting data in and out of the memory faster and more efficiently by reducing the number of commands. There are 12 flexible Burst functions.

The BURST Multi-Read/Multi-Write In-Memory Functions can nearly doubling the amount of data that can be moved with that same bandwidth. *A single Burst function can result in up to 8 sequential reads or writes.*

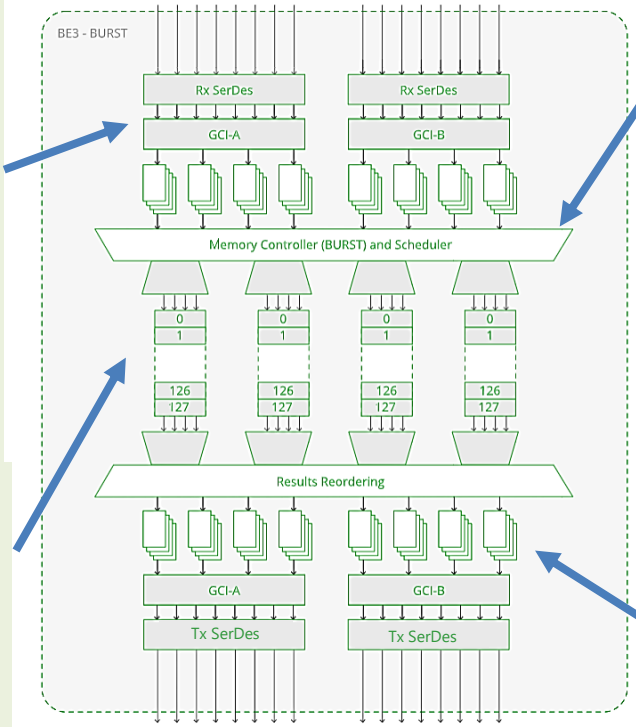
And, the Accelerator Engine can do several BURST Functions simultaneously! Further increasing system performance.

High speed serial I/O

- GCI serial I/O versions of 10, 12.5, 15 and 25 Gbps for high bandwidth (up to 717 Gbps)
- Device can operate with a minimum of 4 lanes.
- Has two, full duplex 8 lane ports that operate independently
- Reduces number of signal pins over traditional memories, increases signal integrity allowing longer board traces to ease board signal routing
- Operates across connectors

Main Memory

- 1Gb
  - 4 partitions/128 banks
  - 16 READ & 16 WRITE ports
- 2.7 ns tRC
- Allows parallel partition & Bank execution
- Up to 6B rd/s + 6B wr/s simultaneously



Memory/Function Controller

- Resolves localized bank conflicts
- Directs read/write function to selected bank of memory
- Manages the sequence of operations to execute a RMW
  - 4-8x reduction in RMW accesses
  - Insures no stale data (mutec)
- Controls parallel function execution
- Four Domain levels for function execution priority setting
- Multiple scheduling domains minimize blocking short latency operation by long latency operations

Result Reordering

- Reorder buffers insure that results are returned to the output of the submitted input port and tagged with priority Domain if used

Software Define - Hardware Accelerated

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https://mosys.com/blazar-family-of-accelerator-engines/

Software and System Architects can improve application performance by accelerating the memory access and utilizing the In Memory Compute Functions.

The different Accelerator Engine devices allow application tuning to achieve increasing levels of performance up to our most powerful engine… the Programable HyperSpeed Engine with 32 Processor Cores.

	Part Number	Description	Package	Interface					Memory		Access Rate	Commands /Functions		
			Pkg Size	Lanes	Rate per Lane			BW	tRC	Size	Billion			Custom
			mm	Tx/Rx	10-12.5G	15G	25-28G	Gb	ns	Gb	Transaction/s	R/W	RMW / ALU	32 RISC Cores
BURST	MSR620	Bandwidth Engine 2 Burst Serial 0.5Gb High Access Memory	FCBGA 19x19	16	✓			320	3.2	0.5	3.3	✓		
BURST	MSR630	Bandwidth Engine 3 Burst Serial 1Gb High Access Memory	FCBGA 27x27	16	✓	✓	✓	717	2.7	1	6.5	✓		
RMW	MSR820	Bandwidth Engine 2 RMW Serial 0.5Gb High Access Memory with ALU for RMW functiions	FCBGA 19x19	16	✓			320	3.2	0.5	3.3	✓	✓	
RMW	MSR830	Bandwidth Engine 3 RMW Serial 1Gb High Access Memory with ALU for RMW functiions	FCBGA 27x27	16	✓	✓	✓	717	2.7	1	6.5	✓	✓	
Program	MSPS30	Programmable Accelerator Engine Serial Interface, 1Gb Memory, 32 RISC Processor cores for custom algorithms, compute, functions	FCBGA 27x27	16	✓	✓	✓	717	2.7	1	24 Internal	✓	✓	✓

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