16Mb [x8 or x16] Automotive Temperature Range MRAM

FEATURES

- Automotive -40 /+125°C temperature range.
- 45 ns Read/Write cycle.
- 3.3 Volt power supply.
- Unlimited Read & Write endurance.
- Retains data on power loss.
- Data non-volatile for >20 years at temperature.
- SRAM compatible timing with existing SRAM controllers.
- Replaces Flash, SRAM, EEPROM or BBSRAM.
- Meets MSL-3 moisture sensitivity requirements.
- RoHS-compliant, SRAM-compatible TSOP2 Package

MR4A08BUYS45
44-TSOP2

MR4A16BUYS45
54-TSOP2

RoHS

INTRODUCTION

The **MR4A08BUYS45** [x8] is a 16,777,216-bit magnetoresistive random access memory (MRAM) device organized as 2,097,152 words of 8 bits. It is available in a 44-pin thin small outline package (TSOP Type 2), compatible with similar low-power SRAM products and other nonvolatile RAM products.

The **MR4A16BUYS45** [x16] is a 16,777,216-bit magnetoresistive random access memory (MRAM) device organized as 1,048,576 words of 16 bits. It is available in a 54-pin thin small outline package (TSOP Type 2), compatible with similar low-power SRAM products and other nonvolatile RAM products.

Both products have a -40/+125°C operating temperature range and offer SRAM-compatible 45ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20 years and automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. Data retention is duty cycle limited at the temperature extremes.

These products are the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly, providing high reliability storage over the automotive temperature range of -40/+125°C. These products are not AEC Q-100 qualified.

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BLOCK DIAGRAMS AND DEVICE PIN FUNCTIONS

Figure 1 – MR4A08BUYS45 Block Diagram

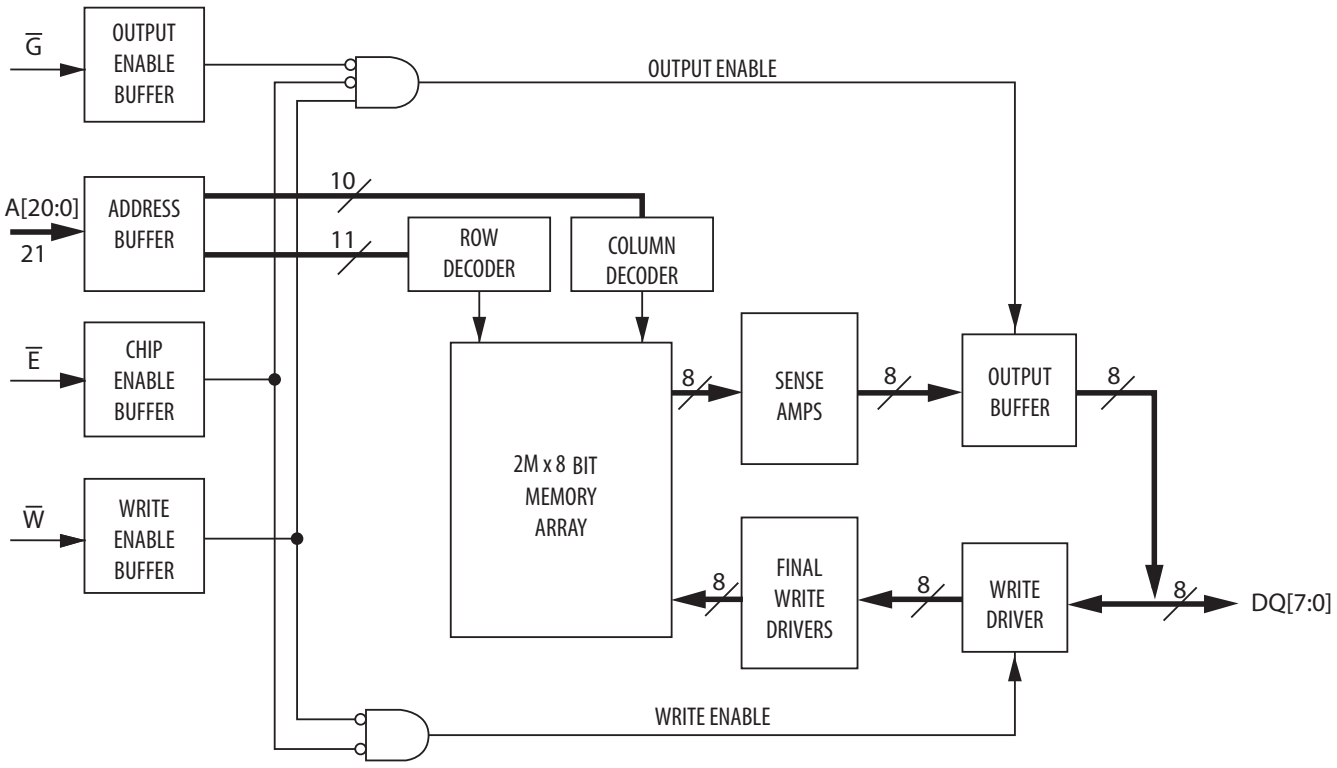


Table 1 – MR4A08BUYS45 Pin Functions

Signal Name	Function
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data I/O
V_{DD}	Power Supply
V_{SS}	Ground
DC	Do Not Connect
NC	No Connection

Figure 2 – MR4A16BUYS45 Block Diagram

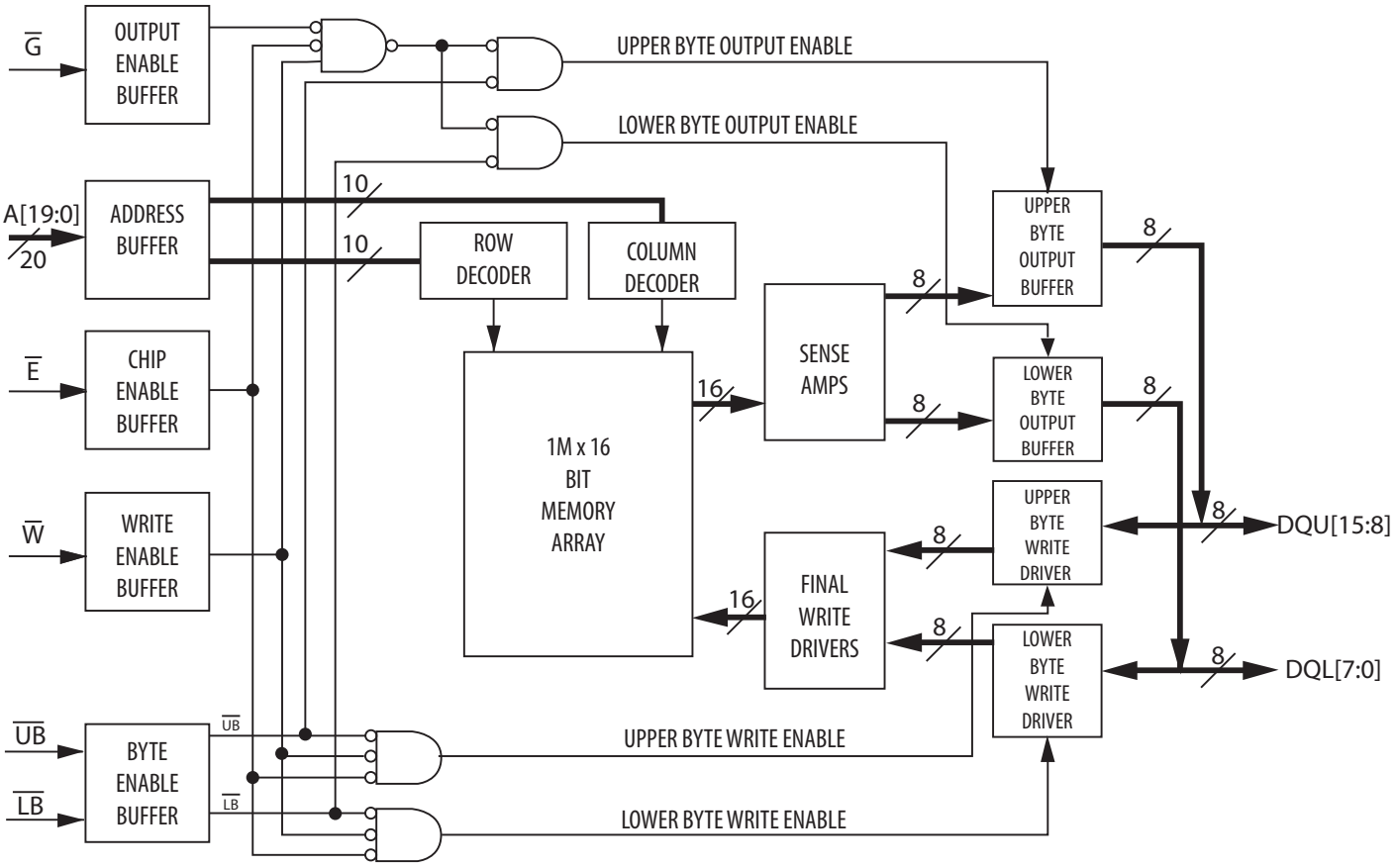
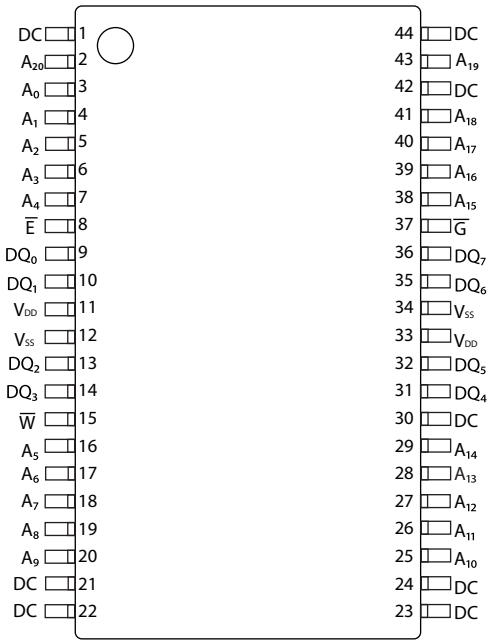


Table 2 – MR4A16BUYS45 Pin Functions

Signal Name	Function
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{UB}$	Upper Byte Enable
$\overline{LB}$	Lower Byte Enable
DQ	Data I/O
V_{DD}	Power Supply
V_{SS}	Ground
DC	Do Not Connect
NC	No Connection

PACKAGE PINOUTS AND OPERATING MODES

Figure 3 – MR4A08BUYS45 TSOP2 Package Pinouts



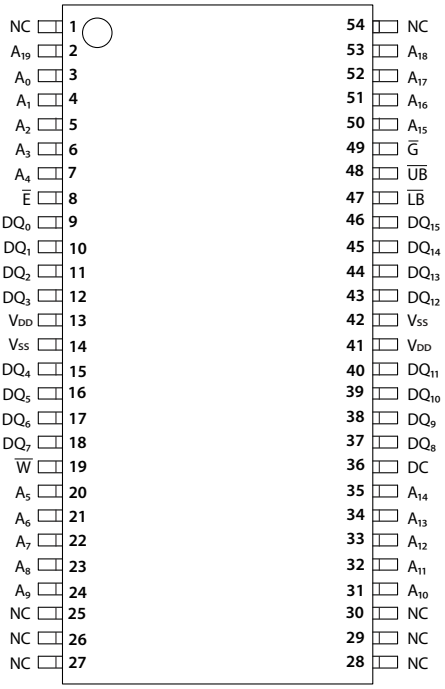
44-TSOP2

Table 3 – MR4A08BUYS45 Operating Modes

$\overline{E}$ [1]	$\overline{G}$ [1]	$\overline{W}$ [1]	Mode	V_{DD} Current	DQ[7:0] [2]
H	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z
L	H	H	Output disabled	I_{DDR}	Hi-Z
L	L	H	Byte Read	I_{DDR}	D_{Out}
L	X	L	Byte Write	I_{DDW}	D_{in}

1. H = high, L = low, X = don't care
2. Hi-Z = high impedance

Figure 4 – MR4A16BUYS45 TSOP2 Package Pinouts



54-TSOP2

Table 4 – MR4A16BUYS45 Operating Modes

$\overline{E}$ [1]	$\overline{G}$ [1]	$\overline{W}$ [1]	$\overline{LB}$ [1]	$\overline{UB}$ [1]	Mode	V_{DD} Current	DQL[7:0] [2]	DQU[15:8] [2]
H	X	X	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z	Hi-Z
L	H	H	X	X	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	X	X	H	H	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	L	H	L	H	Lower Byte Read	I_{DDR}	D_{Out}	Hi-Z
L	L	H	H	L	Upper Byte Read	I_{DDR}	Hi-Z	D_{Out}
L	L	H	L	L	Word Read	I_{DDR}	D_{Out}	D_{Out}
L	X	L	L	H	Lower Byte Write	I_{DDW}	D_{in}	Hi-Z
L	X	L	H	L	Upper Byte Write	I_{DDW}	Hi-Z	D_{in}
L	X	L	L	L	Word Write	I_{DDW}	D_{in}	D_{in}

1. H = high, L = low, X = don't care
2. Hi-Z = high impedance

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

These devices contain circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.
The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field greater than the maximum field intensity specified in the maximum ratings.

Table 5 – Absolute Maxium Ratings

Parameter	Symbol	Value	Unit
Supply voltage [2]	V_{DD}	-0.5 to 4.0	V
Voltage on any pin [2]	V_{IN}	-0.5 to V_{DD} + 0.5	V
Output current per pin	I_{OUT}	±20	mA
Package power dissipation [3]	P_D	0.600	W
Temperature under bias	T_{BIAS}	-45 to 130	°C
Storage Temperature	T_{stg}	-55 to 150	°C
Lead temperature during solder (3 minute max)	T_{Lead}	260	°C
Maximum magnetic field during write	H_{max_write}	8000	A/m
Maximum magnetic field during read or standby	H_{max_read}	8000	A/m

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2. All voltages are referenced to V_{SS}. The DC value of V_{IN} must not exceed actual applied V_{DD} by more than 0.5V. The AC value of V_{IN} must not exceed applied V_{DD} by more than 2V for 10ns with I_{IN} limited to less than 20mA.
3. Power dissipation capability depends on package characteristics and use environment.

Operating Conditions

Table 6 – Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Power supply voltage	V_{DD}	3.0 [1]	3.3	3.6	V
Write inhibit voltage	V_{WI}	2.5	2.7	3.0 [1]	V
Input high voltage	V_{IH}	2.2	-	V_{DD} + 0.3 [2]	V
Input low voltage	V_{IL}	-0.5 [3]	-	0.8	V
Ambient Operating Temperature [4]	T_A	-40	-	+125	°C

1. There is a 2 ms startup time once V_{DD} exceeds $V_{DD,}$(min). See "Power Up and Power Down Sequencing" below.
2. V_{IH}(max) = V_{DD} + 0.3 V_{DC}; V_{IH}(max) = V_{DD} + 2.0 V_{AC} (pulse width ≤ 10 ns) for I ≤ 20.0 mA.
3. V_{IL}(min) = -0.5 V_{DC} ; V_{IL}(min) = -2.0 V_{AC} (pulse width ≤ 10 ns) for I ≤ 20.0 mA.
4. The ambient operature temperature rating assumes a 10% duty cycle (2 years out of 20 years life) for operating temperatures between +85°C and +125°C.

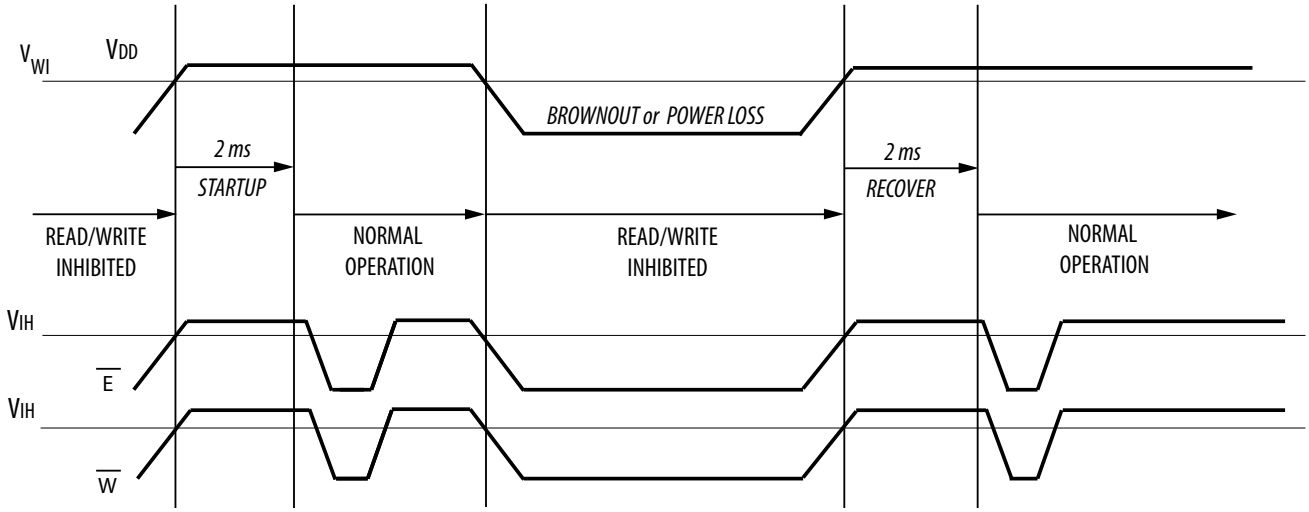
Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI}. As soon as V_{DD} exceeds V_{DD}(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The $\overline{E}$ and $\overline{W}$ control signals should track V_{DD} on power up to V_{DD}- 0.2 V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that a signal remains high if the driving signal is Hi-Z during power up. Any logic that drives $\overline{E}$ and $\overline{W}$ should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI}, writes are protected and a startup time must be observed when power returns above V_{DD}(min).

Figure 5 – Power Up and Power Down Sequencing



DC and Power Supply Characteristics

Table 7 – DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$I_{lkg(I)}$	Input leakage current	All	-	±1	µA
$I_{lkg(O)}$	Output leakage current	All	-	±1	µA
V_{OL}	Output low voltage	I_{OL} = +4 mA	-	0.4	V
		I_{OL} = +100 µA		V_{SS} + 0.2	V
V_{OH}	Output high voltage	I_{OH} = -4 mA	2.4	-	V
		I_{OH} = -100 µA	V_{DD} - 0.2	-	V

Table 8 – Power Supply Characteristics

Symbol	Parameter	Typical	Max	Unit
I_{DDR}	AC active supply current - read modes [1] I_{OUT} = 0 mA, V_{DD} = max.	60	68	mA
I_{DDW}	AC active supply current - write modes[1] V_{DD} = max	152	180	mA
I_{SB1}	AC standby current V_{DD} = max, $\overline{E} = V_{IH}$ *No other restrictions on other inputs.*	9	14	mA
I_{SB2}	CMOS standby current $\overline{E} \geq V_{DD}$ - 0.2 V and $V_{In} \leq V_{SS}$ + 0.2 V or $\geq V_{DD}$ - 0.2 V V_{DD} = max, f = 0 MHz	5	9	mA

1. All active current measurements are measured with one address transition per cycle and at minimum cycle time.

TIMING SPECIFICATIONS

Table 9 – Capacitance [1]

Symbol	Parameter	Typical	Max	Unit
C_{In}	Address input capacitance	-	6	pF
C_{In}	Control input capacitance	-	6	pF
$C_{I/O}$	Input/Output capacitance	-	8	pF

1. f = 1.0 MHz, dV = 3.0 V, T_A = 25 °C, periodically sampled rather than 100% tested.

Table 10 – AC Measurement Conditions

Parameter	Value	Unit
Logic input timing measurement reference level	1.5	V
Logic output timing measurement reference level	1.5	V
Logic input pulse levels	0 or 3.0	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure 6	
Output load for all other timing parameters	See Figure 7	

Figure 6 – Output Load Test Low and High

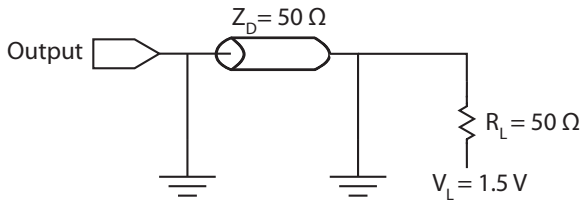
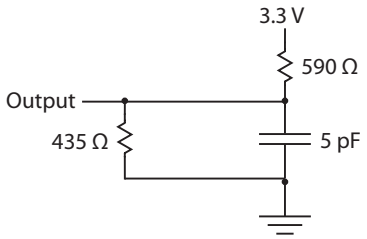


Figure 7 – Output Load Test All Other Parameters



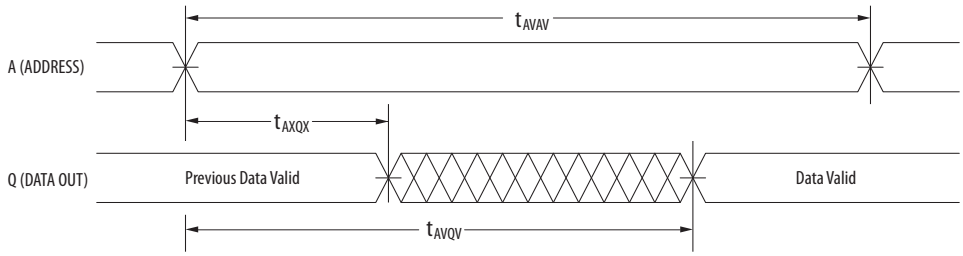
Read Mode

Table 11 – Read Cycle Timing

Symbol	Parameter	Min	Max	Unit
t_{AVAV}	Read cycle time	45	-	ns
t_{AVQV}	Address access time	-	45	ns
t_{ELQV}	Enable access time [2]	-	45	ns
t_{GLQV}	Output enable access time	-	15	ns
t_{BLQV}	Byte enable access time	-	15	ns
t_{AXQX}	Output hold from address change	3	-	ns
t_{ELQX}	Enable low to output active [3]	3	-	ns
t_{GLQX}	Output enable low to output active [3]	0	-	ns
t_{BLQX}	Byte enable low to output active [3]	0	-	ns
t_{EHQZ}	Enable high to output Hi-Z [3]	0	15	ns
t_{GHQZ}	Output enable high to output Hi-Z [3]	0	10	ns
t_{BHQZ}	Byte high to output Hi-Z [3]	0	10	ns

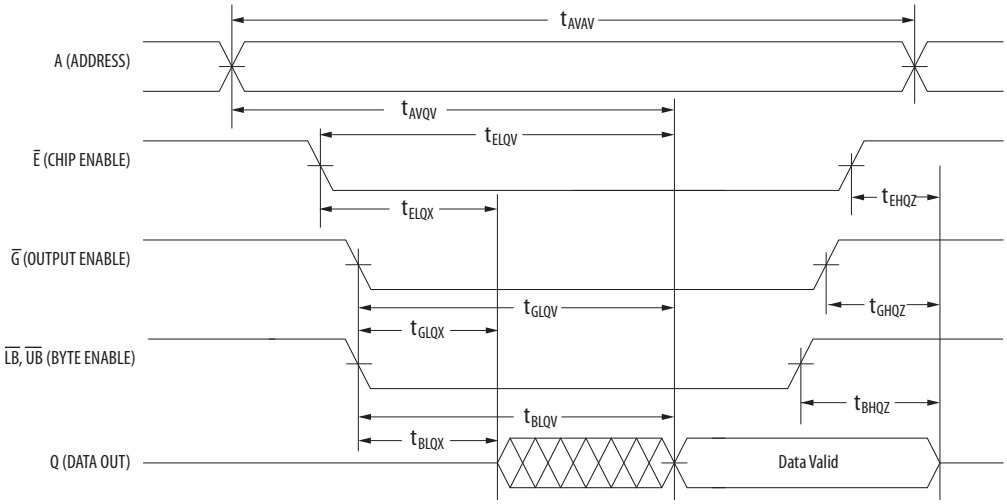
1. $\overline{W}$ is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
2. Addresses valid before or at the same time $\overline{E}$ goes low.
3. This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage.

Figure 8 – Read Cycle 1



Note: Device is continuously selected ($\overline{E} \leq V_{IL}$, $\overline{G} \leq V_{IL}$).

Figure 9 – Read Cycle 2



Write Mode

Table 12 – Write Cycle Timing 1 ($\overline{W}$ Controlled) [1]

Symbol	Parameter	Min	Max	Unit
t_{AVAV}	Write cycle time [2]	45	-	ns
t_{AVWL}	Address set-up time	0	-	ns
t_{AVWH}	Address valid to end of write ($\overline{G}$ high)	30	-	ns
t_{AVWH}	Address valid to end of write ($\overline{G}$ low)	30	-	ns
t_{WLWH} t_{WLEH}	Write pulse width ($\overline{G}$ high)	15	-	ns
t_{WLWH} t_{WLEH}	Write pulse width ($\overline{G}$ low)	15	-	ns
t_{DVWH}	Data valid to end of write	10	-	ns
t_{WHDX}	Data hold time	0	-	ns
t_{WLQZ}	Write low to data Hi-Z [3]	0	15	ns
t_{WHQX}	Write high to output active [3]	3	-	ns
t_{WHAX}	Write recovery time	12	-	ns

1. All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$, $\overline{E}$ or $\overline{UB}$/$\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage. At any given voltage or temperate, $t_{WLQZ}(max) < t_{WHQX}(min)$.

Figure 10 – Write Cycle Timing 1 ($\overline{W}$ Controlled)

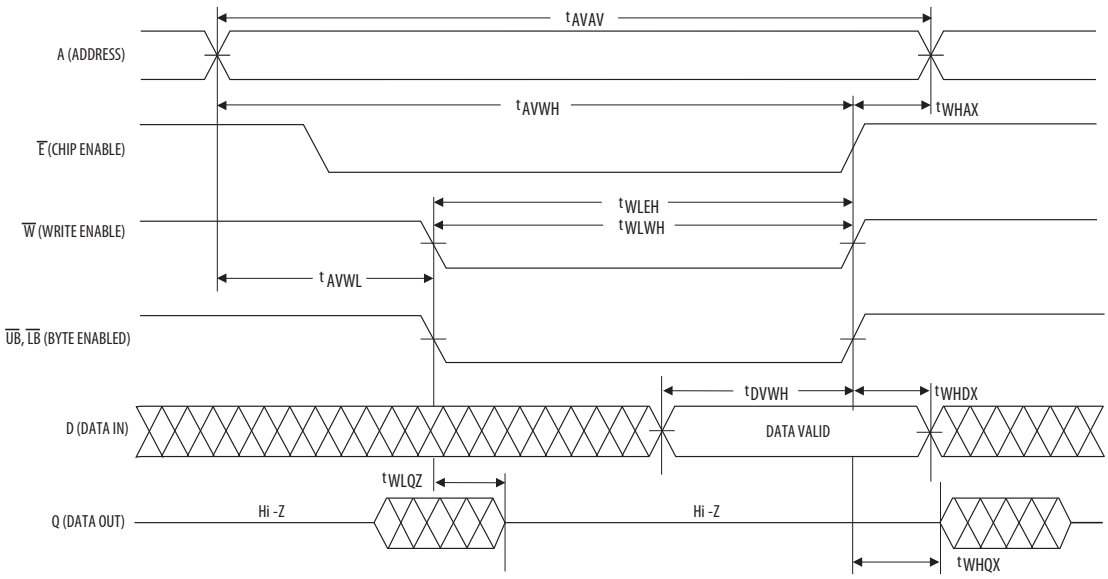


Table 13 – Write Cycle Timing 2 ($\overline{E}$ Controlled) [1]

Symbol	Parameter	Min	Max	Unit
t_{AVAV}	Write cycle time [2]	45	-	ns
t_{AVEL}	Address set-up time	0	-	ns
t_{AVEH}	Address valid to end of write ($\overline{G}$ high)	30	-	ns
t_{AVEH}	Address valid to end of write ($\overline{G}$ low)	30	-	ns
t_{ELEH} t_{ELWH}	Enable to end of write ($\overline{G}$ high)	15	-	ns
t_{ELEH} t_{ELWH}	Enable to end of write ($\overline{G}$ low) [3]	15	-	ns
t_{DVEH}	Data valid to end of write	10	-	ns
t_{EHDX}	Data hold time	0	-	ns
t_{EHAX}	Write recovery time	12	-	ns

1. All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$, $\overline{E}$ or $\overline{UB}$/ $\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. If $\overline{E}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state. If $\overline{E}$ goes high at the same time or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

Figure 11 – Write Cycle Timing 2 ($\overline{E}$ Controlled)

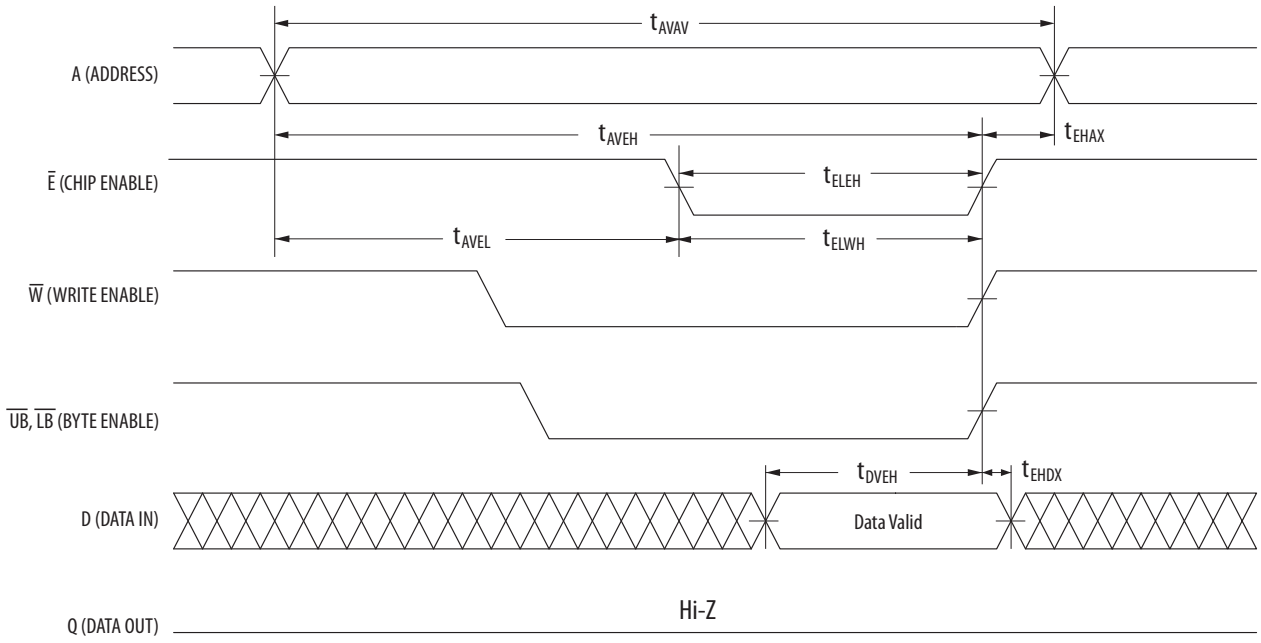
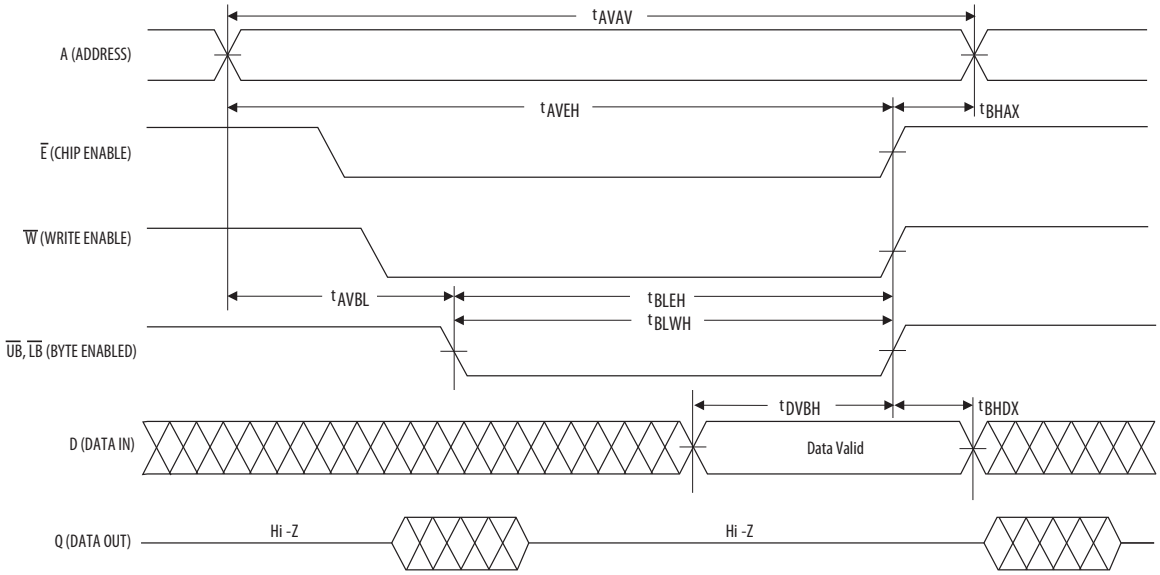


Table 14 – Write Cycle Timing 3 ($\overline{LB}$/$\overline{UB}$ Controlled) [1]

Symbol	Parameter	Min	Max	Unit
t_{AVAV}	Write cycle time [2]	45	-	ns
t_{AVBL}	Address set-up time	0	-	ns
t_{AVBH}	Address valid to end of write ($\overline{G}$ high)	30	-	ns
t_{AVBH}	Address valid to end of write ($\overline{G}$ low)	30	-	ns
t_{BLEH} t_{BLWH}	Write pulse width ($\overline{G}$ high)	15	-	ns
t_{BLEH} t_{BLWH}	Write pulse width ($\overline{G}$ low)	15	-	ns
t_{DVBH}	Data valid to end of write	10	-	ns
t_{BHDX}	Data hold time	0	-	ns
t_{BHAX}	Write recovery time	12	-	ns

1. All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$, $\overline{E}$ or $\overline{UB}$/$\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.

Figure 12 – Write Cycle Timing 3 ($\overline{LB}$/$\overline{UB}$ Controlled)



ORDERING INFORMATION

Table 15 – Part Number Decoder

		Memory	Density	Type	I/O Width	Rev.	Temp	Package	Speed	Packing	Grade
Example Ordering Part Number		MR	4	A	08	B	U	YS	45	R	ES
MRAM	MR										
16 Mb	4										
Async 3.3v	A										
8-bit	08										
16-bit	16										
Rev B	B										
Automotive -40 to 125°C	U										
TSOP2	YS										
45 ns	45										
Tray	Blank										
Tape and Reel	R										
Engineering Samples	ES										
Customer Samples	CS										
Mass Production	Blank										

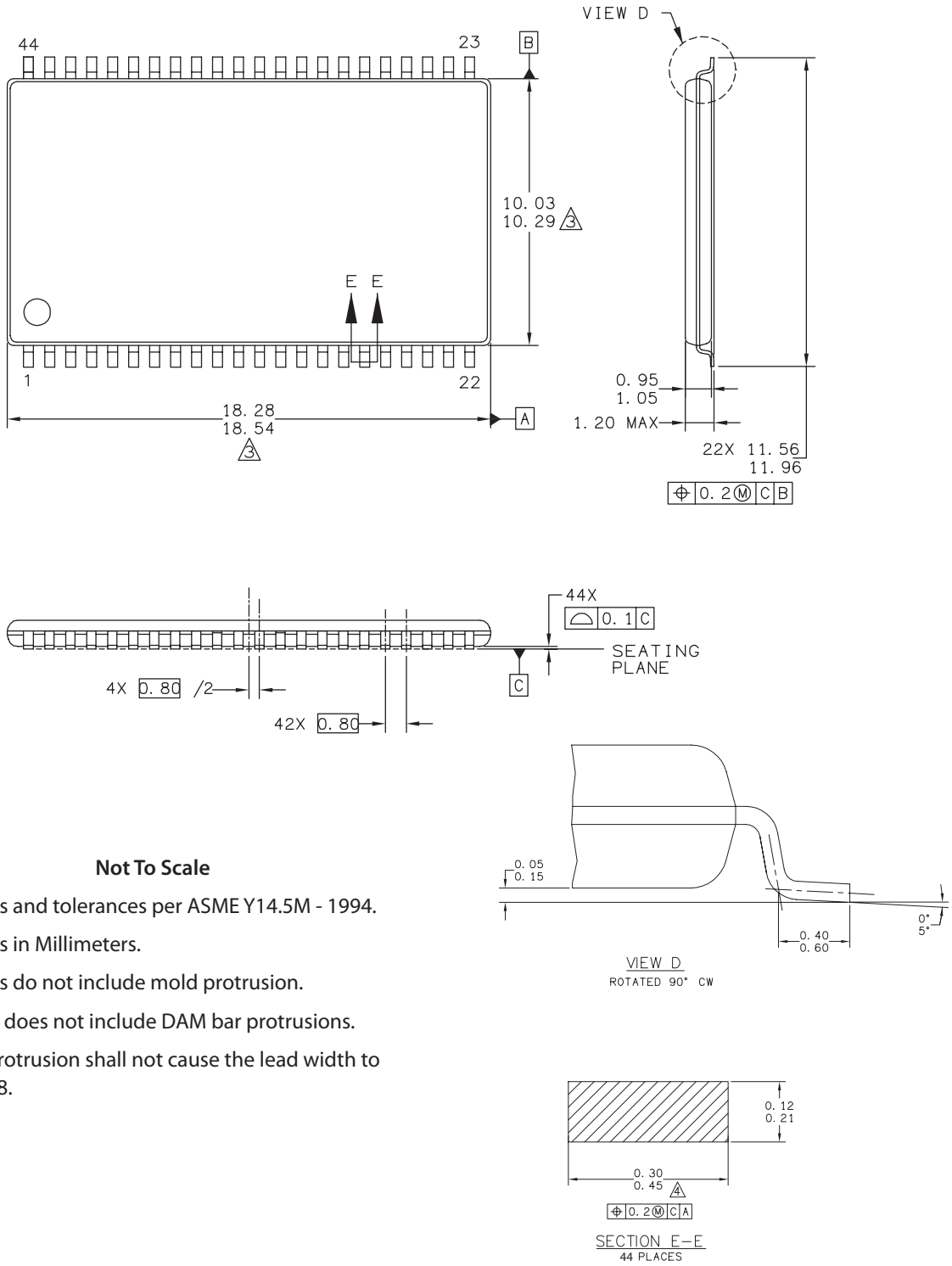
Table 16 – Ordering Part Numbers

Grade	Temp Range	Density	I/O Width	Package	Shipping Container	Order Part Number
Automotive [1]	-40 to +125 °C	16Mb	x8	44-TSOP2	Trays	MR4A08BUYS45
					Tape & Reel	MR4A08BUYS45R
			x16	54-TSOP2	Trays	MR4A16BUYS45
					Tape & Reel	MR4A16BUYS45R

1. Not AEC Q-100 Qualified.

PACKAGE OUTLINE DRAWINGS

Figure 13 – 44-TSOP2 Package Outline Drawing



Not To Scale

1. Dimensions and tolerances per ASME Y14.5M - 1994.
2. Dimensions in Millimeters.
3. Dimensions do not include mold protrusion.
4. Dimension does not include DAM bar protrusions.
5. DAM Bar protrusion shall not cause the lead width to exceed 0.58.

Figure 14 – 54-TSOP2 Package Outline Drawing

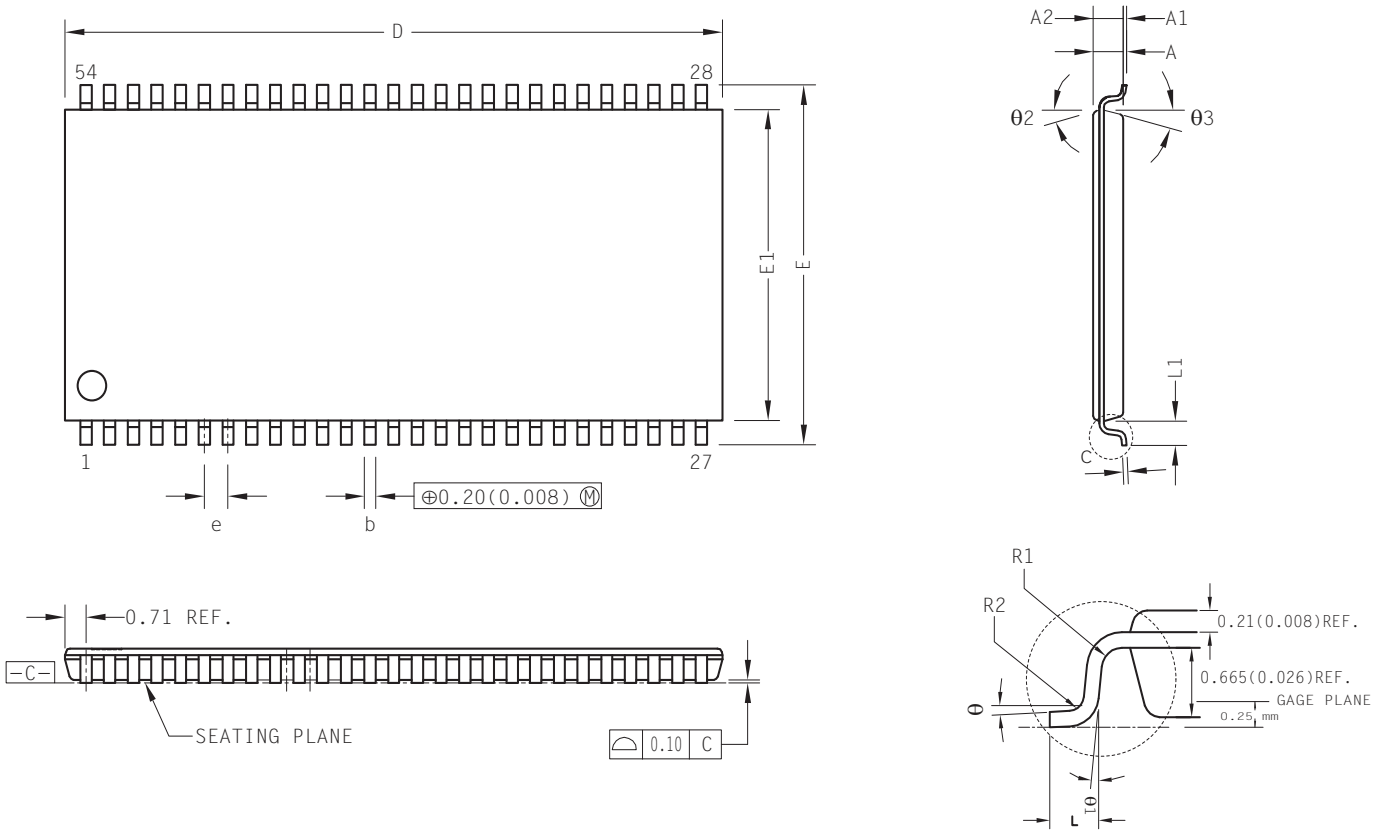


Figure 14 - 54-TSOP2 Package Outline Drawing - Cont'd

Ref	Min	Nominal	Max
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.30	0.35	0.45
c	0.12		0.21
D	22.10	22.22	22.35
E	11.56	11.76	11.95
E1	10.03	10.16	10.29
e	0.80 BSC		
L	0.40	0.50	0.60
L1	0.80 REF		
R1	0.12	-	-
R2	0.12	-	0.25
θ	0°	-	8°
θ1	0.40	-	-
θ2	15° REF		
θ3	15° REF		

1. Dimensions in Millimeters.
2. Package dimensions refer to JEDEC MS-024

REVISION HISTORY

Rev	Date	Description of Change
1.0	November 18, 2015	Initial release.

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