RELIABILITY REPORT

FOR

MAX2691EWS+

WAFER LEVEL PRODUCTS

February 6, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineer

Conclusion

The MAX2691EWS+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX2691 low-noise amplifier (LNA) is designed for GPS L2 applications. Designed in Maxim's advanced SiGe process, the device achieves high gain and low noise figure while maximizing the input-referred 1dB compression point and the 3rd-order intercept point. The MAX2691 provides a high gain of 17.5dB and sub 1dB noise figure. The device operates from a +1.6V to +3.6V single supply. The optional shutdown feature in the device reduces the typical supply current to 4µA. The device is available in a very small, lead-free, RoHS-compliant, 0.86mm x 0.86mm x 0.65mm wafer-level package (WLP).

II. Manufacturing Information

A. Description/Function:	L2 Band GPS Low-Noise Amplifier
B. Process:	MB3
C. Number of Device Transistors:	1057
D. Fabrication Location:	California
E. Assembly Location:	Japan
F. Date of Initial Production:	December 20, 2011

III. Packaging Information

A. Package Type:	4 bmp WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	N/A
G. Assembly Diagram:	#05-9000-4074
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	103°C/W
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	33.86X33.86 mils
B. Passivation:	BCB
C. Interconnect:	Al with top layer 100% Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35um
F. Minimum Metal Spacing:	0.35um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the MB3 Process results in a FIT Rate of 0.05 @ 25C and 0.88 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot SI3XFA006B, D/C 1116)

The WV21-4 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX2691EWS+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SI3YCQ001E, D/C 1017

Note 1: Life Test Data may represent plastic DIP qualification lots.