19-3404; Rev 1; 10/06

EVALUATION KIT AVAILABLE

# LF-to-2.5GHz Dual Logarithmic Detector/ Controller for Power, Gain, and VSWR Measurements



## General Description

The MAX2016 dual logarithmic detector/controller is a fully integrated system designed for measuring and comparing power, gain/loss, and voltage standing-wave ratio (VSWR) of two incoming RF signals. An internal broadband impedance match on the two differential RF input ports allows for the simultaneous monitoring of signals ranging from low frequency to 2.5GHz.

The MAX2016 uses a pair of logarithmic amplifiers to detect and compare the power levels of two RF input signals. The device internally subtracts one power level from the other to provide a DC output voltage that is proportional to the power difference (gain). The MAX2016 can also measure the return loss/VSWR of an RF signal by monitoring the incident and reflected power levels associated with any given load. A window detector is easily implemented by using the on-chip comparators, OR gate, and 2V reference. This combination of circuitry provides an automatic indication of when the measured gain is outside a programmable range. Alarm monitoring can thus be implemented for detecting high-VSWR states (such as open or shorted loads).

The MAX2016 operates from a single +2.7V to +5.25V* power supply and is specified over the extended -40°C to +85°C temperature range. The MAX2016 is available in a space-saving, 5mm x 5mm, 28-pin thin QFN.

## Applications

Return Loss/VSWR Measurements

Dual-Channel RF Power Measurements

Dual-Channel Precision AGC/RF Power Control

Log Ratio Function for RF Signals

Remote System Monitoring and Diagnostics

Cellular Base Station, Microwave Link, Radar, and other Military Applications

RF/IF Power Amplifier (PA) Linearization

***Typical Application Circuit appears at end of data sheet.***

## Features

- ♦ **Complete Gain and VSWR Detector/Controller**
- ♦ **Dual-Channel RF Power Detector/Controller**
- ♦ **Low-Frequency to 2.5GHz Frequency Range**
- ♦ **Exceptional Accuracy Over Temperature**
- ♦ **High 80dB Dynamic Range**
- ♦ **2.7V to 5.25V Supply Voltage Range***
- ♦ **Internal 2V Reference**
- ♦ **Scaling Stable Over Supply and Temperature Variations**
- ♦ **Controller Mode with Error Output**
- ♦ **Available in 5mm x 5mm, 28-Pin Thin QFN Package**

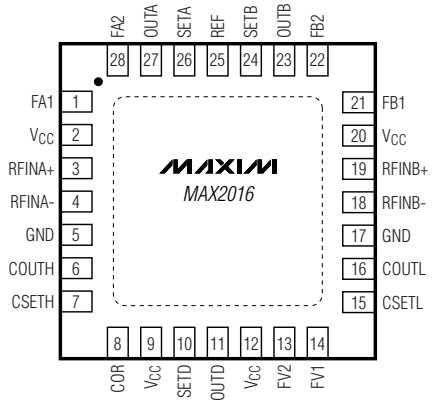
*See *Power-Supply Connection* section.

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | PKG CODE |
|---|---|---|---|
| MAX2016ETI | -40°C to +85°C | 28 Thin QFN-EP*, bulk | T2855-3 |
| MAX2016ETI-T | -40°C to +85°C | 28 Thin QFN-EP*, T/R | T2855-3 |
| MAX2016ETI+D | -40°C to +85°C | 28 Thin QFN-EP*, lead free, bulk | T2855-3 |
| MAX2016ETI+TD | -40°C to +85°C | 28 Thin QFN-EP*, lead free, T/R | T2855-3 |

*EP = Exposed pad.
+Indicates lead-free package.
D = Dry pack.

## Pin Configuration




THIN QFN

# LF-to-2.5GHz Dual Logarithmic Detector/ Controller for Power, Gain, and VSWR Measurements

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ to GND .....-0.3V to +5.25V
Input Power Differential (RFIN_+, RFIN_-).....+23dBm
Input Power Single Ended (RFIN_+ or RFIN _-).....+19dBm
All Other Pins to GND.....-0.3V to ($V_{CC}$ + 0.3V)
Continuous Power Dissipation ($T_A$ = +70°C)
28-Pin, 5mm x 5mm Thin QFN (derate 35.7mW/°C above +70°C).....2.8W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +2.7V to +3.6V, $R_1$ = $R_2$ = $R_3$ = 0Ω, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V, CSETL = CSETH = $V_{CC}$, 50Ω RF system, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Supply Voltage | $V_S$ | $R_6$ = 0Ω | 2.7 | 3.3 | 3.6 | V |
| | $V_S$ | $R_6$ = 37.4Ω | 4.75 | 5 | 5.25 | |
| Total Supply Current | $I_{CC}$ | | | 43 | 55 | mA |
| Supply Current | | Measured in each pin 2 and pin 20 | | 16 | | mA |
| | | Measured in pin 9 | | 2 | | |
| | | Measured in pin 12 | | 9 | | |
| **INPUT INTERFACE** | | | | | | |
| Input Impedance | | Differential impedance at RFINA and RFINB | | 50 | | Ω |
| Input Resistance | R | Resistance at SETD | | 20 | | kΩ |
| | | Resistance at SETA and SETB | | 40 | | |
| **DETECTOR OUTPUT** | | | | | | |
| Source Current | | Measured at OUTA, OUTB, and OUTD | | 4 | | mA |
| Sink Current | | Measured at OUTA, OUTB, and OUTD | | 0.45 | | mA |
| Minimum Output Voltage | | Measured at OUTA, OUTB, and OUTD | | 0.5 | | V |
| Maximum Output Voltage | | Measured at OUTA, OUTB, and OUTD | | 1.8 | | V |
| Difference Output VOUTD | | $P_{RFINA}$ = $P_{RFINB}$ = -30dBm | | 1 | | V |
| OUTD Accuracy | | | | ±12 | | mV |
| **COMPARATORS** | | | | | | |
| Output High Voltage | $V_{OH}$ | $R_{LOAD}$ ≥ 10kΩ | | $V_{CC}$ - 10mV | | V |
| Output Low Voltage | $V_{OL}$ | $R_{LOAD}$ ≥ 10kΩ | | 10 | | mV |
| Input Voltage | | Measured at CSETL and CSETH | | GND to $V_{CC}$ | | V |
| Input Bias Current | | CSETL and CSETH | | 1 | | nA |
| **REFERENCE** | | | | | | |
| Output Voltage on Pin 25 | | $R_{LOAD}$ ≥ 2kΩ | | 2 | | V |
| Load Regulation | | Source 2mA | | -5 | | mV |

## AC ELECTRICAL CHARACTERISTICS—OUTA AND OUTB

(*Typical Application Circuit*, $V_{CC}$ = +2.7V to +3.3V, $R_1 = R_2 = R_3 = 0\Omega$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = 3.3V, CSETL = CSETH = $V_{CC}$, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| RF Input Frequency Range | $f_{RF}$ | AC-coupled input | | | | 2.5 | GHz |
| Return Loss | $S_{11}$ | 0.1GHz to 3GHz | | | 20 | | dB |
| Large-Signal Response Time | | $P_{RFIN}$ = no signal to 0dBm, ±0.5dB settling accuracy | | | 100 | | ns |
| **RSSI MODE—0.1GHz** | | | | | | | |
| RF Input Power Range | | (Note 2) | | | -70 to +10 | | dBm |
| ±3dB Dynamic Range | | $T_A$ = -20°C to +85°C (Note 3) | | | 80 | | dB |
| Range Center | | | | | -32 | | dBm |
| Temperature Sensitivity | | $P_{RFINA} = P_{RFINB}$ = -32dBm | $T_A$ = +25°C to +85°C | | +0.0083 | | dB/°C |
| | | | $T_A$ = +25°C to -20°C | | -0.0083 | | |
| Slope | | (Note 4) | | | 19 | | mV/dB |
| Typical Slope Variation | | $T_A$ = -20°C to +85°C | | | -4 | | µV/°C |
| Intercept | | (Note 5) | | | -100 | | dBm |
| Typical Intercept Variation | | $T_A$ = -20°C to +85°C | | | 0.03 | | dBm/°C |
| **RSSI MODE—0.9GHz** | | | | | | | |
| RF Input Power Range | | (Note 2) | | | -70 to +10 | | dBm |
| ±3dB Dynamic Range | | $T_A$ = -20°C to +85°C (Note 3) | | | 80 | | dB |
| Range Center | | | | | -30 | | dBm |
| Temperature Sensitivity | | $P_{RFINA} = P_{RFINB}$ = -30dBm | $T_A$ = +25°C to +85°C | | +0.0083 | | dB/°C |
| | | | $T_A$ = +25°C to -20°C | | -0.0083 | | |
| Slope | | (Note 4) | | | 18.1 | | mV/dB |
| Typical Slope Variation | | $T_A$ = -20°C to +85°C | | | -4 | | µV/°C |
| Intercept | | (Note 5) | | | -97 | | dBm |
| Typical Intercept Variation | | $T_A$ = -20°C to +85°C | | | 0.02 | | dBm/°C |
| **RSSI MODE—1.9GHz** | | | | | | | |
| RF Input Power Range | | (Note 2) | | | -55 to +12 | | dBm |
| ±3dB Dynamic Range | | $T_A$ = -20°C to +85°C (Note 3) | | | 67 | | dB |
| Range Center | | | | | -27 | | dBm |
| Temperature Sensitivity | | $P_{RFINA} = P_{RFINB}$ = -27dBm | $T_A$ = +25°C to +85°C | | +0.0125 | | dB/°C |
| | | | $T_A$ = +25°C to -20°C | | -0.0125 | | |
| Slope | | (Note 4) | | | 18 | | mV/dB |
| Typical Slope Variation | | $T_A$ = -20°C to +85°C | | | -4.8 | | µV/°C |
| Intercept | | (Note 5) | | | -88 | | dBm |
| Typical Intercept Variation | | $T_A$ = -20°C to +85°C | | | 0.03 | | dBm/°C |

# LF-to-2.5GHz Dual Logarithmic Detector/ Controller for Power, Gain, and VSWR Measurements

## AC ELECTRICAL CHARACTERISTICS—OUTA AND OUTB (continued)

(*Typical Application Circuit*, $V_{CC}$ = +2.7V to +3.3V, $R_1 = R_2 = R_3 = 0\Omega$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = 3.3V, CSETL = CSETH = $V_{CC}$, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **RSSI MODE—2.17GHz** | | | | | | | |
| RF Input Power Range | | (Note 2) | | | -52 to +12 | | dBm |
| ±3dB Dynamic Range | | $T_A$ = -20°C to +85°C (Note 3) | | | 64 | | dB |
| Range Center | | | | | -25 | | dBm |
| Temperature Sensitivity | | $P_{RFINA} = P_{RFINB}$ = -25dBm | $T_A$ = +25°C to +85°C | | +0.0135 | | dB/°C |
| | | | $T_A$ = +25°C to -20°C | | -0.0135 | | |
| Slope | | (Note 4) | | | 17.8 | | mV/dB |
| Typical Slope Variation | | $T_A$ = -20°C to +85°C | | | -8 | | µV/°C |
| Intercept | | (Note 5) | | | -81 | | dBm |
| Typical Intercept Variation | | $T_A$ = -20°C to +85°C | | | 0.03 | | dBm/°C |
| **RSSI MODE—2.5GHz** | | | | | | | |
| RF Input Power Range | | (Note 2) | | | -45 to +7 | | dBm |
| ±3dB Dynamic Range | | $T_A$ = -20°C to +85°C (Note 3) | | | 52 | | dB |
| Range Center | | | | | -23 | | dBm |
| Temperature Sensitivity | | $P_{RFINA} = P_{RFINB}$ = -23dBm | $T_A$ = +25°C to +85°C | | +0.0167 | | dB/°C |
| | | | $T_A$ = +25°C to -20°C | | -0.0167 | | |
| Slope | | (Note 4) | | | 17.8 | | mV/dB |
| Typical Slope Variation | | $T_A$ = -20°C to +85°C | | | -8 | | µV/°C |
| Intercept | | (Note 5) | | | -80 | | dBm |
| Typical Intercept Variation | | $T_A$ = -20°C to +85°C | | | 0.03 | | dBm/°C |

## AC ELECTRICAL CHARACTERISTICS—OUTD

(*Typical Application Circuit*, $V_{CC}$ = +2.7V to +3.3V, $R_1 = R_2 = R_3 = 0\Omega$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = 3.3V, CSETL = CSETH = $V_{CC}$, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| OUTD Center Point | | $P_{RFINA} = P_{RFINB}$ | | 1 | | V |
| Small-Signal Envelope Bandwidth | | No external capacitor on pins FV1 and FV2 | | 22 | | MHz |
| Small-Signal Settling Time | | Any 8dB change on the inputs, no external capacitor on FV1 and FV2, settling accuracy is ±0.5dB | | 150 | | ns |
| Large-Signal Settling Time | | Any 30dB change on the inputs, no external capacitor on pins FV1 and FV2, settling accuracy is ±0.5dB | | 300 | | ns |
| Small-Signal Rise and Fall Time | | Any 8dB step, no external capacitor on pins FV1 and FV2 | | 15 | | ns |

## AC ELECTRICAL CHARACTERISTICS—OUTD (continued)

(*Typical Application Circuit*, $V_{CC}$ = +2.7V to +3.3V, $R_1 = R_2 = R_3 = 0\Omega$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = 3.3V, CSETL = CSETH = $V_{CC}$, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Large-Signal Rise and Fall Time | | Any 30dB step, no external capacitor on pins FV1 and FV2 | | | 35 | | ns |
| ±1dB Dynamic Range | | 0.1GHz | $P_{RFINB}$ = -32dBm | | 80 | | dB |
| | | 0.9GHz | $P_{RFINB}$ = -30dBm | | 75 | | |
| | | 1.9GHz | $P_{RFINB}$ = -27dBm | | 60 | | |
| | | 2.17GHz | $P_{RFINB}$ = -25dBm | | 55 | | |
| | | 2.5GHz | $P_{RFINB}$ = -23dBm | | 50 | | |
| Slope | | $f_{RF}$ = 0.1GHz to 2.5GHz (A-B) | | | -25 | | mV/dB |
| OUTD Voltage Deviation | | $P_{RFINA} = P_{RFINB}$ = -30dBm, $T_A$ = -20°C to +85°C | | | ±0.25 | | dB |
| ±1dB Dynamic Range over Temperature Relative to Best-Fit Curve at +25°C | | $P_{RFINA}$ is swept ; $T_A$ = -20°C to +85°C | 0.1GHz, $P_{RFINB}$ = -32dBm | | 80 | | dB |
| | | | 0.9GHz, $P_{RFINB}$ = -30dBm | | 70 | | |
| | | | 1.9GHz, $P_{RFINB}$ = -27dBm | | 55 | | |
| | | | 2.17GHz, $P_{RFINB}$ = -25dBm | | 50 | | |
| | | | 2.5GHz, $P_{RFINB}$ = -23dBm | | 45 | | |
| Gain Measurement Balance | | $P_{RFINB} = P_{RFINB}$ = -50dBm to -5dBm, $f_{RF}$ = 1.9GHz | | | 0.2 | | dB |
| Channel Isolation | | 0.9GHz | | | 90 | | dB |
| | | 1.9GHz | | | 65 | | |
| | | 2.5GHz | | | 55 | | |

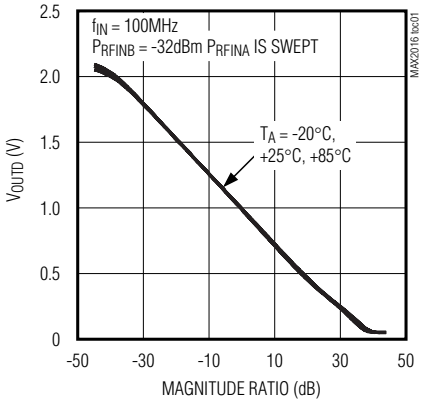
**Note 1:** The MAX2016 is tested at $T_A$ = +25°C and is guaranteed by design for $T_A$ = -40°C to +85°C.
**Note 2:** Typical minimum and maximum range of the detector at the stated frequency.
**Note 3:** Dynamic range refers to the range over which the error remains within the ±3dB range.
**Note 4:** The slope is the variation of the output voltage per change in input power. It is calculated by fitting a root-mean-square straight line to the data indicated by the RF input power range.
**Note 5:** The intercept is an extrapolated value that corresponds to the output power for which the output voltage is zero. It is calculated by fitting a root-mean-square straight line to the data.

# LF-to-2.5GHz Dual Logarithmic Detector/ Controller for Power, Gain, and VSWR Measurements

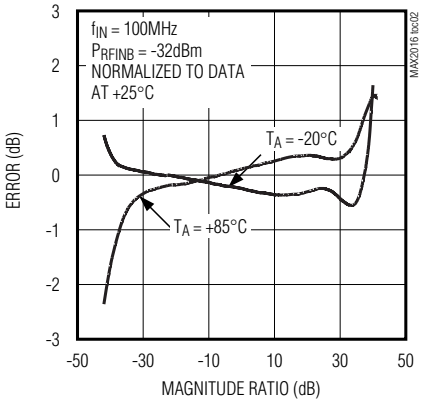
## Typical Operating Characteristics

(MAX2016 EV kit, $V_{CC}$ = 3.3V, $R_1$ = $R_2$ = $R_3$ = 0Ω, CSETL = CSETH = $V_{CC}$, $T_A$ = +25°C, unless otherwise noted.)

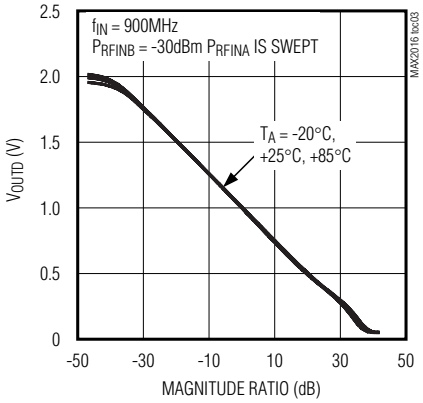
**DIFFERENTIAL OUTPUT VOLTAGE vs. A/B DIFFERENCE**



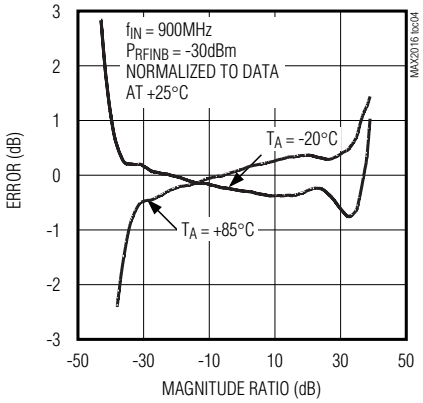

**DIFFERENTIAL OUTPUT-VOLTAGE ERROR vs. A/B DIFFERENCE**



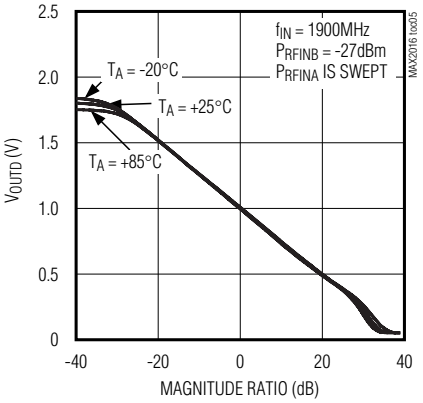

**DIFFERENTIAL OUTPUT VOLTAGE vs. A/B DIFFERENCE**



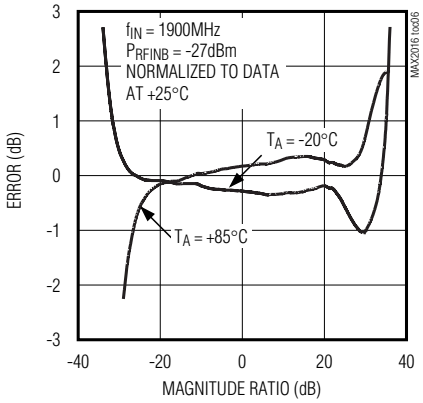

**DIFFERENTIAL OUTPUT-VOLTAGE ERROR vs. A/B DIFFERENCE**




**DIFFERENTIAL OUTPUT VOLTAGE vs. A/B DIFFERENCE**



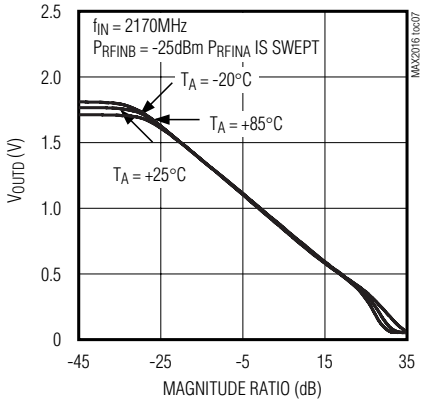

**DIFFERENTIAL OUTPUT-VOLTAGE ERROR vs. A/B DIFFERENCE**



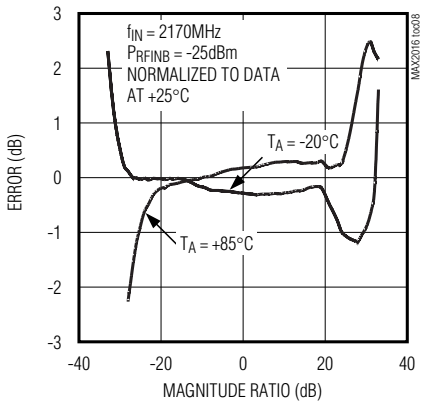
## Typical Operating Characteristics (continued)

(MAX2016 EV kit, $V_{CC}$ = 3.3V, $R_1 = R_2 = R_3 = 0\Omega$, CSETL = CSETH = $V_{CC}$, $T_A$ = +25°C, unless otherwise noted.)

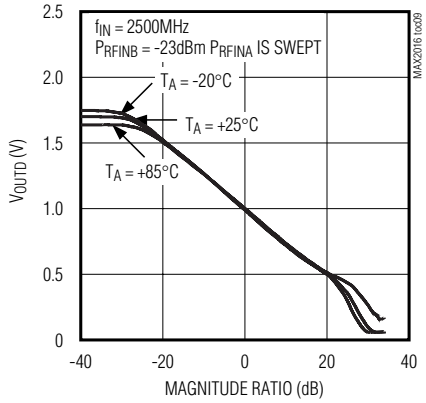
**DIFFERENTIAL OUTPUT VOLTAGE vs. A/B DIFFERENCE**



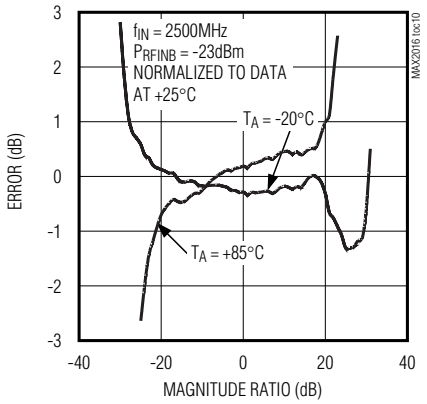

**DIFFERENTIAL OUTPUT-VOLTAGE ERROR vs. A/B DIFFERENCE**



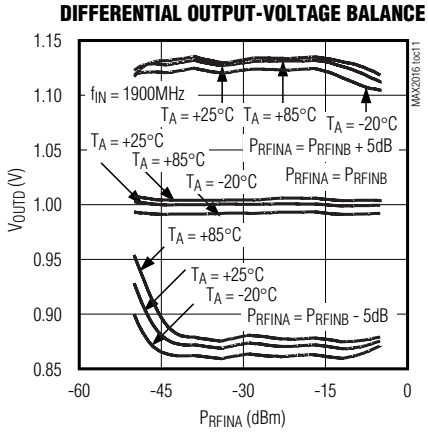

**DIFFERENTIAL OUTPUT VOLTAGE vs. A/B DIFFERENCE**



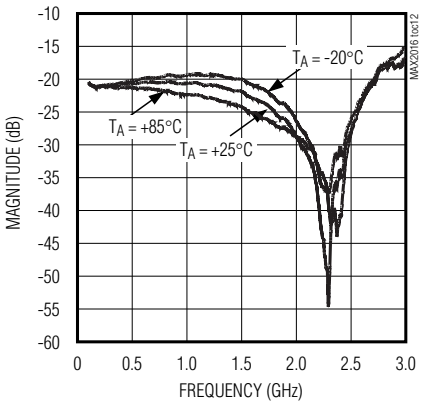

**DIFFERENTIAL OUTPUT-VOLTAGE ERROR vs. A/B DIFFERENCE**




**DIFFERENTIAL OUTPUT-VOLTAGE BALANCE**




**$S_{11}$ MAGNITUDE**

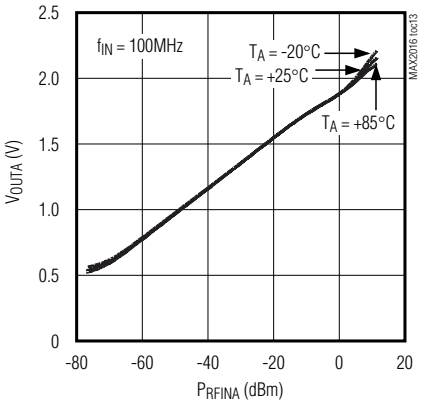


# LF-to-2.5GHz Dual Logarithmic Detector/ Controller for Power, Gain, and VSWR Measurements

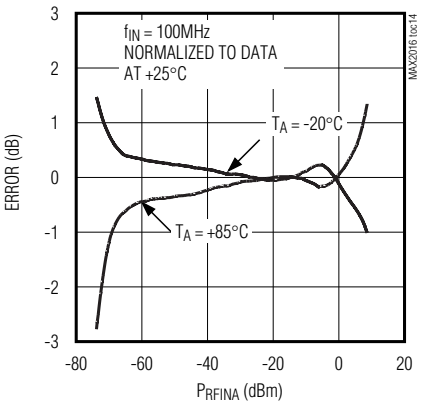
## Typical Operating Characteristics (continued)

(MAX2016 EV kit, $V_{CC}$ = 3.3V, $R_1$ = $R_2$ = $R_3$ = 0Ω, CSETL = CSETH = $V_{CC}$, $T_A$ = +25°C, unless otherwise noted.)

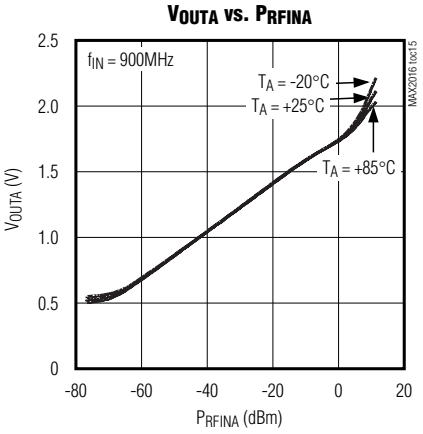
**VOUTA vs. PRFINA**



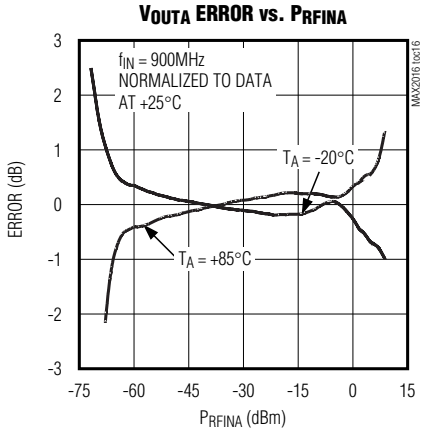

**VOUTA ERROR vs. PRFINA**



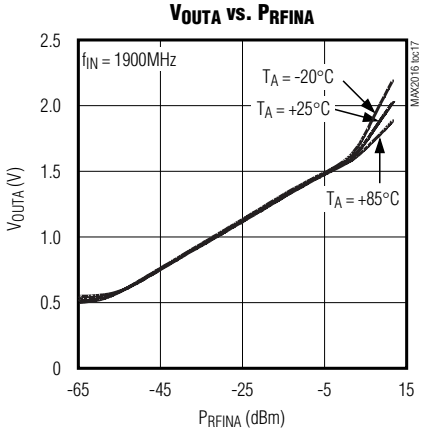

**VOUTA vs. PRFINA**



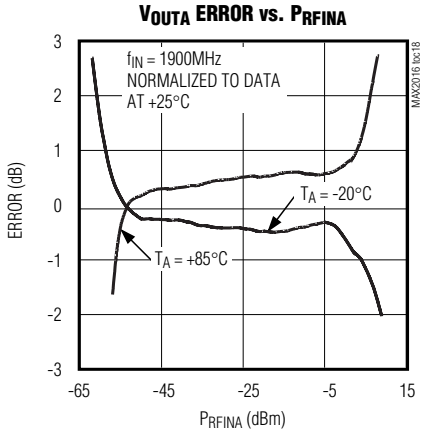

**VOUTA ERROR vs. PRFINA**




**VOUTA vs. PRFINA**



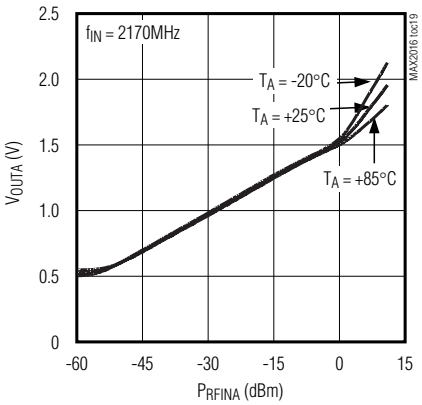

**VOUTA ERROR vs. PRFINA**



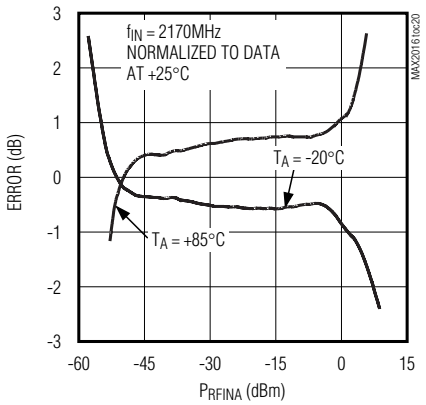
## Typical Operating Characteristics (continued)

(MAX2016 EV kit, $V_{CC}$ = 3.3V, $R_1$ = $R_2$ = $R_3$ = 0Ω, CSETL = CSETH = $V_{CC}$, $T_A$ = +25°C, unless otherwise noted.)

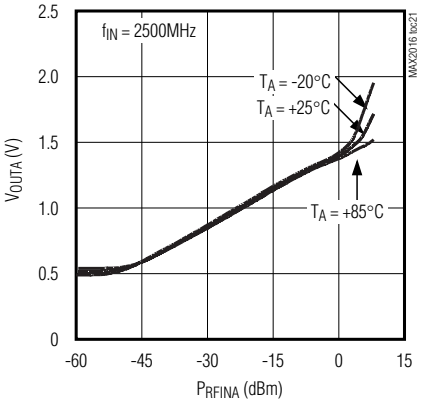
**VOUTA vs. PRFINA**



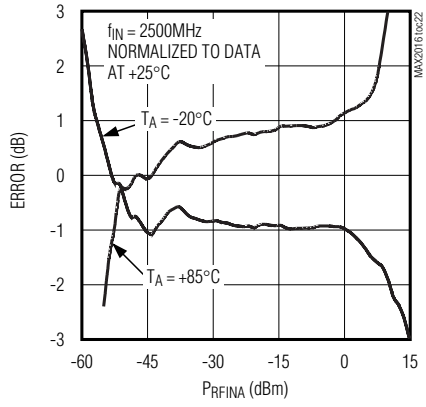

**VOUTA ERROR vs. PRFINA**




**VOUTA vs. PRFINA**




**VOUTA ERROR vs. PRFINA**



# LF-to-2.5GHz Dual Logarithmic Detector/ Controller for Power, Gain, and VSWR Measurements

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 28 | FA1, FA2 | External Capacitor Input. Connecting a capacitor between FA1 and FA2 sets the highpass cutoff frequency corner for detector A (see the *Input Highpass Filter* section). |
| 2, 9, 12, 20 | $V_{CC}$ | Supply Voltage. Bypass with capacitors as specified in the *Typical Application Circuit*. Place capacitors as close to each $V_{CC}$ as possible (see the *Power-Supply Connections* section). |
| 3, 4 | RFINA+, RFINA- | Differential RF Inputs for Detector A. Requires external DC-blocking capacitors. |
| 5, 17 | GND | Ground. Connect to the PCB ground plane. |
| 6 | COUTH | High-Comparator Output |
| 7 | CSETH | Threshold Input on High Comparator |
| 8 | COR | Comparator OR Logic Output. Output of COUTH ORed with COUTL. |
| 10 | SETD | Set-Point Input for Gain Detector |
| 11 | OUTD | DC Output Voltage Representing $P_{RFINA}$ - $P_{RFINB}$. This output provides a DC voltage proportional to the difference of the input RF powers on RFINA and RFINB. |
| 13, 14 | FV2, FV1 | Video-Filter Capacitor Inputs for OUTD |
| 15 | CSETL | Threshold Set Input on Low Comparator |
| 16 | COUTL | Low-Comparator Output |
| 18, 19 | RFINB-, RFINB+ | Differential RF Inputs for Detector B. Requires external DC-blocking capacitors. |
| 21, 22 | FB1, FB2 | External Capacitor Input. Connecting a capacitor between FB1 and FB2 sets the highpass cutoff frequency corner for detector B (see the *Input Highpass Filter* section). |
| 23 | OUTB | Detector B Output. This output provides a voltage proportional to the log of the input power on differential inputs RFINB+ and RFINB- (RFINB). |
| 24 | SETB | Set-Point Input for Detector B |
| 25 | REF | 2V Reference Output |
| 26 | SETA | Set-Point Input for Detector A |
| 27 | OUTA | Detector A Output. This output provides a voltage proportional to the log of the input power on differential inputs RFINA+ and RFINA- (RFINA). |
| EP | GND | Exposed Paddle. EP must connect to the PCB ground plane. |

## Detailed Description

The MAX2016 dual logarithmic amplifier is designed for a multitude of applications including dual-channel RF power measurements, AGC control, gain/loss detection, and VSWR monitoring. This device measures RF signals ranging from low frequency to 2.5GHz, and operates from a single 2.7V to 5.25V (using series resistor, R6) power supply. As with its single-channel counterpart (MAX2015), the MAX2016 provides unparalleled performance with a high 80dB dynamic range at 100MHz and exceptional accuracy over the extended temperature and supply voltage ranges.

The MAX2016 uses a pair of logarithmic amplifiers to detect and compare the power levels of two RF input signals. The device subtracts one power level from the other to provide a DC output voltage that is proportional to the power difference (gain). The MAX2016 can also measure the return loss/VSWR of an RF signal by monitoring the incident and reflected power levels associated with any given load.

A window detector is easily implemented by using the on-chip comparators, OR gate, and 2V reference. This combination of circuitry provides an automatic indication of when the measured gain is outside a programmable range. Alarm monitoring can thus be implemented for detecting high-VSWR states (such as open or shorted loads).

### RF Inputs (RFINA and RFINB)

The MAX2016 has two differential RF inputs. The input to detector A (RFINA) uses the two input ports RFINA+ and RFINA-, and the input to detector B (RFINB) uses the two input ports RFINB+ and RFINB-.

The differential RF inputs allow for the measurement of broadband signals ranging from low frequency to 2.5GHz. For single-ended signals, RFINA- and RFINB- are AC-coupled to ground. The RF inputs are internally biased and need to be AC-coupled. Using 680pF capacitors, as shown in the *Typical Application Circuit*, results in a 10MHz highpass corner frequency. An internal 50Ω resistor between RFINA+ and RFINA- (as well as RFINB+ and RFINB-) produces a good low-frequency to 3.0GHz match.

### SETA, SETB, and SETD Inputs

The SET_ inputs are used for loop control when the device is in controller mode. Likewise, these same SET_ inputs are used to set the slope of the output signal (mV/dB) when the MAX2016 is in detector mode. The center node of the internal resistor-divider is fed to the negative input of the power detector's internal output op amp.

### Reference

The MAX2016 has an on-chip 2V voltage reference. The internal reference output is connected to REF. The output can be used as a reference voltage source for the comparators or other components and can source up to 2mA.

### OUTA and OUTB

Each OUT_ is a DC voltage proportional to the RF input power level. The change of OUT_ with respect to the power input is approximately 18mV/dB ($R_1$ = $R_2$ = 0Ω).

The input power level can be determined by the following equation:

$$P_{RFIN\_} = \frac{V_{OUT\_}}{SLOPE} + P_{INT}$$

where $P_{INT}$ is the extrapolated intercept point of where the output voltage intersects the horizontal axis.

### OUTD

OUTD is a DC voltage proportional to the difference of the input RF power levels. The change of the OUTD with respect to the power difference is -25mV/dB (R3 = 0Ω). The difference of the input power levels (gain) can be determined by the following equation:

$$P_{RFINA} - P_{RFINB} = \frac{(V_{OUTD} - V_{CENTER})}{SLOPE}$$

where $V_{CENTER}$ is the output voltage, typically 1V, when $P_{RFINA}$ = $P_{RFINB}$.

## Applications Information

### Monitoring VSWR and Return Loss

The MAX2016 can be used to measure the VSWR of an RF signal, which is useful for detecting the presence or absence of a properly loaded termination, such as an antenna (see Figure 1). The transmitted wave from the power amplifier is coupled to RFINA and to the antenna. The reflected wave from the antenna is connected to RFINB through a circulator. When the antenna is missing or damaged, a mismatch in the nominal load

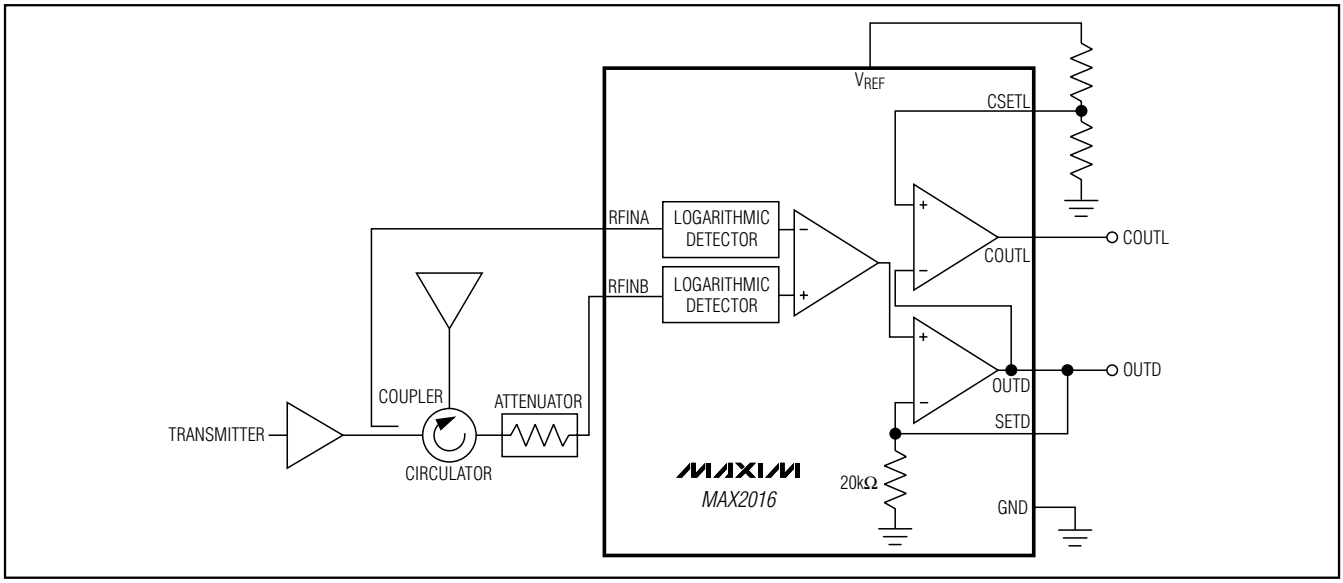



*Figure 1. VSWR Monitoring Configuation*

# LF-to-2.5GHz Dual Logarithmic Detector/ Controller for Power, Gain, and VSWR Measurements

impedance results, leading to an increase in reflected power and subsequent change in the transmission line's VSWR. This increase in reflected power is manifested by an increase in the voltage at OUTD. An alarm condition can be set by using the low comparator output (COUTL) as shown in Figure 1. The comparator automatically senses the change in VSWR, yielding a logic 0 as it compares OUTD to a low DC voltage at CSETL. CSETL, in turn, is set by using the internal reference voltage and an external resistor-divider network.

For accurate measurement of signals carrying significant amplitude modulation, limit the bandwidth of the difference amplifier to be less than the lowest modulation frequency. This will minimize the ripple in the OUTD waveform. This is particularly appropriate if the system-level time delay between the two sense points is significant with respect to the period of modulation.

Figure 1 illustrates a simple level detector. For window-detector implementation, see the *Comparator/Window Detector* section.

### Measuring VSWR and Return Loss

In Figure 2, the two logarithmic amplifiers measure the incident and the reflected power levels to produce two proportional output voltages at OUTA and OUTB. Since OUTD is a DC voltage proportional to the difference of OUTA and OUTB, return loss (RL) and VSWR can be easily calculated within a microprocessor using the following relationships:

$$RL = P_{RFINA} - P_{RFINB} = \frac{(V_{OUTD} - V_{CENTER})}{SLOPE}$$

where return loss (RL) is expressed in decibels, $V_{CENTER}$ is the output voltage (typically 1V) when $P_{RFINA} = P_{RFINB}$, and SLOPE is typically equal to -25mV/dB (for R3 = 0Ω).

VSWR can similarly be calculated through the following relationship:

$$VSWR = \frac{1+10^{-\left(\frac{RL}{20}\right)}}{1-10^{-\left(\frac{RL}{20}\right)}}$$

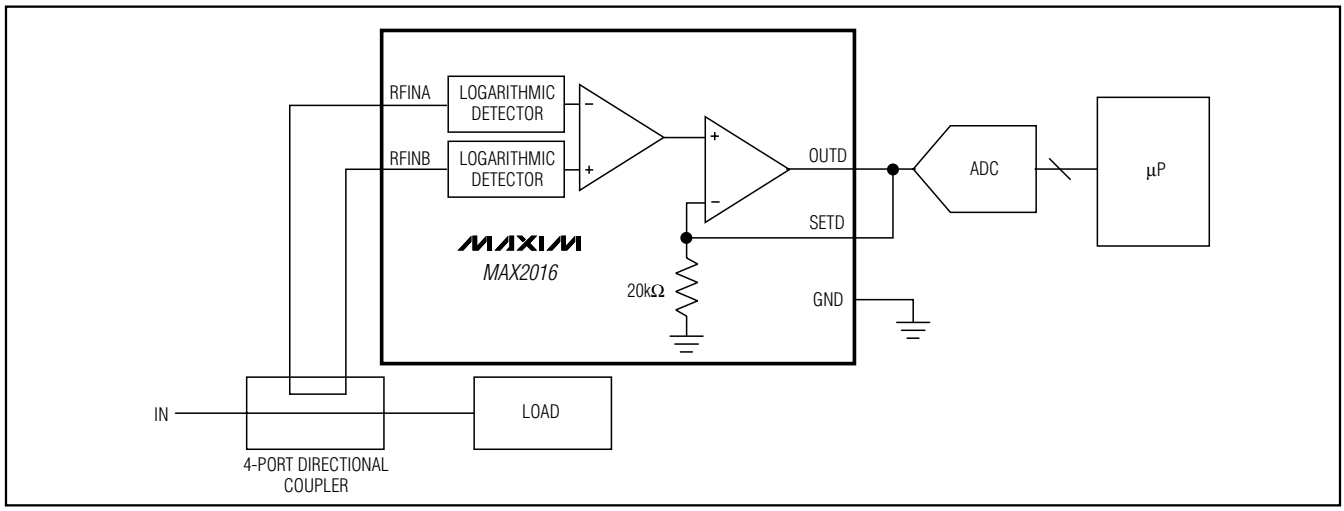



*Figure 2. Measuring Return Loss and VSWR of a Given Load*

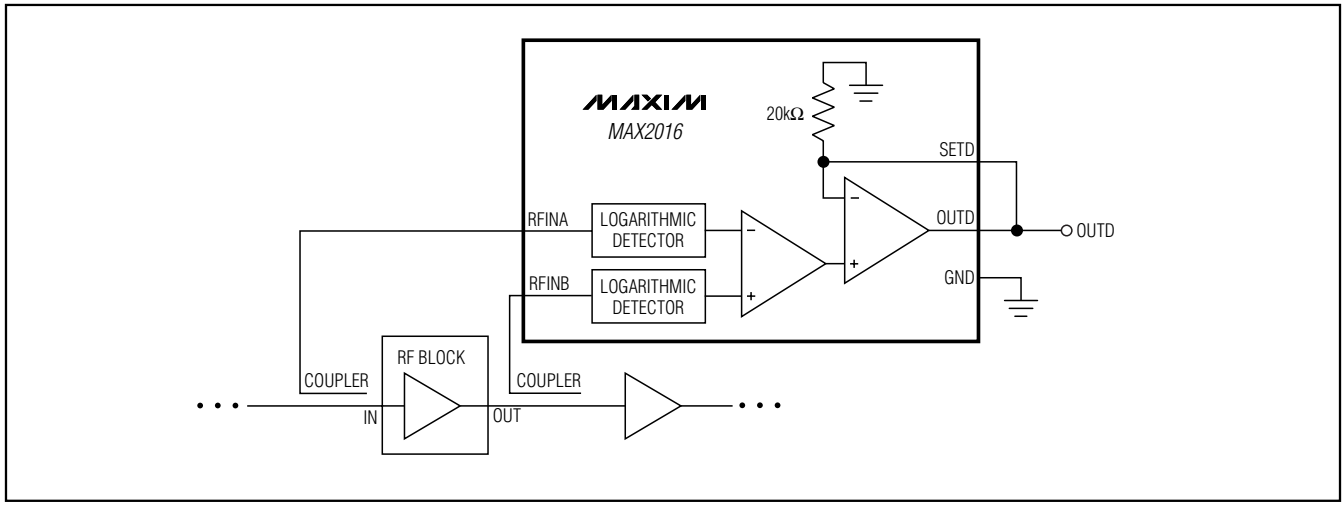



*Figure 3. Gain Measurement Configuration*

### Measuring Gain

The MAX2016 can be used to measure the gain of an RF block (or combination of blocks) through the implementation outlined in Figure 3. As shown, a coupled signal from the input of the block is fed into RFINA, while the coupled output is connected to RFINB. The DC output voltage at OUTD is proportional to the power difference (i.e., gain).

The gain of a complete receiver or transmitter lineup can likewise be measured since the MAX2016 accepts RF signals that range from low frequency to 2.5GHz; see Figure 4. The MAX2016 accurately measures the gain, regardless of the different frequencies present within superheterodyne architectures.

For accurate measurement of signals carrying significant amplitude modulation, limit the bandwidth of the difference amplifier to be less than the lowest modulation frequency. This will minimize the ripple in the OUTD waveform. This is particularly appropriate if the system-level time delay between the two sense points is significant with respect to the period of modulation.

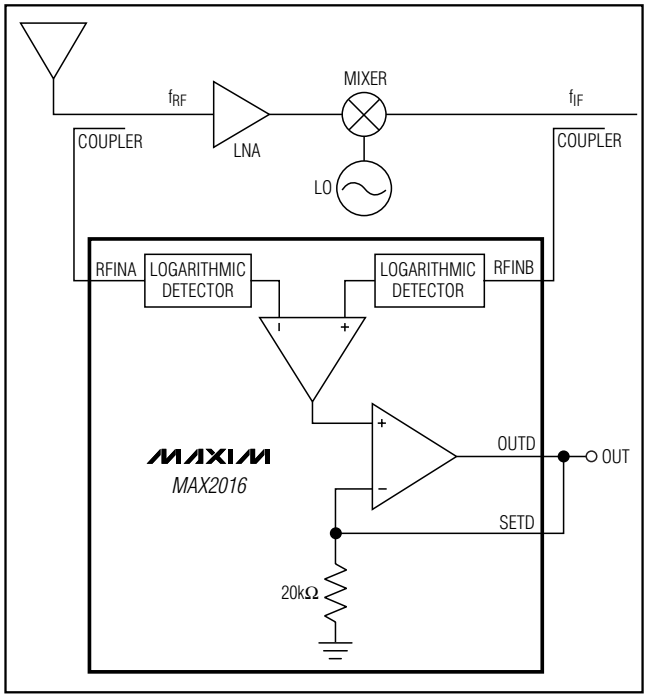



*Figure 4. Conversion Gain Measurement Configuration*

# LF-to-2.5GHz Dual Logarithmic Detector/ Controller for Power, Gain, and VSWR Measurements

### Measuring Power (RSSI Detector Mode)

In detector mode, the MAX2016 acts like a receive-signal-strength indicator (RSSI), which provides an output voltage proportional to the input power. This is accomplished by providing a feedback path from OUTA (OUTB) to SETA (SETB) (R1/R2 = 0Ω; see Figure 5).

By connecting SET_ directly to OUT_, the op-amp gain is set to 2V/V due to two internal 20kΩ feedback resistors. This provides a detector slope of approximately 18mV/dB with a 0.5V to 1.8V output range.

### Gain-Controller Mode

The MAX2016 can be used as a gain controller within an automatic gain-control (AGC) loop. As shown in Figure 6, RFINA and RFINB monitor the VGA's input and output power levels, respectively. The MAX2016 produces a DC voltage at OUTD that is proportional to the difference in these two RF input power levels. An internal op amp compares the DC voltage with a reference voltage at SETD. The op amp increases or decreases the voltage at OUTD until OUTD equals SETD. Thus, the MAX2016 adjusts the gain of the VGA to a level determined by the voltage applied to SETD.

Place the nominal signal levels of RFINA and RFINB near the middle of their respective dynamic ranges to accommodate the largest range of gain compensation. This is nominally -25dBm to -30dBm. If so selected, the nominal voltage applied to SETD will be approximately 1.0V. Operate the SETD voltage within the range of 0.5V to 1.5V for the greatest accuracy of gain control.

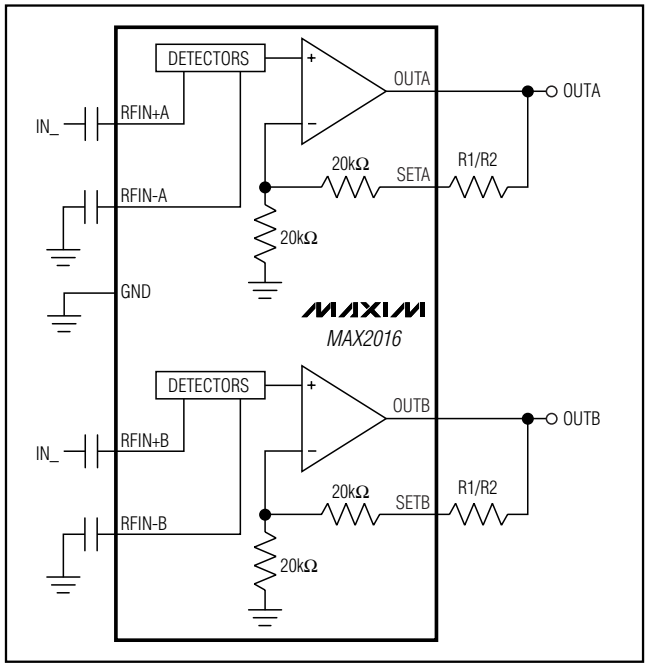



*Figure 5. In Detector Mode (RSSI), OUTA/OUTB is a DC Voltage Proportional to the Input Power*

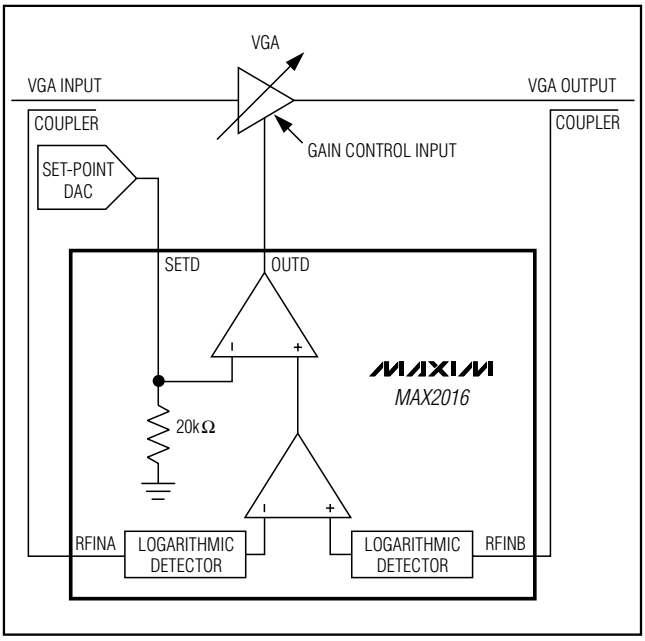



*Figure 6. In Gain-Controller Mode, the OUTD Maintains the Gain of the VGA*

# LF-to-2.5GHz Dual Logarithmic Detector/ Controller for Power, Gain, and VSWR Measurements

### Power-Controller Mode

The MAX2016 can also be used as a power detector/controller within an AGC loop. Figure 7 depicts a scenario where the MAX2016 is employed as the AGC circuit. As shown in the figure, the MAX2016 monitors the output of the PA through a directional coupler. An internal differencing amplifier (Figure 5) compares the detected signal with a reference voltage determined by $V_{SET\_}$. The differencing amplifier increases or decreases the voltage at OUT_, according to how closely the detected signal level matches the $V_{SET\_}$ reference. The MAX2016 maintains the power of the PA to a level determined by the voltage applied to SET_.

Since the logarithmic detector responds to any amplitude modulation being carried by the carrier signal, it may be necessary to insert an external lowpass filter between the differencing amplifier output (OUTA/OUTB) and the gain-control element to remove this modulation signal.

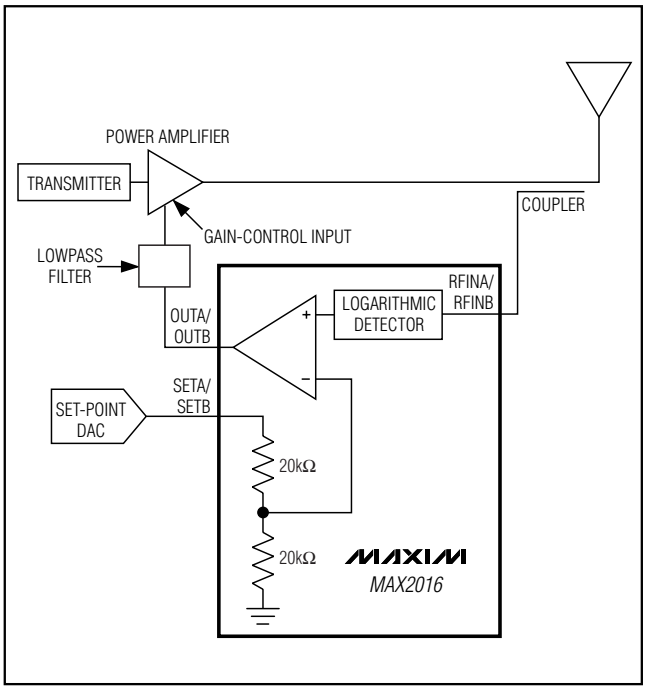



*Figure 7. In Power-Controller Mode, the DC Voltage at OUTA or OUTB Controls the Gain of the PA, Leading to a Constant Output Power Level (**Note:** Only one controller channel is shown within the figure. Since the MAX2016 is a dual controller/detector, the second channel can be easily implemented by using the adjacent set of input and output connections.)*

### OUTA and OUTB Slope Adjustment

The transfer slope function of OUTA and OUTB can be increased from its nominal value by varying resistors R1 and R2 (see the *Typical Application Circuit*). The equation controlling the slope is:

$$\text{SLOPE OUTA OR OUTB} = \left(9\frac{\text{mV}}{\text{dB}}\right)\left[\frac{(\text{R1 or R2})+40\text{k}}{20\text{k}}\right]$$

### OUTD Slope Adjustment

The transfer slope function of OUTD can be increased from its nominal value by varying resistor R3 (see the *Typical Application Circuit*). The equation controlling the slope is:

$$\text{SLOPE OUTD} = \left(-25\frac{\text{mV}}{\text{dB}}\right)\left(\frac{\text{R3}+20\text{k}}{20\text{k}}\right)$$

### Input Highpass Filters

The MAX2016 integrates a programmable highpass filter on each RF input. The lower cutoff frequency of the MAX2016 can be decreased by increasing the external capacitor value between FA1 and FA2 or FB1 and FB2. By default, with no capacitor connecting FA1 and FA2 or FB1 and FB2, the lower cutoff frequency is 20MHz. Using the following equation determines the lowest operating frequency:

$$\text{frequency} = \frac{1}{2\pi RC}$$

where R = 2Ω.

### Differential Output Video Filter

The bandwidth and response time difference of the output amplifier can be controlled with the external capacitor, $C_{15}$, connected between FV1 and FV2. With no external capacitor, the bandwidth is greater than 20MHz. The following equation determines the bandwidth of the amplifier difference:

$$\text{frequency} = \frac{1}{2\pi RC}$$

where R = 1.8kΩ.

Use a video bandwidth lower than the anticipated lowest amplitude-modulation frequency range to yield the greatest accuracy in tracking the average carrier power for high peak-to-average ratio waveforms.

# LF-to-2.5GHz Dual Logarithmic Detector/ Controller for Power, Gain, and VSWR Measurements

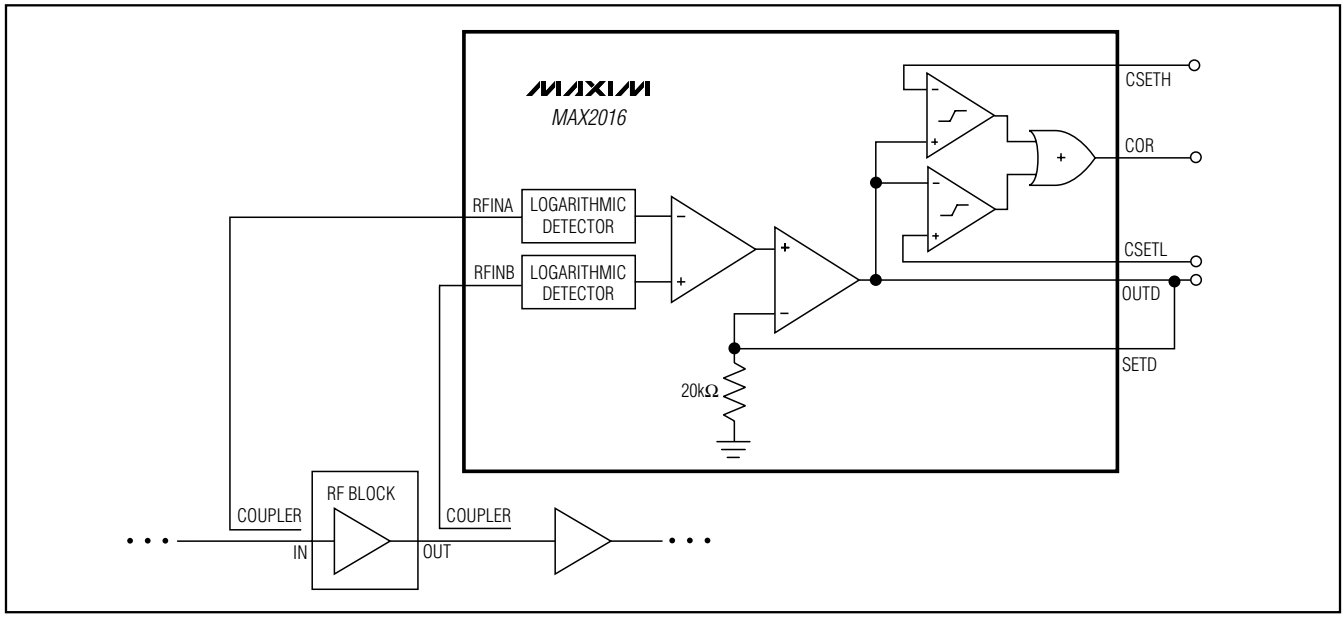



*Figure 8. Window Comparators Monitoring Mode. COR goes high if OUTD drops below CSETL or rises above CSETH.*

### Comparators/Window Detectors

The MAX2016 integrates two comparators for use in monitoring the difference in power levels (gain) of RFINA and RFINB. The thresholds of the two comparators are set to the voltage applied to the CSETL and CSETH pins. The output of each comparator can be monitored independently or from the COR output that ORs the outputs of the individual comparators. This can be used for a window-detector function.

These comparators can be used to trigger hardware interrupts, allowing rapid detection of over-range conditions. These comparators are high-speed devices. Connect high-value bypass capacitors (0.1µF) between each comparator threshold input (CSETL and CSETH) to ground to provide a solid threshold voltage at high switching speeds.

Some applications may benefit from the use of hysteresis in the comparator response. This can be useful for prevention of false triggering in the presence of small noise perturbations in the signal levels, or with signals with large amplitude modulation. To introduce hysteresis into the comparator output, connect a feedback resistor from COUTL to CSTEL. Select the value of this resistor, in combination with the resistive-divider values used to set threshold-level CSETL, to set the amount of hysteresis. Set the parallel combination of resistors connected to CSETL to be less than 10kΩ for best performance.

Figure 8 illustrates the use of these comparators in a gain-monitoring application. The low comparator has its threshold (CSETL) set at a low-gain trip point. If the gain drops below this trip point, the COUTL output goes from a logic 0 to a logic 1. The high comparator has its threshold (CSETH) set at a high trip point. If the gain exceeds this trip point, the COUTH output goes from logic 0 to logic 1. The window comparator output (COR) rests a logic 0 if the gain is in the acceptable range, between CSETL and CSETH. It goes to a logic 1 if the gain is either above or below these limits.

### Power-Supply Connection

The MAX2016 is designed to operate from a single +2.7V to +3.6V supply. To operate under a higher supply voltage range, a resistor must be connected in series with the power supply and $V_{CC}$ to reduce the voltage delivered to the chip. For a +4.75V to +5.25V supply, use a 37.4Ω (±1%) resistor in series with the supply.

### Layout Considerations

A properly designed PCB is an essential part of any RF/microwave circuit. Keep RF signal lines as short as possible to reduce losses, radiation, and inductance. For the best performance, route the ground pin traces directly to the exposed pad under the package. The PCB exposed pad **MUST** be connected to the ground plane of the PCB. It is suggested that multiple vias be used to connect this pad to the lower level ground

planes. This method provides a good RF/thermal conduction path for the device. Solder the exposed pad on the bottom of the device package to the PCB. The MAX2016 Evaluation Kit can be used as a reference for board layout. Gerber files are available upon request at www.maxim-ic.com.

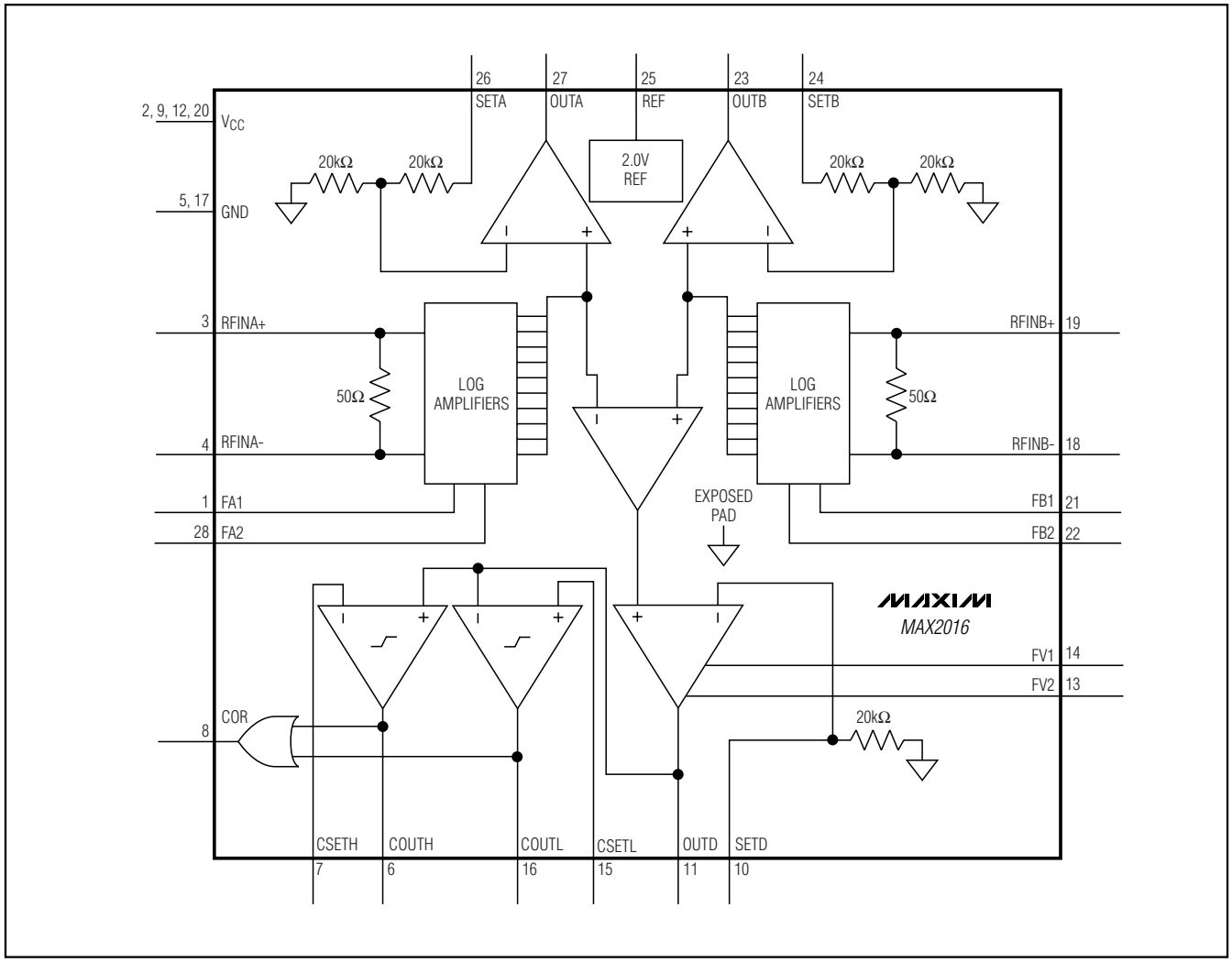
### Power-Supply Bypassing

Proper voltage-supply bypassing is essential for high-frequency circuit stability. Bypass each $V_{CC}$ pin with a capacitor as close to the pin as possible (*Typical Application Circuit*).

### Exposed Pad RF/Thermal Considerations

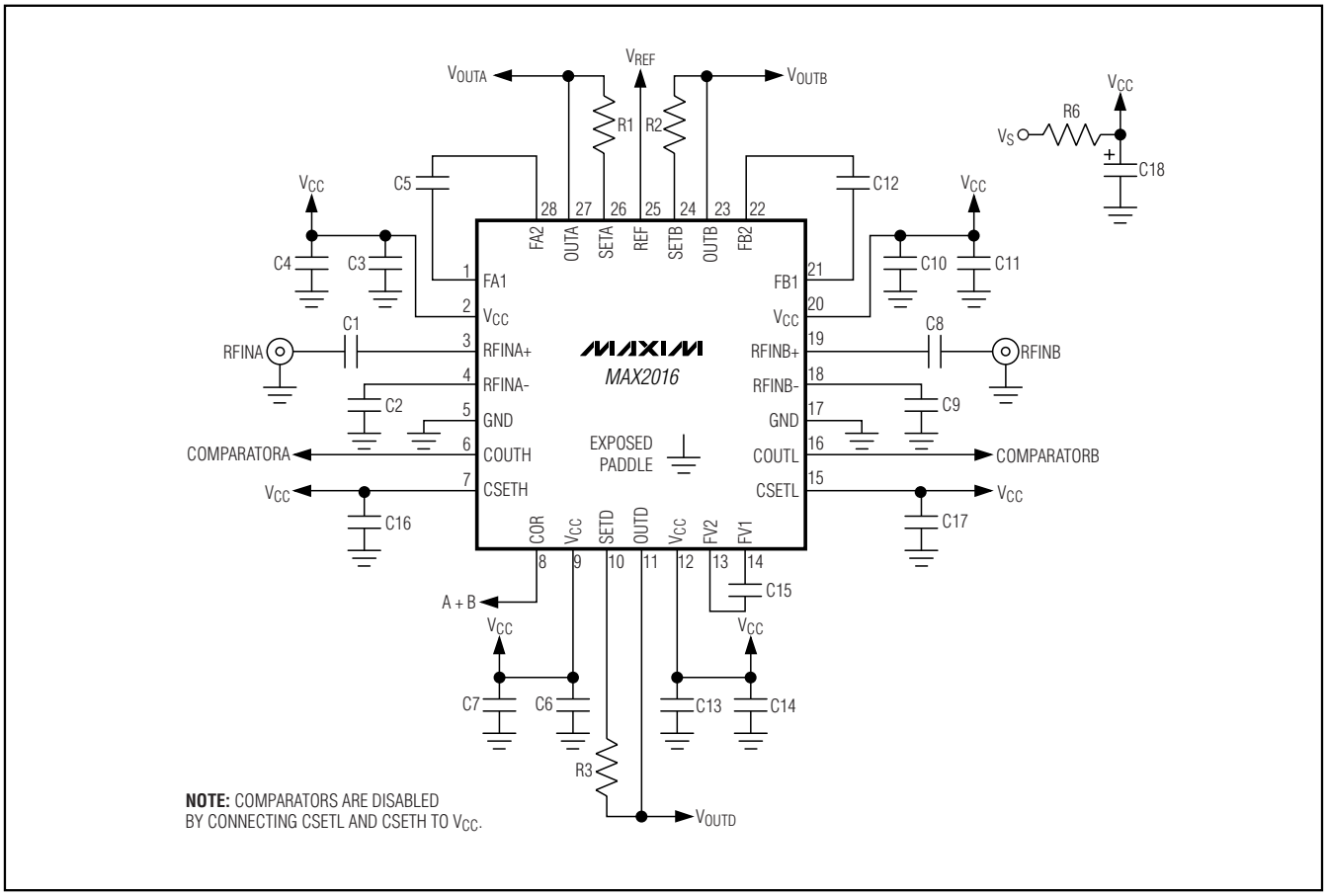
The exposed paddle (EP) of the MAX2016's 28-pin thin QFN-EP package provides two functions. One is a low thermal-resistance path to the die; the second is a low-RF impedance ground connection. The EP **MUST** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes (minimum of four holes to provide ground integrity).

## Functional Diagram



# LF-to-2.5GHz Dual Logarithmic Detector/ Controller for Power, Gain, and VSWR Measurements

## Typical Application Circuit




## Table 1. Component Values Used in the Typical Application Circuit

| DESIGNATION | VALUE | DESCRIPTION |
|---|---|---|
| C1, C2, C8, C9 | 680pF | Microwave capacitors (0402) |
| C3, C6, C10, C13 | 33pF | Microwave capacitors (0402) |
| C4, C7, C11, C14 | 0.1µF | Microwave capacitors (0603) |
| C5, C12, C15, C16, C17 | Not used | Capacitors are optional for frequency compensation, bypass |
| C18 | 10µF | Tantalum capacitor (C case) |
| R1, R2, R3 | 0Ω | Resistors (0402) |
| R6 | 0Ω | Resistor (1206) for $V_S$ = 2.7V to 3.6V |
| | 37.4Ω | ±1% resistor (1206) for $V_S$ = 4.75V to 5.25V |

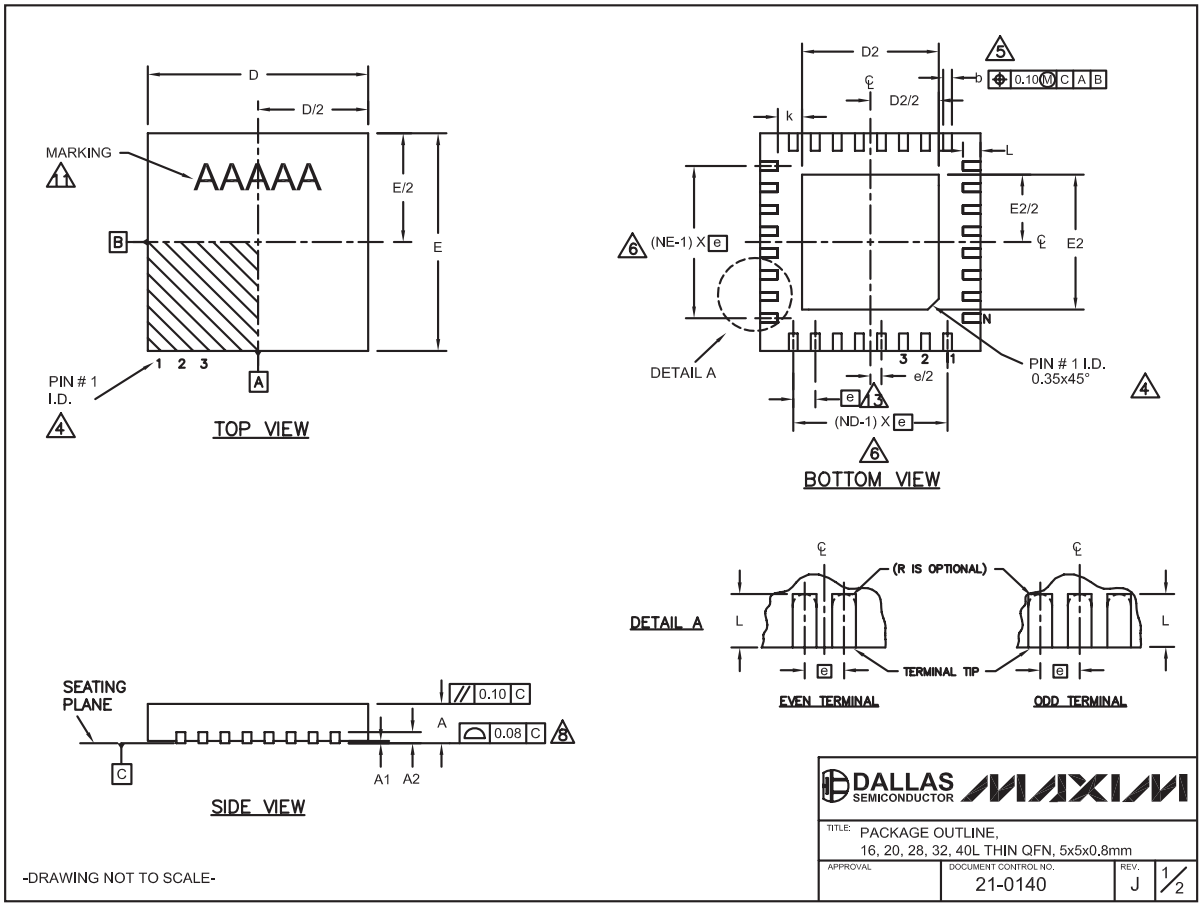
## Chip Information

PROCESS: BiCMOS

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



# LF-to-2.5GHz Dual Logarithmic Detector/ Controller for Power, Gain, and VSWR Measurements

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

| COMMON DIMENSIONS | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PKG. | 16L 5x5 | | | 20L 5x5 | | | 28L 5x5 | | | 32L 5x5 | | | 40L 5x5 | | | |
| SYMBOL | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | |
| A2 | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 | 0.15 | 0.20 | 0.25 | |
| D | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | |
| E | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | | 0.40 BSC. | | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | |
| L | 0.30 | 0.40 | 0.50 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.30 | 0.40 | 0.50 | |
| N | 16 | | | 20 | | | 28 | | | 32 | | | 40 | | | |
| ND | 4 | | | 5 | | | 7 | | | 8 | | | 10 | | | |
| NE | 4 | | | 5 | | | 7 | | | 8 | | | 10 | | | |
| JEDEC | WHHB | | | WHHC | | | WHHD-1 | | | WHHD-2 | | | ----- | | | |

| EXPOSED PAD VARIATIONS | | | | | | |
|---|---|---|---|---|---|---|
| PKG. CODES | D2 | | | E2 | | |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T1655-2 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-5 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-3 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-4 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-5 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-6 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-7 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-8 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855N-1 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T3255-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-5 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T4055-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055-2 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0140 | J | 2/2 |

## Revision History

Pages changed at Rev 1: 1, 5, 10–20