INCH-POUND

MIL-M-38510/2G 8 February 2005 SUPERSEDING MIL-M-38510/2E 24 December 1974 MIL-M-0038510/2F (USAF) 24 OCTOBER 1975

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, TTL, FLIP-FLOPS, MONOLITHIC SILICON

Inactive for new design after 7 September 1995

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535

- 1. SCOPE
- 1.1 <u>Scope.</u> This specification covers the detail requirements for monolithic silicon, TTL, bistable logic microcircuits. Three product assurance classes and a choice of case outlines/lead finish are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).
 - 1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.
 - 1.2.1 <u>Device types.</u> The device types are as follows:

Device type	<u>Circuit</u>
01	Single J-K master-slave flip-flop
02	Dual J-K master-slave flip-flop, no preset
03	Dual J-K master-slave flip-flop, no preset
04	Dual J-K master-slave flip-flop
05	Dual D-type edge-triggered flip-flop
06	Single edge-triggered J-K flip-flop
07	Dual D-type edge-triggered flip-flop, buffered output

1.2.2 <u>Device class</u>. The device class is the product assurance level as defined in MIL-PRF-38535.

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to bipolar@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil

AMSC N/A FSC 5962

1.2.3 <u>Case outlines</u>. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	<u>Terminals</u>	Package style
Α	GDFP5-F14 or CDFP6-F14	14	Flat pack
В	GDFP4-F14	14	Flat pack
С	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
Е	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack

1.3 Absolute maximum ratings.

Supply voltage rangeInput voltage range	
Storage temperature range	
Maximum power dissipation, (P _D)	
flip-flop, <u>1</u> /	. 110 mW <u>1</u> /
Lead temperature (soldering, 10 seconds)	. 300°C
Thermal resistance, junction to case (θ _{JC}):	. 0.09°C/mW for flat packs
	0.08°C/mW for dual-in-line pack
Junction temperature (T _J)	. 175°C

1.4 Recommended operating conditions.

Supply voltage (V _{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V _{IH})	2.0 V dc
Maximum low-level input voltage (V _{IL})	0.8 V dc
Normalized fanout (each output) 2/	10 maximum
Case operating temperature range (T _C)	-55 °C to +125 °C
Input set up time:	
Device type 01, 02, 03 and 04,	≥ clock pulse width
Device type 05, 06, and 07	20 ns
Input hold time	
Device types 01, 02, 03 and 04	0 ns
Device type 05, 06 and 07	5 ns

2. APPLICABLE DOCUMENTS

2.1 <u>General</u>. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

Must withstand the added P_D due to short circuit condition (e.g. I_{OS}) at one output for 5 seconds duration

^{2/} Device will fanout in both high and low levels to the specified number of I_{IL1}/I_{IH1} inputs of the same device type as that being tested.

2.2 Government documents.

2.2.1 <u>Specifications and Standards</u>. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 <u>Order of precedence.</u> In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

- 3.1 <u>Qualification</u>. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).
- 3.2 <u>Item requirements</u>. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.
- 3.3 <u>Design, construction, and physical dimensions.</u> The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.
- 3.3.1 <u>Terminal connections and logic diagrams</u>. The terminal connections and logic diagrams shall be as specified on figures 1.
 - 3.3.2 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 2.
- 3.3.3 <u>Schematic circuits.</u> The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity (DSCC-VAS) upon request.
 - 3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.
- 3.4 <u>Lead material and finish.</u> The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).
- 3.5 <u>Electrical performance characteristics</u>. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.
- 3.6 <u>Electrical test requirements</u>. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III. Subgroups 7 and 8 testing requires only a summary of attributes data.
 - 3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 9/	Device	Lim	nits	Units
		_	Type	Min	Max	
High-level output voltage	V _{OH}	V _{CC} =4.5 V	All	2.4		Volts
Low lovel output valtage	V	$I_{OH} = -400 \mu A$	All		0.4	Volts
Low-level output voltage Input clamp voltage	V _{OL} V _{IC}	$V_{CC} = 4.5 \text{ V}, I_{OL} = 16 \text{ mA}$ $V_{CC} = 4.5 \text{ V}, I_{IC} = -12 \text{ mA}$	All		0.4 -1.5	Volts
Input clamp voltage	V IC	$V_{CC} = 4.5 \text{ V}, I_{IC} = -12 \text{ IIIA}$ $T_{C} = 25^{\circ}\text{C}$	All		-1.5	VOILS
Low-level input current	I _{IL1}	$V_{CC} = 5.5 \text{ V}$	01, 02, 03, 04,	-0.7	-1.6	mA
		V _{IN} = 0.4 V <u>1</u> /	05, 06			
			07	-0.5	-1.6	mA
Low-level input current	I _{IL2}	V _{CC} = 5.5 V	01, 02, 03, 04,	-1.4	-3.2	mA
		$V_{IN} = 0.4 \text{ V } \underline{2}/$	05	4.0	0.0	
			07	-1.0	-3.2	mA
Low-level input current	I _{IL3}	$V_{CC} = 5.5 \text{ V}$	01, 02, 03, 04	-0.7	-3.2	mA
High-level input current	-	$V_{IN} = 0.4 \text{ V} \underline{6}/$ $V_{CC} = 5.5 \text{ V}$	All		40	^
High-level input current	I _{IH1}	$V_{CC} = 5.5 \text{ V}$ $V_{CC} = 2.4 \text{ V} / 5 / 5$	All		40	μΑ
High-level input current	I _{IH2}	$V_{IN} = 2.4 \text{ V} \underline{5}/$ $V_{CC} = 5.5 \text{ V}$	All		100	μА
riigir level iliput current	IH2	$V_{IN} = 5.5 \text{ V} \frac{5}{4}$	All		100	μΑ
High-level input current	I _{IH3}	V _{CC} = 5.5 V	All <u>11</u> /		80	μА
,		$V_{IN} = 2.4 \text{ V } 3/$	_			'
High-level input current	I _{IH4}	$V_{CC} = 5.5 \text{ V}$	All		200	μА
		$V_{IN} = 5.5 \text{ V} \ \underline{3} / \ \underline{7} /$,
High-level input current	I _{IH5}	$V_{CC} = 5.5 \text{ V}$	01, 02, 03, 04,	-50	-850	μΑ
		$V_{IN} = 2.4 \ V \ 7/8/$	05, 07		120	μΑ
High-level input current	I _{IH6}	$V_{CC} = 5.5 \text{ V}$	05, 07		300	μΑ
		$V_{IN} = 5.5 \text{ V} \underline{8}/$ $V_{CC} = 5.5 \text{ V}$				
Short-circuit output current	los	$V_{CC} = 5.5 \text{ V}$	All	-20	-57	mA
		$V_{IN} = 0$ <u>4/</u> $V_{CC} = 5.5$ V				
Supply current per device	I _{CC}	$V_{CC} = 5.5 \text{ V}$	01		20	mA
		$V_{IN} = 5 V$	02, 03, 04		40	
10/			05, 06, 07	40	30	
Maximum clock frequency 10/	f _{MAX}		01, 02, 03	10		MHz
			04, 05, 07	15		
Propagation delay to high logic level	4	-	06 01, 02, 03, 04,	15 5	39	no
(clear or preset to output)	t _{PLH}		01, 02, 03, 04,	3	39	ns
(cical of preset to output)			06	5	62	
			07	5	31	
Propagation delay to low logic level	t _{PHL}	$V_{CC} = 5 V$	01, 02, 03, 04,	5	50	ns
(clear or preset to output)	YPHL	CL = 50 pF minimum	05		00	110
($RL = 390\Omega \pm 5\%$	06	5	62	
			07	5	39	
Propagation delay to high logic level	t _{PLH}	1	06	5	62	ns
(clock to output)			01, 02, 03, 04,	5	39	
			05			
]	07	5	31	
Propagation delay to low logic level	t _{PHL}		06	5	62	ns
(clock to output)			01, 02, 03, 04,	5	50	
			05		<u> </u>	
			07	5	39	

^{1/} Input condition – J or K for device types 01, 02, 03, 04, 06, and preset or D for device types 05 and 07, and clock, clear or preset for device type 06.

^{2/} Input condition – Clock for device types 01, 02, 03 and 04, and clear or clock for device types 05 and 07.

^{3/} Input condition – Clear or preset for device types 01, 02, 03, 04, 05, 06 and 07 and clock for device types 05 and 07.

^{4/} No more than one output should be shorted at a time.

^{5/} Input condition – J or K for device types 01, 02, 03, 04, 06, and D for device types 05 and 07, and clock for device type 06.

^{6/} Input condition – Clear or preset for device types 01, 02, 03 and 04.

^{7/} Input condition – Clock for device types 01, 02, 03 and 04.

- 8/ Input condition Clear for device types 05 and 07.
- 9/ See table III for complete terminal conditions.
- <u>10/</u> Minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
- $\underline{11}$ / For device types 02 and 03, limits are 0 to 120 μ A.

TABLE II. Electrical test requirements.

	Subgroups	(see table III)
MIL-PRF-38535	Class S	Class B
test requirements	devices	devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 7, 8, 9	1*, 2, 3, 7, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7 9
Group B test when using the method 5005 QCI option	1, 2, 3,	N/A
Group C end-point electrical parameters	1, 2, 3,	1, 2, 3
Additional electrical subgroups for Group C periodic inspections	N/A	10, 11
Group D end-point electrical parameters	1, 2, 3	1, 2, 3

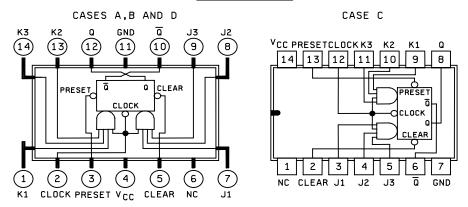
^{*}PDA applies to subgroup 1.

4. VERIFICATION

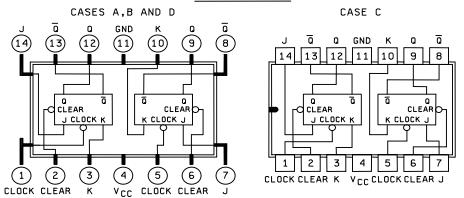
- 4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.
- 4.2 <u>Screening.</u> Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:
 - a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
 - b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
 - c. Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.
 - 4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.
- 4.4 <u>Technology Conformance inspection (TCI)</u>. Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A. B. C. and D inspections (see 4.4.1 through 4.4.4).

- 4.4.1 <u>Group A inspection.</u> Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 4, 5, and 6 shall be omitted.
 - 4.4.2 Group B inspection. Group B inspection shall be in accordance with table II MIL-PRF-38535.
- 4.4.3 <u>Group C inspection.</u> Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burnin test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- 4.4.4 <u>Group D inspection.</u> Group D inspection shall be in accordance with table V of MIL-PRF-38535. Endpoint electrical parameters shall be as specified in table II herein.
 - 4.5 Methods of inspection. Methods of inspection shall be specified and as follows:
- 4.5.1 <u>Voltage and current.</u> All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

DEVICE TYPE 01



DEVICE TYPE 02



DEVICE TYPE 03

CASE C

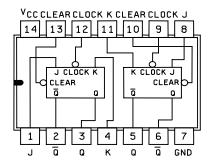
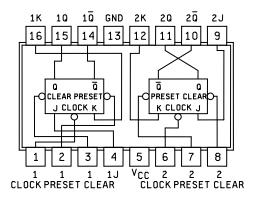
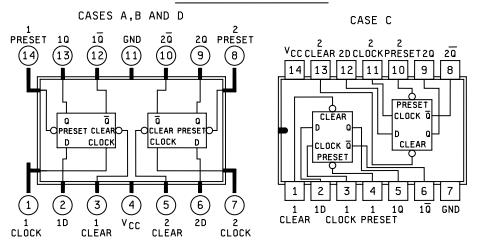


FIGURE 1. Logic diagram and terminal connections.

DEVICE TYPE 04 CASES E AND F



DEVICE TYPES 05 AND 07



DEVICE TYPE 06

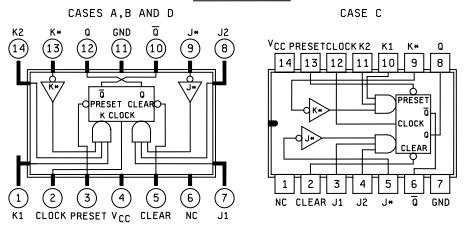


FIGURE 1. Logic diagram and terminal connections – Continued.

Device type 01

Truth table											
t	t _n										
J	K	Q									
L	L	Q_n									
L	Н	L									
Н	L	Н									
Н	Н	\overline{Q}_n									

Positive logic: Low input to preset sets Q to high-level

Low input to clear sets Q to low-level

Preset and clear are independent of clock and dominate regardless of the state of clock or J of K inputs.

NOTES: $1. J = J1 \bullet J2 \bullet J3$

2. K = K1 • K2 • K3

3. t_n = Bit time before clock pulse.

4. $t_n + 1$ = Bit time after clock pulse.

Device type 02 and 03

Truth table each flip-flop											
t	t _n + 1										
J	K	Q									
L	L	Qn									
L	Н	L									
Н	L	Н									
Н	Н	Qn									

Positive logic: Low input to clear sets Q to low-level

Clear is independent of clock and dominate regardless of the state of clock or J or K inputs.

NOTES: 1. t_n = Bit time before clock pulse.

2. $t_n + 1 = Bit time after clock pulse.$

FIGURE 2. Truth tables.

Device type 04

Truth table each flip-flop												
t	t _n											
J	K	Q										
L	L	Qn										
L	Н	L										
Н	L	Н										
Н	Н	$\overline{\overline{Q}}_n$										

Positive logic: Low input to preset sets Q to high-level

Low input to clear sets Q to low-level

Preset and clear are independent of clock and dominate regardless of the state of clock or J of K inputs.

NOTES: 1. t_n = Bit time before clock pulse.

2. $t_n + 1 = Bit time after clock pulse.$

Device type 05 and 07

Truth table each flip-flop											
t _n	t _n -	+ 1									
INPUT D	OUTPUT Q	OUTPUT Q									
L	L	Н									
Н	Н	L									

Positive logic: Low input to preset sets Q to high-level

Low input to clear sets Q to low-level

Preset and clear are independent of clock and dominate

regardless of the state of clock or D input.

NOTES: 1. t_n = Bit time before clock pulse.

2. $t_n + 1 = Bit time after clock pulse.$

FIGURE 2. <u>Truth tables</u> – Continued.

Device type 06

Truth table											
t	t _n										
J	K	Q									
L	L	Qn									
L	Н	L									
Н	L	Н									
Н	Н	Q n									

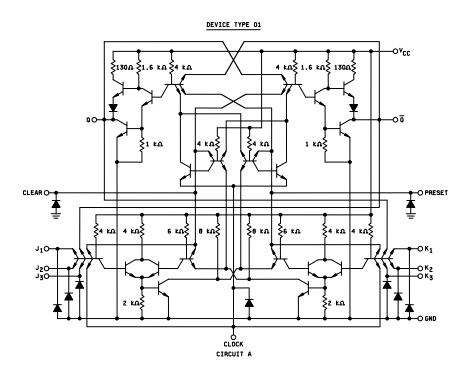
Positive logic: Low input to preset sets Q to high-level

Low input to clear sets Q to low-level Preset or clear function can occur only When clock input is low.

NOTES: 1. J = J1 • J2 • $\overline{J^*}$

- 2. K = K1 K2 \overline{K}^* 3. t_n = Bit time before clock pulse.
- 4. $t_n + 1$ = Bit time after clock pulse.
- 5. If inputs J* or K* are not used must be grounded.

FIGURE 2. <u>Truth tables</u> – Continued.



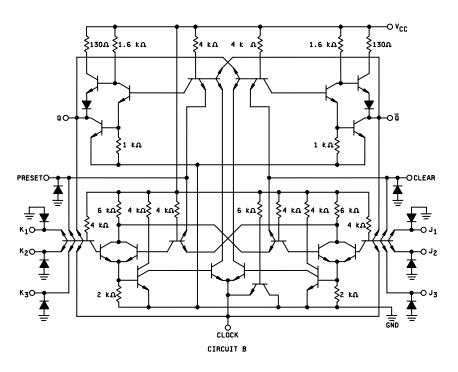


FIGURE 3. Schematic circuits.

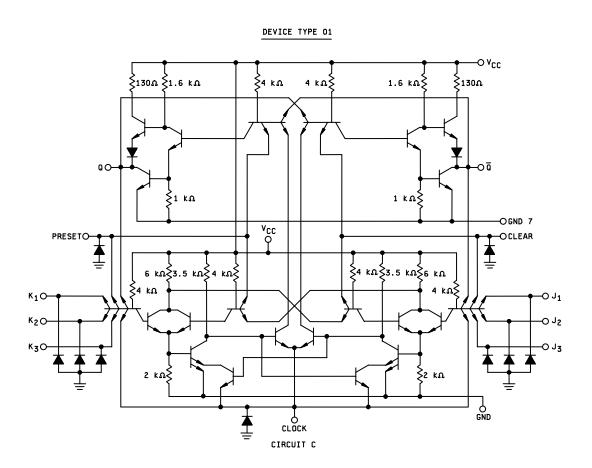


FIGURE 3. <u>Schematic circuits</u> – Continued.

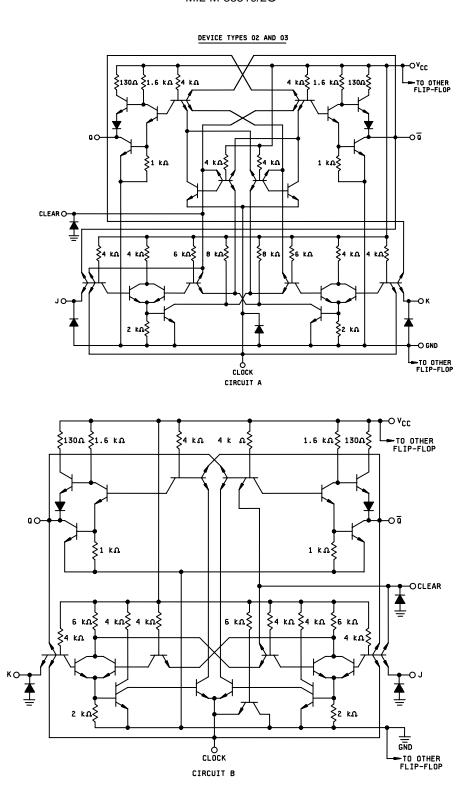
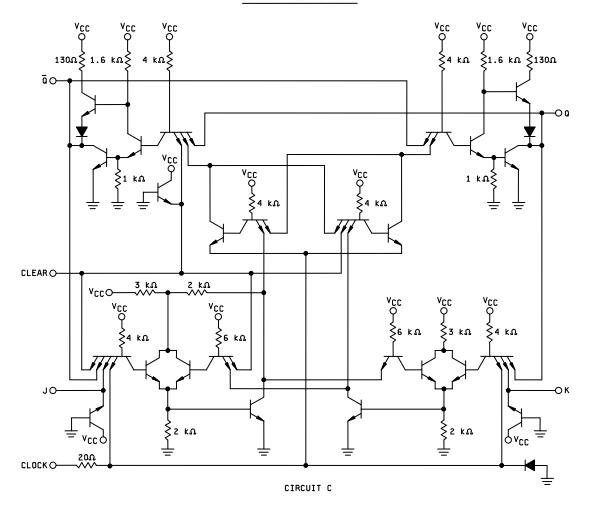


FIGURE 3. Schematic circuits - Continued.

DEVICE TYPES 02 AND 03



- 1. Circuits A, B, and C are the only acceptable variations for device types 02 and 03.
- 2. All resistance values shown are nominal.

FIGURE 3. Schematic circuits - Continued.

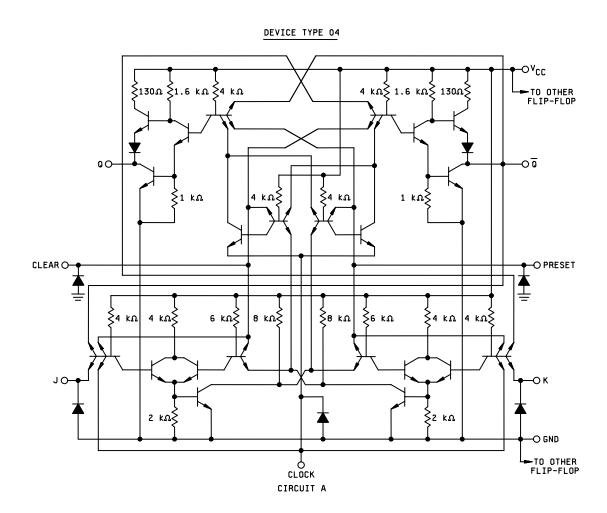


FIGURE 3. <u>Schematic circuits</u> – Continued.

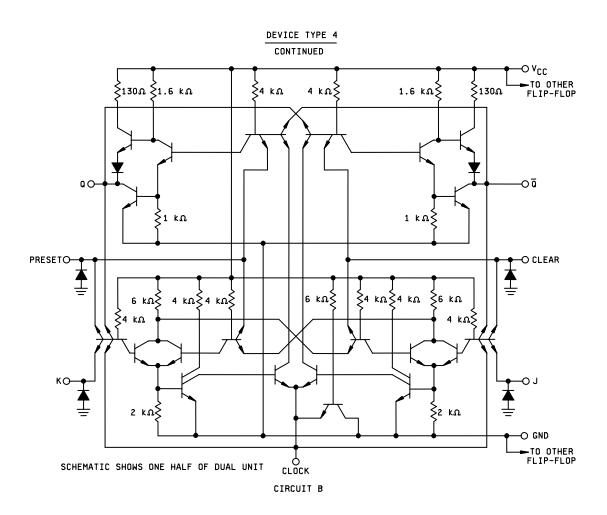
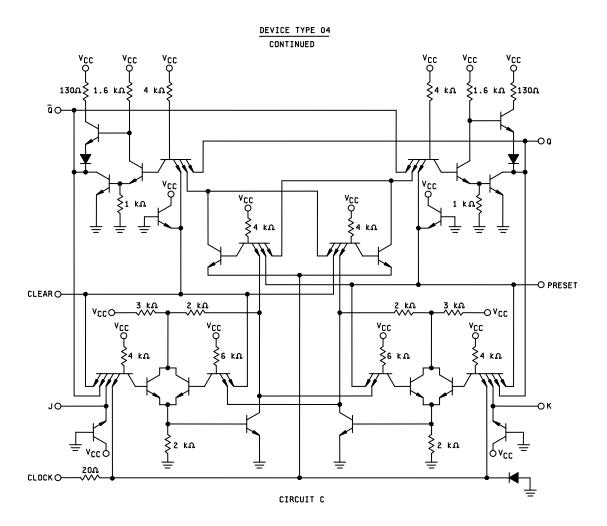
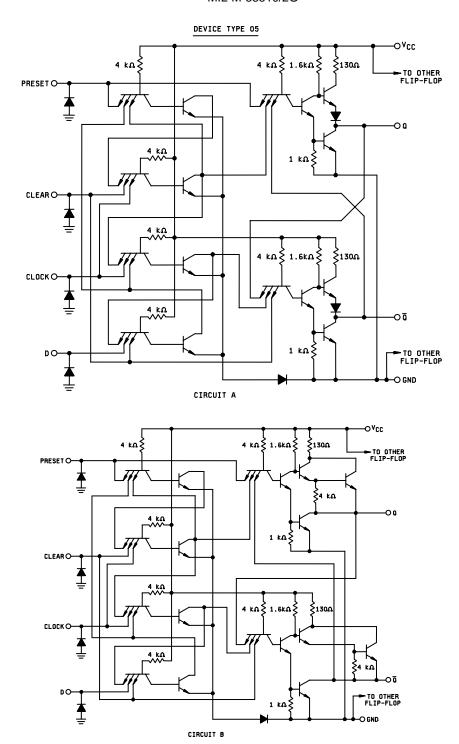


FIGURE 3. <u>Schematic circuits</u> – Continued.



- 1. Circuits A, B and C are the only acceptable variation for device type 04.
- 2. All resistance values shown are nominal.

FIGURE 3. <u>Schematic circuits</u> – Continued.



- Circuits A, B, and C are the only acceptable variations for device type 05. All resistance values shown are nominal.
- 2.

FIGURE 3. Schematic circuits - Continued.

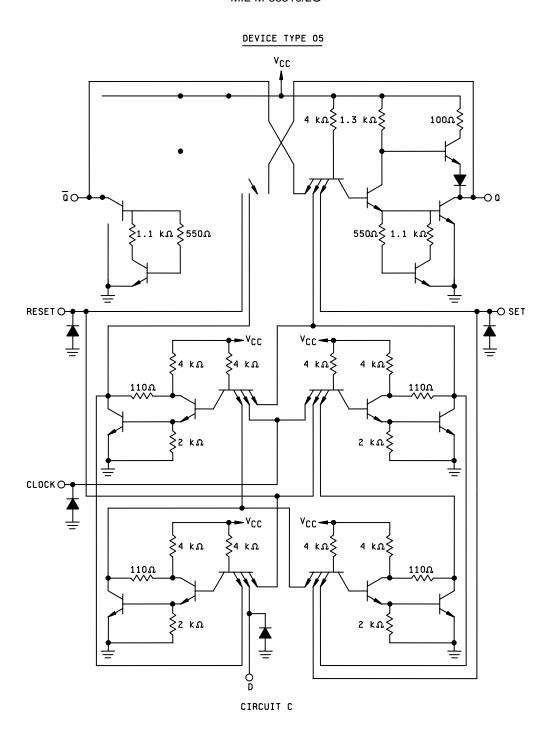
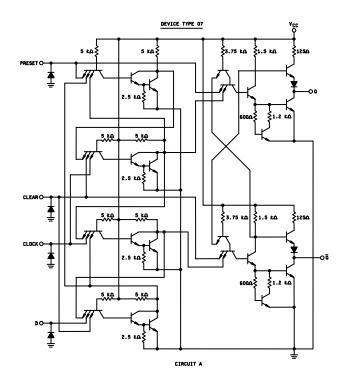


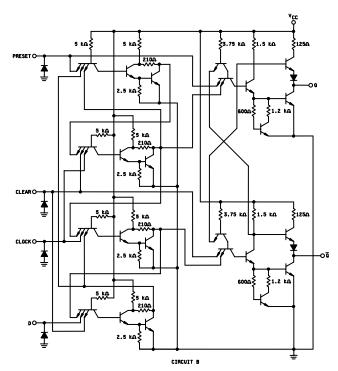
FIGURE 3. <u>Schematic circuits</u> – Continued.

DEVICE TYPE 06 -O v_{cc} \$1300 \$1.6 ku **ξ**4 kΩ. 1.6 kΩ\$ 4 kΩ} **}**130Ω **§**1 kΩ ์าหก≷ **}**1 kΩ O GND 4 kΩ\$ **∮**4 kΩ. **§**4 kΩ **≶4 kΩ**. O CLEAR PRESETO -O J1 4 kn \$ 2.5 kn \$ -O J2 CLOCKO-

NOTE: All resistance values shown are nominal.

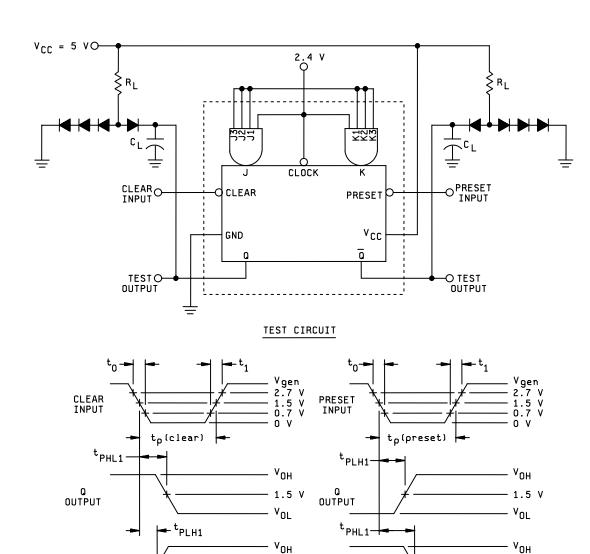
FIGURE 3. Schematic circuits – Continued.





- Circuits A and B are the only acceptable variations for device type 07.
 All resistance values shown are nominal.

FIGURE 3. Schematic circuits – Continued.



VOLTAGE WAVEFORMS

1.5 V

VOL

Q OUTPUT 1.5 V

 v_{OL}

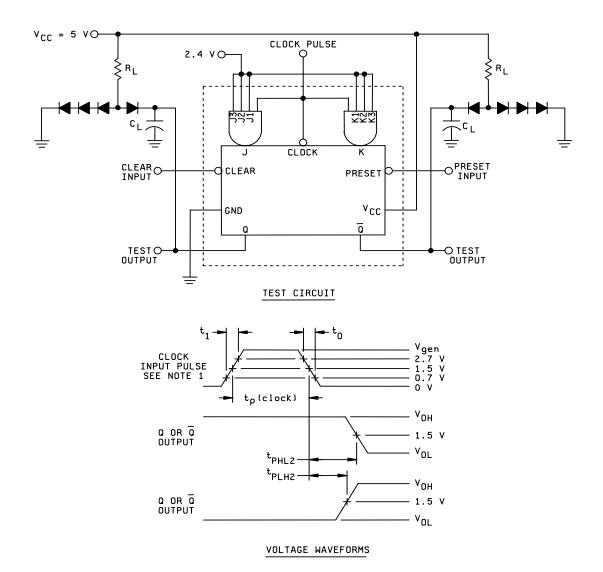
NOTES:

- 1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
- 2. Clear or preset input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 = 10 \text{ ns}$, $t_p(clear) = t_p(preset) = 30 \text{ ns}$, PRR = 1 MHz, and $Z_{OUT} \approx 50\Omega$.
- 3. $C_L = 50$ pF, minimum (C_L includes probe and jig capacitance).
- 4. $R_L = 390\Omega \pm 5\%$.

Q OUTPUT

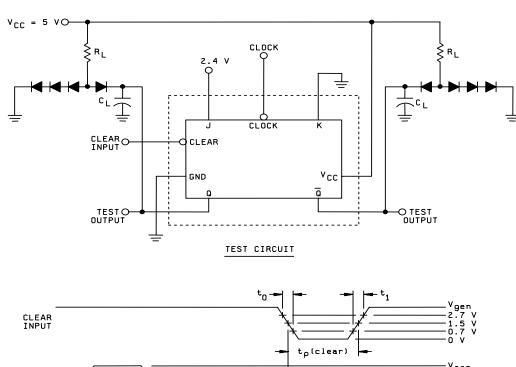
- 5. All diodes are 1N3064, or equivalent.
- 6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset output switching, clear shall have a negative pulse (see table III).

FIGURE 4. Clear and preset switching test circuit and waveforms for device type 01.



- 1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen}=3$ V, $t_1=t_0 \le 10$ ns, t_p (clock) = 25 ns, and PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are $V_{gen}=3$ V, $t_1=t_0 \le 10$ ns, t_p (clock) = 20 ns, and PRR = see table III.
- 2. $J = J1 \cdot J2 \cdot J3$; and $K = K1 \cdot K2 \cdot K3$
- 3. All diodes are 1N3064, or equivalent.
- 4. $C_L = 50 \text{ pF minimum } (C_L \text{ includes probe and jig capacitance}).$
- 5. $R_L = 390\Omega \pm 5\%$

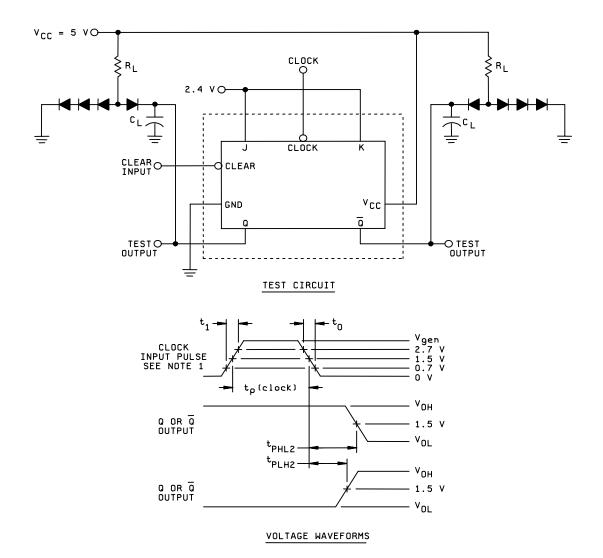
FIGURE 5. Synchronous switching test circuit for device type 01.



CLOCK INPUT t_p(clock) ^tPHL1 Q OUTPUT t_{PLH1} ٧он 1.5 V · V_{OL} VOLTAGE WAVEFORMS

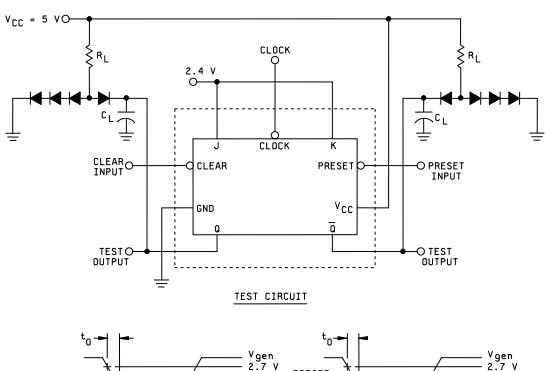
- Clear inputs dominate regardless of the state of clock or J-K inputs.
 Clear input pulse characteristics: V_{gen} = 3 V, t₀ = t₁ = 10 ns, t_p(clear) = 30 ns, PRR = 1 MHz.
 All diodes are 1N3064, or equivalent.
- 4. $C_L = 50 \text{ pF}$, minimum (C_L includes probe and jig capacitance).
- 5. $R_L = 390\Omega \pm 5\%$.
- 6. Clock input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_p \text{ (clock)} \ge 25 \text{ ns}$, PRR = 1 MHz.

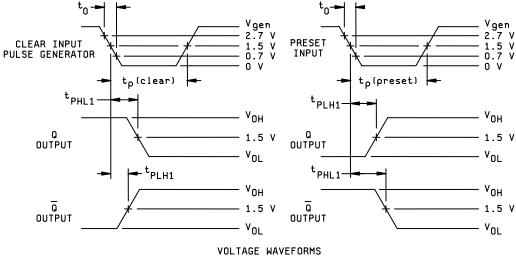
FIGURE 6. Clear switching test circuit and waveforms for device types 02 and 03.



- 1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen}=3$ V, $t_1=t_0\leq 10$ ns, t_p (clock) = 25 ns, and PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are $V_{gen}=3$ V, $t_1=t_0\leq 10$ ns, t_p (clock) = 20 ns, and PRR = 10 MHz for subgroups 9, 10, and 11.
- 2. All diodes are 1N3064, or equivalent.
- 3. $C_L = 50$ pF minimum (including jig and probe capacitance).
- 4. $R_L = 390\Omega \pm 5\%$

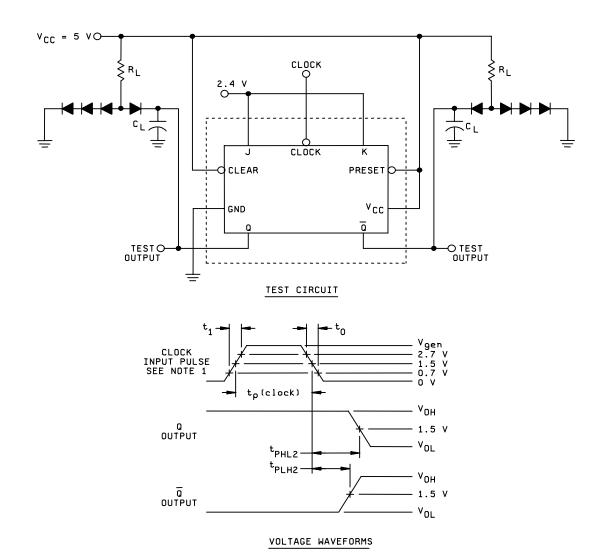
FIGURE 7. Synchronous switching test circuit for device type 02 and 03.





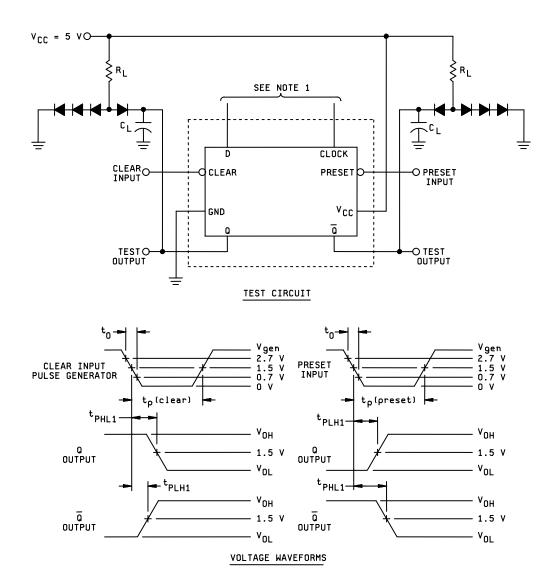
- 1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
- 2. Clear or preset input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 = 10 \text{ ns}$, $t_p(clear) = t_p(preset) = 30 \text{ ns}$, PRR = 1 MHz, and $Z_{OUT} \approx 50\Omega$.
- 3. $C_L = 50$ pF, minimum (including jig and probe capacitance).
- 4. $R_L = 390\Omega \pm 5\%$.
- 5. All diodes are 1N3064, or equivalent.
- 6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset to output switching, clear input shall have a negative pulse (see table III).

FIGURE 8. Clear and preset switching test circuit and waveforms for device type 04.



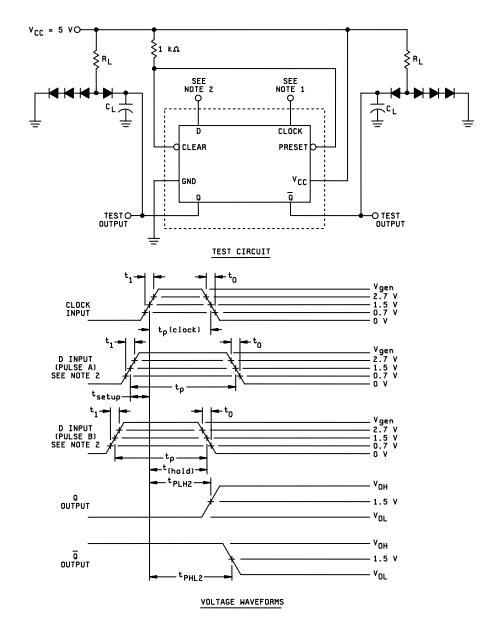
- 1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen}=3$ V, $t_1=t_0 \le 10$ ns, t_p (clock) = 25 ns, and PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing t_{MAX} the clock input characteristics are $V_{gen}=3$ V, $t_1=t_0 \le 10$ ns, t_p (clock) = 20 ns, and PRR = see table III.
- 2. All diodes are 1N3064, or equivalent.
- 3. $C_L = 50 \text{ pF minimum (including jig and probe capacitance)}$.
- 4. $R_L = 390\Omega \pm 5\%$

FIGURE 9. Synchronous switching test circuit for device type 04.



- 1. Clear and preset inputs dominate regardless of the state of clock or D inputs.
- 2. All diodes are 1N3064, or equivalent.
- 3. Clear or preset input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_o \le 7 \text{ ns}$, t_p (clear) = t_p (preset) = 35 ns, and PRR = 1 MHz.
- 4. $C_L = 50$ pF, minimum (including jig and probe capacitance).
- 5. $R_L = 390\Omega \pm 5\%$.
- 6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset to output switching, clear input shall have a negative pulse (see table III).

FIGURE 10. Clear and preset switching test circuit and waveforms for device types 05 and 07.



- 1. Clock input pulse has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_o = t_1 \le 10 \text{ ns}$, t_p (clock) = 30 ns, and PRR = 1 MHz. When testing f_{MAX} , PRR = see table III.
- 2. D input (pulse A) has the following characteristics: $V_{gen}=3$ V, $t_o=t_1 \le 10$ ns, $t_{SETUP}=25$ ns, $t_p=60$ ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: $V_{gen}=3$ V, $t_o=t_1 < 7$ ns, $t_{hold}=6$ ns, $t_p=60$ ns, and PRR is 50% of the clock PRR.
- 3. All diodes are 1N3064, or equivalent.
- 4. $C_L = 50 \text{ pF minimum (including jig and probe capacitance)}$.
- 5. $R_L = 390\Omega \pm 5\%$

FIGURE 11. Synchronous switching test circuit (high level data) for device types 05 and 07.

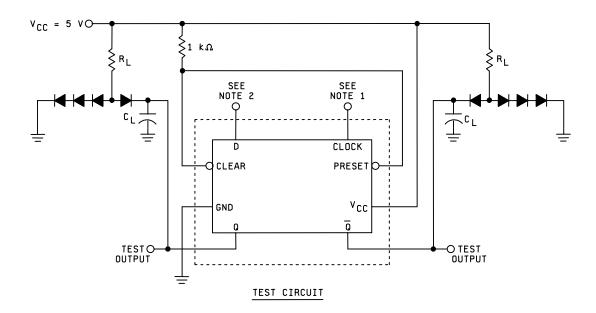
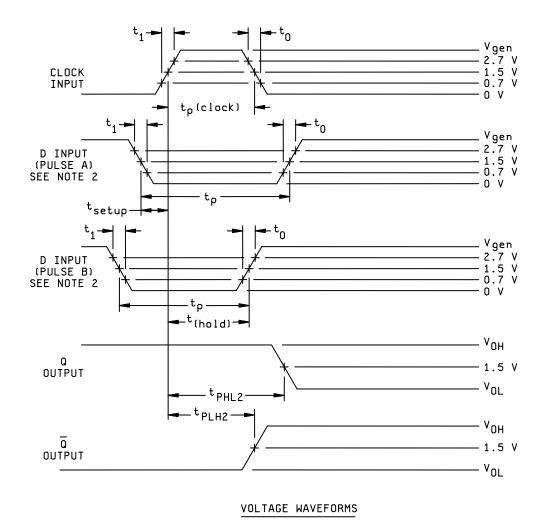
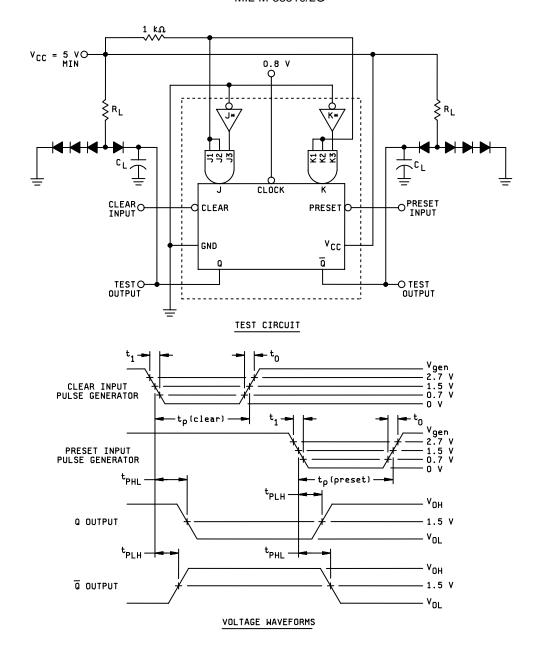


FIGURE 12. Synchronous switching test circuit (low-level data) for device types 05 and 07.



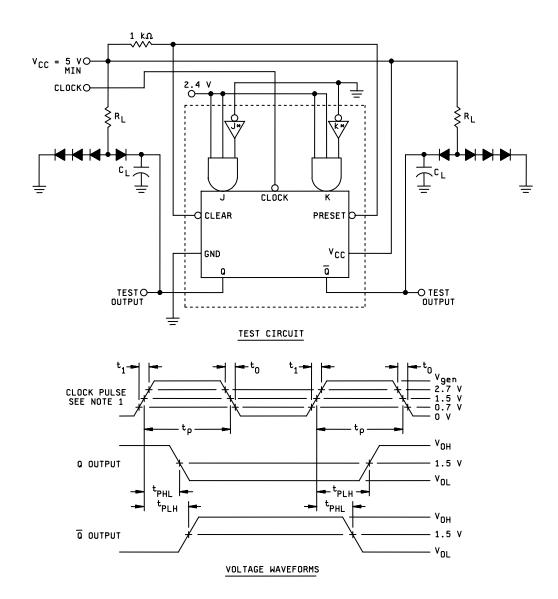
- 1. Clock input pulse has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_o = t_1 < 10 \text{ ns}$, t_p (clock) = 30 ns, and PRR = 1 MHz.
- 2. D input (pulse A) has the following characteristics: $V_{gen}=3$ V, $t_o=t_1 \le 10$ ns, $t_{SETUP}=25$ ns, $t_p=60$ ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: $V_{gen}=3$ V, $t_o=t_1 < 10$ ns, $t_{hold}=6$ ns, $t_p=60$ ns, and PRR is 50% of the clock PRR.
- 3. All diodes are 1N3064, or equivalent.
- 4. $C_L = 50$ pF minimum (including jig and probe capacitance).
- 5. $R_L = 390\Omega \pm 5\%$

FIGURE 12. Synchronous switching test circuit (low-level data) for device types 05 and 07 – Continued.



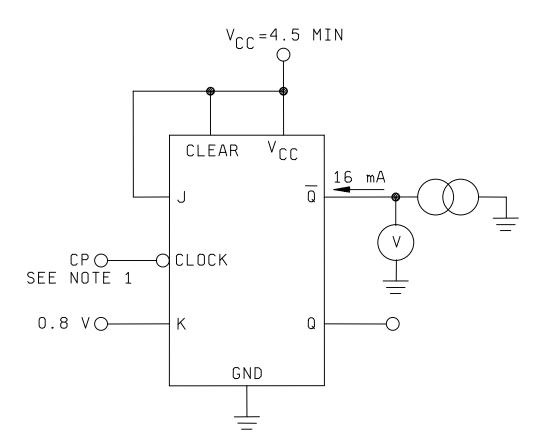
- 1. Preset or clear function can occur only when clock input is low. Gated inputs are inhibited.
- 2. All diodes are 1N3064, or equivalent.
- 3. $C_L = 50$ pF, minimum, including jig and probe capacitance.
- 4. Clear or preset input pulse characteristics: V_{gen} = 3.0 V, t_o = 5 ns, t_1 ≤ 10 ns, t_p = 25 ns.
- 5. $R_L = 390\Omega \pm 5\%$.

FIGURE 13. Clear and preset switching test circuit and waveforms for device types 06.



- 1. Clock input pulse has the following characteristics: V_{gen} = 3 V, t_1 = $t_0 \le 10$ ns, t_p = 30 ns, and PRR = 1 MHz. When testing f_{MAX} , PRR = see table III.
- 2. All diodes are 1N3064, or equivalent.
- 3. $C_L = 50 \text{ pF}$ minimum including jig and probe capacitance.
- 4. $R_L = 390\Omega \pm 5\%$

FIGURE 14. Synchronous switching test circuit for device type 06.



- 1. Apply normal clock pulse, then sink -12 mA on the clock input.
- 2. The output \overline{Q} is measured after -12 mA is applied to the clock to insure it is still in the low state.

FIGURE 15. Input clamp voltage test circuit for device types 01, 02, 03, and 04 (circuit B).

TABLE III. Group A inspection for device type 01. 1/

			>	"	31	×	3	3	,,	3	3	"	= :			3	=		3 3	MA	*	31	n	,,	* E	<u> </u>	*	3	,,	"	μĄ		"	"	"	"	3 :	: :		:			,	3 3		33
Test limits	Mari	Max					0.4	3	*	,,	-1.5	n	,	= :	= :	y,	n :		0.5	-1.6	n	"	"	"	* c	-3.2	-1.6	-3.2	-1.6	-3.2	40	: 3	"	"	"	100	,,	. ,	: 3	: :	= ;	80	80	200		3
Ţ	MAile	Ξ	2.4	3	"	"														-0.7	"	31	"	,,,	3 7	-1.4	-0.7	-1.4	-0.7	-1.4																
	Meas.	<u> </u>	Ø	ΙØ	Ø	ıø	Ø	ΙØ	Ισ	Ø	L L	JZ	SL :	K4	2	K3	Clear	Preset	Clock	J.	JZ	J3	K1	K2	K3	Clock	Preset	Preset	Clear	Clear	۲,	Z E	Σ¥	K2	K3	J1	J2	J3	- S	22 5	K3	Clear	Preset	Preset	Clear	Clock
14	11	2	0.8 V	2.0 V			2.0 V	0.8 V								-12 mA			> 8 0	GND	GND	GND	4.5 V	4.5 V	0.4 \	? ?	'n	31	"	"			GND	GND	2.4 V				GIND	GND	5.5 \	4.5 \	GND	GND	4.5 V	GND
13	01	Z	0.8 V	2.0 V			2.0 V	0.8 V							-12 mA				780	GND	GND	GND	4.5 V	0.4 V	4.5 V	2 =	"	3	'n	"			GND	2.4 V	GND				GND	5.5 V	GND	4.5 V	GND	GND	4.5 V	GND
12	∞ (3	4 mA		4 mA		16 mA			16 mA																																				
1	, 0		"	,,		,,	,	,,	,	,	,,	,,				,		,,	3	, ,	,,	"	n	,,	3 3	,,	,,	,	,,	"	,,		,,	"	,,	,,	,,					4	,	, ,	: 3	25
		ງ 		4 mA		4 mA		16 mA	16 mA																																				1	
-			^			4	>		16				٨٢						>	, >	>	>	0	0	0.3	>					0 (1>				(0	>				0	>	> (
6	Ω 2	Σ Γ	2.0 V	0.8 V			0.8 V					Н	-12 mA						45	4.5	4.5	0.4	GNI	GNI	GND	ř	39	3	,	"		2.4 V					GND					BNB	4.5	4.5	5 2	GND
ω.	4 5	75	2.0 V	0.8 V			0.8 V	2.0 V				-12 mA							457	4.5 V	0.4 V	4.5 V	GND	GND	GND	?	n	3	n	"	GND	SND GND				GND	5.5 V	GND				GND	4.5 V	4.5 V	באב פאם	GND
7	n <u>z</u>	5	2.0 V	0.8 V			0.8 V	2.0 V			-12 mA								457	0.4 V	4.5 V	4.5 V	GND	GND	GND	è =	n	я	'n	"	2.4 \	ON O				5.5 V	GND	GND				GND	4.5 V	4.5 V	ON C	GND
9	- 5) N																																												
2	2 2	Clear			2.0 V	0.8 V			2.0 V	0.8 V							-12 mA		45 V	B	В	В				В			0.4 V	0.4 V	GND	GND				GND	GND	GND				2.4 V	GND	GND	5.5 V	ָ בֿ
4 ;	14	8	4.5 V	"	"	"	,,	"	3	,,	"	n	= :			"	= :	,,	3 3	5.5 V	"	"	n	"	3 3	n	"	3	,,,	"	3 3	: 3	"	"	,,,	,,,	3	: 3		: :	= :		,,	3 3	: 3	3
8	13	Preset			0.8 V	2.0 V			0.8 V	2.0 V								-12 mA					В	В	Ф а	3	0.4 V	0.4 V					GND	GND	GND				GIND	GND	GND		2.4 V	5.5 V		GND
2	7.5	Sock	Α	٧			4	٧											-12 mA A*	4.5 V	'n	33	"	"	, , ,	0.4 V	4.5 V	31	'n	"	GND	: 12	'n	"	"	"	3 .					A	Α.	∢ <	A 7	5.5 V
- (o 7	2	0.8 V	2.0 V			2.0 V	0.8 V						-12 mA					V 8 0	GND	'n	"	0.4 V	4.5 V	4.5 \	2 =	'n	31	'n	"			2.4 V	GND	GND			7	2.5	GND	GND	4.5 V	GND	GND	4.5 V	GND
Case A, B, D	Case C	l est No.	1	2	3	4	5	9	2	80	6	10			13	14	15	16	17 CKT B	18	19	20	21	22	23	25	26 CKT A	26 CKT B	27 CKT A	27 CKT B	28	30	31	32	33	34	35	36	3/	38	39	40	41	42	43	45
MIL-			3006	3	*	"	3007	"	3	,	"	3	3 3	: :	. :	,	3	7	3 3	3009	,,	*	"	"	3 3	3	"	3	33	я	3010	: 3	n	"	"	"	3 3	: 3		: 3	:	,	,,	3 3	: 3	ä
Symbol			V _{ОН}	"	"	"	Vol	"	33	,,	Vic	n	2 :	: :		×	3	z	2 2	7	3	,,	"	"	* _		=======================================	3	,	29	H	: 3	n	,	"	I _{IH2}	35 25	: 3	: 3	: :		IH3	I _{IH3}	IH4	: 3	25
Subgroup			1 2/	$T_C = 25$ °C	3	u	"	3	3	*	"	"	3 :	: :		,	3 :	*	3 3	3	"	3	77	"	3 3	"	"	*	3	77	3 3	: 3	"	3	"	"	3 :	: 3		: :		,	,,	3 3	: 3	я

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01, 1/ - Continued.

Ī		Unit	Ϋ́	3	"	"	"	* <	<u> </u>	"	ä																																			T	T	
	est illuits	Max	-700	-850	-1000	-700	-850	-1000	-57	20	20			HorL	as shown $3/$	я	"	: 3	3	я	n	n	"	"	n	3	= =	: "	: "	я		"	3	"	3 3	: 3	n	3	n	31	n	11	n	я :	3		: 3	n
-	_	Min	-20	-200	-400	-50	-200	-400	-20						as																																	
	Meas.	terminal	Clock	"	n	,,	,,	¥ (Ø 10	, N	Vcc			ΙΝ	output	"	3 3	: 3	,,	3	"	n	2	**	,,	3 3	2 3	: 3	: 3	"		2	,	"	3 3	: :	,	"	n	,,	"	n	*	2 :	3 3	s 3	: 3	×
,	4 1	K3	GND	"	"	n	n	" " " " " " " " " " " " " " " " " " " "	4.5 V	GND	GND			В	В	Α	∢ •	∢ <	τ <	۷ ۵	c ac	В	В	В	В	B	ω (ם מ	20 0	۵ ۵	n a	а	V	Α	∢ .	∢ <	۷ ۵	. <	V	A	Α	A	A	A	∢ .	∢ <	∢ ⊲	(∢
9	10	Z Z	GND	"	"	,,	n	" " " " " " " " " " " " " " " " " " " "	4.5 V	GND	GND			В	В	Α	۷,	∢ 0	۵ ۵	<u>α</u>	ο «	. ⋖	V	Α	В	B i	ω (ממ	20 0	۵ ۵	n a	В	A	Α	∢ .	∢ <	< ⊲	<	<	A	Α	Α	A	Α.	∢ .	⋖ <	∢ ⊲	(4
9	7 8	ø												L 3/	I	I	Ι:		c 3	- 1	: 1	I	I	7			_ .	J .	<u> </u>	-			_	7	Ι:	Ι.		J		I	I	I	I	I	=	Ξ-	4	1
;		GND	GND	"	n	,,	n	3 3	"	n	"			GND	,,	n	,,	: "	3	"	"	"	"	"	n	× :	= =	: 3	: "	33	. ,,	"	3	"	3 3		"	3	n	n	y ·	11	n	,	,		: 3	n
	2 હ	10	5						GND					/≅Н	7				J _	<u> </u>	J	ı	_	I	I	_	=	I :	-	c 2	c I	I	I	I			- - -	: _	I	I	I	I	_	_	_	_ =	I I	ΞΞ
	ט ע) S	GND	"	"	,,	"	" " " " " " " " " " " " " " " " " " "	4.5 V	GND	GND			В	В	В	В	9 0	۵ ۵	0 a	a a	В	В	В	A	∢.	∢ .	Α «	∢ <	τ 0	n a	В	¥	A	∢.	∢ <	€ 4	<	A	4	Α	A	∢	Α.	∢ .	⋖ <	∢ ⊲	τ ∢
	δ 4	JZ	GND		n	,,	"		4.5 \		GND			В	В	В	В	9 0	۵ ۵	0 a		В	В	В	A	Α.	∢ (200	20 0	٥ <	4 4	. ∠	A	A	۷.	∀ <	₹ 4	. ✓	A	A	Α	A	A	∀	۷.	4 <	∀ 4	(∢
-	3 '		GND		n		n		4.5 \ 4.5 \		GND				В	3	8 (200	0 0) «				3	3	m /	m /	-	∢ <		4 4	. 4	-	A	Α,	∢ <	4 4	. 4	A	A	A	A	A	_	_	m (2 A	
-	۰ ۲		95		,				4.	G	G									1									1	1					-		-								_		8 8 8 7	
-			٥	D	D			1	Q		D	V _{IC} tests are omitted	V _{IC} tests are omitted.																																		1	
-	0 0	O	>	GND	GN			>	GND		GND			N B	A	A	Α,	Α <	Σ <	(4	Α .	A	A	В	A	∢ .	∢ <	∢ <	∢ <	τ <	4 4	×	A	A	∢ .	∀ <	ξ α	n m	В	В	В	В	Α .	A	∢ .	∢ <	∀ □	α «
-	14 4		5.5	"	"		,,	+	2	,,	"	125°C and	-55°C and	4.5	"	n	2 2	: 3	3	31	31	n	'n	"	n	3 :	= =	: 3	: 3	3	3	"	3	99	3 3	: 3	n	3	n	3	"	11	n	3	= =	: 3	: 3	"
	3 3	۵				GNE	GNE	GND	5	GND		xcept T _c =	xcept T _C =	⋖	В	Α	∢ •	∢ <	τ <	€ 4	< ∢	< <	4	Α	A	∢ ·	∢ <	∢ <	∢ <	τ <	∢ ∢	< <	∢	A	∢ .	∢ <	< ⊲	< <	A	В	В	В	В	∢ •	∢ ⋅	∢ <	∢ ⊲	ζ <
•	12	Clock	2.4 V	3	"	n	"	* C	3	31	"	group 1, e	group 1, e	В	В	В	۷ ۷	20 0	Δ <	τ α	2 60	Α	В	В	В	∢ 1	ω (n <	< 0	۵ ۵	ם מ	В	В	A	ω.	∢ (Δ α	<	В	В	A	В	∢	Α	∢ .	< 0	თ ⊲	< <
,	- o	조	GND	n	"	n	"	" V	4.5 V	GND	GND	s as for sub	s as for sub	В	В	В	а	n <	<	۲ ⊲	< ⊲	< <	4	Α	В	В	ω (ם מ	20 0	۵ ۵	20 00	а	A	A	∢ .	∢ <	< ⊲	< <	⋖	∢	٧	Α	∢	∢	ω (a	თ ⊲	4 Α
4	Case A, B, D	Test No.	46 CKT A	46 CKT B	46 CKT C	47 CKT A	47 CKT B	47 CKT C	49	50	51	Same tests, terminal conditions and limits as for subgroup 1, except $T_{\rm c}$ = 125°C and	Same tests, terminal conditions and limits as for subgroup 1, except $T_{\rm C}$ = -55°C and	52	53	54	55	56	2/	200	60	61	62	63	64	65	99	/9	89	60	71	72	73	74	75	76	78	62	80	81	82	83	84	85	86	87	χχ α	06
	STD-883	method	3010	n	n	,,		* 5044	3011	3005	3005	terminal con	terminal con																																			
F	ogungo			,,	77	,,	n	= _	s s	8	3 8	Same tests, t	Same tests, i						1																	$\frac{1}{1}$										1		\prod
ŀ	dnoubane		-	$T_C = 25^{\circ}C$	n		,,	3 3	3	×	29	2	3	7 2/ 4	$T_C = 25^{\circ}C$		= 3	: 3	,,	3	"	×	2	27	"	= :	= =	: 3	: 3	37	2	2	,	"	3 3	: :	3	"	"	,,	"	n	"	= :	= :	: :	: 3	3

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01. 1/- Continued.

MIL-	Case A, B, D	1	2	3	4	2	9	7	8	6	10	11	12	13	14		Tes	t limits	
STD-883	Case C	6	12	13	14	2	1	3	4	2	9	7	8	10	11	Meas.			
method	Test No.	K1	Clock	Preset	οοΛ	Clear	NC	11	JZ	13	ΙΟ	GND	ø	K2	K3	terminal	Min		Unit
	91	В	Α	Α	4.5 V	Α	В	В	Α	А	т	GND	7	Α	Α	ΙΑ	I	orL	
	92	В	В	Α	4.5 V	A	В	В	Α	A	٦	GND	н	A	Α	output	Ass	3/ nwor	
sts, terminal cou	nditions and limits	as for sub	group 7, exc	$sept T_c = 12$		ιi													
(Fig. 5)	93	2.4 V	Z	5.0 V	5.0 V	5.0 V		2.4 V		.4 V		GND	OUT	2.4 V	2.4 V	Ø	10	_	MHz
(Fig. 5)	94	3	Z	5.0 V	n	5.0 V		3	3	3	OUT	3		"	3	ıσ	10		MHz
3003	92	"	2.4 V	ſ	"	Z		'n	'n	,,	OUT	,,		,,	"	Clear to Q		55	ns
(Fig. 4)	96	"	n	Z	"	7		7	y	u		n	OUT	3	"	Preset to Q		55	n
39	26	"	"	ſ	"	Z		n	,,	,,		"	OUT	,,	n	Clear to Q	"	40	"
3	86	"	n	Z	,,	7		3	3	3	OUT	3		3	3	Preset to Q	3	40	3
3003 (Fig 5	66	я	≧	5.0 V	2	5.0 V		*	*	2	OUT	2		3	3	Clock to Q	я	30	ns
39	100	'n	,,	"	n	"		n	n,	n		,,	OUT	,,	"	Clock to Q	"	30	,,
3	101	я	з	"	n	3		3	3	3	TUO	2		я	3	Clock to Q	3	40	z
9	102	'n	,,	"	n	"		n	n,	n		,,	OUT	,,	"	Clock to Q		40	,,
(Fig 5)	103	"	"	11	27	"		"	"	"		"	OUT	n	"	Ö	10	1	MHz
(Fig 5)	104	"	"	**	"	"		,,	"	**	TUO	,		39	,	ΙØ	10	_	MHz
3003 (Fig. 4)	105	"	2.4 V	٦	"	Z		,,	,,	ä	OUT	ņ		3	n	Clear to Q	2	36	ns
3	106	n	n	Z	"	7		3	3	3		"	OUT	3	"	Preset to Q	"	39	*
10	107	"	n	J	"	Z		"	,,	"			OUT	11	"	Clear to Q	"	20	"
29	108	"	n	Z	"	7		3	3	3	DUT	3		3	*	Preset to Q	,	20	3
(Fig 5)	109	я	Z	5.0 V	n	5.0 V		3	3	3	OUT	3		ä	3	Clock to D	3	39	ns
39	110	"	n,	и	n	n		n	m,	,,		"	OUT	n	"	Clock to Q	"	39	n,
2	111	"	"	**	"	"		,,	,	,	DUT	*		**	"	Clock to Q	39	20	*
"	112	"	n	и	79	n		11		,,		,,	OUT	,,	n,	Clock to Q	**	20	,
sts, terminal cou	nditions and limits	as for sub	group 10, e)	xcept T _C = -	55°C.														
	STD-883 method sts, terminal co (Fig. 5) (Fig	STD-883 Case C Desiry Case A, B, D Case C Desiry C Desiry Case C Desiry Case C Desiry Case C Desiry Case C Desiry	MIL. Case A, B, D 1 STD-883 Case C 9 method Test No. K1 92 B 93 St, terminal conditions and limits as for sub at a frequency and limits as for sub at a frequency and limits as for sub a frequency and limits as for sub at a frequency and limits as for sub a frequency and limits a frequency a	MIL. Case A B, D 1 2 MIL. Case G 9 12 Method Test No. K1 Clock 91 B A 91 B B 92 B B 93 2.4 V IN (Fig. 5) 94 " IN (Fig. 5) 94 " IN (Fig. 4) 96 " 2.4 V (Fig. 5) 99 " " " 98 " " " 101 " " " 102 " " (Fig. 5) 103 " " (Fig. 5) 104 " " " 105 105 " " " 107 " " " 107 " " " 110 " " " 111 " " " 111 " " sis, terminal conditions and limits as for subgroup 10, each of the conditions	Mil. Case A, B, D 1 2 3 STD-883 Case C 9 12 13 Method Test No. K1 Clock Preset 91 B A A 91 B B A A 101 S.0 V (Fig. 5) 94 " N 5.0 V (Fig. 4) 96 " " N " 98 " " N " 101 " " " " 102 " " " " 103 3003 99 " " 104 " " " " 105 105 " " 107 " " 107 " " 110 " " 111 " " 112 sis, terminal conditions and limits as for subgroup 10, except T _C = 13	Case A, B, D 1 2 3 Case C 9 12 13 Test No. K1 Clock Preset 91 B A A 92 B A A 94 " 5.0 V 95 " IN 5.0 V 96 " IN 5.0 V 96 " " IN 100 " " " 101 " " " 103 " " " 104 " " " 105 " " IN 107 " " IN 107 " " " 109 " " " 109 " " " 109 " " " 109 " " " 109 " " " </td <td>3 >> 5</td> <td> </td> <td>V V V V V V V V V V V V V V V V V V V</td> <td>V V V A B B B A A B B B A A B B B B A A B B B B A A B B B B A A B B B B A A B B B B A A B B B B A A B B B B A A B B B B A B A B B B B A B A B B B B A B A B B B B A B A B B B B A B A B B B B A B A B B B B A B A B B B B A B A B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B B A B A B B B B B A B A B B B B B B A B A B B B B B B A B A B B B B B B A B A B B B B B B B A B A B B B B B B B A B A B</td> <td>V V A B B B A A A A A A A A A A A A A A</td> <td>V V V V V V V V V V V V V V V V V V V</td> <td>Clear NC J1 J2 J3 G G D J1 J2 C Clear NC J1 J2 J3 G G D G D G D G D G D G D G D G D G D</td> <td>Color NC</td> <td>\$\begin{array}{c c c c c c c c c c c c c c c c c c c </td> <td>5 6 7 8 9 10 11 12 13 13 14 15 15 16 17 18 19 10 11 12 13 14 15 16 10 11 12 13 14 15 16 10 11 12 11 12 10 11 12</td> <td> 5 6 7 8 9 10 11 12 13 14 2 Clear NC J1 J2 J3 Q GND Q K3 4 5 6 7 B B A A H GND L A A 5 Clear NC J1 J2 J3 Q GND C A 5 Clear NC J1 J2 J3 Q GND C A 5 Clear NC J1 J2 J3 Q GND C A 5 Clear NC J4 C A A H GND L A A 5 Clear NC J4 C A C A 5 Clear NC J4 C A C 6 Clear NC J4 C A C 7 Clear NC C C 7 Clear NC C C 8 Clear NC C C 9 Clear NC C C 10 C C C 11 C C C C 12 C C C 13 C C C 14 Clear C C 15 Clear C C 16 Clear C C 17 Clear C C 18 Clear C C 19 Clear C C 10 C C C 11 C C C 11 C C C 12 C C C 13 C C C 14 Clear C 15 Clear C C 16 C C C 17 C C 18 C C C 19 C C C 10 C C C 10 C C C 11 C C C 11 C C C 12 C C C 13 C C C 14 C C C 15 C C C 16 C C C 17 C C C 17 C C C 18 C C C 18 C C C 19 C C C 10 C C C 10 C C C 11 C C C 11 C C C 12 C C C 13 C C C 14 C C C 15 C C C 16 C C C 17 C C C 17 C C C 18 C C C 19 C C C 10 C C C 10 C C C 11 C C C 11 C C C 12 C C C 13 C C C 14 C C C 15 C C C 15 C C C 16 C C C 17 C C C 17 C C C 18 C C C 18 C C C 19 C C C 10 C C C 10 C C C 10 C C C 11 C C C 11 C C C 11 C C C 12 C C C 13</td> <td> S 6 7 8 9 10 11 12 13 14 Meas </td> <td> S S S S S S S S S S</td>	3 >> 5		V V V V V V V V V V V V V V V V V V V	V V V A B B B A A B B B A A B B B B A A B B B B A A B B B B A A B B B B A A B B B B A A B B B B A A B B B B A A B B B B A B A B B B B A B A B B B B A B A B B B B A B A B B B B A B A B B B B A B A B B B B A B A B B B B A B A B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B A B A B B B B B B A B A B B B B B A B A B B B B B B A B A B B B B B B A B A B B B B B B A B A B B B B B B B A B A B B B B B B B A B A B	V V A B B B A A A A A A A A A A A A A A	V V V V V V V V V V V V V V V V V V V	Clear NC J1 J2 J3 G G D J1 J2 C Clear NC J1 J2 J3 G G D G D G D G D G D G D G D G D G D	Color NC	\$\begin{array}{c c c c c c c c c c c c c c c c c c c	5 6 7 8 9 10 11 12 13 13 14 15 15 16 17 18 19 10 11 12 13 14 15 16 10 11 12 13 14 15 16 10 11 12 11 12 10 11 12	5 6 7 8 9 10 11 12 13 14 2 Clear NC J1 J2 J3 Q GND Q K3 4 5 6 7 B B A A H GND L A A 5 Clear NC J1 J2 J3 Q GND C A 5 Clear NC J1 J2 J3 Q GND C A 5 Clear NC J1 J2 J3 Q GND C A 5 Clear NC J4 C A A H GND L A A 5 Clear NC J4 C A C A 5 Clear NC J4 C A C 6 Clear NC J4 C A C 7 Clear NC C C 7 Clear NC C C 8 Clear NC C C 9 Clear NC C C 10 C C C 11 C C C C 12 C C C 13 C C C 14 Clear C C 15 Clear C C 16 Clear C C 17 Clear C C 18 Clear C C 19 Clear C C 10 C C C 11 C C C 11 C C C 12 C C C 13 C C C 14 Clear C 15 Clear C C 16 C C C 17 C C 18 C C C 19 C C C 10 C C C 10 C C C 11 C C C 11 C C C 12 C C C 13 C C C 14 C C C 15 C C C 16 C C C 17 C C C 17 C C C 18 C C C 18 C C C 19 C C C 10 C C C 10 C C C 11 C C C 11 C C C 12 C C C 13 C C C 14 C C C 15 C C C 16 C C C 17 C C C 17 C C C 18 C C C 19 C C C 10 C C C 10 C C C 11 C C C 11 C C C 12 C C C 13 C C C 14 C C C 15 C C C 15 C C C 16 C C C 17 C C C 17 C C C 18 C C C 18 C C C 19 C C C 10 C C C 10 C C C 10 C C C 11 C C C 11 C C C 11 C C C 12 C C C 13	S 6 7 8 9 10 11 12 13 14 Meas	S S S S S S S S S S

NOTES:

A = Normal clock pulse. B = Momentary, GND, then 4.5 V. J = Input pulse t_0 = 100 ns, PRR = 1 MHz, $V_{\rm OL}$ = 0 V, $V_{\rm OH}$ = 4.5 V

*After clock pulse apply –12 mA to clock pin to insure \overline{Q} is still in the low state (see figure 15).

1/ Terminal conditions (pins not designated may be $H \ge 2.0 \, V_i$ or $L \le 0.8 \, V_i$ or open). 2/ Input voltages shown are: $A = 2.0 \, \text{volts}$ minimum and $B = 0.8 \, \text{volts}$ maximum. 3/ Output voltages stall be either; (a) $H = 2.4 \, V_i$ minimum and $L = 0.4 \, V_i$ maximum when using a high speed checker double camparator; or (b) $H \ge 1.5 \, V_i$ and $L < 1.5 \, V_i$ when using a high speed checker single comparator. 4/ Tests shall be performed in sequence. 5/ E_{max} minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 02. 1/

		Unit	>	3	3	,,	3	3	3	3	3 3	,,	"	3	n	3	: "		,	"	,,		۳A	: "	: :	,,	,	3 3		,,	μA	: 3	n	"	,	2 :	"	3 3	:	: :	ņ	n	2 3	3 3	3
Test limits		Max							0.4	3	3 3	з	23	-1.5	"	31		. "	4	- C.D	-1.5	-0.5	-1.6	. "	: 3	-3.2	-3.2	9.1-	-1.6	-3.2	40	: 3	,,	100	"	3 :	"	80	080	200	"	"	-200	-850	-/00
Ė		Min	2.4	n	n	n	"	n															-0.7	: 3	: 3	-1.4	-1.4	-0.7	-1.4	-1.4													-20	-200	-50
	Meas.	terminal	Ø	<u>0</u>	<u>0</u> 1	Q2	<u>a</u> 2	<u>Q</u> 2	Ω	<u>0</u> 1	Q1	2 10	2 00	77	J2	K1	K2	Clear 1	Clock 1	Close	Clock 2	Clock 2	J1	K1	JZ K2	Clock 1	Clock 2	Clear 1	Clear 2	Clear 2	J1	K1	52 K2	J1	K1	J2	K2	Clear 1	Clear 2	Clock 1 Clear 1	Clock 2	Clear 2	Clock 1	Clock 1	Clock 2 Clock 2
14	14	J1	2.0 V	0.8 V					0.8 V	2.0 V				-12 mA					7 5 7	v. 0.			0.4 V			4.5 V		4.5 V	4.0 V		2.4 V			5.5 V				GND	2	OND CND			GND	GND	
13	13	10		4 mA	4 mA					16 mA																																		Ī	
12	12	ğ	4 mA						16 mA		16 mA																																	1	
17	11	GND	GND		,	,,,	,	*	,	*	3 3	×	33	3	"	и :		. "	, ,	"	"	"	я :	: 3	: 3	"	,,	3 3	3	"	и :	. "	"	"	"	3 :	"	3 3	: :	: 3	"	"		3 3	3
10	10	K2				0.8 V	V 0.:				\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	0.8 V					-12 mA					0.8 V			0.4.V		4.5 V						2.4 V				5.5 V				GND			CIV	GND
6	6	Q2				4 mA					16 20	-	16 m A	5			-					0					4										4)								
-		6				4	hA	υĄ			2,		+	2																														1	$\frac{1}{1}$
8	8	IQ				1	/4 mA	4 mA				/ 16 mA			Υı							/			_		/					,				,						0			
7	7	2 J2				2.0 V	0.8 \				λα ο	2.0 V			-12 mA							4.5 V		+	0.4 V		4.5 V		+	4.5 V		7 7 7	-			5.5 V		6	GND			GND		_	GND
9	9	ö						0.8 V					> 80	2						12 m	┿	4.5 V			4.5 V	2	В		0.4 V	0.4 V			B	1		GND	Ф	L	п		5.5 V	ш		u	2.4 V
2	2	Clock 2				Α	٧				<	< <									-12 mA	*A		ì	ير او	õl	0.4 V		4.5 V	4.5 V			OND OND	5		GND	GND	ć	GND		5.5 V	GND		7 4 7	2.4 V
4	4	Vcc	4.5 V	*	3	n	,,	3	3	3	3 3	3	3	3	и	я :	: :	: 3		n	"	n	5.5 V	: 3	: 3	3	"	3 3	3	"	5.5 V	: 3	n	я	"	3 :	,	3 3	: :	: :	n	n	3 :	3 3	"
8	3	K1	0.8 V	2.0 V					2.0 V	0.8 V						-12 mA			Λα Ο	0.0				0.4 V		4.5 V						2.4 V			5.5 V				2	GND			GND	GND	
2	2	Clear 1			0.8 V						0.8 V							-12 mA	757	v C.4			4.5 V	4.5 V		В		0.4 \	V 4.0		GND	a		GND	В			ш	i	5.5 V E			ш	2.4 V	
1	1	Clock 1	Α	٧					A	٧								40 00 1	-12 mA	ζ			2/	ای/		0.4 V		4.5 V	4.5 V		GND	GND		GND	GND			GND	, , , ,	5.5 V GND			2.4 V	2.4 V	
Case A. B. D	Case C	Test No.	+	2	8	4	2	9	7	8	9	11	12	13	14	15	16	1/	18 CKT B	10 CN 0	20	20 CKT B	21	22	23	25	26	27 CKT A, C	28 CKT A.C.	28 CKT B	29	30	32	33	34	35	36	37	38	39	41	42	43 CKT A, C	43 CKT B	44 CKT A, C 44 CKT B
MIL-	STD-883	method	3006	n	n	,,	29	×	3007	"	3 3	я	77										3009	: 3	: 3	3	"	3 3	3	"	3010	: 3	и	3	"	3 :	,,	3 3	: :	: 3	33	и	× :	3 3	35
Symbol	,		V	n	**	"	"	3	NoL	n	3 3	3	"	Vic	,,	"	: 3	:	3	3	"	"	μΠ	: 3	: :	6111	211	IL3	31	99	1H1	: 3	"	<u>H</u>	33	2	,,	1 _{IH3} <u>7</u> /	// EHI	, "H4	3	"	l _{IH5}	3 3	3
Subaroup			_	$T_C = 25^{\circ}C$	3	39	,	,	"	,,	3 3	"	31	*	39	"	: 3	:	n	"	"	"	2 3	: 3	: 3	3	"	3 3	"	"	31	: 3	,,	31	n	2	"	3 3	: 3	: 3	"	"	99	3 3	, 9

See notes at end of device type 02.

TABLE III. Group A inspection for device type $\overline{02}$. $\underline{1}$ - Continued.

		Onit	mA	з	"	3	и																																		T			Ī	T	
Test limits		Max	-57	,,	n	3	40			1 or L	s shown 3/	"	,,	=		: 3	n	"	25	25	31	,,,	n	*	я :	,		3 3	"	"	3	,,,	n	: :			=	s s	: :	. :	: :	3	: 3	"	3	
Ā		Min	-20	25	n	3					as a																																			
	Meas.	terminal	10	Ø	Q2	Q 2	Vcc			All	output	я	2	31	= :	: 3	"	n	"	"	*	"	"	z	3	"	= :	: :	3	*	"	3	"	3 3	: 3	: 3	= :	: :	: :	: 3	: 3	33	: 3	3	3	
14	4	L L	2.4 V	4.5 V			4.5 V			⋖	∢	A	A	¥	∢ .	∢ ⊲	< <	A	A	A	٧	В	В	В	В	В	ω (m <	۷ ۵	. ≺	В	В	В	∢ .	∢ (я (ω (ω <	۷.	۱ ک	<u>α</u>	> ۵	∢ <	< <	< <	:
13	13	۵ 1	GND							Н3/	I	I	I	I	Τ:	I I	-	_	I	I	7	7	7	7	I	I	<u> </u>	T	c				т	= :	-	I :	Ξ.	_ -	١.	_ _ -	_		-		_ _ _	<u>-</u>
12	12	۵1		GND						L 3/		7	٦		_ 	_ _	, ,	I	7	7	ェ	I	I	I		7	4		J _	ı	I	I	L				_ :	= :	r :	ı:	-	-		c 1	c _	<u>-</u>
1	1	GND	GND		**	3	11			GND	n	,,	,,	,	a :	: 3	,,	33	"	3	3	,,	n	3	3 :		s :	2 2	3	"	3	,,	n	* *		: :	s :		: :			33	: 3	"	-	-
10	10				0 \	2.4 V	GND				В	В	Α	V	Α.	∢ ላ	< <	∢	A	A	V	В	В	В	В	В	<u>в</u>	ω α	0 60	В	A	A	Α	۷,	∢ •	∢ (<u>в</u>	ω <	¥ (m (20 0	۵ ۵	<u>α</u> α	۵ ۵	0 00	-
σ	ာ တ	02			GND					L 3/		7		7	7		, <u>T</u>	I	_	7	ェ	н	I	I			_		J _	ı	ェ	I		7.	_ -	_	_ _]:	I	r :	= :	-	-	_	c 1		-
α	ο &	IQ 2				GND				Н3/	I	I	I	I	-	I I	-	_	I	I	7	7	7	٦	I	ı	<u> </u>	T 3		-	_	_	I	= :	-	r :	-	_	_	_	_ -		r _	_ 	_ _ _	<u>-</u>
7	,	JZ			4.5 V		4.5 V					A	A	A	Α.	∢ ⊲	. A	4	A	A	A	В	В	В	В	В	а (a <	4	. A	В	В	В	Α,	∢ (9	а (ω <	∢ .	۱ ک	20 0	٥ <	∢ <	4 <	۲ ۵	<u>-</u>
9	9	Clear 2			4.5 V 4		4.5 V 4	d.	j.	В	В	В	В	m	В.	4 4	. <	V	A	A	4	A	A	A	В	V.	Α,	⋖ <	4	. 4	A	A	A	а.	⋖ <	۷.	Α,	< <	۷.	۷,	∢ <	(<	∢ <	₹ 4	K 80	<u>-</u>
	2				GND 4.		D 4.	s are omitte	-55°C and V _{IC} tests are omitted.		1	8	8	_	ω .	m d		_	~	-	·	3	1	~	~	m .		m .	0 4		~	_	3	7.		7		m -	-		10	0 -	1 0	0 -		-
F	+-		>					nd V _{IC} test	nd V _{IC} tests	> =										1			1				-							,		,							,	_		
F	3 6		V 5.5 V	, 0	**	=	" GND	; = 125°C a	; = -55°C a	3 4.5	. В			, V			, A	* *		, V		" B			* B	<u> </u>			0 0	* B	, V	* <	, Н	Α.	Α .	V	. ·	 M <	K I	· · ·	 	0 0	200	- 0 a	- - 	= 125°C a
-	2 2	_	GND 2.4	4.5 V (4.5 V G	, except T _c	, except T _C			В				V 4			\ \			A			В			Α <		. A			/ /			Α.			-	_					K 8	. except T
_		ok 1 Clear						subgroup 1	subgroup 1																													1								subgroup 7
-	-	Clock	2.4 V	A			D	mits as for	mits as for	В	4	В	В	A	ш	B ⊲	(A	4	В	A	ш	В	A	В	В	ш		ω α		В	ш	A	В	Α,	∢ <	Α.	۷ (ω <	Α.	∢ •	< α		∢ α	۵ ۵		mits as for
Case A B	Case C	Test No.	45	46	47	48	49	Same tests, terminal conditions and limits as for subgroup 1, except $T_{\rm C}$ = 125°C and $V_{\rm IC}$ tests are omitted.	Same tests, terminal conditions and limits as for subgroup 1, except $T_{\rm C} =$	20	51	52	53	54	55	57	28	26	09	61	62	63	64	92	99	29	89	69	71	72	73	74	75	76	77	8/	79	80	81	82	83	40	82	90	ر 88	Same tests, terminal conditions and limits as for subgroup 7, except T _C = 125°C and -55°C.
- IIW	STD-883	method	3011	3011**	3011**	3011	3002	terminal co	terminal co																																					terminal co.
lodmyS	5		sol	n	**	3	201	Same tests,	Same tests,																																	l		†		Same tests,
Clibarding	5		1 T _c = 25°C		77	3	29	2	3	7 2/ 4/	$T_{\rm C} = 25^{\circ}{\rm C}$		n		= :	: :	"	n	"	"	39	n	11	×	77	"	= :	= =	77	37	"	39	11	2 3	: 3	: :	= :	= =	: :	: 3	: 3	"		"	3	8 2/ 4/

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02, 1/ - Continued.

		.=	Z																Z										
nits	L		MHz	"	n	3	"	*	3	3	3	*	3	*	3	3	3	3	"MHz	3	n	su	*	"	3	n	3	n	3
Test limits	:	Max					25	25	40	40	30	ä	3	3	40	3	3	3				38	39	20	20	36	3	3	3
		Ξ Wi	10	'n	я	=	2	3	3	3	3	3	3	3	3	4	3	3	10	3	3	2	3	3	3	3	3	3	3
	Meas.	terminal	ά	<u>0</u>	O ₂	Q 2	Clear 1 to ∑ 1	Clear 2 to $\overline{\mathbb{Q}}$ 2	Clear 1 to Q1	Clear 2 to Q2	Clock 1 to Q1	Clock 1 to Q 1	Clock 2 to Q2	Clock 2 to Q 2	Clock 1 to Q1	Clock 1 to Q 1	Clock 2 to Q2	Clock 2 to Q 2	2 او	5 8	Q 2	Clear 1 to Q 1	Clear 2 to $\overline{\mathbb{Q}}$ 2	Clear 1 to Q1	Clear 2 to Q2	Clock 1 to Q1	Clock 1 to Q 1	Clock 2 to Q2	Clock 2 to Q 2
14	14	۲	2.4 V	2.4 V			2.4 V		2.4 V		2.4 V	2.4 V			2.4 V	2.4 V			2.4 V			2.4 V		2.4 V		2.4 V	2.4 V		
13	13	۱۵ 1		OUT			OUT					OUT				OUT			OUT			OUT					OUT		
12	12	δ	OUT						OUT		OUT				OUT				OUT					OUT		OUT			
11	11	GND	GND	"	n	2	3	n	39	3	2	79	"	n	31	"	39	n	"	*	39	3	"	3	3	я	*	я	3
10	10	¥			2.4 V	2.4 V		GND		GND			2.4 V	2.4 V			2.4 V	2.4 V		2.4 V	2.4 V		GND		GND			2.4 V	2.4 V
6	6	Q2			OUT					OUT			OUT				DOUT			TUO					DOUT			DOUT	
8	œ	IQ 2				TUO		DOUT						DOUT				DOUT			OUT		DOUT						TUO
7	7	75			2.4 V	2.4 V		2.4 V		2.4 V			2.4 V	2.4 V			2.4 V	2.4 V		2.4 V	2.4 V		2.4 V		2.4 V			2.4 V	2.4 V
9	9	Clear 2						Z		Z			5.0 V	5.0 V			5.0 V	5.0 V					Z		z			5.0 V	5.0 V
2	2	Clock 2			Z	Z		Z		Z			Z	Z			Z	<u>z</u>		Z	Z		Z		Z			Z	Z
4	4	% \	5.0 V	,,	n	3	3	3	3	×	3	3	3	3	¥	*	3	3	3 3	3	3	3	3	n	3	3	=	3	*
က	က	조	2.4 V	2.4 V			GND		GND		2.4 V	2.4 V			2.4 V	2.4 V			2.4 \ 2.4 \			GND		GND		2.4 V	2.4 V		
2	5	Clear 1					Z		Z		5.0 V	5.0 V			5.0 V	5.0 V						Z		Z		5.0 V	5.0 V		
-	_	Clock 1	Z	Z			롣		Z		Z	≧			Z	Z			ZZ			≧		Z		Z	롣		
Case A, B, D	Case C	Test No.	88	06	91	95	66	94	92	96	26	86	66	100	101	102	103	104	105 106	107	108	109	110	111	112	113	114	115	116
MIL-			(Fig 7)	31	3	3	3003 (Fig 6)	3	3	z	3003 (Fig 7)	3	3	3	з	2	ä	3	(Fig 7)	3	3	3003 (Fig 6)	3	3	3	3003 (Fig 7)	3	3	3
Symbol			F _{MAX} 6/	"	n	z	1 ф∟н1	tр∟нл	€ РНL1	t РНL1	^t РLH2	z	3	3	€РН∟2	3	ä	3	F _{MAX} <u>6</u> /	3	3	tР∟нл	≀н⊓а	t РН∟1	t РНL1	^t РLH2	3	3	3
Subgroup			6	$T_{\rm C} = 25^{\circ}{\rm C}$	77	4	3	3	3	3	z	:	ä	2	3	3	n	2	10 T _C = 125°C	"	3	3	"	25	25	3	3	3	3

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02. 1/ - Continued.

													5°C.	cept T _C = -5	roup 10, exc	as for subg	Same tests, terminal conditions and limits as for subgroup 10, except $T_c = -55$ °C.	s, terminal cor	Same test	
		to Q 2																		
,, ,,	"	Clock 2				"	2.4 V		TUO	2.4 V	2.0 V	Z	,				120	n	,,	
		to Q2																		
n n	,,	Clock 2				"	2.4 V	OUT		2.4 V	2.0 V	Z	,,				119	"	*	
		to 0																		
3	3	Clock 1	2.4 \	_ L∩o		3							3	2.4 V	5.0 V 2.4 V	Z	118	3	3	
		to Q1																		
20 us	2	Clock 1	2.4 V		OUT	GND							5.0 V	5.0 V 2.4 V	5.0 V	N	117	3003	t _{PHL2}	
Max Unit	Min	terminal	J1	<u>0</u>	DQ	GND	K2	Q2	Q ₂	J2	Clear 2	Clock 2	Vcc	K1	Clear 1	Clock 1	Test No.	method		
		Meas.	14	13	12	11	10	6	8	7	9	5	4	3	2	1	Case C	STD-883		
Test limits	<u>"</u>		14	13	12	11	10	6	8	7	9	2	4	3	2	1	Case A, B, D		Subgroup Symbol	

NOTES:
A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
C = This note has been deleted.
D = Momentary 4.5 V, then GND.
E = Momentary ground, then 2.4 V.
F = Momentary ground, then 5.5 V.
J = This note has been deleted.

* After clock pulse apply $-12\,\mathrm{mA}$ to clock pin to insure \overline{Q} is still in the low state (see figure 15).

** Test time limit \leq 100 ms.

1/ Terminal conditions (pins not designated may be H≥ 2.0 V, or L≤ 0.8 V, or open.)
2/ Input voltages shown are. A = 2.0 V minimum and B = 0.8 V maximum.
3/ Youthy voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
4/ Tests shall be performed in sequence.
5/ Input shall be one normal clock pulse, then 4.5 V
6/ Final war, minimum limit specified is the frequency of the input pulse. The output frequency shall ge one-half of the input frequency.
1/ For CKT A, I_{H3} limits are 0 to 120 µA.

TABLE III. Group A inspection for device type 03. 1/

	ı			l							ı		П	1	1		П	1		1	1			-	1	_	1		П		1	1		-	-		_		П	,	,		_	$\overline{}$	П
S	Unit	^	"	3	"	n	"	n	n	n	39	3	"	3 3	"	"	"	3	, ,	2	"	mA	"	3 3	: 3	"	"	29	"		m,	"	"	:	: :	: :	"	"	"	n	"	3 3	"	"	27
Test limits	Max							0.4	"	n	¥	3	"	-1.5	"	3	"	3	4.5	5 7	-0.5	-1.6	"	3 3	: 0	2.5	-3.2	-3.2	-1.6	-3.2	04,	"	"	100	: :	: :	Ö	80	200	n	n	, 200	-850	-200	-850
	Min	2.4	я	3	n	n	3															-0.7	n	: :	104	1.25	-0.7	-1.4	-0.7	-1.4												50	-30	-20	-80
	Meas. terminal	Ω1	<u>Ω</u>	1Q 1	Q2	<u>0</u> 2	Q 2	۵1	۵ 1	۵1	Q2	QI 2	Q2	7 2	J2	K2	Clear 1	Clock 1	Clock 1	Clock 2	Clock 2	J1	X	J2	K2	Clock -	Clear 1	Clear 1	Clear 2	Clear 2	5 X	75	K2	٠ ا	K1	72	Clear 1	Clear 2	Clock 1	Clear 1	Clock 2	Clear 2	Clock 1	Clock 2	Clock 2
14	Vcc	4.5 V	3	3		*		"		n		3		3	77		n		=	,,	,,	5.5 V	"	3 3	: 3	"		"	"	3 3		"	,,			= =	"	31	п	n	"	3 3	3	3	з
13	Clear 1			0.8 V						0.8 V							-12 mA		4.5 V			4.5 V	4.5 V		٥	۵	0.4 \	0.4 V		2	GND B)		GND	a		ш	J	GND	ш		CINC	OND OND	:	
12	Clock 1	Α	A					Α	٧									-12 mA	* *			2/	2/		7 7 7	V 4.0	4.5 V	4.5 V			GND	5		GND	GND		CIND	5	5.5 V	GND		247	2.4 V	i	
11	ξŽ				0.8 V	2.0 V					2.0 V	0.8 \				-12 mA					0.8 V				0.4 V	157	v. C:						2.4 V			7 2 2	v C.C				GND			GND	GND
10	Clear 2						0.8 V						0.8 V						12 m	VII 71	4.5 V			4.5 V	4.5 V	۵	۵		0.4 V	0.4 V		GND	В			GND	۵	Ш			GND	ட		GND	GND
6	Clock 2				Α	A					∢	∢								-12 mA	* *			ίΩ ί	2/	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	v +:-		4.5 V	4.5 \		GND	GND			GND		GND			5.5 V	GND		2.4 V	2.4 V
8	JZ				2.0 V	0.8 V					0.8 V	2.0 \			-12 mA						4.5 V			0.4 V		7 5 7			4.5 V	4.5 V		2.4 V				5.5 V		GND			GND	GND		GND	GND
7	GND	GND	"	3	n	39	7	n	"	"	3	3	"	2 2	33	"	99	3	: :	3	n	33	n	3 3		"	n	"	"	3 3		33	39 :	: :	: :		'n	3	и	n	n	3 3	n	3	39
9	IQ 2					4 mA	4 mA					16 mA		Ì																												Ť		Ī	
2	Q2				4 mA						16 mA		16 mA																													Ì			
4	조	0.8 V	2.0 V					2.0 V	0.8 V					, C	¥1171-				0.8 V				0.4 V		4 5 7/	v C:4					247				5.5 V				GND			CNC	GNB	;	
က	۵1	4 mA						16 mA		16 mA																																Ī			
2	ıα		4 mA	4 mA					16 mA																																				
1	J.	2.0 V	V 8.0					0.8 V	2.0 V					-12 mA					4.5 \			0.4 V			7 5 7	V C.4	4.5 V	4.5 V		2 7 7	V 4.7			5.5 V			CIND	5	GND	GND		CNC	GND	;	
Case C	Test No.	1	2	3	4	2	9	7	8	6	10	-	12	13	15	16	17	18	18 CKT B	200	20 CKT B	21	22	23	24 26	97	27 CKT A. C	27 CKT B	28 CKT A, C	28 CKT B	30	31	32	33	34	35	30	38	39	40	41	42	43 CKT B	44 CKT A, C	44 CKT B
MIL-	STD-883 method	3006	77	77	"	**	"	3007	7	n	з	3	39									3009	29	= =	: 3	"		39		* 00	3010	3	39	: :	: :	, ,	3	*	n	"	3	3 3		y	33
Symbol		V _{ОН}	29	3	39	31	3	Vol	31	,,	3	3	"	V _{IC}	31	ņ	n			77	3	1111	"	3 3	-	112	112	23	"	3 -	E .	33	3	HZ.	: 3	3 3	/2	I _{IH3} 7/	I _{IH4}	,	=	3	, H2	"	=
Subgroup		1	$T_C = 25^{\circ}C$	3	29	3	3	"	3	з	3	3	я	3 3	3	*	n	2	3 3	75	3	3	"	2 3	: 3	"	*	,,	n	3 3	: 3	3	"	: :	: :	: :	3	2	77	"	3	2 2	3	3	9

See notes at end of device type 03.

TABLE III. Group A inspection for device type 03. 1/- Continued.

See notes at end of device type 03.

TABLE III. Group A inspection for device type 03. 1/- Continued.

	Unit		MHz	3	,,	"	ns	3	,,	ıı	ns	3	,,	3	,,	3	,,	3	MHz	3	,,	ä	ns	3	,,	11	ns	3	11	3	,,	3	,,	z	
Toot limits			_				25	25	40	40	30	3	"	n	40	n	"	n					36	39	20	20	39	3	n	n	20	,	"	3	
F	Min		10	3	,,	3	2	3	"	11	2	2	"	3	"	3	"	n	10	3	"	"	2	я	n	"	2	3	n	3	"	3	"	a a	
	Meas.	terminal	Q1	ıα	Q2	IQ 2	Clr 1 to \overline{Q}_1	Clr 2 to $\overline{\mathbb{Q}}_2$	Clr 1 to Q1	Clr 2 to Q2	Clk 1 to Q1	CR 1 to Q	Clk 2 to Q2	Clk 2 to $\overline{\mathbb{Q}}_2$	Clk 1 to Q1	Clk 1 to Q 1	Clk 2 to Q2	Clk 2 to $\overline{\mathbb{Q}}_2$	Ω1	ıα	Q2	OI 2	Clr 1 to Q 1	Clr 2 to $\overline{\mathbb{Q}}_2$	Clr 1 to Q1	Clr 2 to Q2	Clk 1 to Q1	CR 1 to Ql	Clk 2 to Q2	Clk 2 to Q 2	Clk 1 to Q1	Clk 1 to Q 1	Clk 2 to Q2	Clk 2 to $\overline{\mathbb{Q}}_2$	
-	<u>†</u> \	20.	5.0 V	3	,,,	39	*	*	"	n	×	3	n	39	n	39	n	"	11	3	"	"	ä	×	n	n	n,	3	n	*	"	,,	"	n	
0,	Clear 1	200	5.0 V	5.0 V			Z		N		5.0 V	5.0 V			5.0 V	5.0 V			5.0 V	5.0 V			Z		Z		5.0 V	5.0 V			5.0 V	5.0 V			
,	Clock 1		Z	Z			⋖		Α		Z	Z			Z	Z			Z	Z			∢		Α		Z	Z			N	Z			
7	- X	7			2.4 V	2.4 V		GND		GND			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V		GND		GND			2.4 V	2.4 V			2.4 V	2.4 V	
	Clear 2	2 12 2			5.0 V	5.0 V		z		Z			5.0 V	5.0 V			5.0 V	5.0 V			5.0 V	5.0 V		z		Z			5.0 V	5.0 V			5.0 V	5.0 V	
	Clock 2				N	Z		∢		Α			Z	Z			Z	Z			N	Z		∢		Α			Z	z			N	Z	
	. 12 C				2.4 V	2.4 V		2.4 V		2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V		2.4 V		2.4 V			2.4 V	2.4 V			2.4 V	2.4 V	
-	GND	j	GND	3		3	*	3	,,,		2	2	,	3	n	"		*	n	2	, ,	*	3	2	n	,	я	3	,	3	,,,	"	, ,	,	
-	P 10	0 ₂				OUT		OUT						OUT				OUT				OUT		OUT						OUT				OUT	
-	20	4			OUT					OUT			OUT				OUT				OUT					OUT			OUT				OUT		
	t 7	2	2.4 V	2.4 \			GND		GND		2.4 V	2.4 \			2.4 V	2.4 V			2.4 V				GND		GND		2.4 V	2.4 V			2.4 V	2.4 V			55°C.
c	, <u>o</u>		OUT						OUT		OUT				OUT				OUT						OUT		OUT				OUT				except T _C =
c	7 10	o L		DOUT			OUT					TUO				OUT				OUT			OUT					TUO				OUT			group 10, e
-	- 5	5		2.4 \			2.4 V		2.4 V		2.4 V				2.4 V				2.4 V				2.4 V		2.4 V		2.4 V				2.4 V				as for sub
0	Test No.		88		91	92		94	36				66	100	101		103		105		107	108	109	110				114	115	116			119	120	Same tests, terminal conditions and limits as for subgroup 10, except $T_{\rm C}$ = -
-																			/9		,										,		,		al condition
N	STD-883	method	(Fig. 7) <u>6</u> /	3	"	3	3003 (Fig. 6)	3	"	33	3003	(Fig. 7)	n	3	n	3	n	3	(Fig. 7)	3	"	3	3003 (Fig 6)	3	n,	"	3003	(Fig 7	n	3	"	3	"	3	sts, termina
o demis	2		F _{MAX}	*	"	,,	фгн	t _{РLН}	t _{PHL}	t _{PHL}	t _{PLH}	*	3	,,	tPHL	,,	3	*	F _{MAX}	3	"	7	ф⊩н	t _{РLН}	t _{PHL}	t _{PHL}	t _{PLH}	3	"	,	t _{PHL}	"	"	2	Same te
di care	dpoisons		6	$T_C = 25^{\circ}C$	77	"	3	n	n	"		2	3	"	3	"	3	*	10	T _C = 125°C	11	"	"	39	"	"	3	=	3	,,	n	,	n	ĸ	11

See notes at end of device type 03.

* After clock pulse apply -12 mA to clock pin to insure \overline{Q} is still in the low state (see figure 15). A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
C = This rome has been deleted.
D = Momentary 4.5 V. then GND.
E = Momentary ground, then 2.4 V.
F = Momentary ground, then 5.5 V.

** Test time limit ≤100 ms.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
4/ Tests shall be performed in sequence.
5/ Ontput normal clock pulse, then 4.5 V.
5/ The normal clock pulse, then 4.5 V.
5/ The output frequency shall be one-half of the input frequency.
7/ For CKT A, I_{Hz} limits are 0 to 120 µA.

46

ABLE III. Group A inspection for device type 04. 1/

	Unit	>	3	3	*	n	3	31	*	n	3	n	3	: :	:		= :	= 3	: 3	"	*	"	"	n	,	,	ΨΨ,	,,	,,	3		3	,,	,	3 3	: 3	3	u	3	μĄ	: 3	: 3	n	я	3 3	1
Test limits	Мах									0.4	3	"	3 :		n		; !	-1.5	: 3	,,	3	ņ	n	n	,,	a .	9.1-	"	"	-3.2	2 2	,	-1.6	-3.2	-1.6	3.5	-3.2	-1.6	-3.2	40	: 3	: 3	100	3	3 3	1
Ι'	Min	2.4	,	3	,,	"	,	3	,,																	1	-0.7	n	"	-1.25	3 3	3	-0.7	-1.4	-0.7	4.T-	-1.4	-0.7	-1.4							
	Meas. terminal	۵1	Ω 1	10	δ	Q2	<u>Q</u> 2	Q 2	Q2	۵1	۱۵ ۲	Ω 1	۵1	Q2 = 0	Σ I0	2 2	Q2 ::	J.	Σ <u>Σ</u>	7 CX	Clock 1	Preset 1	Clear 1	Clock 2	Preset 2	Clear 2	۲ X	JS	K2	Clock 1	Clock 1	Clock 2	Clear 1	Clear 1	Preset 1	Preset 1	Clear 2	Preset 2	Preset 2	J.	Σ <u>τ</u>	J2 K2	7 5	. X	J2 K2	1.14
16	K1	0.8 V	2.0 V							2.0 V	0.8 V								-12 mA								0.4 V			4.5 V	4.5 V		4.5 V	4.5 V	4.5 V	4.5 V					2.4 V			5.5 V		ĺ
15	۵1	4 mA			4 mA					16 mA			16 mA																																	1
14	۵ 1		4 mA	4 mA							16 mA	16 mA																																		
13	GND	GND	"	"	31	,,	"	"	31	,,	z	"	,,	: :	*		= :	= 3	: 3	n	3	n	n	я	3	3 3	: :	n	,,	3	3 3	3	"	n	3 3	: 3	31	"	3 :	= :	: 3	: 3	я	я	3 3	
12	K2					0.8 V	2.0 V							2.0 V 0.8 V						-12 m A	101171								0.4 V		157	4.5 V				757	757	4.5 V	4.5 V			747	v t.7		557	,
11	O2					4 mA			4 mA					16 mA			16 mA																													
10	₫ 2						4 mA	4 mA						16 mA	16 mA																															
6	J2					2.0 V	0.8 V							0.8 V					40 00	VIII 71 -								0.4 V			157	4.5 V				157	45.7	4.5 V	4.5 V			2.4 V			5.5 V	
8	Clear 2							0.8 V	2.0 V						2.0 V		0.8 V									-12 mA		В	4.5 V			В				\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	0.4.0					GND			GND	
_	Preset 2							2.0 V	0.8 V						0.8 \		2.0 V								-12 mA				В		α	3						0.4 V	0.4 V			CINC	وَ		CNS	<u>.</u>
	Clock 2					Α	A							∢ ∢										-12 mA				4.5 V	4.5 V		7 7 7	0.4 V				757	7.5.4	4.5 V	4.5 V		2	ON C	֖֖֝֝֝֝֝֝֝֝֝֝֝֝֝֝֝֝֝ ֓֞֞֓		GND	į
2		4.5 V	"	19	n	n	"	"	n	n	3	"	3 9	: :	"		= :	= 3	. "	n	n	n	n	я	n	"	7 9.5	n	11	я	, ,	3	"	"	3 3	: 31	"	"	3 .	= :		: 3	n	n	3 3	
4	JJ	2.0 V	V 8.0							0.8 V	2.0 V							-12 mA									0.4 V			4.5 V	4.5 V		4.5 V	4.5 V	4.5 V	4.5 V				2.4 V			5.5 V	,		
3	Clear 1			0.8 V	2.0 V							2.0 V	0.8 \										-12 mA			1	B 4.5 V				В		0.4 V	0.4 V					!	GND			GND	<u>)</u>		
2	Preset 1			2.0 V	0.8 V							0.8 V	2.0 V									-12 mA					а	1		В					0.4 \	0.4 \					GND			GND		
	Clock 1	A	٧							A	∢										-12 mA						4.5 V 4.5 V			0.4 V	0.4 V		4.5 V	4.5 V	4.5 V	4.5 V				GND	GND		GND	GND		
Case E & F	Test No.	1	7	က	4	5	9	7	8	6	10	11	12	13	15		16	45	18	61	21	22	23	24	25	26	27	29	30	31	32	34	35 A, C	32 B	36 A, C	30 B	37.B	38 A, C	38 B	39	40	41	43	44	45 46	>
MIL-	STD-883 method	3006	3	"	3	77	3	3	3	3007	ä	n	я :	: :	3		:										3006	3	n	3	3 3	3	"	"	3 3	: 3	я	3	"	3010	: 3	: 3	×	я	3 3	
Symbol		V _{ОН}	*	n	"	77	"	3	"	Vol	3	*	2 :	: "	,,	3	* ;	V _{IC}	: 3	"	"	"	"	"	,,	× .	1111	"	n	1112	3 3	31	ILI3	"	3 3	: 3	"	2	3 .	IH1	: :	: 3	1	,, ,,	" "	
Subgroup		1	$T_{\rm C} = 25^{\circ}{\rm C}$	3	*	"	3	3	*	"	3	3	3 :	: :	*		2 3	: 3	: 3	"	,	,,	39	39	,	3 3	: :	33	и	27	3 3	3	"	n	3 3	. 3	27	27	3 :	: :	: 3	: 3	"	я	2 2	

See notes at end of device type 04.

TABLE III. Group A inspection for device type 04. 1/ - Continued.

Γ	Unit	η	"	"	"	"	"	*	n	n	n	n	'n	n	11	mA	*	,,	×	n	71																						
Test limits	Max	160	11	"	"	200	"	,,	"	n	n	-200	-850	-200	-850	-22	39	n	"	40	40			HorL	as shown 3/	"	n	3	. "	35	n	n	n	"	n	3	я	×	3 3	n	n	"	"
ř	Min											-20	-200	-20	-200	-20	"	n,	"						as																		
	Meas.	Clear 1	Preset 1	Clear 2	Preset 2	Clear 1	Preset 1	Clear 2	Preset 2	Clock 1	Clock 2	Clock 1	Clock 1	Clock 2	Clock 2	Q1	<u>0</u> 1	Q2	<u>Q</u> 2	V _{CC}	Vcc			All	output		-			-	=	-	-		=		-			=	=	=	-
16	X	4.5 V	GND			4.5 V	GND			GND		GND	GND			2.4 V	2.4 V			GND	GND			В	В	В	A	∢ .	∢ <	< ⊲	Α Α	٧	٧	Α	В	В	В	В	<u>а</u>	<u>α</u>	o a		ω α
15	Ø															GND								F3/	J	7	7	_	_ =	= =	ī	I	I	I	I	I	I	_	_	_		-	I
14	10																GND							/E H	I	I	I	Ι:	Ι-	_		_	_	٦	٦	٦	٦	I	I	c 1	<u> </u>	I	
13	GND	GND	n	"	н	11	"	"	"	"	"	"	"	"	,,	n	"	n	"	"	"			GND	"	п	n	= :	: 3	3	n	"	"	п	n	"	и	"	= =	"	"	,,	"
12	SZ.			4.5 V	GND			4.5 V	GND		GND			GND	GND			2.4 V	2.4 V	GND	GND			В	В	В	٧	∢ .	∢ <	(∢	< <	۷	۷	Α	В	В	В	В	а с	0 α	a a	<u>د</u>	В
11	07																	GND						F <u>3</u> /	L	L	L	٦.	7	I	н	I	I	Н	н	I	Н	٦	_ -	7 _		_	ı
10	<u>Q</u> 2																		GND					H 3/	I	I	I	Ι:	Ι-		1	_	_	٦	٦	_	_	I	Ι:	c 1	=	I	:
6	JZ			GND	4.5 V			GND	4.5 V		GND			GND	GND			2.4 V	2.4 V	GND	GND			A	Α	Α	A	۷.	Α <	< ⊲	Α .	В	В	В	В	В	В	В	<u>а</u>	<u>α</u>	ο «	. ⋖	Α.
8	Clear 2			В				ь			GND			GND	GND			4.5 V	GND	GND	4.5 V			В	В	В	В	а	æ <	< ⊲	. Α	٨	٨	Α	A	٧	A	В	< <	۲ ⊲	< <	. ⊲	< <
7	Preset 2				В				ட									GND	4.5 V	4.5 V	GND	itted.	itted.	A	٨	Α	A	∢ .	∢ 0	2 60	<u>а</u>	В	В	В	A	4	4	٧	∢ <	< ⊲	< <	∠	< <
9	Clock 2			GND	GND			GND	GND		5.5 V			2.4 V	2.4 V			2.4 V	2.4 V	GND	GND	and V _{IC} tests are omitted.	sts are om	В	A	В	В	∢ (20 0	Δ 4	B	В	٧	В	В	٧	В	В	В	ζα	o a	۱۷	В
2	0	5.5 V	"	"	"	**	"	,,	"	"	"	"	"	"	**	"	"	n	3	"	"	and V _{IC} te	and V _{IC} tes	4.5 V	"	n	n		: "	"	"	"	"	**	"	×	×	×		"	"	,,	"
4	L L	GND	4.5 V			GND	4.5 V			GND		GND	GND			2.4 V	2.4 V			GND	GND	₅ = 125°C	= -55°C a	A	A	Α	A	∢ .	∢ <	< ⊲	< ∢	В	В	В	В	В	В	В	ω α	0 α	ο «	. ⋖	< <
3	Clear 1	В				Ь				GND		GND	GND			4.5 V	GND			GND	4.5 V	except T	except T	В	В	В	В	В	я <	۷ ۷	Α .	Α	Α	Α	Α	Α	Α	В	< <	۷ ۵	ζ 4	A	. A
2	Preset 1		Е				Ь									GND	4.5 V			4.5 V	GND	1 dnoub	1 dnoabqr	٨	٧	٧	٧	∢ .	۵ ک	2 60	В	В	В	В	٧	Α	Α	Α	∢ <	۷ ⊲	< 4	₹	< ≺
1	Clock 1	GND	GND			GND	GND			5.5 V		2.4 V	2.4 V			2.4 V	2.4 V			GND	GND	ts as for s	ts as for s	В	Α	В	В	Α (20 00	Δ 4	В	В	A	В	В	A	В	В	ω <	τ α	a a	۷	В
Case E & F	Test No.	47	48	49	50	51	52	53	54	55	26	57 CKT A, C	57 CKT B	58 CKT A, C	58 CKT B	** 69	09	61**	62	63	64	ditions and limi	ditions and limi	65	99	29	89	69	70	12	73	74	75	92	77	78	79	80	8 8	83	84	85	98
MIL-	STD-883 method	3010	n	27	"	31	"	n	"	"	77	3	"	"	n	3011	*	27	"	3005	3005	Same tests, terminal conditions and limits as for subgroup 1, except $T_{\text{c}} = 125^{\circ}\text{C}$	Same tests, terminal conditions and limits as for subgroup 1, except $T_C = -55^{\circ}C$ and V_{IC} tests are omitted.																				
Symbol	,	돼	n	n	n	IH4	n	"	"	3	3	H	z	"	n	sol	3	2	3	8	8_8	Same tests	Same tests,																				
Subaroup	-	-	$T_C = 25$ °C	11	и	**	11	n	"	37	37	"	3	"	27	"	,	**	,,	n	"	2	3	7 2/ 4/	$T_{\rm C} = 25^{\circ}{\rm C}$	"	3	2 :	: 3	"	,,	3	3	11	3	,	3	3	2 2	"	n	*	"

See notes at end of device type 04.

TABLE III. Group A inspection for device type 04. 1/- Continued.

	Unit																		MHz	*	"	33	su	3	z	*	3	3	×	3	su	3	2	3	3
400	Max	HorL	shown <u>3</u> /	: 3	n	"	"	n	и	n	31	3	3 3	. "	3	n	n						25	n	3	ä	40	2	z	2	30	3	z	3	40
	Min		as																10	*	n	"	Ŋ	ä	3	ä	3	2	3	2	2	3	3	3	3
	Meas. terminal	All	Output	: 3	3	,	"	"	3	3	3	3	3		3	"	"		0	10	Q2	<u>0</u> 2	Clear 1 to Q 1	Preset 1 to Q1	Clear 2 to $\overline{\square}$ 2	Preset 2 to Q2	Clear 1 to Q1	Preset 1 to $\overline{\mathbb{Q}}$ 1	Clear 2 to Q2	Preset 2 to $\overline{\mathbb{Q}}$ 2	Clock 1 to Q1	Clock 1 to Q 1	Clock 2 to Q2	Clock 2 to Q 2	Clock 1 to Q1
0	5 ∑	A	Α,	∢ ∢	< <	∢	Α	A	В	٧	∢	В	В	m <	(⊲	- A	В		2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V
7	5 5	H 3/	Ι.			ェ	Н	7	I	I	I	I	Ι.		J _	.	I		DOUT					OUT			TUO				OUT				OUT
	1 O	L <u>3</u> /	_ :	I	ı	7	7	ェ	I	_	_	_	_ :	=	- - -	· _	7			OUT			OUT					OUT				DOUT			
ć	GND	GND	# X	: 3	"	"	"	"	"	,,	"	31	3	: :	,,	,	,		GND	"	"	"	3	3	3	3	3	3	3	*	3	3	3	3	я
ç	2 Z	4	۷,	∢ ∢	. ⋖	⋖	Α	V	В	4	A	В	В	m <	۷ ۵	(B	В				2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V	
7	70	Н <u>3</u> /	Ι.			ェ	I	_	I	I	I	ı	Ι.		J _	J	I				OUT					OUT			OUT				OUT		
	01	\ \^		ıı	ı	_	7	I	ェ	_	٦		_ :		- 1	 -	7				H	OUT			OUT					OUT				OUT	
						_	1			_	_			_			_									>									
L				B A	-							Α .		+	-	a @					2.4 V	2.4			2.4 V	V 2.4 V				V 2.4 V				V 2.4 V	
	t 2 Clear 2	∢ .	Α,	A A	Α .	A	A	A	В	A	A	▼ ·	Α.	∀ <	(4	< <	A				>	>			Z	5.0 V				5.0 V				V 5.0 V	
-	2 Preset 2	¥.	Α.	∢ ∢	<	٧	A	A	В	В	⋖	∢ ·	Α.	∢ <	< ⊲	Α .	A				5.0	5.0 V			7 2.0 V	<u>Z</u>			2	Z			5.0 V	5.0 V	
: [ŏ		Α (m m	<	В	Α	В	4	∢	A	∢ •	۱ ۲	m <	۲۵	< <	В	5°C.	L		Z	Z			2.4 V	2.4 V			2.4 V	2.4 V			Z	Z	
	c Noc	4.5 V	# :	: 3	"	2	,,	"	я	3	3	3 :	s :	: 3	3	3	3	°C and -5	5.0 V		ä	3	3	3	2	3	3	3	3	3	3	3	3	3	3
_	ľ	В	В	m 4	< <	٧	Α	A	В	∢	A	∢	B (a <	τ α	a a	В	t T _C = 125	2.4 \	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V				2.4 V			2.4 V
c	1 Clear 1	∢ '	Α.	∢ ∢	<	∢	Α	A	В	A	⋖	∢ ·	Α.	∢ <	< ⊲	< ∢	A	о 7, ехсер					Z	5.0 V			Z	5.0 V			5.0 V	5.0 V			5.0 V
c	Preset 1	4	∢ ⋅	∢ ∢	<	4	Α	A	В	В	A	∢ ·	∢ ·	∢ <	< ⊲	<	∢	r subgroup	5.0 V	5.0 V			5.0 V	Z			5.0 V	Z			5.0 V	5.0 V			5.0 V
	Clock 1	В	۷ ۷	m a	<	В	Α	В	A	A	A	∢ .	∢ 1	a <	< 4	<	В	mits as for	Z	Z			2.4 V	2.4 V			2.4 V	2.4 V			Z	Z			Z
L	Test No.	87	88	68	91	92	93	94	92	96	97	98	66	100	101	103	104	ditions and lin	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121
	STD-883 method													1				Same tests, terminal conditions and limits as for subgroup 7, except $T_{\rm c}$ = 125°C and -55°C.	(Fig. 9)	N VOI	и	"	3003 (Fig 8)	×	3	3	a a	"	3	*	3003 (Fig 9)	34	3	*	n
O alone	ogiligo																	Same tests,	F	3	,,	*	фгнл	2	3	:	фнил	3	3	:	фгнг	3	3	3	фнг2
4.0	dpoisans	7 2/ 4/	T _C = 25°C	: 3	3	**	,,	11	3		ä	n :	= :	: 3	2	"	"	8 2/ 4/		$T_{\rm C}=25^{\circ}{\rm C}$,	75	3	2	3	2	2	3	3	3	3	3	3	*	з

See notes at end of device type 04.

TABLE III. Group A inspection for device type 04. 1/ - Continued.

	Unit	su	3	3	MHz	77	"	n	su	3	ä	3	×	z	3	z	su	3	3	3	3	3	3	n	
Test limits	Мах	40	3	3					39	3	9	3	20	3	3	a a	39	3	"	3	20	3	3	29	
j e	Min	2	ä	3	10	3	n	3	2	3	ä	3	3	3	3	3	2	"	3	3	3	3	3	n	
	Meas.	Clock 1 to Q 1	Clock 2 to Q2	Clock 2 to $\overline{\mathbb{Q}}$ 2	Q	۵ 1	Q2	<u>Q</u> 2	Clear 1 to Q 1	Preset 1 to Q1	Clear 2 to $\overline{\mathbb{Q}}$ 2	Preset 2 to Q2	Clear 1 to Q1	Preset 1 to $\overline{\mathbb{Q}}$ 1	Clear 2 to Q2	Preset 2 to $\overline{\mathbb{Q}}$ 2	Clock 1 to Q1	Clock 1 to Q 1	Clock 2 to Q2	Clock 2 to $\overline{\mathbb{Q}}$ 2	Clock 1 to Q1	Clock 1 to Q 1	Clock 2 to Q2	Clock 2 to $\overline{\mathbb{Q}}$ 2	
16	조	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			
15	ğ	OUT			OUT					OUT			OUT				OUT				OUT				
41	. IQ	OUT			H	OUT			TUO					TUO				OUT				TUO			
13	GND	GND	n	3	n	3	n	"	3	3	"	3	3	3	3	3	3	3	3	3	3	3	3	я	
12	. Z		2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V	
7	05		OUT				OUT					OUT			OUT				OUT				OUT		
10	Q 2			OUT				DUT			OUT					TUO				OUT				OUT	
6	72		2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V	
8	Clear 2		5.0 V	5.0 V			5.0 V				Z	5.0 V			Z	5.0 V				5.0 V			5.0 V	5.0 V	
5 6 7 8 9 10	Preset 2		5.0 V	5.0 V			5.0 V				5.0 V	Z			5.0 V	Z				5.0 V			5.0 V	5.0 V	
9	2 >		Z	Z			Z				2.4 V	2.4 V			2.4 \	2.4 V				<u>z</u>			Z	<u>z</u>	
2 E	0	5.0 V	3	2	n,	"	n,	n	3	3	*	*	3	3	3	3	3	3	"	3	n	3	×	n	
4		2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			2.4 V	2.4 V			s = -55°C.
8	Clear 1									5.0 V			Z	5.0 V			5.0 V	5.0 V				5.0 V			except T _c
2	t 1	5.0 V			5.0 V	2.0 V			5.0 V	Z			5.0 V	Z			5.0 V	5.0 V			5.0 V	5.0 V			ogroup 10,
<u></u>	Clock 1	Z			Z					2.4 V			2.4 V	2.4 V			Z	Z			Z	Z			s as for sub
Case E & F	-	122	123	124	125	126	127	128			131	132	133	134	135	136	137	138	139	140	141	142	143	144	ions and limits
Ü.	g -	3003 (Fig 8)	3	3	(Fig 9)	u	,,	"	3003 (Fig 8)	3	3	3	3	3	3	3	3003 (Fig 9)	33	3	3	3	3	3	3	rminal condit.
Symbol		t _{PHL2}	3	3	F _{MAX} 5/ (3	"	*	t _{PLH1} (3	:	3	ф РНL1	3	3	3	t _{PLH2}	*	3	*	tрн∟2	:	3	*	Same tests, terminal conditions and limits as for subgroup 10, except $T_{\rm C}$ = -55 $^{\circ}\text{C}$
Subaroup		9 T _C = 25°C	3	3	Ш	$T_C = 125$ °C	"	я	3	29	3	39	19	3	29	3	29	z	**	2	39	3	99	3	11 8

See notes at end of device type 04.

NOTES:
A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
C = This note has been deleted.
E = Momentary ground, then 2.4 V.
F = Momentary ground, then 5.5 V.
** = Test time limit < 100 ms.
J = This note has been deleted.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open.)
2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
3/ Output voltages shown are: H = 2.4 V. minimum and L = 0.4 V. maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
4/ Tests shall be performed in sequence.
5/ Fixex. minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 05. 1/

	Unit	>	> =		,,	"	*	n	*		,,	3 3		,,	,,	"		3				,,	,	3 4	¥H,			,	,	33	ď,	,,	3	"		,,	,,	"	: :	"	3 3	: :
Test limits	Max U									0.4	,			,	,,		•	-1.5	,,			"	n	+	+	-3.2	3.2	2.2	3.2	4.8	40	2 8		80	, ,	,	200	,,		20	50	300
Test	Min	7.0	t .	*	,	,	,		,	0								ì						1				T				, _	_	~			2			1	- 0	n
	_	C	1									_							_	<u> </u>	_	01	0.1		7 0		H	╁			-				7 0		L	1	01 0		21	_
Meas.	terminal	5	10	10	ğ	Q2	<u>Q</u> 2	Ω 2	02	10	Q 7	δı	Ω	<u>Q</u> 2	Q 2	Ø2	1Q 2	D1	Clock	Clear 1	Preset 1	Clock 2	Clear 2	Preset 2	נט ק	Preset 1	Preset 2	Clear 1	Clock 2	Clear 2	70	D1	D2	Clock 1	Preset 1	Preset	Clock 1	Preset 1	Clock	Clear 1	Clear	Clear 1 Clear 2
14	Preset	-		GND	0.8 V							2.0 V	0.0 \								-12 MA			2	GND	0.4 V	4	OND GND			4.5 V	4.5 V		4.5 V	2.4 V		4.5 V	5.5 V		4.5 V		4.5 V
13	ğ	Var.	<u> </u>		4 mA						16 mA	16 mA																														1
12	10	-	4 mA	4 mA						16 mA		7 W	AIII OI																													
11	GND	CINC			"	"	"	,	3	3	33	3 3		"	,,,	"	:	"	n	: :	. "	"	n	3 3	: "	,	,,		"	n	3 3	,,,	,	"		"	*	n	2 2	"	31 3	: 3
10	,						4 mA	4 mA						16 mA			16 mA																									
o o	075					4 mA			4 mA						16 mA	16 mA																										Ť
10	Preset	2				•		GND	0.8 V						H	2.0 V	7 8.0							-12 mA		O NIS	0.4 V		GND	SND	45.7	2	4.5 V		7 2	2.4 V			4.5 \		4.5 V	4.5 V
7	Clock	+				Α	٧	GND						٧	A	7						-12 mA		-	1 5 1	-	GND		0.4 V (_	7 7 7	+	4.5 V	H	/ / / /	+		\dashv	5.5 V	\vdash	P B	7 B
6						2.0 V	8 \	O						2.0 V	0.8 V						-12 mA	+			7.70	+	GND		GND	-	/ / / /	t	5.5 V 4	H	-	4.5 \		\dashv	4.5 \	H	GND	GND
5	2					2.	o.	0.8 V	GND					2.	H	0.8 V	>				-1	:	-12 mA	-	4 5 7	-	GND		4.5 V G		CIND	+	GND 5.		+	4.5 \	-	\dashv	GND 4.5 V	+	2.4 V G	5.5 V G
14		7	2	3	,,	n	2	, 0			,,	, ,		,	,	, 0.8	. 5.	п	,		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	,		* [2.5 \	, ,			4.9	, 0				,,	, , ,			,	, , ,	H		
	_	-	ŕ									-												+	+	-					9	9					9	> 2		Н		
1 3	Clear	,	> >	0.8 V	GND					>	H	0.8 \	7.7					Αι		-12 mA				+	۷ 4.5 V	GND	H	0.4 \	H		CAND /	/ GND	-	H	V 4.5 V		dn9 /	\dashv		2.4 V	\dashv	5.5 V
2 2	L	0	0.8 V							2.0 V	0.8 V							-12 mA	_					+	0.4 V	GND	H	4.5 V		_	2.4 V	5.5 V	┝	4.5 V	-		4.5 V	\dashv		GND	i	GND
3 -	Clock	<	< <	GND						⋖	A								-12 mA					,	4.5 V	GND		4.5 V			4.5 V	4.5 V		2.4 V	m		5.5 V	В		В	(m
Case A, B D Case C	Test No.	+	- 2	က	4	5	9	7	8	6	10	11 2	71	13	14	15	16	17	18	19	27	22	23	24	52	27	28	30.7/	31	32 7/	33	32	36	37	38	40	41	42	43	45	46	47
	method	3008	3	3	"	"	,,	n	3	3007	я	3 3		"	,,	"	=							0000	3008	3	,,	3	99	"	3010	,,	"	39	3 3	n	3	,,	= =	"	3 3	: 3
Symbol		\ \ \	<u>.</u>	3	"	27	n	3	3	VoL	"	, ,		39	,,	,,	3	V _{IC}	2	= =	. "	71	n	a -	111	39	"	11.2	"	"	H_	111	길	I _{IH3}	3 3	n		n	3 3	I _{IH5}	FE .	911
Subgroup			T _c = 25°C	3	"	27	"	3	31	3	,,	3 3		"	"	"	3	и	,,	= 3	. "	"	n	3 3	: "	3	,,		,,	"	3 3	,,	31	,,	3 3	n	*	n	a a	n	"	: :

See notes at end of device type 05.

TABLE III. Group A inspection for device type 05. 1/- Continued.

Ī		Unit	mA	3	"	,	"	,,																																MHz	3	3	3
1	est illuits	Max	-57	3	3	2	30	30			HorL	as shown 3/		: :	: 12	33	"	"	"	"	×	=	3 3	= =	= 3	s :		3	= =	: 3	: 3		n	"	я	3	"	"					
F	_	Min	-20	3	,,	39						as																												10	2	"	,,
	000	reas. terminal	ğ	ΙQ -	02	<u>0</u> 2	Vcc	Vcc			All	outputs	3 3	3 3	: :	33	33	"	n	"	,,	:	,,		: :	= :	:	,,		: 3	: 3	, ,,	,,	"	"	,,	31	33		ğ	10	Q2	Q 2
;	4 ,	Preset	GND				GND				В	Α	۷.	ω (m 0	0 60	4	٨	В	A	Α	¥	V I	а	8	а .	A	V.	Α,	Αď	n <	τ <	< A	(m	∢	∢	∢	Α		5.0 V	5.0 V		
	2 .	م 2	GND								н	7	7	Ξ:		- I		_	I	I	I	I	7	Ξ:	I	Ι.	_		7	Ξ:	r :	c -		ı	I	7		7		OUT			
	71	» IQ		GND							Н 3/	エ	Ι.	_ _ .	_	ı	I	I	Γ		_	_	Ι.	_ :	Ι:	Ξ:	I	I	Ι.	٦.			_ 	: _	_	I	I	I			OUT		
,	_ r	GND	GND	*	"	n	n	,,			GND	"	3 :	: :	: 3	"	"	"	"	"	"	4	z :	: :			4	"	: :	: 3	: 3	. "	"	"	"	,,	"	39		GND	3	'n	*
9	2 0	۵ ₂				GND					Н 3/	I	Ι.	_	- ا		I	I	7	٦	٦	7	Ι.	-	Ξ:	Ι:	I	I	Ι.		7 -	7 7	=		7	I	I	н					OUT
	n 0	02			GND						H 3/	٦	_ :	Ι:			_	_	I	I	I	I	_ :	Ι:	Ι:	Ι.	_	_	_	Ι:	Ξ:	Е _	,	ı	I	_	7	7				OUT	
	0 5	10 Preset 2			GND		GND				В	A	Α.	<u>а</u>	ω α	0 00	4	4	В	Α	A	⋖	∢ 1	м (9 (В	⋖	⋖	Α,	∢ 0	n <	∢ <	(4	a B	4	4	٧	Α				5.0 V	2.0 V
1	,	×					GND	Н			В	В	В	m <	∢ <	τ «	<	۷	Α	A	В	В	∢.	Α,	Α.	Α.	⋖	⋖	м «	∢ <	۷ <	∢ <	(4	. ≺	4	4	٧	Α				z	
	٥	12 D2					GND	Н	e omitted.	e omitted.	В	В	В	<u>а</u>	n 0	0 4	<	4	Α	A	V	Ф	В	В .	۷ı	В	Ф	В	⋖・	< <	Α <	∢ <	(<	В	В	В	В	Α				Н	ш
_	o 9	13 Clear 2				GND		GND	/ _{IC} tests a	lc tests ar	В	В	Α.	Α «	∢ 0	0 00	В	V	Α	Α	A	⋖	Α.	Vά	В	В	В	Α.	Α,	∢ <	∢ <	τ α	2 4	. ⋖	A	В	V	А	55°C.				
	4 ;	1	5.5 V	3		,		, ,	25°C and \	5°C and ∿	4.5 V	n	3 :	: :	: 3	я	"	"	**	и	n		z :	# 3		:		,	: 3	: 3	: "	. 3	y,	я	,	,	"	27	25°C and -	5.0 V	3	n	*
	ο,	Clear 1	-	GND				GND	κ cept T _C = 125 $^{\circ}$ C and V $_{\rm IC}$ tests are omitted	cept T_C = -55°C and V_{IC} tests are omitted.		В	∢.	∢ <	< □	0 00	В	۷	А	A	A	V	∢.	۱ ک	8 6	В	m	Α.	∢ .	∢ <	∢ <	< α	o ≪	< <	A	В	V	Α	$cept T_C = 125^{\circ}C$ and -55°C.	_			
	7						H	GND	up 1, exc	up 1, exc	В	В	В	<u>а</u>	n 0	0 4	<	۷	Α	A	A	В	В	м .	۷ı	В	В	В	Α,	∢ <	۷ <	∢ <	(4	<u>а</u>	В	В	В	Α	up 7, exce	Ш	ш		
-	- 0	Glock 1					GND	Н	for subgro	for subgro	В	В	В	м <	∢ <	τ «	< <	4	Α	A	В	В	Α.	۷,	Α.	Α.	Α.	⋖	В	∢ <	∢ <	4 <	(4	. ∠	⋖	4	4	Α	for subgro	z	Z		
0	0 0								d limits as	d limits as																													d limits as				
	Case A, B D	Case C Test No.	49	20	51	52	53	54	ditions and	ditions and	52	26	57	28	29	61	62	63	64	92	99	29	89	69	0/ i	71	72	73	74	75	1,6	//	79	80	81	82	83	84	ditions and	85	98	87	88
C I	MIL'S D	method	3011	×	"	31	3005	3005	Same tests, terminal conditions and limits as for subgroup 1, e»	Same tests, terminal conditions and limits as for subgroup 1, ey																													Same tests, terminal conditions and limits as for subgroup 7, ey	(Fig. 11)	3	n	и
	Symbol		sol	3	"	n	lcc	lcc	Same tests,	Same tests,																													Same tests,	F _{MAX} 6/	3	n	3
ć	dnoibane		1	T _C = 25°C	"	"	39	n	2	3	7 2/ 4/	$T_C = 25^{\circ}C$	= :	: :	: 3	я	я	,	"	79	*	y.	3	:	:	=	,	"	: :	: 3	: 3	"	3	3	"	"	3	n	8 2/ 4/	6	$T_{\rm C} = 25^{\circ}{\rm C}$	n	ä

See notes at end of device type 05.

TABLE III. Group A inspection for device type 05. 1/ - Continued.

	11-11	Unit	su	*	*	"	3	я	,	,	su	3	"	ä	*	3	,	*	MHz	3	3 3	ns	,	3	*	"	3	,,	3
Test limits		Max	25	,	"	40	3	3	×	3	30	3	n	3	40	4	×	,	n	3	3	30	×	4	*	20	3	"	3
		Min	5	3	a a	3	z	я	3	39	2	я	n	я	×	79	*	×	10	3	2 2	2	3	79	3	×	я	,,	3
	Meas.	terminai	Clear 1 to Q 1	Preset 1 to Q1	Clear 2 to $\overline{\mathbb{Q}}$ 2	Preset 2	Clear 1 to Q1	Preset 1 to $\overline{\mathbb{Q}}$ 1	Clear 2 to Q2	Preset 2 to $\overline{\mathbb{Q}}$ 2	Clock 1 to Q1	Clock 1 to Q 1	Clock 2 to Q2	Clock 2 to Q 2	Clock 1 to Q1	Clock 1 to Q 1	Clock 2 to Q2	Clock 2 to \$\overline{\Omega} 2\$	20	10	20 00	Clear 1 to Q 1	Preset 1 to Q1	Clear 2 to Q 2	Preset 2 to Q2	Clear 1 to Q1	Preset 1 to $\overline{\mathbb{Q}}$ 1	Clear 2 to Q2	Preset 2 to $\overline{\mathbb{Q}}$ 2
14	4	Preset 1	ſ	Z			7	Z			5.0 V	В			Ф	5.0 V			5.0 V	5.0 V		٦	Z			7	Z		
13	\dagger			DOUT			OUT				OUT				OUT				OUT				OUT			OUT			
12	9	<u>0</u>	TUO					TUO				TUO				TUO				OUT		DOUT					TUO		
1	\ C	GND	GND	3	3	=	3	3	3	39	3	n	"	3	3	n n	3	×	3	3	3 3	3	3	n n	3	3	n	n n	3
10	8	<u>Q</u> 2			TUO					OUT				DOUT				OUT			OUT			TUO					OUT
6	o (Q2				OUT			TUO				OUT				OUT				DOUT				OUT			OUT	
8 9	10	Preset 2			٦	Z				Z			5.0 V	Ф				5.0 V			5.0 V			7	Z				Z
7	+	Clock 2 P											Z	Z				Z			ZZ								
9													(A) N	(A) N			IN (B)	IN (B)			шш								
	13				Z	¬			z	٦			N B				5.0 V	<u>Z</u> m						z	7			Z	٦
4 ;	+		>	3	= ,	Ĺ	_		=			_		, 2.0 V	_	_	5.0			_	3 3				<u> </u>		_		
	4		۱ 5.0 ۷				7	-		•		>		-	>						-	-				7		_	_
8	Ť	_	Z	7			≥	7				4) 5.0			3) 5.0	9 (c						≥	7			≥	ר		
2	4	_									(A) N	(A) N			(B) N	(B) N			ш	Ш									
	e :										롣	Z			롣	Z			≧	롣									
Case A, B, D	Case C	Test No.	88	06	91	92	93	94	92	96	26	86	66	100	101	102	103	104	105	106	107	109	110	111	112	113	114	115	116
MIL-			3003 (Fig 10)	3	11	"	3	35	"	*	3003 <u>5/</u> (Fig 11)	(Fig 12)	(Fig 11)	(Fig 12)	(Fig 12)	(Fig 11)	(Fig 12)	(Fig 11)	(Fig 11)	33	3 3	3003 (Fig 10)	"	3	3	39	*	"	=
Symbol			t РLH1	я	"	ä	tрн∟1	39	3	39	t _{РLН2}	3	3	3	tрнц2	3	3	39	F _{MAX} <u>6</u> /	з	3 3	ф.	3	3	я	tрн∟1	3	"	3
Subgroup			9 T _C = 25°C	3	z	3	3	3	3	3	3	3	3	3	3	3	3	3	10 T _C = 125°C)	2 2	3	3	3	2	3	3	,	3

See notes at end of device type 05.

TABLE III. Group A inspection for device type 05. 1/ - Continued.

Case C Case C Case C Case C Case C Case C Cock 1 Dock 1 Dock 1 Amass. Miss. Miss. Miss. Miss. Unit 117 IN IN (A) 50 V " Clock 2 GOCK 2 " " OUT 5.0 V " OUT " OUT 5.0 V " " OUT " OUT 5.0 V " " OUT " OUT 5.0 V " " " " OUT " OUT " <t< th=""><th></th><th>Case A, B, D</th><th>1</th><th>2</th><th>3</th><th>4</th><th>2</th><th>9</th><th>7</th><th>8</th><th>6</th><th>10</th><th>11</th><th>12</th><th>13</th><th>14</th><th></th><th></th><th>Test limits</th><th></th></t<>		Case A, B, D	1	2	3	4	2	9	7	8	6	10	11	12	13	14			Test limits	
Clock 1 D1 Clear 1 V _{CC} Clear 2 D2 Clock 2 Preset 2 Q2 Q2 GND Q1 Q1 Preset 1 terminal Min Max M	Case	C															Meas.			
IN IN A) B A A A A A A A A	Tes	t No.	Clock 1	D1	Clear 1	Vcc	Clear 2	D2	Clock 2	Preset 2	Q2	<u>Q</u> 2	GND	10	Q1	Preset 1	terminal	Min	Мах	Unit
IN IN (A) 5.0 V B IN (A) IN 5.0 V OUT OUT B Clock 1		17	Z	(A) N	Ф	×							×		OUT	5.0 V	Clock 1 to Q1	2	38	ns
Note	_	18	Z	(V) <u>N</u>	5.0 V	3							39	TUO		Ф	Clock 1 to Q 1	n	2	3
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		119				×	m	N(A)	Z	5.0 V	OUT		×				Clock 2 to Q2	n	n	3
IN (B) 5.0 V " S.0 V N (B) N		120				3	5.0 V	(A) N	Z	а		OUT	39				Clock 2 to Q 2	n	2	3
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		121	Z	IN (B)	5.0 V	×							×		OUT	ш	Clock 1 to Q1	n	40	3
## Solver In (B) IN B OUT ## Clock 2 # # Clock 2 # # To Q2 ## In (B) IN 5.0 v OUT ## Clock 2 # # To Q2 ## In (B) IN 5.0 v OUT ## Clock 2 # # To Q2 ## In (B) IN 5.0 v OUT ## Clock 2 # # To Q2 # To Q3 # To		122	Z	IN (B)	Ф	n							n	OUT		5.0 V	Clock 1 to Q 1	n	3	3
" B IN (B) IN 5.0 V OUT " Glock 2 " "		123				×	5.0 V	IN (B)	Z	В	OUT		×				Clock 2 to Q2	n	n	3
		124				3	В	IN (B)	Z	5.0 V		OUT	**				Clock 2 to Q 2	"	"	3

NOTES:
A = Normal clock pulse.
B = Momentary GND, then 4.5 V.

E = Input D connected to \overline{Q} .

J = Input pulse, $t_p \ge 100$ ns, PRR = 1 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).

2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.

3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.

4/ Tests shall be performed for both D input pulses (A and B).

5/ Tests shall be performed for both D input pulses (A and B).

5/ Tests shall be performed for both D input pulses (A and B).

5/ Tests shall be one-half of the input frequency.

55

TABLE III. Group A inspection for device type 06. 1/

ş		Unit	>	2	*	"	"	*	n	"	11	,,	: 3	n	n	3	n	"	mA	"	¥	3	=		n n	n	ΥΠ	, ,,	я	"	n	3 3	: 3	n	n	"	3	"	"	11	"	n	n	mA	3	n	n	
Test limits		Max					0.4	"	"	"	-1.5	"	: "	"	"	3	"	"	-1.6	"	n	3	4	: 3	: 3	"	40	n	n	31	"	3 3	: 0	99.	ņ	"		,,	n	80	80	200	200	-57	-57	30	30	
		Min	2.4	3	n	"													2.0-	"	я	3	=	: :	, ,,	n																		-20	-50			
	Meas.	terminal	Ø	Ισ	Ισ	Ø	Ø	IQ	Ισ	Ø	J1	J2	, Z	- X	**	Clock	Preset	Clear	J1	JZ	*`	Υ -	K2	** \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \	Clock	Clear	J.	JS	*L	K1	K2	* *	Clock	- 6	3 *\	- X	K2	**	Clock	Preset	Clear	Preset	Clear	Ø	ΙØ	Vcc	Vcc	
14	11	K2	V 8.0	2.0 V			2.0 V	V 8.0						Δm C1-	VIII 71							4.5 V	0.4 V		457	è				GND	2.4 V					GND	5.5 V			GND	4.5 V	GND	4.5 V					
13	6	*	2.0 V	0.8 V	GND	GND	0.8 V	2.0 V							-12 mA							0.4 V	0.4 V	0.4 V	0.4.V	ż				4.5 V	4.5 V	2.4 V				4.5 V	4.5 V	5.5 V		4.5 V	GND	4.5 V	GND	GND	GND			
12	8	Ø	4 mA			4 mA	16 mA			16 mA																																		GND				
11	7	GND	GND	3	n			"	3	11	"	я :	: 3	"	"	,,	"	,,	39	"	77	,,	4	: :	: "	"	"	"	n	33	"	3 3	: 3	37	ņ	"	31	"	"	"	11	31	"	"	3	,,	,,	
10	9	ΙΟ		4 mA	4 mA			16 mA	16 mA				Ī											Ì									l												GND			
6	5	*	0.8 \	2.0 V	GND	GND	2.0 V	0.8 V	GND	GND			-12 mA						0.4 V	0.4 V	0.4 V					0.4 V	4.5 V	4.5 V	2.4 V				7 1	4.5 V	5.5 \					GND	4.5 V	GND	4.5 V	GND	GND			
8	4	JZ	2.0 V	0.8 V			0.8 V	2.0 V				-12 mA							4.5 V	0.4 V						4.5 V	GND	2.4 V					2	GND 55.V						4.5 V	GND	4.5 V	GND					
7	3	7	2.0 V	0.8 V		\vdash	0.8 V				-12 mA								H	4.5 V						+	-	GND	Н				4	2.5 V	+				H			4.5 V	-					
9	1	NC									•								,						1	+														,								pattimo a.
2	2	Clear			0.8 V	2.0 V			2.0 V	0.8 V								-12 mA	В	В						0.4 V	GND	GND					2	בואם פואם פואם	2						2.4 V		5.5 V		GND	GND		V _o tests a
4	14	Vcc	4.5 V	3	n	"	"	n	*	"	"	я :	. "	n	,	3	"	H	5.5 V	,,	n	3		: 3	: "	n	"	"	n	"	"	3 3	: 3	"	n	,,		,,	n	,,	**	"	×	"	:	,,	"	25°C and
3	13	Preset			2.0 V	0.8 V			0.8 V	2.0 V		H	1				-12 mA	<u> </u>				В	В		V 7 V					GND	GND					GND	GND			2.4 V		5.5 V		GND			GND	ant T _c = 1
2			4	4	GND	GND	Α		GND	GND						-12 mA	┿	t	GND	GND		GND	GND	7 7	0.4 V	╁							2.4 V	1	ŀ				5.5 V	_			_	GND	GND			IID 1 exc
H	10		8 \	2.0 V		H	2.0 V					H	40	<u> </u>	-	-)			0.4 \ 0.4	4		457	+				2.4 V	QN.	+	7	1	-	5 \	GND				2 \	GND	-		_			or subaro
_			Ö	2.			2.	0						71-								o o	4		A	f				2.	g			1	-	5.	G			9	4.	g	4			-		imits as f
Case A, B D	Case C	Test No.	-	2	ဇ	4	2	9	7	8	6	10	- 2	13 12	14	15	16	17	18	19	20	21	22	23	24	26	27	28	29	30	31	32	33	35	38	37	38	39	40	41	42	43	44	45	46	47	48	ditions and I
MIL-STD-	883	method	9008	3	39	39	2008	"	n	39									6008	n	77	27		: 3		"	3010	"	27	29	"	"	: 3		"	25	"	"	27	n	"	"	n	3011	3	3008	n	Same tests terminal conditions and limits as for subgroup 1 except $T_c = 125^{\circ}$ C and V_c tests are omitted
Symbol			V _{он}	33	39	11	Vol	,	y	n	V _{IC}	"	: 3	"	n	"	"	"	l _{IL1}	"	ņ	# :	=	" "	"	"	-H	n	"	29	"	2 2	•	IH2		77	39	n	"	I _{H3}	29	I _{IH4}	n	los	=	8	3	Same tests.
Subgroup			-	$T_{\rm C}=25^{\circ}{\rm C}$:	"	,,	*	3	39	n	,	: 3	,	n	"	77	"	"	n	¥	3	=	: 3	: 9	"	n	77	77	"	"	3 3	: 3		"	37	39	n	n	n	11	n	n	"	=	"	n	2

See notes at end of device type 06.

TABLE III. Group A inspection for device type 06. 1/- Continued.

1, 1, 1, 1, 1, 1, 1, 1,		O 0 al	V V V V V V V V V V V V V V V V V V V	Los A A A A A A A A A A A A A A A A A A A			
Note		0 < < < < < < < < < < < < < < < < < < <	A C <t< td=""><td>4 0 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4</td><td></td><td></td><td></td></t<>	4 0 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4			
		< < < < < < < < < < < < < < < < < < <		BAAAAAAAAAAAAAAAAAAAAAA			
		< < < < < < < < < < < < < < < < < < < <			44444444444444444		
		< < < < < < < < < < < < < < < < < < <					
		< < < < < < < < < < < < < < < < < < < <			4444444444444444		
		< < < < < 0 < < < < < < < < < < < < < <			<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<		< 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0 0 < 0 0
		< < < a a a a a a a a a a a a a a a a a			444444444444444		
		< < < 0 < < < < < < < < < < < < < < < <			<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<		
		< < \alpha < < < < < < < < < < < < < < < < < < <	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		444444444444		A B B A B B A B B A B B B A B B B A B B B B A B B B A B
		< m < < < < < < < < < < < < < < < < < <	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		444444444444		
		n < < < < < < < < < < < < <	: 2 2 2 2 2 2 2 2 2 2 2		44444444444		
		444444444	: 2 2 2 2 2 2 2 2 2 2		44444444444		
		44444444	3 3 3 3 3 3 3 3 3 3		<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<		
		4 4 4 4 4 4 4	2 2 2 2 2 2 2 2		444444444		
		< < < < < < < < < < < < < < < < < < <	2 2 2 2 2 2 2		4444444		B A B B A B B A
		<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<	3 3 3 3 3 3		. 4 4 4 4 4 4		
H H H H H H H H H H H H H H H H H H H		< < < <	2 2 2 2 2		4 4 4 4 4		B A B B A B
H H H H H H H H H H H H H H H H H H H		4444	3 3 3 3 3		4444		B B B A
H H H H H H H H H H H H H H H H H H H		444	3 3 3 3		4444		B A B B
H H H H H H H H H H H H H H H H H H H		A 4	3 3 3		4 4 4		B > B
H H H H H H H H H H H H H H H H H H H		٧	3 3		4 4		В
		ζ	"		٨		В
H H H H H H H H H H H H H H H H H H H		Α					
H H H H H H H H H H H H H H H H H H H		4	и		4		Α
H H H H H H H H H H H H H H H H H H H		Α	'n		٧	В	В
A A A A A A A A A A A A A A A A A A A		В	"		Α		В
" " " " " " " " " " " " " " " " " " "		В	и		Α	A A	
A B L " L		В	'n		٧		
A B L " L		В	и		В		
	В	В	и		В		
A B L " L		В	"		В		В
B A H " L		В	"		Α		В
" H		⋖	¥		⋖	В	Ф
B A H "		٧	,,		A	A	
B A L		۷	"		В	В	A
.π .π .π		×	"		В		В
" "		∶∢	"		٨		<u> </u>
		(<	37		(<		o <
B A L H		٧			4		A
B A L " L		В	77		٧	A	Α
B A L "		A	n		٧		Α
A B L " H		٧	"		A		В
т "		٨	"		В	В	В
В Н	-	⋖	"		В		A

See notes at end of device type 06.

TABLE III. Group A inspection for device type 06. 1/ - Continued.

		Unit	MHz	MHz	su	31	n	,,	Su	3	n	*	MHz	MHz	su	n	n	3	Su	*	n	3	
Test limits		Max			20	3	"	"	20	39	"	ä			62	"	"	"	62	×	"	"	
		Min	20	20	2	3	n	*	2	*	n	3	15	15	2	31	n	n	2	3	n	"	
	Meas.	terminal	Ø	Ισ	Clear to Q	Preset to Q	Clear to Q	Preset to Q	Clock to Q	Clock to Q	Clock to Q	Clock to Q	ø	Ισ	Clear to Q	Preset to Q	Clear to Q	Preset to G	Clock to Q	Clock to Q	Clock to Q	Clock to Q	
14	11	K2	2.4 V	2.4 V	5.0 V	"	"	n	2.4 V	n	"	n	2.4 V	2.4 V	5.0 V	"	'n	"	2.4 V	n	'n	"	
13	6	*	GND	GND	GND	,,	"	3	GND	3	"	3	GND	GND	GND	"	"	и	GND	3	"	я	
12	8	Ø	DOUT			DUT	OUT		DOUT		OUT		OUT			DUT	DUT		OUT		DUT		
11	7	GND	GND	3	3	"	"	3	"	3	"	3	"	n	3	"	'n	n	"	3	'n	n	
10	9	Ισ		OUT	OUT			OUT		OUT		OUT		OUT	OUT			OUT		OUT		OUT	
6	2	*	GND	GND	GND	31	"	n	GND	n	"	n	GND	GND	GND	"	'n	"	GND	n	'n	"	
8	4	JZ	2.4 V	2.4 V	5.0 V	,,	"	3	2.4 V	"	"	3	2.4 V	2.4 V	5.0 V	"	"	3	5.0 V	3	"	3	
7	3	L)	2.4 V	2.4 V	5.0 V	"	n	n	2.4 V	39	n	n	2.4 V	2.4 V	5.0 V	n	n	"	5.0 V	n	n	"	
6	1	NC																					
5	2	Clear	5.0 V	5.0 V	Z	"	"	3	5.0 V	3	"	3	5.0 V	5.0 V	Z	"	"	"	5.0 V	3	"	"	
4	14	Vcc	5.0 V	"	,,	,,	"	"	"	**	"	"	"	"	,,	"	"	"	"	"	"	39	T55°C
3	13	Preset	5.0 V	5.0 V	Z	,,	"	19	5.0 V	39	"	n	5.0 V	5.0 V	Z	"	'n	n	5.0 V	n	'n	n	avcent T _e
2	12	Clock	Z	z	0.8 V	29	"	3	Z	3	"	*	Z	Z	0.8 V	"	n	"	Z	=	n	77	o 01 dilore
1	10	Σ	2.4 V	2.4 V	5.0 V	"	"	3	2.4 V	3	"	3	2.4 V	2.4 V	5.0 V	"	'n	ä	2.4 V	3	'n	u	ac for cub
Case A, B D	Case C	Test No.	93	94	92	96	26	86	66	100	101	102	103	104	105	106	107	108	109	110	111	112	Same tests terminal conditions and limits as for subgroup 10
MIL-STD-	883	method	(Fig. 14)	(Fig. 14)	3003 (Fig. 13)	,	3	3	3003	(Fig. 14)	3	*	(Fig. 14)	(Fig. 14)	3003 (Fig. 13)	3	ä	3	3003	(Fig. 14)	2	"	terminal cond
Symbol			F _{MA} × 5/	F _{MA} × <u>5</u> /	фгн	H⊓dţ	t _{PHL}	t _{PHL}	(Fig. 15)	фгн	t _{PHL}	фнг	F _{MA} × 5/	/ <u>5</u> ×₩4	фгн	t _{PLH}	thHL	⊤н⊲	t _{PLH}	фгн	tpHL	⊤н⊲	Same tests
Subgroup			6	$T_C = 25^{\circ}C$	3	"	39	3	"	3	39	*	10	T _C = 125°C	3	"	39	3	39	3	39	"	7

NOTES:
A = Normal clock pulse.
B = Momentary GND, then 4.5 V.

^{1/} Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
4/ Tests shall be performed in sequence.
5/ Fight 1.5 V and L < 1.5 V when the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 07. 1/

		Chit	>	*	3	,,	,,	*	*	n	3	*	*	"	3	n	"	=	,,	3	: :		. "	,,	,,	mA	"	я :	= =	: 3	"	2	μĄ	: 3	3	3	,,	3	: :	,	,,	n	= =	: :	2
Test limits	ŀ	Max									0.4 V	*	"	,,,	3	n	33	3	-1.5	"	: :	: 3	: 3	,,	"	-1.6	H	я :	* c	-3.2	»	,,	40	100	100	80	"	a .	200		,,	"	120	120	300
Te		Zi.	2.4	"	n	"	,,,	"	n	n																-0.5	"	я :		0.1-	'n	,,													
	Meas.	terminal	۵1	<u>0</u>	10	۵1	Q2	<u>Q</u> 2	Q 2	Q2	۵ 1	ğ	10	Q1	Q 2	Q2	Q2	Q 2	D1	Clock 1	Clear 1	Preset 1	DZ Olest o	Clock z	Preset 2	D 1	Preset 1	D2	Preset 2	Clock 1	Clock 2	Clear 2	5 6	2 2	22	Clock 1	Preset 1	Clock 2	Preset 2 Clock 1	Preset 1	Clock 2	Preset 2	Clear 1	Clear 2	Clear 2
14	4	Preset	-		2.0 V	0.8 V							2.0 V	0.8 V							+	-12 mA				0.4 V	H		+	GND 4.5.V	+		GND	CINC	+	<u> </u>	H		+	5.5 V	_		_		
13	5	ō	4 mA			4 mA						16 mA	16 mA																																
12	9	10		4 mA	4 mA						16 mA			16 mA																															-
11	7	GND	GND	,	,	"	"	39	77	n	,	3	"	,	3	n	"	3	»	,,	3 3		. "	"	y,	n	"	я :	s s	: 3	×	,,	3 3	: 3	3	"	"	n	: :	,,	"	n	3 3	: 3	33
10	8	Q 2						4 mA	4 mA						16 mA			16 mA																											
6	6	Q2					4 mA			4 mA						16 mA	16 mA																												
8	10	Preset	7						2.0 V	0.8 V							2.0 V	0.8 \							-12 mA			0.4 V	0.4 V		GND	4.5 V		GND	GND			GND	2.4 V		GND	5.5 V			
7	11	Clock	1				Α	٧							∢	٧							V C F	- 12 MA				4.5 V	0.4 V		0.4 V	0.8 V		4.5 V	4.5 V			2.4 V	В		2.5 V	В		GNS	GND
9	12	D2					2.0 V	0.8 V							2.0 V	0.8 V						4 07	-12 mA					0.4 V	0.4 V		0.4 V	4.5 V	0.437	Z.4 V	5.5 V				4.5 V			4.5 V	Ċ	GND	GND
2	13	Clear 2	7						0.8 V	2.0 V							0.8 V	2.0 V						40.00	WII 71 -			4.5 V	4.5 V		4.5 V	0.4 V	2	GIND	GND			В	4.5 V		В	4.5 V	;	2.4 v	5.5 V
4	14	Vcc	4.5 V	39	n	"	"	39	,	31	"	"	"	31	=	n	27	=	n	31		= 3	: 3	"	"	5.5 V	"	я :	3 3	. "	"	"	, ,	: 3	3	3	"	я	: :	*	"	31	: :		3
3	-	Clear 1			0.8 V	2.0 V							0.8 V	2.0 V							-12 mA					4.5 V	4.5 V		7 2 7	4.5 V	5		GND	CNC	5	В	4.5 V		В	4.5 V			2.4 V	7 7 7	;
2	2	10	2.0 V	0.8 V							2.0 V	0.8 V							-12 mA							0.4 V	0.4 V		24.0	0.4 V 4.5 V	2		2.4 V	7 2 7	200		4.5 V			4.5 V			GND	CINC	į į
Ш	3	Clock 1	- Α	4							٧	A								-12 mA						4.5 V	0.4 V		2	0.4 \	5		4.5 V	457	è	2.4 V	В		5.5 V	В			GND	CINC	<u>د</u> ز
Case A, B D	Case C	Test No.	1	2	က	4	2	9	7	8	6	10	11	12	13	14	15	16	17	18	19	20	21	77	24	25	26	27	28	30	31	32	33	34	36	37	38	39	40	42	43	44	45	46	48
MIL-STD-	883	method	3006	,,	*	39	n	,,	7	39	3007	n	"	39	=	,,	39	=								3009	n	39	= =	. ,	33	29	3010	: 3	39	39	n	3 :	= =	n	n	n	3 3	: 3	25
Symbol			V _{Он}	*	*	"	n	*	3	39	NoL	n	"	39	*	79	29	*	V _{IC}	n	2 3	. 3	: :	3	"	1111	п	**	=	11.2	33	99	-E-	: !	ZH."	I _{H3}	п	3			n	"	I _{H5}	: -	,,, ,,,
Subgroup			٦	$T_{\rm C}=25^{\circ}{\rm C}$	"	39	n	"	n	39	37	n	"	39	=	"	"	=	39	n	2 3		: 3	**	"	"	п	39	: :	. 3	3	n	3 3	: 3	31	"	n	3 :	, ,	"	"	n	3 3	: 3	39

See notes at end of device type 07.

TABLE III. Group A inspection for device type 07. 1/ - Continued.

Subdroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	2		7	8	6	10	11	12	13	14			Test limits	
•	,	883	Case C	က	2	-	14	13		11	10	6	8	7	9	2	4	Meas.			
		method	Test No.	Clock 1	10	Clear 1	Vcc	Clear 2	D2	Clock 2	Preset 2	02	<u>Q</u> 2	GND	IQ L	Q1	Preset	terminal	Min	Max	Unit
1	los	3011	49				5.5 V							GND		GND	GND	۵	-20	-57	mA
$T_C = 25^{\circ}C$	"	,,	20			GND	"							n	GND			آ م	n	3	y
,,	,,	n	51				"				GND	GND		n				Q2	"	ņ	'n
×	,	99	52				я	GND					GND	3				Q 2	з	3	3
n	2	3005	53	GND	GND		n		GND	GND	GND	GND		"			GND	۸		30	"
"	201	3005	54	GND	GND	GND	3	GND	GND	GND	GND			31				8 /8		30	я
2	Same tests	; terminal conc	Same tests, terminal conditions and limits as subgroup 1, except $T_{\rm C}\!=\!$	s as subgro	oup 1, exce		125°C and V _{IC} tests are omitted	c tests are	omitted.												
ъ	Same tests	; terminal conc	Same tests, terminal conditions and limits as subgroup 1, except $T_{\text{\scriptsize C}} =$	as subgro	oup 1, exce		-55°C and V _{IC} tests are omitted	c tests are	omitted.												
7 2/ 4/			22	В	В	В	4.5 V	В	В	В	В	H 3/	Н3/	GND	H 3/	Н3/	В	₩		HorL	
$T_{\rm C} = 25^{\circ}{\rm C}$			26	В	В	В	3	В	В	В	V	-	Ŧ	31	T		A	outputs	ä	as shown 3/	
31			22	В	В	٧	"	¥	В	В	A		I	"	I	7	٧	. 31		"	
33			28	В	В	٧	"	A	В	В	В	I	_	"	_	I	В	39		"	
"			29	A	В	٧	"	A	В	٧	В	I	_	"	_	I	В	39		"	
n			09	A	В	В	"	В	В	A	В	I	I	"	I	I	В	3		"	
33			61	A	A	В	'n	В	A	A	В	I	I	,,	I	н	В	33		"	
n			62	Α	٧	В	"	В	A	A	Α	7	I	,,	I	_	A	"		,,	
n			63	Α	Α	Α	,,	Α	Α	Α	Α	٦ _	I	"	I	٦	Α	"		**	
n			64	A	٧	۷	"	A	A	A	В	I	_	"	_	I	В	"		"	
"			92	Α	Α	٧	"	A	A	Α	Α	I	7	"	_	I	A	37		"	
"			99	В	Α	A	"	Α	Α	В	Α	I	7	"	7	Н	A	n		**	
77			29	В	В	A	n	A	В	В	A	I	7	"	7	I	A	37		"	
77			89	Α	В	Α	37	Α	В	Α	Α	7	I	11	I	L	Α	"		39	
11			69	Α	В	Α	37	Α	В	Α	В	I	7	11	7	Н	В	19		"	
19			20	A	A	В	31	В	A	Α	В	I	I	11	I	Н	В	19		"	
"			11	A	В	В	,,	В	В	A	В	I	I	,,	I	I	В	"		,	
"			72	Α	В	В	"	В	В	A	Α		I	"	I	_	A	37		"	
"			73	Α	В	A	"	A	В	A	Α	7	I	,,	I	٦	A	"		,,	
n			74	В	A	۷	"	A	A	В	A		I	"	I	7	A	n		"	
"			75	۷	٧	٧	"	A	۷	A	٧	I	7	"	7	I	٧	"		"	
39			9/	A	A	٧	n	A	∢	A	В	I	٦	"	7	I	В	39		"	
"			2.2	A	A	٨	'n	A	Α	A	Α	I		"	_	н	A	"		"	
"			78	Α	Α	В	,,	В	Α	Α	Α	٦ _	I	"	I	٦	Α	"		**	
77			62	Α	Α	Α	"	Α	Α	Α	Α	7	I	"	I	Г	Α	n		27	
77			80	Α	В	Α	33	Α	В	Α	В	I	7	"	7	Н	В	"		39	
"			81	Α	В	Α	"	Α	В	Α	Α	I	7	"	_	Η	Α	n		"	
8 2/ 4/	Same tests	; terminal conc	Same tests, terminal conditions and limits as for subgroup 7, except T_{C}	as for sub	group 7, e	xcept T _c =	= 125°C and -55°C.	1-55°C.													

See notes at end of device type 07.

TABLE III. Group A inspection for device type 07. 1/- Continued.

_		,																				,		,
		Onit	MHz	,,	"	3	ns	=	3	3	3	3		"		*	ns	3	3	3	ä	3	3	3
Test limits		Мах					25	=	a	*	33	36		36		33	25	3	×	3	33	*	=	2
		Min	10	n	"	n	2	=	3	3	*	u		n		"	2	3	3	*	3	3	3	3
	Meas	terminal	Ω	Ω 1	Q2	<u>Q</u> 2	Clear 1	Preset 1	Clear 2 to $\overline{\Omega}$ 2	Preset 2 to Q2	Clear 1 to Q1	Preset 1	0 0	Clear 2	to Q 2	Preset 2 to Q2	Clock 1 to Q1	Clock 1 to Q 1	Clock 2 to Q2	Clock 2	Clock 1	Clock 1 to Q 1	Clock 2 to Q2	Clock 2 to \overline{Q} 2
14	4	Preset	5.0 V	5.0 V			Z	Z			Z	Z					5.0 V	Ф			В	5.0 V		
13	ĸ	۵,	OUT					OUT			OUT						OUT				OUT			
12	y	, IQ		TUO			OUT					OUT						DOUT				TUO		
11	7	GND	GND	"	"	"	3	3	×	я	3	"		:		"	я	z	3	n	"	"	3	3
10	α	, IQ				OUT			OUT					OUT						OUT				OUT
6	б	, OZ			TUO					TUO						DOUT			OUT				TUO	
8	10	Preset 2			5.0 V	5.0 V			Z	Z				Z		Z			5.0 V	В			В	5.0 V
7	11	Clock 2			Z	Z													Z	z			Z	z
9	12	D2			ш	Э													IN (A)	(A) N			IN (B)	IN (B)
2	13	Clear 2			5.0 V	5.0 V			Z	Z				Z		Z			В	5.0 V			5.0 V	В
4	14	Vcc	5.0 V	"	"	u	3	3	я	×	3	,,		3		"	я	я	3	я	"	n	3	3
3		Clear 1	5.0 V	5.0 V			Z	Z			Z	Z					В	5.0 V			5.0 V	В		
2	0	Б	ш	ш													(A)	(A)			IN (B)	IN (B)		
-	ď	Clock	Z	Z													Z	Z			Z	Z		
Case A, B D	╀	Test No.	82	83	84	85	98	87	88	68	06	91		92		63	94	92	96	26	86	66	100	101
MIL-STD- (<u> </u>	method	(Fig. 11)	"	,,	n	3003 ((Fig. 10)	3	z	3	ä	n		3		*	3003 <u>5/</u> (Fig. 11)	(Fig. 12)	(Fig. 11)	(Fig. 12)	(Fig. 12)	(Fig. 11)	(Fig. 12)	(Fig. 11)
Symbol			F _{MA} ×	**	"	2	фгн	3	3	3	t _{PHL}	*		n		39	фгн	3	3	3	t _{PHL}	3	3	3
Subgroup			6	$T_{\rm C} = 25^{\circ}{\rm C}$	"	z	3	3	z	3	=	z		3		3	3	3	33	ä	3	3	3	3

See notes at end of device type 07.

TABLE III. Group A inspection for device type 07, 1/ - Continued.

												1	ı			ı				1	1	1	
	Unit	MHz	n	"	n	su		,,	n	3	3	n	z	3	su	я	*	3	"	n	ä	31	
Test limits	Max					31			3	"	39	42	42	39	31	3	"	3	39	"	×	и	
	Min	10	"	"	n	2		n n	"	3	39	3	3	3	2	3	n	"	n	y	3	77	
Meas.	terminal	۵1	۵ 1	Q2	<u>Q</u> 2	Clear 1	20 0	Preset 1 to Q1	Clear 2 to $\overline{\mathbb{Q}}$ 2	Preset 2 to Q2	Clear 1 to Q1	Preset 1 to Q 1	Preset 2 to $\overline{\mathbb{Q}}$ 2	Clear 2 to Q2	Clock 1 to Q1	Clock 1 to Q 1	Clock 2 to Q2	Clock 2 to Q 2	Clock 1 to Q1	Clock 1 to Q 1	Clock 2 to Q2	Clock 2 to \overline{\Omega} 2	
4 4	Preset	5.0 V	5.0 V			Z	:	Z			롣	Z			5.0 V	а			В	5.0 V			
13	Ω	OUT					!	OUT			OUT				OUT				OUT				
12	10		OUT			OUT						TUO				TUO				TUO			
11	GND	GND	"	"	n	×		n n	"	3	3	3	3	3	3	3	3	"	я	n	3	n	
10	<u>Q</u> 2				OUT				OUT				OUT					OUT				OUT	
o o	Q2			DUT						OUT				OUT			OUT				OUT		Ī
8 10	Preset 2			5.0 V	5.0 V				Z	Z			Z	Z			5.0 V	В			Ф	5.0 V	
7	Clock 2			Z	Z												Z	Z			Z	Z	
12	D2			ш	Э												(A) NI	(A) NI			IN (B)	IN (B)	Ī
5 13	Clear 2			5.0 V	V 0.3				<u>Z</u>	Z			Z	Z			ш	2.0 V			5.0 V	В	
4 14	Vcc	2.0 V	n	n	n	"		,,	"	3	,,	n	з	"	"	з	"	n	"	n	ä	99	= -55°C.
e +	Clear 1	2.0 \	5.0 V			Z		Z			Z	Z			ш	5.0 V			5.0 V	ш			except T _C
2	D1	Е	Е												IN (A)	N (A)			IN (B)	IN (B)			group 10,
- 8	Clock 1	Z	Z												Z	Z			Z	Z			as for subg
Case A, B D Case C	Test No.	102	103	104	105	106		107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	tions and limits
MIL-STD- 883	method	(Fig. 11)	"	29	"	3003 ((Fig. 10)	` ·	9	39	z	3	39	29	3	3003 <u>5/</u> (Fig. 11)	(Fig. 12)	(Fig. 11)	(Fig. 12)	(Fig. 12)	(Fig. 11)	(Fig. 12)	(Fig. 11)	Same tests, terminal conditions and limits as for subgroup 10, except T_{C}
Symbol		F _{MA×} 6/	я	77	"	фгн	:	35	3	z	t _{PHL}		3	з	фгн	3	z	3	фн∟	з	з	a	Same tests,
Subgroup		10	$T_{\rm C} = 125^{\circ}{\rm C}$	39	"	u			33	99	29	35	35	"	79	35	79	31	*	3	3	99	11

NOTES:
A = Normal clock pulse.
B = Momentary GND, then 4.5 V.

E = Input D connected to \overline{Q} .

^{1/} Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.</p>
4/ Tests shall be performed in sequence.
5/ Tests shall be performed for both D input pulses (A and B).
6/ F_{M×x}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

MIL-M-38510/2G

5. PACKAGING

5.1 <u>Packaging requirements</u>. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)

- 6.1 <u>Intended use.</u> Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.
 - 6.2 Acquisition requirements. Acquisition documents should specify the following:
 - a. Title, number, and date of the specification.
 - b. PIN and compliance identifier, if applicable_ (see 1.2).
 - c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
 - d. Requirements for certificate of compliance, if applicable.
 - e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
 - f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
 - g. Requirements for product assurance options.
 - h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
 - I Requirements for "JAN" marking.
 - j. Packaging Requirements (see 5.1)
- 6.3 <u>Qualification</u>. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43218-3990.
- 6.4 <u>Superseding information</u>. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

MIL-M-38510/2G

6.5 <u>Abbreviations, symbols, and definitions.</u> The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

GND	Electrical ground (common terminal)
V _{IN}	Voltage level at an input terminal

- 6.6 <u>Logistic support.</u> Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.
- 6.7 <u>Substitutability.</u> The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type
01	SN5472 (Circuit A)
01	DM5472 (Circuit B)
01	MC5472 (Circuit C)
02	SN5473 (Circuit A)
02	DM5473 (Circuit B)
02	S5473 (Circuit C)
03	SN54107 (Circuit A)
03	DM54107 (Circuit B)
03	S54107 (Circuit C)
04	SN5476 (Circuit A)
04	DM5476 (Circuit B)
04	S5476 (Circuit C)
05	5474 (Circuit A)
05	DM5474 (Circuit B)
06	5470
07	SN5479 (Circuit A)
07	MC5479 (Circuit B)

6.8 <u>Change from previous issue.</u> Marginal notations are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

MIL-M-38510/2G

Custodians:

Army - CR Navy - EC Air Force - 11 Preparing activity: DLA - CC

Review activities:

DLA - CC

Army – SM, MI Navy - AS, CG, MC, SH TD Air Force – 03, 19, 99 (Project 5962-2096)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organization and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.