INCH-POUND
MIL-M-38510/210E
27 March 2006
SUPERSEDING
MIL-M-38510/210D
16 May 1986

MILITARY SPECIFICATION

MICROCIRCUIT, DIGITAL, 16,384 BIT SCHOTTKY, BIPOLAR, PROGRAMMABLE READ-ONLY MEMORY (PROM), MONOLITHIC SILICON

Inactive for new design after 24 July 1995

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, programmable read-only memory (PROM) microcircuits which employ thin film nichrome (NiCr) resistors, platinum-silicide, tungsten (W), titanium-tungsten (TiW) or zapped vertical emitter as the fusible link or programming element. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

Device type	Circuit	Access times (ns)
01	2048 words/8 bits per word PROM with uncommitted collector	100, 50
02	2048 words/8 bits per word PROM with active pull-up and a third high-impedance state output	100, 50
03	2048 words/8 bits per word PROM with uncommitted collector	55, 30
04	2048 words/8 bits per word PROM with active pull-up And a third high-impedance state output	55, 30
05	4096 words/4 bits per word PROM with active pull-up and a third high-impedance state output	80, 40

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to mailto:memory@dla.mil . Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil

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1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -10 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction to case (θ_{JC}): 1/	
Cases J, L, and R	40°C/W maximum
Case K	60°C/W maximum
Case 3	0.08°C/W maximum 2/
Output voltage range	-0.5 V dc to +V_{CC}
Output sink current	100 mA
Maximum power dissipation (P_D) 3/	1.02 W
Maximum,unction temperature (T_J) 4/	+175°C

1.4 Recommended operating conditions.

Supply voltage	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc
Normalized fanout (each output)	8 mA 5/
Case operating temperature range (T_C)	-55 °C to +125 °C

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outline

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1/ Heat sinking is recommended to reduce the junction temperature.
2/ When a thermal resistance value is included in MIL-STD-1835, it shall supersede the value stated herein.
3/ Must withstand the added P_D due to short circuit test (e.g. I_{OS}).
4/ Maximum junction temperature shall not be exceeded except for allowable short circuit duration burn-in screening conditions per method 5004 of MIL-STD-883.
5/ 16 mA for circuits A, B, D, F, H, and I devices.

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(Copies of these documents are available online at *http://assist.daps.dla.mil/quicksearch/* or *http://assist.daps.dla.mil* or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Truth table

3.3.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered itme drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.3.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.3.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table II, and where applicable, the altered item drawing. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$	Device type	Limits		Unit
				Min	Max	
High-level output voltage	V_{OH}	V_{CC} = 4.5 V; I_{OH} = -2 mA; V_{IH} = 2.0 V; V_{IL} = 0.8 V	02,04,05	2.4		V
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V; I_{OL} = 8 mA; 2/ V_{IH} = 2.0 V; V_{IL} = 0.8 V	01,02 03,04,05		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V; I_{IN} = -10 mA; T_C = 25°C	01,02 03,04,05		-1.5	V
Maximum collector cut-off current	I_{CEX}	V_{CC} = 5.5 V; V_O = 5.2 V	01,03		100	µA
High-impedance (off-state) output high current	I_{OHZ}	V_{CC} = 5.5 V; V_0 = 5.2 V	02,04,05		100	µA
High-impedance (off-state) output low current	I_{OLZ}	V_{CC} = 5.5 V; V_0 = 0.5 V	02,04,05		-100	µA
High-level input current	I_{IH}	V_{CC} = 5.5 V; V_{IN} = 5.5 V	01,02 03,04,05		50	µA
Low-level input current	I_{IL}	V_{CC} = 5.5 V; V_{IN} = 0.5 V	01,02 03,04,05		-250	µA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V; V_0 = 0.0 V 3/	02,04,05	-10	-100	mA
Supply current	I_{CC}	V_{CC} = 5.5 V; V_{IN} = 0; outputs = open	01,02 03,04,05		185	mA
Propagation delay time, high-to-low level logic, address to output	t_{PHL1}	V_{CC} = 4.5 V and 5.5 V; C_L = 30 pF (see figure 4)	01,02		100	ns
			03,04		55	
			05		80	
Propagation delay time, low-to-high level logic, address to output	t_{PLH1}		01,02		100	ns
			03,04		55	
			05		80	
Propagation delay time, high-to-low level logic, enable to output	t_{PHL2}		01,02		50	ns
			03,04		30	
			05		40	
Propagation delay time, low-to-high level logic, enable to output	t_{PLH2}		01,02		50	ns
			03,04		30	
			05		40	

1/ Complete terminal conditions shall be specified in table III.

2/ I_{OL} = 16 mA for circuits A, B, D, F, H, I, and J.

3/ Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

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TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III) 1/, 2/, 3/	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters for unprogrammed devices	1*, 2, 3, 7*, 8	1*, 2, 3, 7*, 8
Final electrical test parameters for programmed devices	1*, 2, 3, 7* 8, 9, 10, 11	1*, 2, 3, 7*, 8, 9,
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8 9, 10, 11
Group B end-point electrical parameters subgroup 5	1, 2, 3, 7, 8, 9, 10, 11	N/A
Group C end-point electrical parameters	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8
Group D test requirements	1, 2, 3, 7, 8	1, 2, 3, 7, 8

1/ * PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 shall consist of verifying the pattern specified.

3.8 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.8.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.3.2.1, table II, and table III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.8.2 Maunufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see Appendix A MIL-PRF-38535.)

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.

d. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer’s discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein. Class S devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and as specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Electrical test requirements shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be omitted.

c. For unprogrammed devices, a sample shall be be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.3.2.1). If more than 2 devices fail to program, the lot shall be rejected, At the manufacturer’s option, the sample may be increased to 24 total devices with no more than 4 total device failures allowed.

d. For unprogrammed devices, 10 devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail in all three subgroups, the lot shall be rejected. At the manufacturer’s option, the sample may be increased to 20 total devices with no more that 4 total device failures allowed.

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4.4.2 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

c. For qualification, at least 50 percent of the sample selected for testing in subgroup 1 shall be programmed (see 3.3.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 1 tests.

4.4.3 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Programming procedure identification. The programming procedure to be utilized shall be identified by the manufacturer’s circuit designator. The circuit designator is cross referenced in 6.5 herein with the manufacturer’s symbol.

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4.7 Programming procedure for circuit A. The programming characteristics of table IVA and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming. The waveforms on figure 5A and the programming characteristics of table IVA shall apply to these procedures.

b. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible. An open circuit shall not be used to address the PROM.

c. Apply V_{PL} voltage to V_{CC}.

d. Bring the $\overline{CE}_X$ inputs high and the CE_X inputs low to disable the device. The chip enables are TTL compatible. An open circuit shall not be used to disable the device.

e. Disable the programming circuitry by applying a voltage of V_{OPD} to the outputs of the PROM.

f. Raise V_{CC} to V_{PH} with rise time less than or equal to t_{TLH}.

g. After a delay equal to or greater than t_{D1}, apply only one pulse with amplitude of V_{OPE} and duration of t_P to the output selected for programming. Note that the PROM is supplied with fuses intact, which generates an output high. Programming a fuse will cause the output to go low.

h. Lower V_{CC} to V_{PL} following a delay of t_{D2} from programming enable pulse applied to an output.

i. Enable the PROM for verification by applying V_{IL} to $\overline{CE}_X$ and V_{IH} to CE_X.

j. Apply V_{PHV} to V_{CC} and verify bit is programmed.

k. Repeat 4.7a through 4.7j for all other bits to be programmed in the PROM.

l. If any bit does not verify as programmed, it shall be considered a programming reject.

4.8 Programming procedure for circuit B. The programming characteristics of table IVB and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming. The waveforms on figure 5B and the programming characteristics of table IVB shall apply to these procedures.

b. Apply V_{IH} $\overline{CE}_1$ and the binary address of the PROM word to be programmed. Raise V_{CC} to V_{CCP}.

c. After a t_D delay, apply only one V_{OP} to the output to be programmed high. Apply V_{OP} to one output at a time.

d. After a t_D delay, a pulse $\overline{CE}_1$ to a V_{IL} level for a duration of t_P.

e. After t_P and a t_D delay, remove V_{OP} from the programmed output.

f. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OP} pulses to each output to be programmed and pulsing $\overline{CE}_1$ to the V_{IL} level, allowing for proper delays between V_{OP} and $\overline{CE}_1$.

g. Repeat 4.8b through 4.8e for all bits to be programmed.

h. To verify programming, lower V_{CCP} to V_{CC}. Connect a 10 kΩ resistor between each output and V_{CC}. Apply V_{IL} to $\overline{CE}_1$ input. The programmed outputs should remain in the high state and the unprogrammed outputs should go to the low level.

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i. If any bit does not verify as programmed, it shall be considered a programming reject.

4.9 Programming procedures for circuit C, device types 02 and 04. The programming characteristics of table IVC and the following procedures shall be used for programming device types 02 and 04.

a. Connect the device in the electrical configuration for programming. The waveforms on figure 5C, device types 02 and 04, and the programming characteristics of table IVC, device types 02 and 04, shall apply to these procedures.

b. Terminate all device outputs with a 10 kΩ resistor to V_{CC}. Apply V_{IH} to CE_1.

c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP}.

d. After a t_D delay (10 μs), apply only one V_{OUT} pulse to the output to be programmed. Program one output at a time.

e. After a t_D delay (10 μs), pulse $\overline{CE}_1$ input to logic "0" for a duration of t_P.

f. After a t_D delay (10 μs), remove the V_{OUT} pulse from the programmed output. (Programming a fuse will cause the output to go to a high-level logic in the verify mode.)

g. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OUT} pulses to each output to be programmed allowing a delay to t_D between pulses as shown on figure 5C.

h. Repeat 4.9b through 4.9g for all other bits to be programmed.

i. To verify programming, after t_D (10 μs) delay, lower V_{CC} to V_{CCH} and apply a logic "0" level to $\overline{CE}_1$ input. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} and verify that the programmed output remains in the "1" state.

j. If any bit does not verify as programmed, it shall be considered a programming reject.

4.10 Programming procedures for circuit C, device type 05. The programming characteristics of table IVC, device type 05, and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming. The output pins shall be terminated with a 10 kΩ resistor to GND and bypass VCC to GND with a 0.01 μF capacitor. The waveforms on figure 5C, device type 05, and the programming characteristics of table IVC, device type 05, shall apply to these procedures.

b. Disable the device by applying V_{IH} to $\overline{CE}_2$ input and V_{IL} to $\overline{CE}_1$. The chip enable pins are TTL compatible.

c. Apply V_{IL} to all other pins.

d. Address the PROM with the binary address of the selected word to be programmed and reset T_P = 5 μs. Address inputs are TTL compatible.

e. After a delay of TD_1, raise the V_{CC} pin to V_{CCP}.

f. After a delay of TD_2, raise the corresponding output pin to V_{OPF}.

g. After a delay of TD_3, lower $\overline{CE}_2$ to V_{IL} for a duration of T_P and simultaneously lower the output to V_{IL} and wait TD_4.

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h. Return the $\overline{CE}_2$ to V_{IH}.

i. Wait TD_5 and lower V_{CC} to V_{CCV}.

j. Wait TD_6 and lower $\overline{CE}_2$ to V_{IL} for the duration to T_V.

k. A properly blown fuse will read VOL and unblown fuse will read VOH.

1. If the fuse is blown, go to n.
2. If the fuse is unblown, go to 1.

l. If T_P is less than 30 μs, increment T_P by 5 μs and go to e. If T_P is ≥ 5 μs go to m.

m. If T_P is ≥ 30 μs, the device is a reject.

n. After a delay of TD_7, select the next output or address to be programmed.

o. Repeat steps 4.10d through 4.10k until all required addresses are programmed.

p. To verify the program keep V_{CC} pin at V_{CCV}. Apply V_{IL} to $\overline{CE}_2$. The programmed fuse will go to the low level and unblown fuse shall remain in the high level.

4.11 Programming procedures for circuit D. The programming characteristics on table IVD, and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming. The waveforms on figure 5D and the programming characteristics of table IVD shall apply to these procedures.

b. Select the word to be programmed by applying the appropriate voltages to the address pins as well as the required voltages to chip enable pins to select the device.

c. Apply the proper power, V_{CC} = 6.5 V, GND = 0 V.

d. Verify that the bit to be programmed is in the “0” logic state.

e. Enable the chip for programming by application of the chip enable voltage, $V_{P(CE1)}$ = 21.0 V to $\overline{CE}_1$ (pin 20). CE_2 and CE_3 should be left high.

f. Apply I_{OP} programming current ramp to the output to be programmed. The other outputs shall be left open. Only one output may be programmed at a time. During the rise of the current ramp, the required current will be achieved to program the junction. As programming occurs a drop in voltage can be sensed at the output of the device. Upon detection of V_{PS}, the current shall be held for t_{hap} and then shut off.

g. Verify that the programmed bit is in the “1” logic state. Lower $V_{P(CE1)}$ to 0 V and read the output.

Note: The PROM is supplied with fuses generating a low-level logic output. Programming a fuse will cause the output to go to a high-level logic in the verify mode.

h. Lower V_{CC} to 0 V. The power supply duty cycle shall be equal to or less than 50 percent.

i. If the bit verifies as not having been programmed at V_{CC} = 6.5 V, then repeat the programming ramp sequence up to 15 times until the bit is programmed. If after 16 programming attempts, the bit does not program, then the device shall be considered a reject.

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j. If the bit verifies as having been programmed at V_{CC} = 6.5 V, then one of the following two conditions shall be followed:

(1) If the current required to program was less than $I_{OP(max)}$, then proceed to step 1.

(2) If the current required to program was equal to or greater than IOP(max), then the device shall be considered a reject and no further attempts at programming other bits shall be attempted.

k. Repeat 4.11a through 4.11j for all other bits to be programmed.

l. If any bit does not verify as programmed, it shall be considered a programming reject.

4.12 Programming procedures for circuit E. The programming characteristics for this device have been discontinued.

4.13 Programming procedures for circuit F. The programming characteristics on table IVF and the following procedures shall be used for programming the devices:

a. Connect the device in the electrical configuration for programming. The waveforms on figure 5F and the programming characteristics of table IVF shall apply to these procedures.

b. Raise V_{CC} to 5.5 V.

c. Address the PROM with binary address of the selected word to be programmed. Address inputs are TTL compatible.

d. Disable the chip by applying V_{IH} to the $\overline{CE}$ inputs and V_{IL} to the CE inputs. The chip enable inputs are TTL compatible.

e. Apply the V_{PP} pulse to the programming pin $\overline{CE}_1$. In order to insure that the output transistor is OFF before increasing voltage on the output pin, the program pins voltage pulse shall precede the output pins programming pulse by T_{D1} and leave after the programming pins programming pulse by T_{D2} (see figure 5F).

f. Apply one V_{OUT} pulse with duration of t_P to the output selected for programming. The outputs shall be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.

Note: The PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.

g. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.

h. Repeat 4.13b through 4.13g for all other bits to be programmed.

i. Enable the chip by applying V_{IL} to the $\overline{CE}$ inputs and V_{IH} to the CE inputs, and verify the program. Verification may check for a low output by requiring the device to sink 12 mA at V_{CC} = 4.2 V and 0.2 mA at V_{CC} = 6.2 V at T_C = 25°C.

j. If any bit does not verify as programmed, it shall be considered a programming reject.

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4.14 Programming procedures for circuit G. The programming characteristics on table IVG and the following procedures shall be used for programming the devices:

a. Connect the device in the electrical configuration for programming. The waveforms on figure 5G and the programming characteristics of table IVG shall apply to these procedures.

b. Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more 'active low' chip Enable inputs. NOTE: Address and Enable inputs must be driven with TTL logic levels during programming and verification.

c. Increase V_{CC} from nominal to V_{CCP} (10.5 ±0.5 V) with a slew rate limit of I_{RR} (1.0 to 10.0 V/μs). Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0 V.

d. Select the output where a logical high is desired by raising that output voltage to V_{OP} (10.5 ±0.5 V). Limit the slew rates to I_{RR} (1.0 to 10.0 V/μs). This voltage change may occur simultaneously with the V_{CC} increase to V_{CCP}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kΩ minimum (remember that the outputs of the device are disabled at this time).

e. Enable the device by taking the chip Enable(s) to a low level. This is done with a pulse PWE for 10 μs. The 10 μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.

f. Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 5.0 V (±0.25 V). The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits.

g. If the device is not to be tested for V_{OH} over the entire temperature range subsequent to programming, the verification of step 4.14f is to be performed at a V_{CC} level of 4.0 V (±0.2 V). V_{OH}, during the 4 V verification, must be at least 2.0 V. The 4 V V_{CC} verification assures minimum V_{OH} levels over the entire temperature range.

h. Repeat 4.14b through 4.14f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of VCC at the programming voltage must be limited to a maximum of 25 percent. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

i. If any bit does not verify as programmed, it shall be considered a programming reject.

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4.15 Programming procedures for circuit H. The programming characteristics of table IVH and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming. The waveforms on figure 5H and the programming characteristics of table IVH shall apply to these procedures.

b. Address the word to be programmed, apply 5 V to V_{CC} and active levels to all chip Enable inputs.

c. Verify the status of a bit location by checking the output level.

d. Decrease V_{CC} to 0 V.

e. For bit locations that do not require programming, skip steps 4.15f through 4.15l.

f. Increase V_{CC} to $V_{CC(pr)}$ with a minimum current capability of 250 mA.

g. Apply $V_{S(pr)}$ to all chip Enable inputs. $I_I \leq 25$ mA. Active-high enables may be left high.

h. Connect all outputs, except the one to be programmed, to V_{IL}. Only one bit is to be programmed at a time.

i. Apply the output programming pulse for 20 μs. Minimum current capability of the programming supply should be 250 mA.

j. After terminating the output pulse, disconnect all outputs from V_{IL} conditions.

k. Reduce the voltage at $\overline{CE}$ input to V_{IL}.

l. Decrease V_{CC} to 0 V.

m. Return to 4.15e until all outputs in the word have been programmed.

n. Repeat 4.15c through 4.15l for each word in memory.

o. Verify programming of every word after all words have been programmed using V_{CC} values of 4.5 V and 5.5 V.

p. If any bit does not verify as programmed, it shall be considered a programming reject.

4.16 Programming procedures for circuit I. The programming characteristics in table IVI and the following procedures shall be used for programming the device:

a. Connect the device in the electrical configuration for programming. The waveforms on figure 5I and the programming characteristics of table IVI shall apply to these procedures.

b. Terminate all outputs with a 300 Ω resistor to V_{ONP}. Apply V_{IHP} to the $\overline{CE}_2$, CE_3, and CE_4 inputs and V_{ILP} to the $\overline{CE}_1$ inputs.

c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP}.

d. After a delay of t_1, apply only one V_{OP} pulse with a duration of t_P, t_2 and $d(V_{OP})/dt$ to the output selected for programming. After a delay of t_2 and $d(V_{OP})/dt$, pulse $\overline{CE}_2$ from V_{IHP} to V_{CEP} for the duration of t_P, $2d(V_{CE})/dt$, and t_3; $\overline{CE}_2$ is then to go to V_{ILP} level.

e. To verify programming after $\overline{CE}_1$ has been set to V_{ILP}, lower V_{CC} to V_{CCL} after a delay of t_4. The programmed output should remain in the logic '1' state.

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f. The outputs should be programmed one output at a time, since the internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a low-level logic output. Programming a fuse will cause the output to go to a high level logic in the verify mode.

g. Repeat 4.16b through 4.16f for all other bits to be programmed.

h. If any bit does not verify as programmed, it shall be considered a programming reject.

4.17 Programming procedures for circuit J. The programming characteristics in table IVJ and the following procedures shall be used for programming the device:

a. Connect the device in the electrical configuration for programming. The waveforms on figure 5J and the programming characteristics of table IVJ shall apply to these procedures.

b. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.

c. Disable the chip by applying input high (V_{IH}) to the $\overline{CS}$ input. $\overline{CS}$ input must remain at V_{IH} for programming. The chip select is TTL compatible. An open circuit should not be used to disable the chip.

d. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.

e. Raise V_{CC} to V_{PH} with rise time equal to t_r.

f. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_P to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.

g. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.

h. Lower V_{CC} to 4.5 V following a delay of t_d from the last programming enable pulse applied to an output.

i. Enable the PROM for verification by applying a logic “0” (V_{IL}) to the $\overline{CS}$ input.

j. Repeat 4.17a through 4.17i for all other bit to be programmed in the PROM.

k. If any bit does not verify as programmed, it shall be considered a programming reject.

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Device type	01, 02, 03, 04	05	02 and 04
Case outline	J, K, and L	R	3
Terminal number	Terminal symbol		
1	A7	A8	NC
2	A6	A7	A7
3	A5	A6	A6
4	A4	A5	A5
5	A3	A4	A4
6	A2	A3	A3
7	A1	A2	A2
8	A0	A1	A1
9	O1	A0	A0
10	O2	GND	NC
11	O3	O4	O1
12	GND	O3	O2
13	O4	O2	O3
14	O5	O1	GND
15	O6	$\overline{CE}_2$	NC
16	O7	$\overline{CE}_1$	O4
17	O8	A11	O5
18	CE_3	A10	O6
19	CE_2	A9	O7
20	$\overline{CE}_1$	V_{CC}	O8
21	A10	----	NC
22	A9	----	CE_3
23	A8	----	CE_2
24	V_{CC}	----	$\overline{CE}_1$
25	----	----	A10
26	----	----	A9
27	----	----	A8
28	----	----	V_{CC}

FIGURE 1. Terminal connections.

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Device types 01, 02, 03, and 04

WORD NO.	6/	6/	6/	ADDRESS											DATA							
	$\overline{CE}_1$	CE_2	CE_3	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O8	O7	O6	O5	O4	O3	O2	O1
NA	L	H	H	X	X	X	X	X	X	X	X	X	X	X	5/	5/	5/	5/	5/	5/	5/	5/
NA	H	X	X	X	X	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC

Device type 05

WORD NO.	6/	6/	ADDRESS												DATA			
	$\overline{CE}_1$	$\overline{CE}_2$	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1
NA	L	L	X	X	X	X	X	X	X	X	X	X	X	X	5/	5/	5/	5/
NA	H	X	X	X	X	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC

NOTES:
1. NA = Not applicable.
2. X = Input may be high level, low level, or open circuit.
3. OC = Open circuit (high resistance output).
4. Program readout can only be accomplished with enable input at low level.
5. The outputs for an unprogrammed device shall be high for circuits A, C, (device type 05), E, F, and J and low for circuits B, C (device types 02, 04), D, G, and I.
6. Enable inputs are ANDED.

FIGURE 2. Truth table (unprogrammed).

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Device types 01 and 02
Circuit A

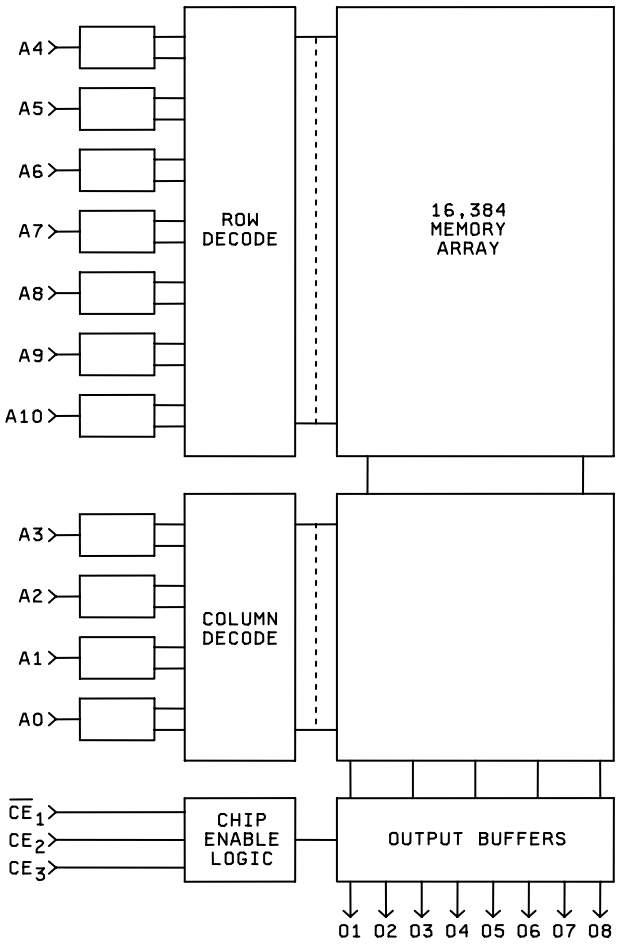

FIGURE 3. Functional block diagrams.

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Device type 05
Circuit A

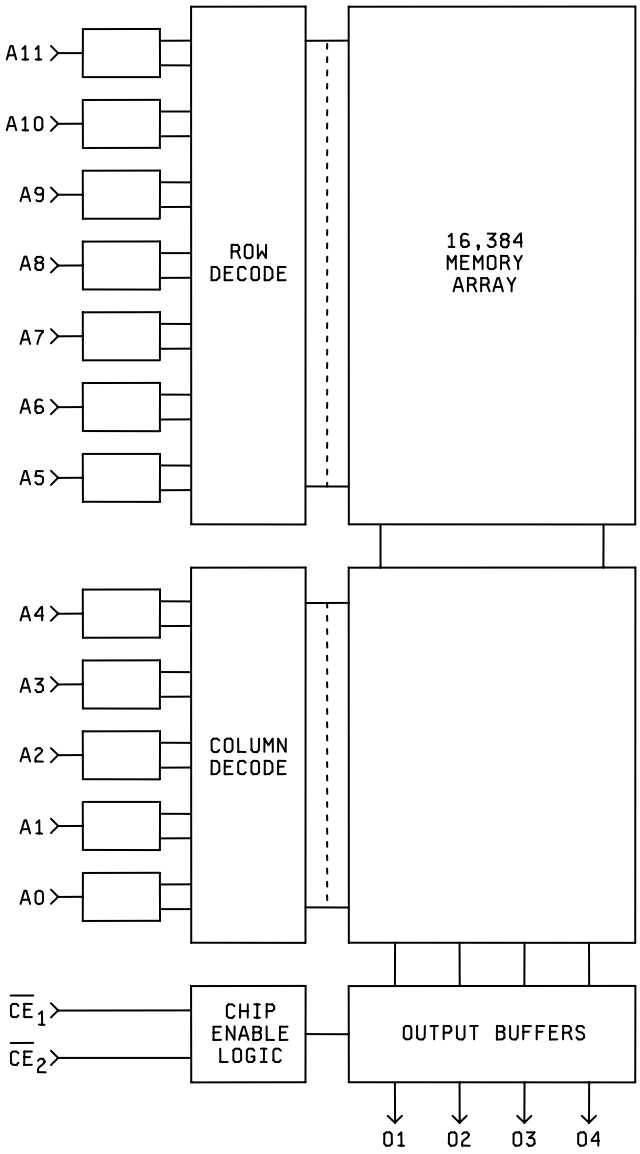

FIGURE 3. Functional block diagrams – Continued.

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Device types 01 and 02
Circuit B

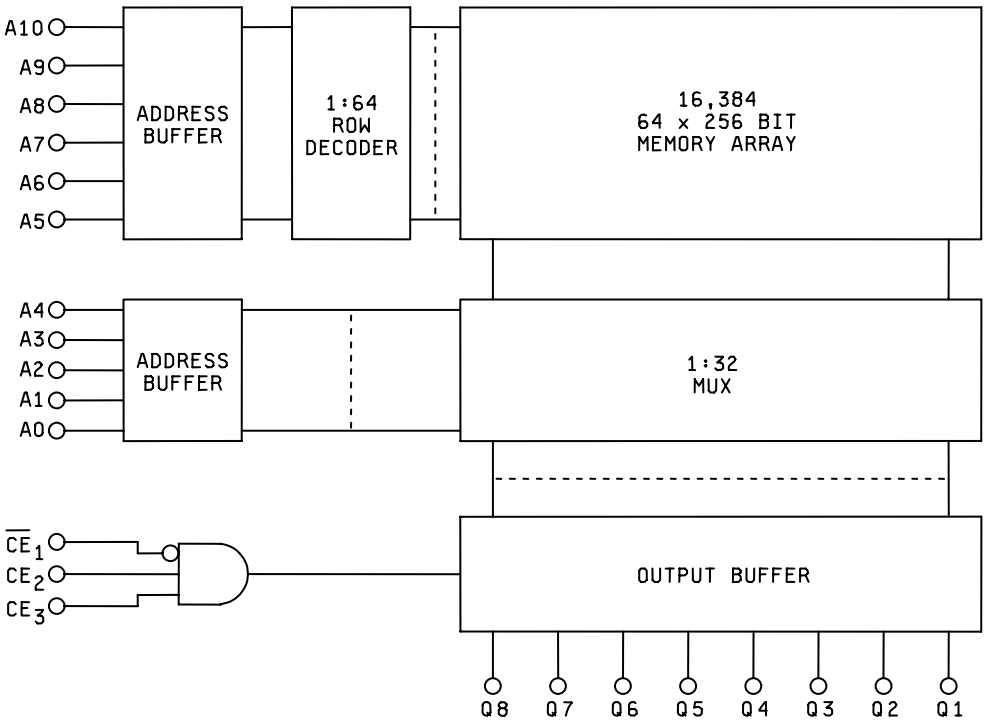

FIGURE 3. Functional block diagram – Continued.

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Device types 01, 02, and 04
Circuit C

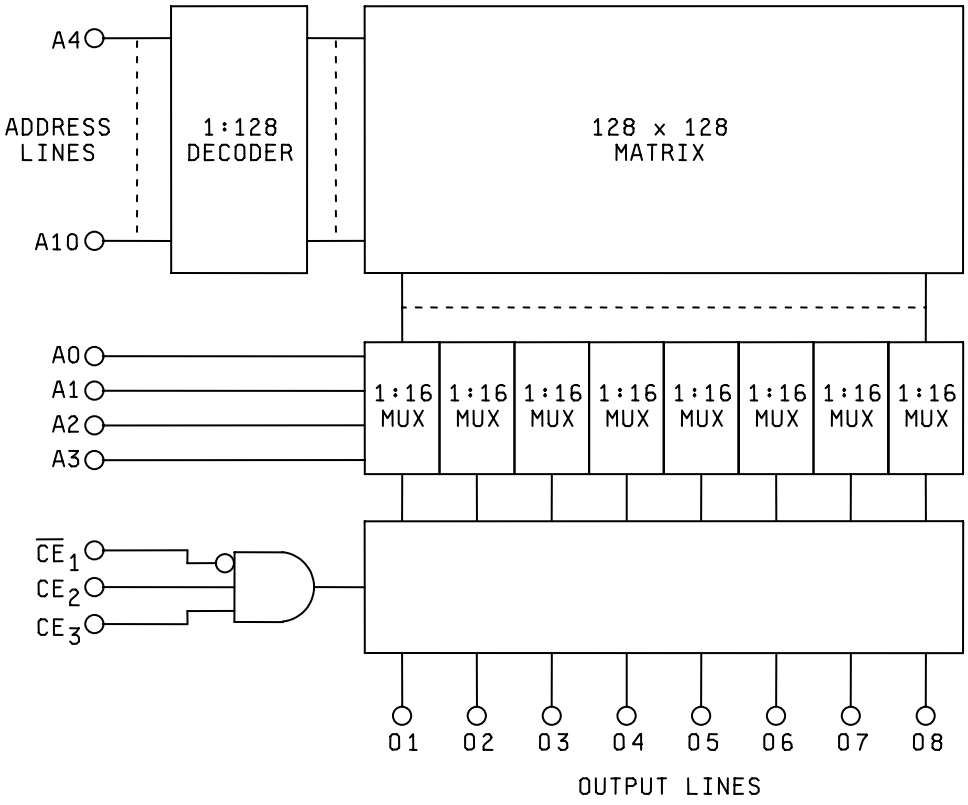

FIGURE 3. Functional block diagrams – Continued.

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Device type 05
Circuit C

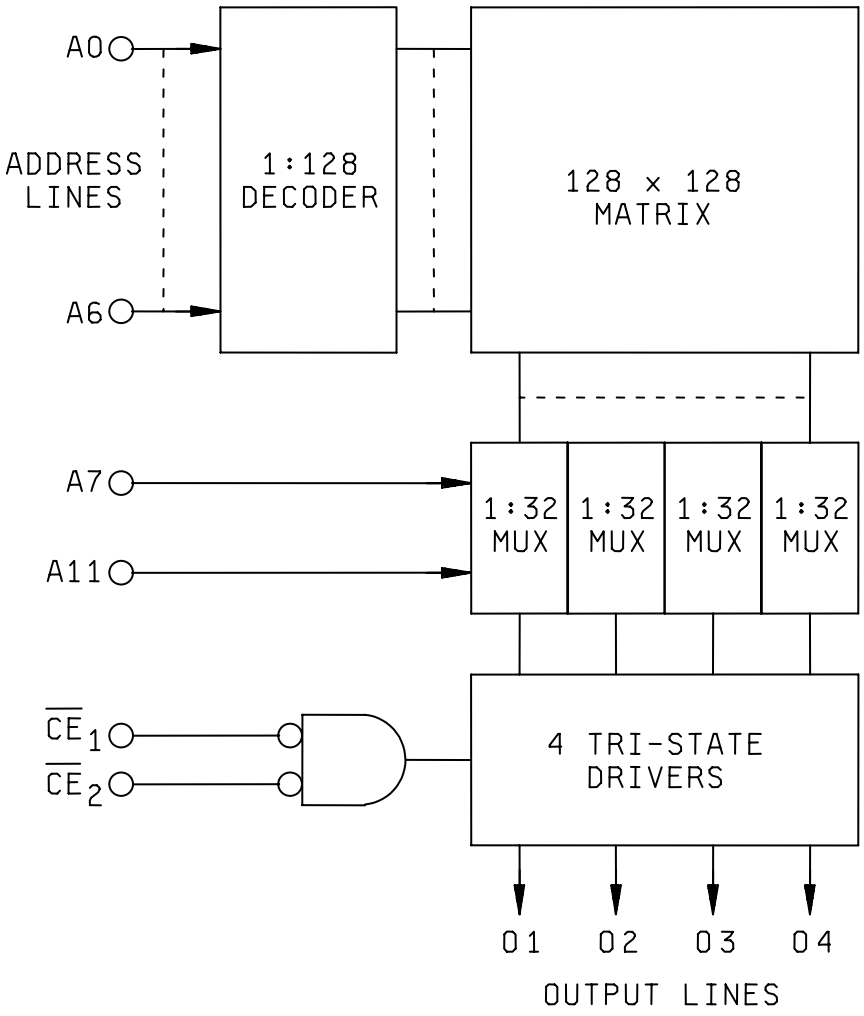

FIGURE 3. Functional block diagrams - Continued

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Device types 02, 03, and 04
Circuit D

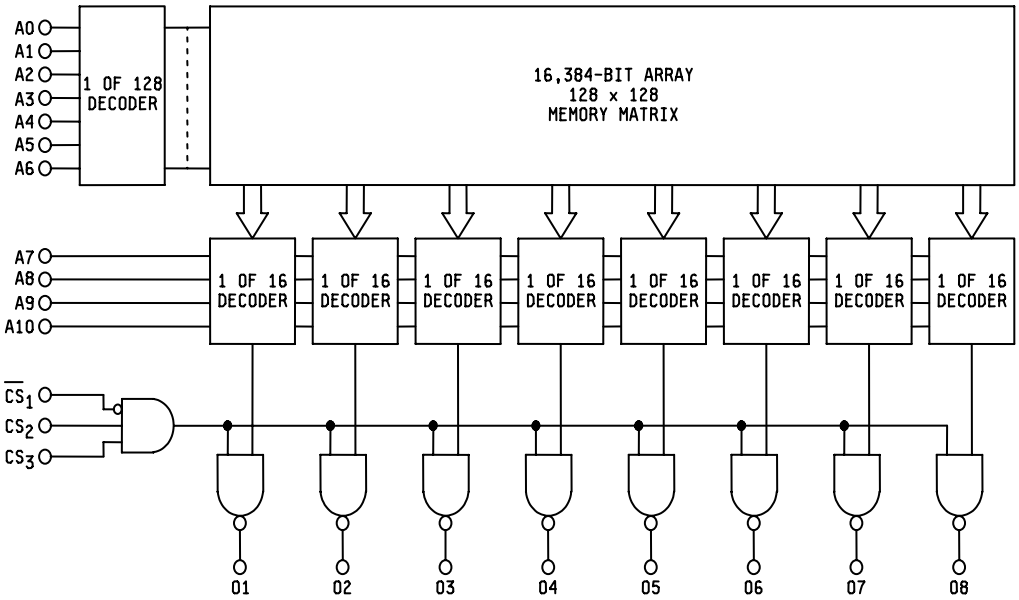

FIGURE 3. Functional block diagrams – Continued.

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Device type 02
Circuits F and I

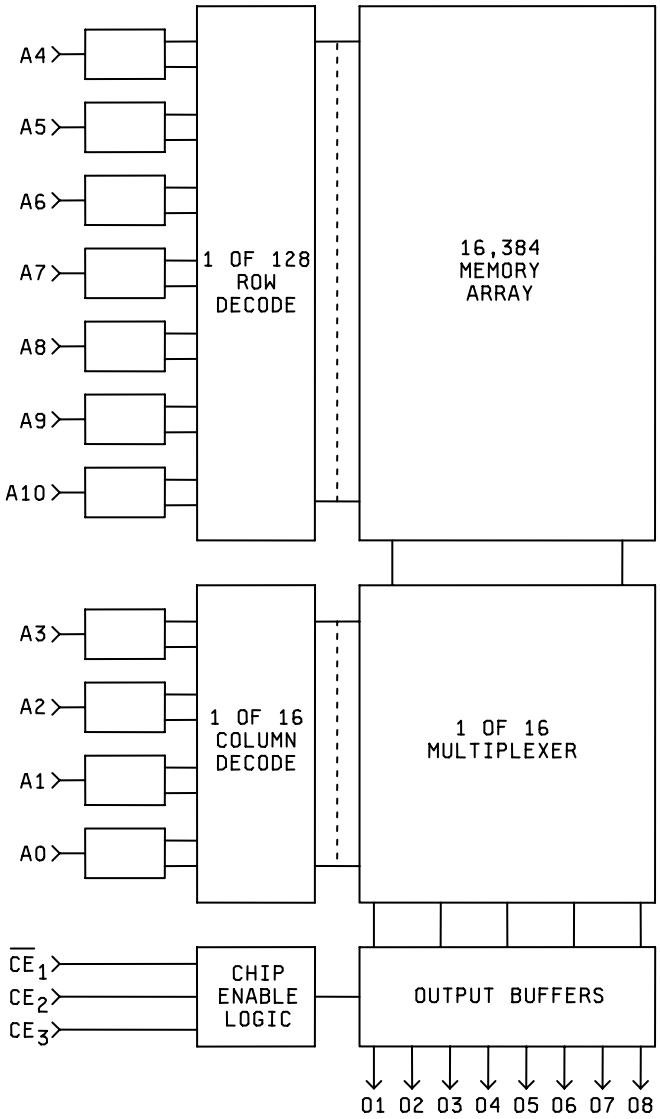

FIGURE 3. Functional block diagrams – Continued.

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Device type 01
Circuit G

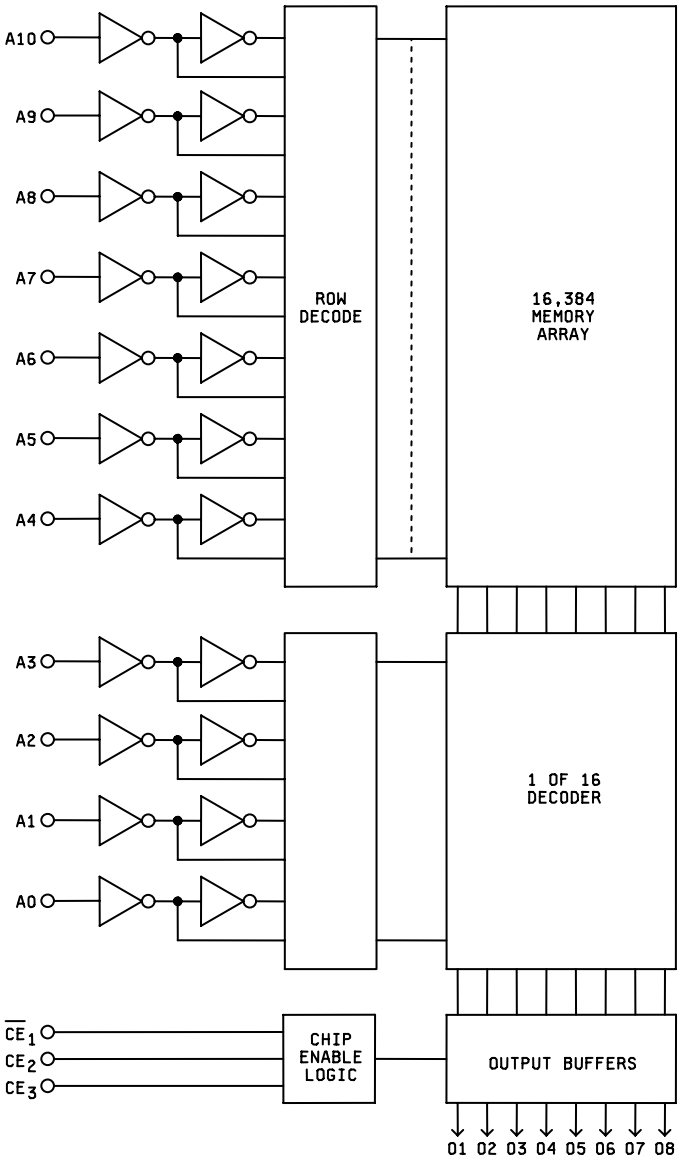

FIGURE 3. Functional block diagrams – Continued.

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Device type 02
Circuit G

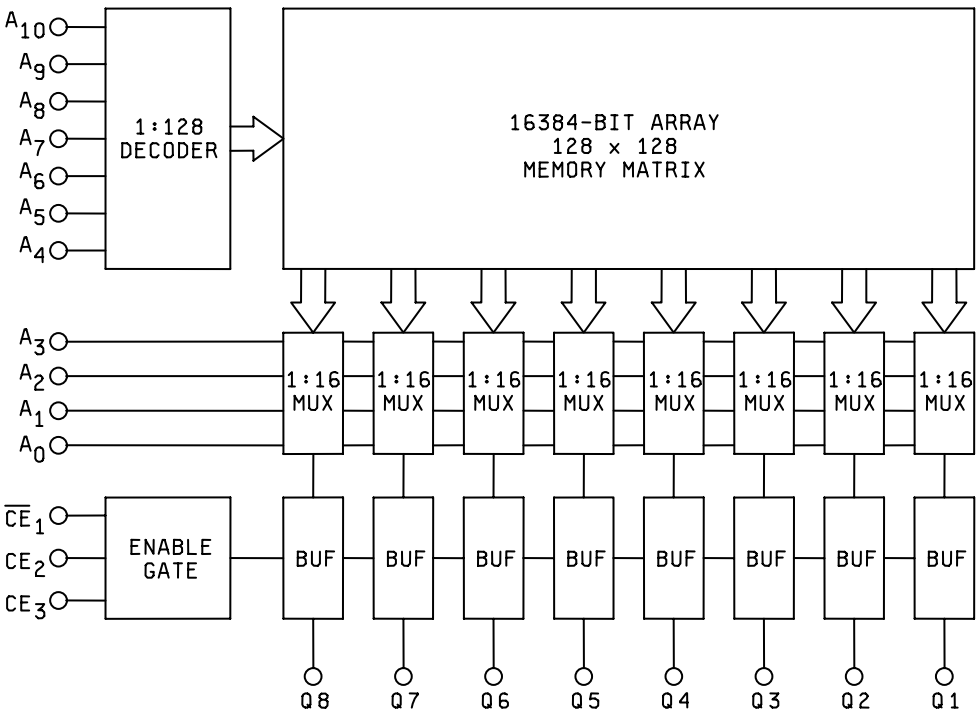

FIGURE 3. Functional block diagrams – Continued.

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Device types 02 and 04
Circuit H

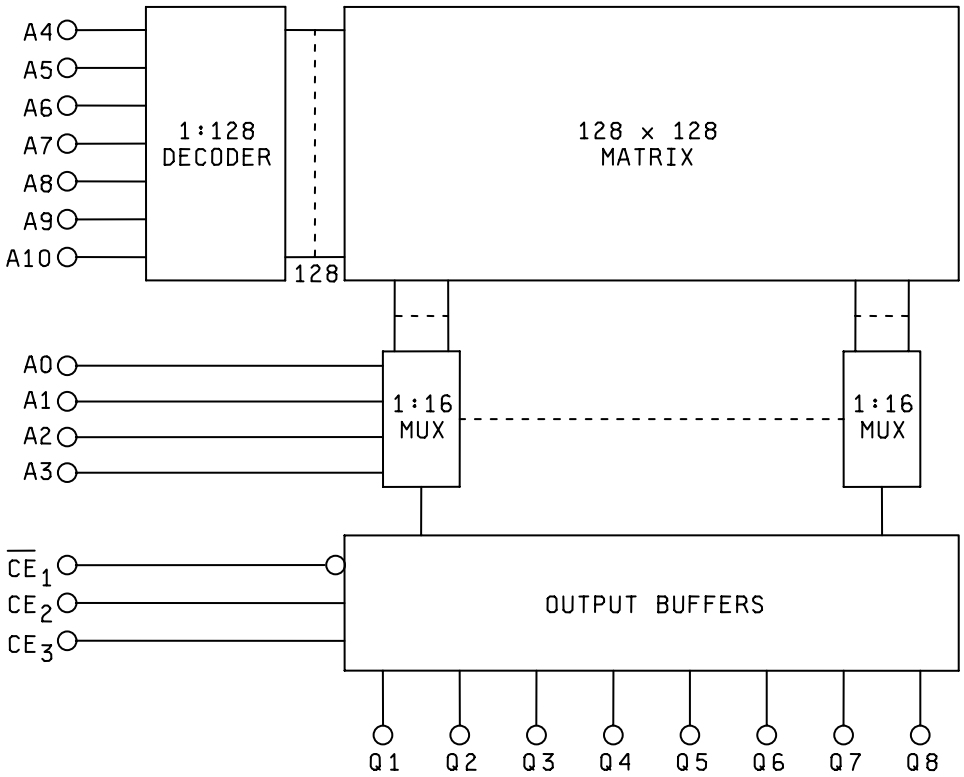

FIGURE 3. Functional block diagram – Continued.

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Device type 02
Circuit J

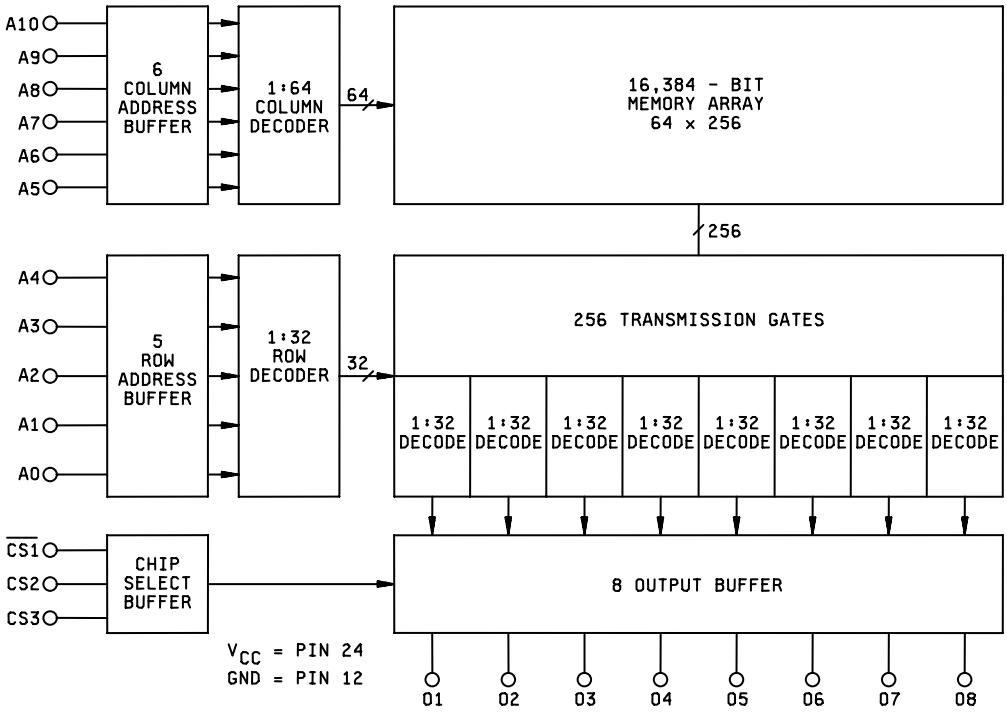

FIGURE 3. Functional block diagrams – Continued.

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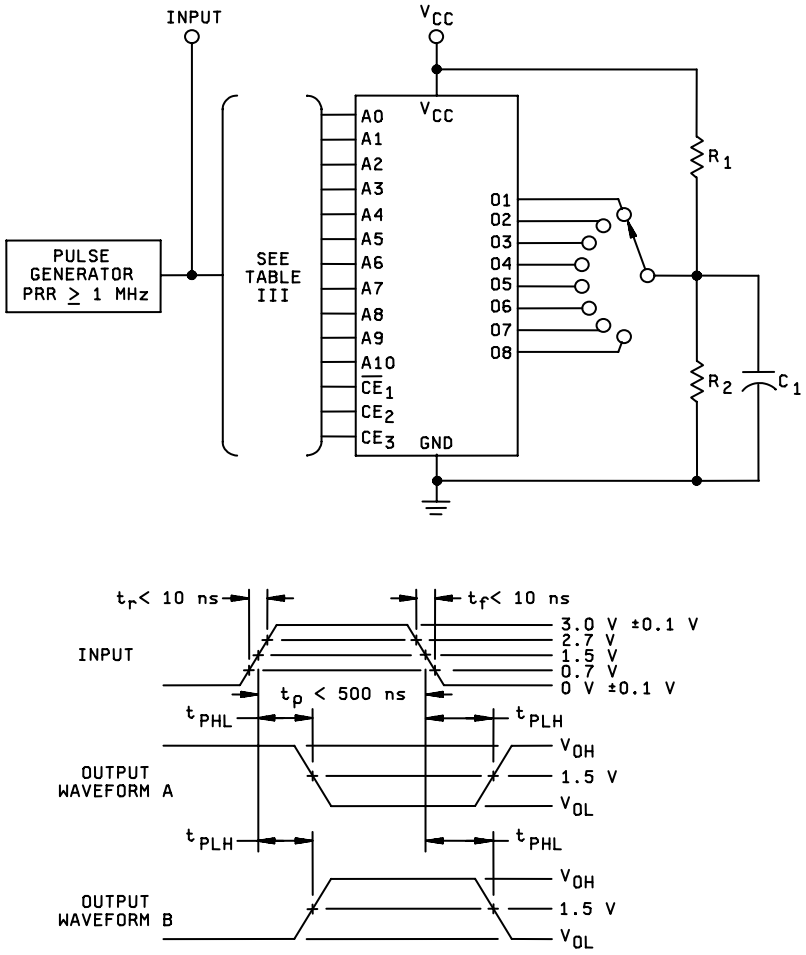
Device types 01, 02, 03, and 04



NOTES:
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory
2. C_L = 30 pF minimum, including jig and probe capacitance, R_1 =330 Ω ±25%, and R_2 = 680 Ω ±20%.
3. Outputs may be under load simultaneously.

FIGURE 4. Switching time test circuit.

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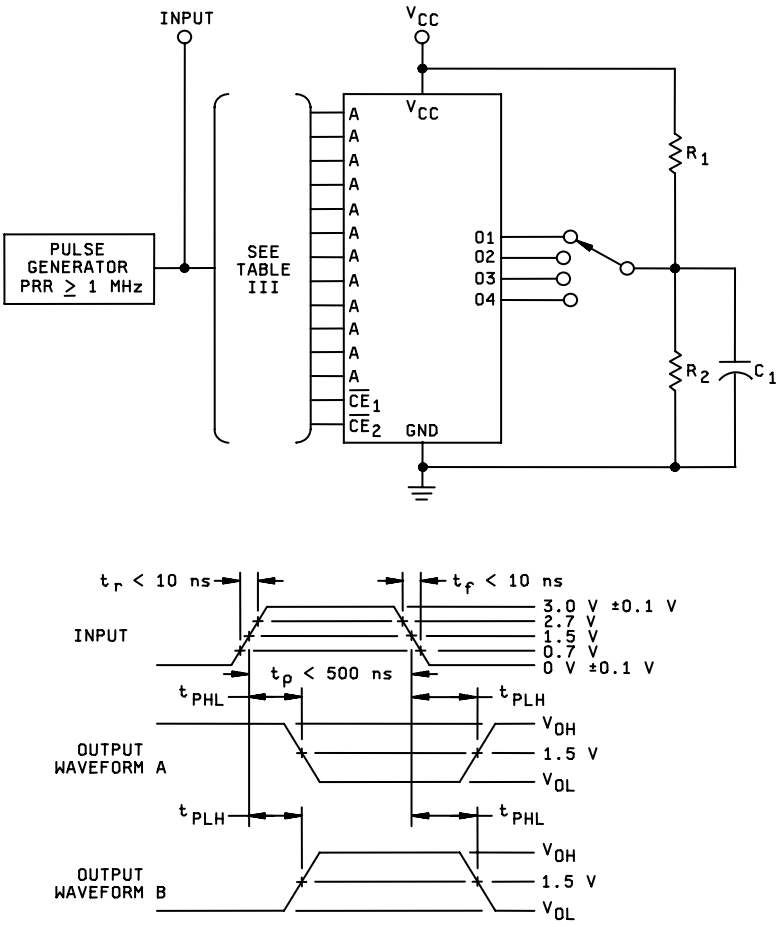
Device type 05



NOTES:
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory
2. C_L = 30 pF minimum, including jig and probe capacitance, R_1 =330 Ω ±25%, and R_2 = 680 Ω ±20%.
3. Outputs may be under load simultaneously.

FIGURE 4. Switching time test circuit – Continued.

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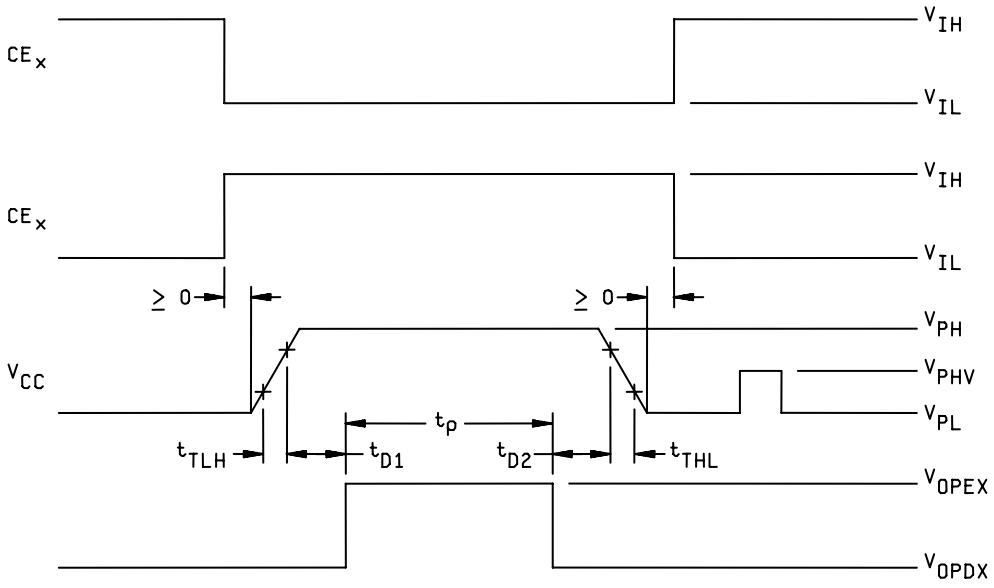

NOTE:
1. All other waveform characteristics shall be as specified in table IVA.

FIGURE 5A. Programming voltage waveforms during programming for circuit A.

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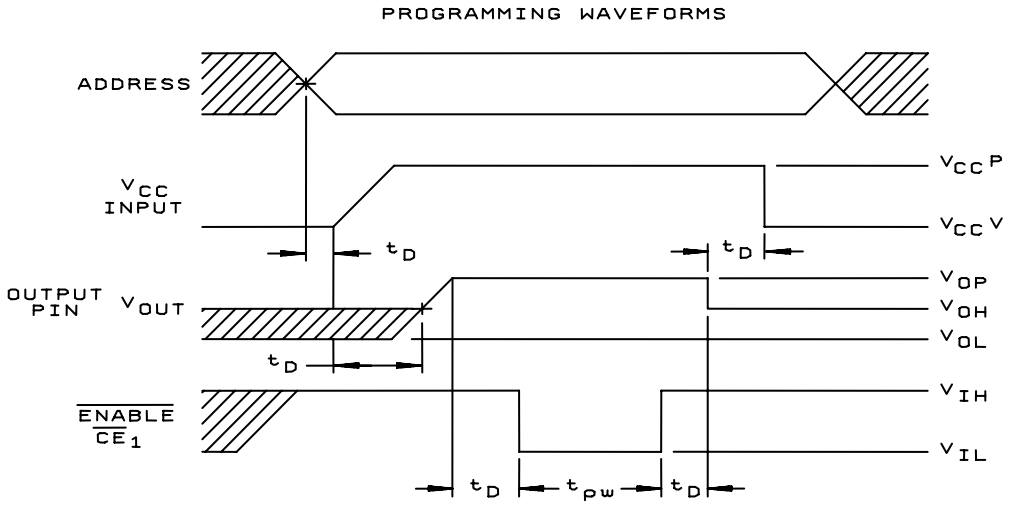
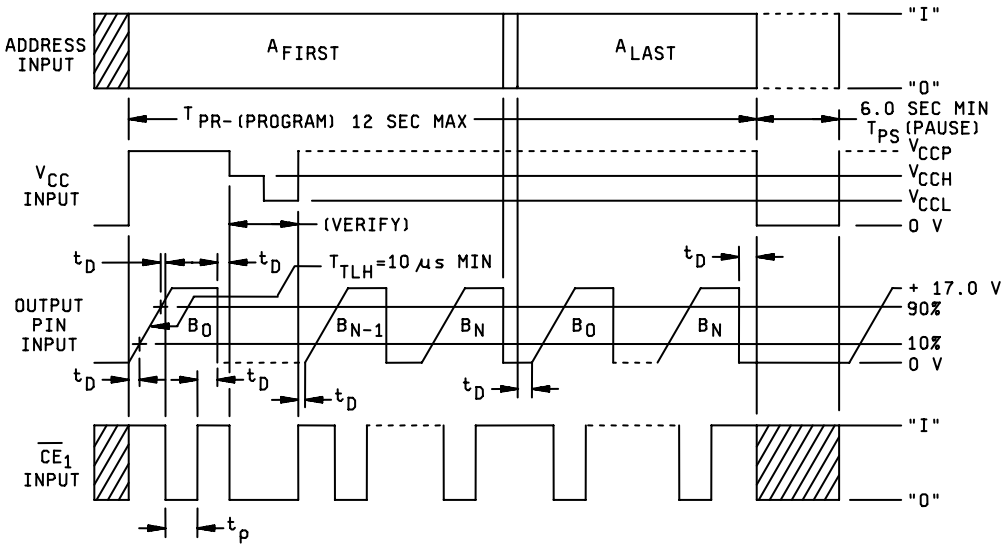


FIGURE 5B. Programming voltage waveforms during programming for circuit B.



NOTE: All other waveforms characteristics shall be as specified in table IVC.

FIGURE 5C. Programming voltage waveforms during programming for circuit C, device types 02 and 04.

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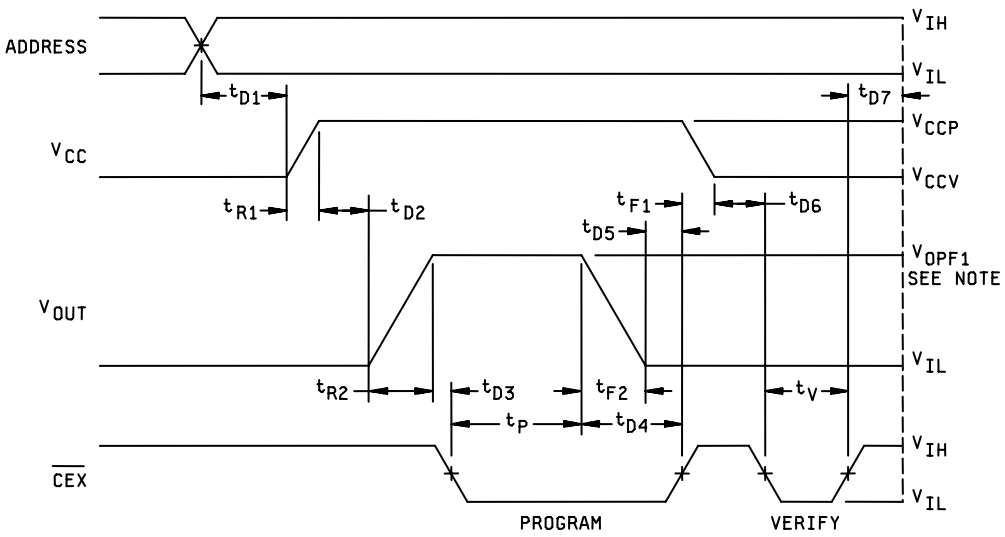

*Current clamp or voltage clamp will be needed.

FIGURE 5C. Programming voltage waveforms during programming for circuit C, device type 05 - Continued.

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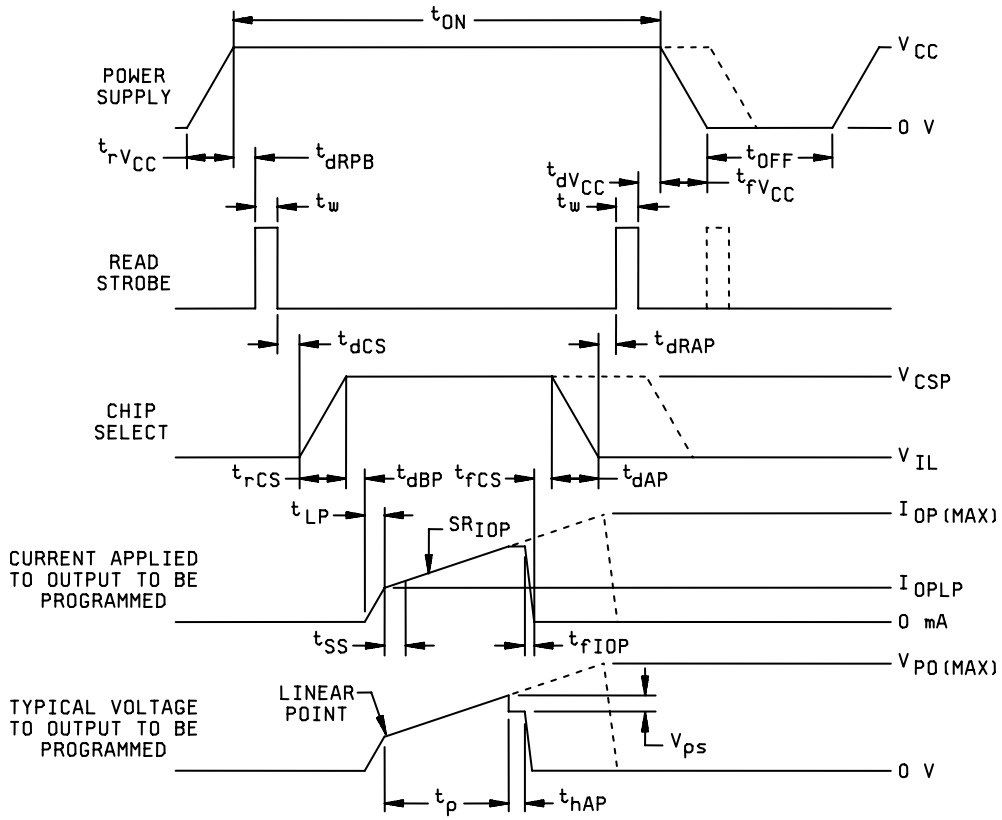

FIGURE 5D. Programming voltage waveforms during programming for circuit D.

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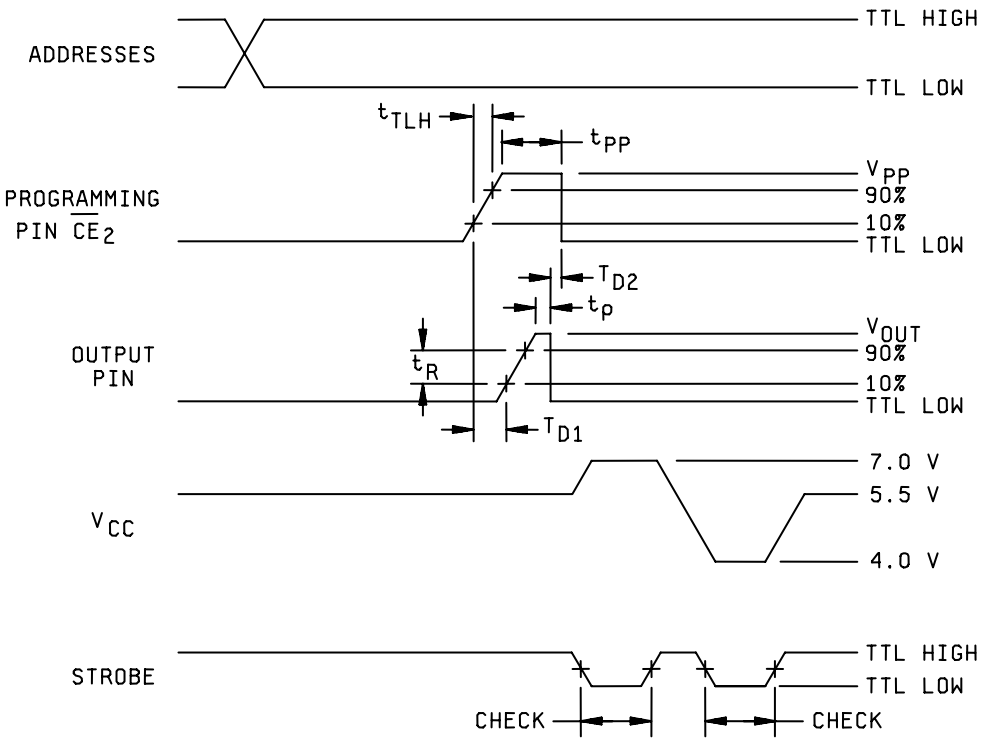
FIGURE 5E. Programming waveforms for circuit E have been discontinued.



NOTES:
1. Output load is 0.2 mA and 12 mA during 7.0 V and 4.0 V check, respectively.
2. All other waveform characteristics shall be as specified in table IVF.

FIGURE 5F Programming voltage waveforms during programming for circuit F.

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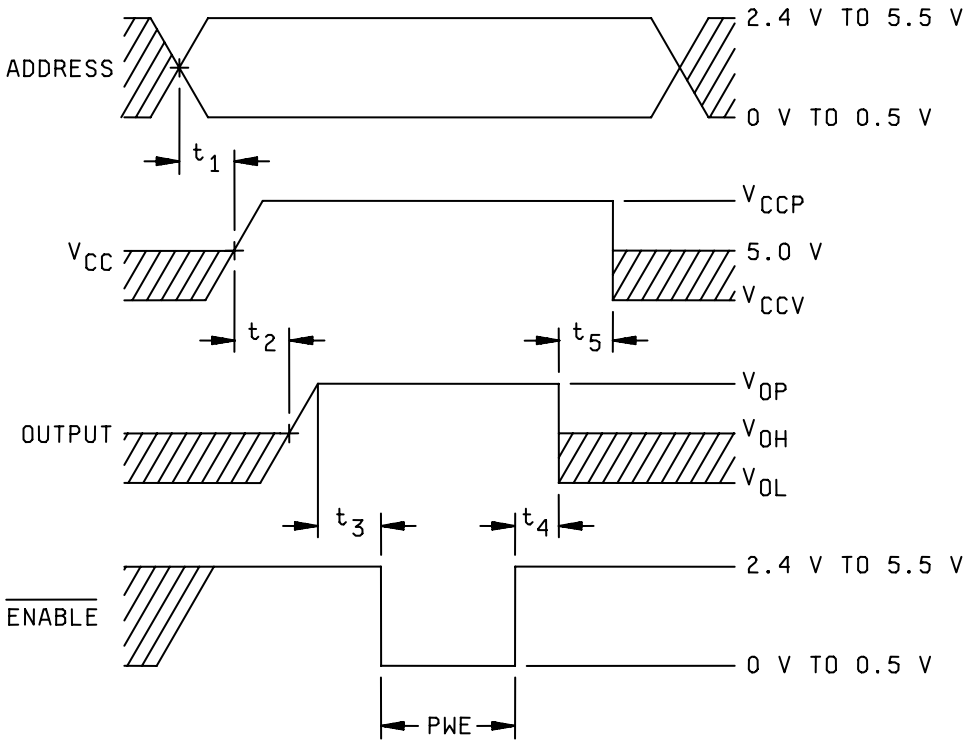

FIGURE 5G. Programming voltage waveforms during programming for circuit G.

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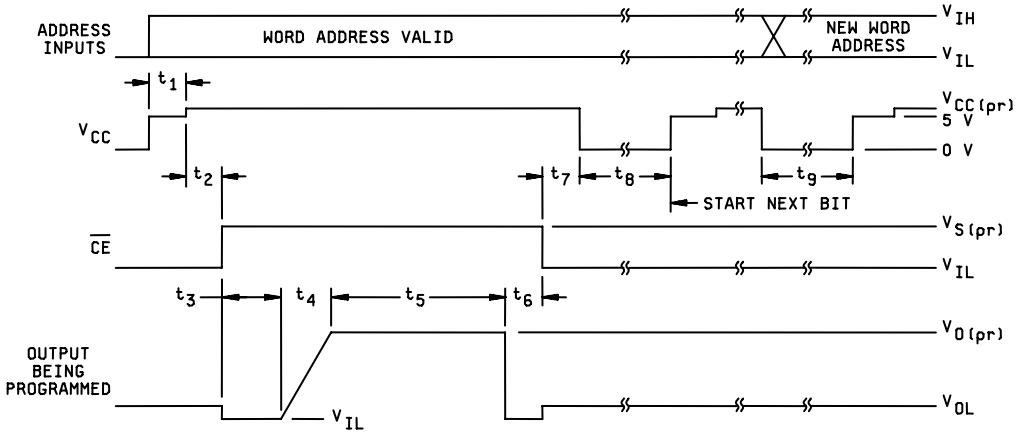

FIGURE 5H. Programming voltage waveforms during programming for circuit H.

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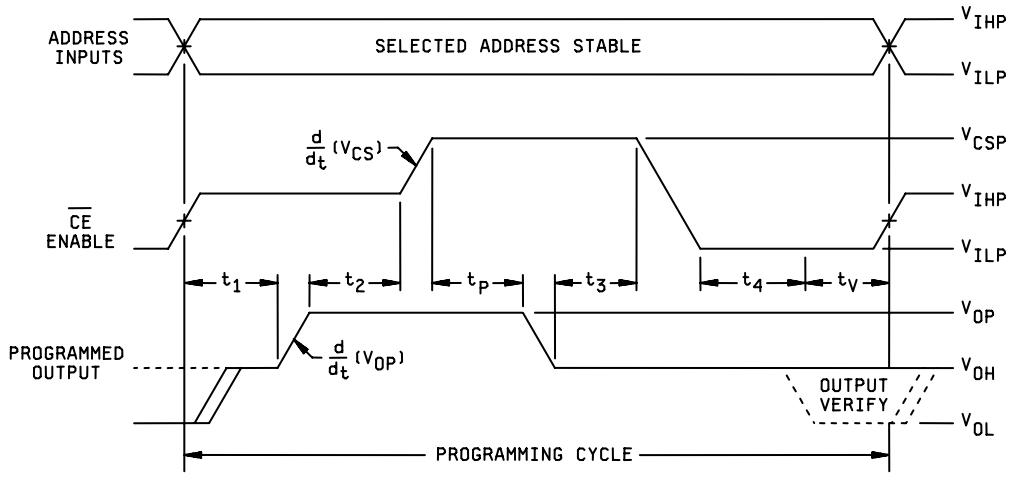

NOTES:
1. All delays between edges are specified from completion of the first edge, not midpoints.
2. Delays t_1, t_2, t_3, and t_4 must be greater than 100 ns; maximum delays of 1 μs are recommended to minimize heating during programming.
3. During t_V the output being programmed is switched to the load R and verified.
4. Outputs not being programmed are connected to V_{ONP} through resistor which provides output current limiting.

FIGURE 5I. Programming voltage waveforms during programming for circuit I.

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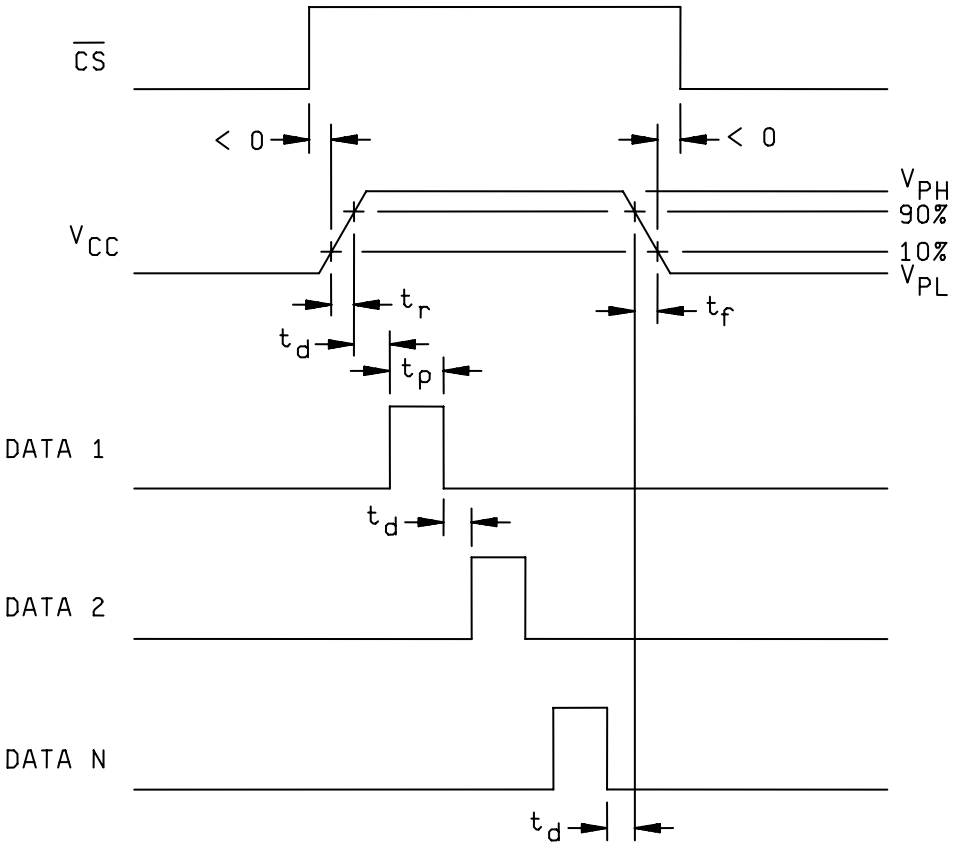

FIGURE 5J. Programming voltage waveforms during programming for circuit J.

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TABLE III. Group A inspection for device types 01 and 03.
Terminal conditions: (Outputs not designated are open or resistive coupled to GND or voltage.
Inputs not designated are high ≥ 2.0 V or ≤ 0.8 V.

Subgroup	Symbol	MIL-STD-883 method	Cases J,K	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		Unit
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	01	02	03	GND	04	05	06	07	08	CE_3	CE_2	$\overline{CE}_1$	A10	A9	A8	V_{CC}		Min	Max	
1 T_C=+25°C	V_{IC}		1 2 3 4 5 6 7 8 9 10 11 12 13 14	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA				GND “ “ “ “ “ “ “ “ “ “ “ “ “						-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	4.5V “ “ “ “ “ “ “ “ “ “ “ “ “	A7 A6 A5 A4 A3 A2 A1 A0 CE_3 $\overline{CE}_2$ $\overline{CE}_1$ A10 A9 A8		-1.5 “ “ “ “ “ “ “ “ “ “ “ “ “	V “ “ “ “ “ “ “ “ “ “ “ “ “
	V_{OL}	3007 “ “ “ “ “ “ “	15 16 17 18 19 20 21 22	1/ 2/ “ “ “ “ “ “ “	1/ 2/ “ “ “ “ “ “ “	2/ “ “ “ “ “ “ “	2/ “ “ “ “ “ “ “	2/ “ “ “ “ “ “ “	2/ “ “ “ “ “ “ “	2/ “ “ “ “ “ “ “	2/ “ “ “ “ “ “ “	3/	3/	3/	“ “ “ “ “ “ “ “	3/	3/	3/	3/	3/	2.0V “ “ “ “ “ “ “	2.0V “ “ “ “ “ “ “	0.8V “ “ “ “ “ “ “	2/ “ “ “ “ “ “ “	2/ “ “ “ “ “ “ “	2/ “ “ “ “ “ “ “	“ “ “ “ “ “ “ “	01 02 03 04 05 06 07 08		0.5 “ “ “ “ “ “ “	“ “ “ “ “ “ “ “
	I_{IL}	3009 “ “ “ “ “ “ “ “ “ “ “ “ “	23 24 25 26 27 28 29 30 31 32 33 34 35 36	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V				“ “ “ “ “ “ “ “ “ “ “ “ “ “						0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	5.5V “ “ “ “ “ “ “ “ “ “ “ “ “	A7 A6 A5 A4 A3 A2 A1 A0 CE_3 $\overline{CE}_2$ $\overline{CE}_1$ A10 A9 A8	-1.0 “ “ “ “ “ “ “ “ “ “ “ “ “	-250 “ “ “ “ “ “ “ “ “ “ “ “ “	µA “ “ “ “ “ “ “ “ “ “ “ “ “
	I_{IH}	3010 “ “ “ “ “ “ “ “ “ “ “ “ “	37 38 39 40 41 42 43 44 45 46 47 48 49 50	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V				“ “ “ “ “ “ “ “ “ “ “ “ “ “						5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	“ “ “ “ “ “ “ “ “ “ “ “ “ “	A7 A6 A5 A4 A3 A2 A1 A0 CE_3 $\overline{CE}_2$ $\overline{CE}_1$ A10 A9 A8		50 “ “ “ “ “ “ “ “ “ “ “ “ “	“ “ “ “ “ “ “ “ “ “ “ “ “ “
	I_{CEX}		51 52 53 54 55 56 57 58									5.2V	5.2V	5.2V	“ “ “ “ “ “ “ “	5.2V	5.2V	5.2V	5.2V	5.2V	0.5V	0.5V	4.5V				“ “ “ “ “ “ “ “	01 02 03 04 05 06 07 08		100 “ “ “ “ “ “ “	“ “ “ “ “ “ “ “
	I_{CC}	3005	59	GND	GND	GND	GND	GND	GND	GND	GND				“								GND	GND	GND	GND	“	V_{CC}		185	mA

See footnotes at end of table.

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TABLE III. Group A inspection for device types 01 and 03 – Continued.
Terminal conditions: (Outputs not designated are open or resistive coupled to GND or voltage.
Inputs not designated are high ≥ 2.0 V or ≤ 0.8 V.

Subgroup	Symbol	MIL-STD-883 method	Cases J,K	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		Unit
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	01	02	03	GND	04	05	06	07	08	CE_3	CE_2	$\overline{CE}_1$	A10	A9	A8	V_{CC}		Min	Max	
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C.																														
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C.																														
7 T_C=+25°C	Funct-ional tests	4/	60	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	GND	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	Outputs		4/	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																														
9 T_C=+25°C	t_{PHL1} t_{PLH1} t_{PHL2} t_{PLH2}	GALPAT Fig. 4 Sequen-tial Fig. 4	61 62 63 64	5/ 5/ 8/ 8/	5/ 5/ 8/ 8/	5/ 5/ 8/ 8/	5/ 5/ 8/ 8/	5/ 5/ 8/ 8/	5/ 5/ 8/ 8/	5/ 5/ 8/ 8/	5/ 5/ 8/ 8/	6/ " " "	6/ " " "	6/ " " "	GND " " "	6/ " " "	6/ " " "	6/ " " "	6/ " " "	6/ " " "	5.5V 5.5V 8/ 8/	5.5V 5.5V 8/ 8/	GND GND 8/ 8/	5/ 5/ 8/ 8/	5/ 5/ 8/ 8/	5/ 5/ 8/ 8/	5/ 5/ 8/ 8/	Outputs " " "		7/ 7/ 9/ 9/	ns " " "
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = +125°C																														
11	Same tests, terminal conditions, and limits as for subgroup 10, except T_C = -55°C																														

See footnotes at end of table.

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TABLE III. Group A inspection for device types 02 and 04.
Outputs not designated are open or resistive coupled to GND or voltage.
Terminal conditions: Inputs not designated are high ≥ 2.0 V or ≤ 0.8 V.

Subgroup	Symbol	MIL-STD-883 method	Case 3	2	3	4	5	6	7	8	9	11	12	13	14	16	17	18	19	20	22	23	24	25	26	27	28	Measured terminal	Test limits		Unit
			Cases J,K,L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24				
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE_3	CE_2	$\overline{CE}_1$	A10	A9	A8	V_{CC}		Min	Max	
1 T_C=+25°C	V_{IC}		1 2 3 4 5 6 7 8 9 10 11 12 13 14	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA				GND " " " " " " " " " " " " " "						-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	4.5V " " " " " " " " " " " " " "	A7 A6 A5 A4 A3 A2 A1 A0 CE_3 $\overline{CE}_2$ CE_1 A10 A9 A8		-1.5 " " " " " " " " " " " " " "	V " " " " " " " " " " " " " "
	V_{OL}	3007 " " " " " " "	15 16 17 18 19 20 21 22	1/ 2/ " " " " " " "	1/ 2/ " " " " " " "	2/ " " " " " " "	2/ 13/ " " " " " " "	2/ " " " " " " "	2/ " " " " " " "	2/ " " " " " " "	2/ " " " " " " "	3/	3/	3/	" " " " " " " "	3/	3/	3/	3/	3/	2.0V " " " " " " "	2.0V " " " " " " "	0.8V " " " " " " "	2/ 13/ " " " " " " "	2/ " " " " " " "	2/ 13/ " " " " " " "	" " " " " " " "	O1 O2 O3 O4 O5 O6 O7 O8		0.5 " " " " " " "	" " " " " " " "
	V_{OH}	3006 " " " " " " "	23 24 25 26 27 28 29 30	2/ 14/ 15/ 16/ 17/ " " " " " " "	2/ 12/ 15/ 16/ 17/ " " " " " " "	2/ 15/ 16/ 17/ " " " " " " "	2/ 15/ 16/ 17/ " " " " " " "	2/ 15/ 16/ 17/ " " " " " " "	2/ 15/ 16/ 17/ " " " " " " "	2/ 15/ 16/ 17/ " " " " " " "	2/ 15/ 16/ 17/ 18/ " " " " " " "	-2mA	-2mA	-2mA	" " " " " " " "	-2mA	-2mA	-2mA	-2mA	-2mA	" " " " " " " "	" " " " " " " "	" " " " " " " "	2/ 15/ 16/ 17/ " " " " " " "	2/ 15/ 16/ 17/ " " " " " " "	2/ 15/ 16/ 17/ " " " " " " "	" " " " " " " "	O1 O2 O3 O4 O5 O6 O7 O8	2.4 " " " " " " "		" " " " " " " "
	I_{IL}	3009 " " " " " " "	31 32 33 34 35 36 37 38 39 40 41 42 43 44	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V				" " " " " " " " " " " " " "						0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	5.5V " " " " " " " " " " " " "	A7 A6 A5 A4 A3 A2 A1 A0 CE_3 $\overline{CE}_2$ CE_1 A10 A9 A8	-1.0 " " " " " " " " " " " " "	-250 " " " " " " " " " " " " "	µA " " " " " " " " " " " " "
	I_{IH}	3010 " " " " " " "	45 46 47 48 49 50 51 52 53 54 55 56 57 58	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V				" " " " " " " " " " " " " "						5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	" " " " " " " " " " " " " "	A7 A6 A5 A4 A3 A2 A1 A0 CE_3 $\overline{CE}_2$ CE_1 A10 A9 A8		50 " " " " " " " " " " " " "	" " " " " " " " " " " " " "

See footnotes at end of table.

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TABLE III. Group A inspection for device types 02 and 04 – Continued.
Outputs not designated are open or resistive coupled to GND or voltage.
Terminal conditions: Inputs not designated are high ≥ 2.0 V or ≤ 0.8 V.

Subgroup	Symbol	MIL-STD-883 method	Case 3	2	3	4	5	6	7	8	9	11	12	13	14	16	17	18	19	20	22	23	24	25	26	27	28	Measured terminal	Test limits		Unit
			Cases J,K,L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24				
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE3	CE2	$\overline{CE}_1$	A10	A9	A8	V_{CC}		Min	Max	
1 T_C=+25°C	I_{OHZ}		59									5.2V			GND						0.5V	0.5V	4.5V				5.5V	O1		100	µA
			60										5.2V		"						"	"	"				"	O2		"	"
			61											5.2V	"						"	"	"				"	O3		"	"
			62												"	5.2V					"	"	"				"	O4		"	"
			63												"		5.2V				"	"	"				"	O5		"	"
			64												"			5.2V			"	"	"				"	O6		"	"
			65												"				5.2V		"	"	"				"	O7		"	"
			66												"					5.2V	"	"	"				"	O8		"	"
	I_{OLZ}		67									0.5V			"						"	"	"				"	O1		-100	"
			68										0.5V		"						"	"	"				"	O2		"	"
			69											0.5V	"						"	"	"				"	O3		"	"
			70												"	0.5V					"	"	"				"	O4		"	"
			71												"		0.5V				"	"	"				"	O5		"	"
			72												"			0.5V			"	"	"				"	O6		"	"
			73												"				0.5V		"	"	"				"	O7		"	"
			74												"					0.5V	"	"	"				"	O8		"	"
	I_{OS}	3011	75	14/ 2/ 15/ 16/ 17/	2/ 15/ 12/ 16/ 17/	2/ 15/ 16/ 17/	2/ 15/ 16/ 17/	2/ 15/ 16/ 17/	17/ 2/ 15/ 16/	2/ 15/ 16/ 17/	18/ 2/ 15/ 16/ 17/	GND	GND	GND	"						4.5V	4.5V	0.5V	2/ 15/ 16/ 17/	2/ 15/ 16/ 17/	2/ 15/ 16/ 17/	"	O1	-10	-100	mA
		"	76	"	"	"	"	"	"	"	"				"	5.2V					"	"	"	"	"	"	"	O2	"	"	"
		"	77	"	"	"	"	"	"	"	"				"		5.2V				"	"	"	"	"	"	"	O3	"	"	"
		"	78	"	"	"	"	"	"	"	"				"			5.2V			"	"	"	"	"	"	"	O4	"	"	"
		"	79	"	"	"	"	"	"	"	"				"				5.2V		"	"	"	"	"	"	"	O5	"	"	"
		"	80	"	"	"	"	"	"	"	"				"					5.2V	"	"	"	"	"	"	"	O6	"	"	"
		"	81	"	"	"	"	"	"	"	"				"						"	"	"	"	"	"	"	O7	"	"	"
		"	82	"	"	"	"	"	"	"	"				"						"	"	"	"	"	"	"	O8	"	"	"
	I_{CC}	3005	83	GND	GND	GND	GND	GND	GND	GND	GND				"								GND	GND	GND	GND	"	V_{CC}		185	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C.																														
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C.																														
7 T_C=+25°C	Funct-ional tests	4/	84	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	GND	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	Outputs		4/	
8	Same tests, terminal conditions, and limits as for subgroup 7, except TC = +125°C and -55°C.																														
9 T_C=+25°C	t_{PHL1}	GALPAT	85	5/	5/	5/	5/	5/	5/	5/	5/	6/	6/	6/	GND	6/	6/	6/	6/	6/	5.5V	5.5V	GND	5/	5/	5/	5/	Outputs		7/	ns
	t_{PLH1}	Fig. 4	86	5/	5/	5/	5/	5/	5/	5/	5/	"	"	"	"	"	"	"	"	"	5.5V	5.5V	GND	5/	5/	5/	5/	"		7/	"
	t_{PHL2}	Sequen-tial	87	8/	8/	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/	8/	8/	8/	"		9/	"
	t_{PLH2}	Fig. 4	88	8/	8/	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/	8/	8/	8/	"		9/	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = +125°C.																														
11	Same tests, terminal conditions, and limits as for subgroup 10, except T_C = -55°C.																														

See footnotes at end of table.

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TABLE III. Group A inspection for device type 05.
Outputs not designated are open or resistive coupled to GND or voltage.
Terminal conditions: Inputs not designated are high ≥ 2.0 V or ≤ 0.8 V.

Subgroup	Symbol	MIL-STD-883 method	Case R Test no.	1 A8	2 A7	3 A6	4 A5	5 A4	6 A3	7 A2	8 A1	9 A0	10 GND	11 O4	12 O3	13 O2	14 O1	15 $\overline{CE}_2$	16 $\overline{CE}_1$	17 A11	18 A10	19 A9	20 V_{CC}	Measured terminal	Test limits Min	 Max	Unit
1 T_C=+25°C	V_{IC}		1	-10mA									GND										4.5V	A8		-1.5	V
			2		-10mA								"										"	A7		"	"
			3			-10mA							"										"	A6		"	"
			4				-10mA						"										"	A5		"	"
			5					-10mA					"										"	A4		"	"
			6						-10mA				"										"	A3		"	"
			7							-10mA			"										"	A2		"	"
			8								-10mA		"										"	A1		"	"
			9									-10mA	"										"	A0		"	"
			10										"					-10mA					"	$\overline{CE}_2$		"	"
			11										"						-10mA				"	CE_1		"	"
			12										"							-10mA			"	A11		"	"
			13										"								-10mA		"	A10		"	"
			14										"									-10mA	"	A9		"	"
	V_{OL}	3007	15	1/ 2/	2/	2/ 19/	2/ 19/	2/ 19/	2/ 19/	2/ 19/	2/ 19/	2/ 19/	"	3/	3/	3/	3/	0.8V	0.8V	2/	2/	2/	"	O4		0.5	"
		"	16	"	"	"	"	"	"	"	"	"	"					"	"	"	"	"	"	O3		"	"
		"	17	"	"	"	"	"	"	"	"	"	"					"	"	"	"	"	"	O2		"	"
		"	18	"	"	"	"	"	"	"	"	"	"					"	"	"	"	"	"	O1		"	"
	V_{OH}	3006	19	2/	"	2/	2/	2/	2/	2/	2/	2/	"	-2mA	-2mA	-2mA	-2mA	"	"	"	"	"	"	O4	2.4		"
		"	20	"	"	"	"	"	"	"	"	"	"					"	"	"	"	"	"	O3	"		"
		"	21	"	"	"	"	"	"	"	"	"	"					"	"	"	"	"	"	O2	"		"
		"	22	"	"	"	"	"	"	"	"	"	"					"	"	"	"	"	"	O1	"		"
	I_{IL}	3009	23	0.5V									"										5.5V	A8	-1.0	-250	µA
		"	24		0.5V								"										"	A7	"	"	"
		"	25			0.5V							"										"	A6	"	"	"
		"	26				0.5V						"										"	A5	"	"	"
		"	27					0.5V					"										"	A4	"	"	"
		"	28						0.5V				"										"	A3	"	"	"
		"	29							0.5V			"										"	A2	"	"	"
		"	30								0.5V		"										"	A1	"	"	"
		"	31									0.5V	"										"	A0	"	"	"
		"	32										"					0.5V					"	$\overline{CE}_2$	"	"	"
		"	33										"						0.5V				"	CE_1	"	"	"
		"	34										"							0.5V			"	A11	"	"	"
		"	35										"								0.5V		"	A10	"	"	"
		"	36										"									0.5V	"	A9	"	"	"
	I_{IH}	3010	37	5.5V									"										"	A8		50	"
		"	38		5.5V								"										"	A7		"	"
		"	39			5.5V							"										"	A6		"	"
		"	40				5.5V						"										"	A5		"	"
		"	41					5.5V					"										"	A4		"	"
		"	42						5.5V				"										"	A3		"	"
		"	43							5.5V			"										"	A2		"	"
		"	44								5.5V		"										"	A1		"	"
		"	45									5.5V	"										"	A0		"	"
		"	46										"					5.5V					"	$\overline{CE}_2$		"	"
		"	47										"						5.5V				"	CE_1		"	"
		"	48										"							5.5V			"	A11		"	"
		"	49										"								5.5V		"	A10		"	"
		"	50										"									5.5V	"	A9		"	"

See footnotes at end of table.

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TABLE III. Group A inspection for device type 05 – Continued.
Outputs not designated are open or resistive coupled to GND or voltage.
Terminal conditions: Inputs not designated are high ≥ 2.0 V or ≤ 0.8 V.

Subgroup	Symbol	MIL-STD-883 method	Case R Test no.	1 A8	2 A7	3 A6	4 A5	5 A4	6 A3	7 A2	8 A1	9 A0	10 GND	11 O4	12 O3	13 O2	14 O1	15 $\overline{CE}_2$	16 $\overline{CE}_1$	17 A11	18 A10	19 A9	20 V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C=+25°C	I_{OHZ}		51										GND	5.2V	5.2V			4.5V	4.5V				5.5V	O4		100	µA
			52										"					"	"				"	O3		"	"
			53										"			5.2V		"	"				"	O2		"	"
			54										"				5.2V	"	"				"	O1		"	"
	I_{OLZ}		55										"	0.5V	0.5V			"	"				"	O4		-100	"
			56										"					"	"				"	O3		"	"
			57										"			0.5V		"					"	O2		"	"
			58										"				0.5V	"					"	O1		"	"
	I_{OS}	3011	59	2/	2/	2/	2/	2/	2/	2/	2/	2/	"	GND	GND			0.5V	0.5V	2/	2/	2/	"	O4	-10	-100	mA
		"	60	"	"	"	"	"	"	"	"	"	"					"	"	"	"	"	"	O3	"	"	"
		"	61	"	"	"	"	"	"	"	"	"	"			GND		"	"	"	"	"	"	O2	"	"	"
		"	62	"	"	"	"	"	"	"	"	"	"				GND	"	"	"	"	"	"	O1	"	"	"
	I_{CC}	3005	63	GND	GND	GND	GND	GND	GND	GND	GND	GND	"					GND	GND	GND	GND	GND	"	V_{CC}		185	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C.																										
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C.																										
7 T_C=+25°C	Funct-ional tests	4/	64	4/	4/	4/	4/	4/	4/	4/	4/	4/	GND	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	Outputs		4/	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and T_C = -55°C.																										
9 T_C=+25°C	t_{PHL1}	GALPAT	65	5/	5/	5/	5/	5/	5/	5/	5/	5/	GND	6/	6/	6/	6/	GND	GND	5/	5/	5/	5/	Outputs		80	ns
	t_{PLH1}	Fig. 4	66	5/	5/	5/	5/	5/	5/	5/	5/	5/	"	"	"	"	"	GND	GND	5/	5/	5/	5/	"		80	"
	t_{PHL2}	Sequen-	67	8/	8/	8/	8/	8/	8/	8/	8/	8/	"	"	"	"	"	8/	8/	8/	8/	8/	8/	"		40	"
	t_{PLH2}	tial Fig. 4	68	8/	8/	8/	8/	8/	8/	8/	8/	8/	"	"	"	"	"	8/	8/	8/	8/	8/	8/	"		40	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = +125°C.																										
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.																										

1/ For unprogrammed devices, apply 13.0 V on pin 1(A7) and pin 2 (A6), for device types 01 and 02, and on pin 1 (A8) for device type 05 for circuit A devices.

2/ For programmed devices, select an appropriate address to acquire the desired output state. V_{IH} = 2.0 V, V_{IL} = 0.8 V.

3/ I_{OL} = 8 mA for circuits C and G. I_{OL} = 16 mA for circuits A, B, D, F, H, I, and J.

4/ The functional tests shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II and 3.3.2.1). All bits shall be tested. Terminal conditions shall be as follows:

a. Inputs: H = 2.4 V, L = 0.4 V
b. Outputs: Output voltage shall be:
   H $\geq$ 1.5 V and L $\leq$ 1.5 V.
c. The functional tests shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V.

5/ GALPAT (programmed PROM). This program will test all bits in the array, the addressing and interaction between bits for ac performance, t_{PHL1} and t_{PLH1}. Each bit in the pattern is fixed by being programmed with an “H” or “L”.

Description:
1. Word 0 is read.
2. Word 1 is read.
3. Word 0 is read.
4. Word 2 is read.
5. Word 0 is read.
6. The reading procedure continues back and forth between word 0 and the next higher numbered word until word 2047 or 4095 is reached, then increments to the next word and reads back and forth as in step 1 through 7 and shall include all words.
7. Pass execution time = $(n^2 + n)$ x cycle time. n = 2048 or 4096.
8. The GALPAT tests shall be performed with V_{CC} = 4.5 V and 5.5 V.

6/ The outputs are loaded per figure 4.

7/ t_{PHL1}, t_{PLH1} = 100 ns for device types 01 and 02 and 55 ns for device types 03 and 04.

8/ Sequential test (programmed PROM). This program will test all bits in the array for t_{PHL2} and t_{PLH2}.

Description:
1. Each word in the pattern is tested from the enable lines to the output lines for recovery.
2. Word 0 is addressed. Enable line is pulled HI to LO and LO to HI. t_{PHL2} and t_{PLH2} are read.
3. Word 1 is addressed. Same enable sequence as above.
4. The reading procedure continues until word 2047 or 4095 is reached.
5. Pass execution time = 2048 x cycle time (or 4096 x cycle time).
6. The sequential tests shall be performed with V_{CC} = 4.5 V and 5.5 V.

9/ t_{PHL2}, t_{PLH2} = 50 ns for device types 01 and 02 and 30 ns for device types 03 and 04.

10/ For uprogrammed devices, apply 13 V on pin 8 (A0) for circuit I devices.

11/ For unprogrammed devices, 12.0 V on pin 6 (A2) and 0.0 V on pin 5 (A3) for circuit F devices.

12/ For unprogrammed devices, apply 13 V on pin 2 (A6) for circuit I devices.

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13/ For unprogrammed devices, apply 10 V to pin 4 (A4), apply V_{OH} to pin 21 (A10), and apply V_{OL} to pin 23 (A8) for circuit H.

14/ For unprogrammed devices, apply 10.5 V on pin 1 (A7) for circuit B devices..

15/ For unprogrammed devices, apply 10.5 V to pin 3 (A5), apply 0 V to pins 4, 5, 6, 7, 8 (A4, A3, A2, A1, A0), and apply 3 V to pins 1, 2, 21, 22, 23, (A7, A6, A10, A9, A8) for circuit G devices.

16/ For unprogrammed devices type 02 (82S191), with date codes before 8626. apply 10.0 V on pin 6 (A2); apply 5.0 V to all other addresses for circuit C devices.

17/ For unprogrammed device types 02 (with date codes 8626 or later) and 04 (82S191A), apply 10.0 V on A4; apply 5.0 V on A0, A1, A2, A3 and A6; and apply 0.5 V on A5, A7, A8, A9 and A10 for circuit C devices.

18/ For unprogrammed devices, apply 12.0 V on pin 8 (A0) for circuit D devices.

19/ For unprogrammed device type 05, apply 15.0 V to pin 4 (A5); apply 0.0 V to pins 5, 9 (A4, A0); apply 4.5 V to pins 3, 6, 7, 8 (A6, A3, A2, A1) for circuit C devices.

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TABLE IVA. Programming characteristics for circuit A.

Parameter	Symbol	Limits 1/			Unit
		Min	Recommended	Max	
Address input voltage 2/	V_{IH} V_{IL}	2.4 0.0	5.0 0.4	5.0 0.5	V V
Programming Voltage to V_{CC} low Program verify Verify voltage	V_{PH} 3/ V_{PL} V_{PHV} V_R 4/	10.75 0.0 ---- 4.5	11.0 0.0 5.5 ----	11.25 1.5 ---- 5.5	V “ “ “
Programming input low current at V_{PH}	I_{ILP}	----	-300	-600	µA
Programming voltage (V_{CC}) transition time	t_{TLH} t_{THL}	1 1	5 5	10 10	µs µs
Programming delay	t_{D1} t_{D2}	10 1	10 5	20 5	µs µs
Programming pulse width	t_P 5/	90	100	110	µs
Programming duty cycle	PDC	----	30	60	%
Output voltage Enable Disable	 V_{OPE} 6/ V_{OPD}	 10.5 0.0	 10.5 5.0	 11.0 5.5	 V V

During the programming the chip must be disabled for proper operation.

1/ T_A = +25°C.

2/ No inputs should be left open for V_{IH}.

3/ V_{PH} source must be capable of supplying one ampere.

4/ It is recommended that post programming dual verification be made at V min$_R$ and V max $_R$.

5/ Note step j in programming procedure.

6/ V_{OPE} source must be capable of supplying 10 mA minimum.

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TABLE IVB. Programming characteristics for circuit B.

Parameter	Symbol	Conditions 1/	Limits			Unit
			Min	Recommended	Max	
V_{CC} required during programming	V_{CCP}		10.5	11.0	11.5	V
VOUT current limit during programming	I_{OP}		20	25	30	mA
Output programming voltage	V_{OUT}		10.5	11.0	11.5	V
Pulse width of programming voltage	t_P		9	10	11	µs
Programming delay	t_D		0	1	10	µs
V_{CCP} or V_{OUT} transition time	t_{TLH}	Rise time of V_{CC} or V_{OUT}	1	5	10	V/µs
V_{CCP} current	I_{CCP}		800	900	1,000	mA
Low V_{CC} for verification	V_{CCL}		3.9	4.0	4.1	V
High V_{CC} for verification	V_{CCH}		5.8	6.0	6.2	V
Address input voltage	V_{IH}		2.4	5.0	5.5	V
	V_{IL}		0.0	0.4	0.8	V
Maximum duty cycle during automatic programming of program pin and output pin	D.C.	t_P / t_C	----	25	50	%

1/ T_C = +25°C.

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TABLE IVC. Programming characteristics for circuit C, device types 02 and 04.

Parameter	Symbol	Conditions 1/	Limits			Unit
			Min	Recommended	Max	
Programming voltage to V_{CC}	V_{CCP} 2/	I_{CCP} = 375 ±75 mA Transient or steady-state	8.5	8.75	9.0	V
Verificaiton upper limit	V_{CCH}		5.3	5.5	5.7	V
Verificaiton lower limit	V_{CCL}		4.3	4.5	4.7	V
Verify threshold	V_S 3/		1.4	1.5	1.6	V
Programming supply current	I_{CCP}	V_{CCP} = +8.75 ±0.25 V	300		450	mA
Input voltage, high level "1"	V_{IH}		2.4		5.5	V
Input voltage, low level "0"	V_{IL}		0	0.4	0.8	V
Input current	I_{IH}	V_{IH} = +5.5 V			50	µA
Input current	I_{IL}	V_{IL} = +0.4 V			-500	µA
Output programming voltage	V_{OUT} 4/	I_{OUT} = 200 ±20 mA; Transient or steady-state	16	17	18	V
Output programming current	I_{OUT}	V_{OUT} = 17 V ±1 V	180	200	220	mA
Programming voltage transition time	t_{TLH}		10		50	µs
$\overline{CE}$ programming pulse width	t_P		300	400	500	µs
Pulse sequence delay	t_D		10			µs

1/ T_C = +25°C.

2/ Bypass V_{CC} to GND with a 0.01 µF capacitor to reduce voltage spikes.

3/ V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

4/ Care should be taken to insure the 17 V ±1 V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

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TABLE IVC. Programming characteristics for circuit C, device type 05 – Continued.

Parameter	Symbol	Conditions 1/	Limits			Unit
			Min	Recommended	Max	
Programming voltage to V_{CC} 2/	V_{CCP}	I_{CCP} = 425 ±75 mA Transient or steady-state	8.5	8.75	9.0	V
Verify voltage	V_{CCV}		4.75	5.0	5.25	V
Input voltage, high level "1"	V_{IH}	I_{IH} = 50 µA	2.4	3.0	5.5	V
Input voltage, low level "0"	V_{IL}	I_{IL} = 500 µA	0.0	0.0	0.5	V
Forced output current	I_{OPF}	V_{OPF} = 17.5 ± 0.5 V	150	185	220	mA
Forced output voltage (program) 3/	V_{OPF1}	I_{OPF} = 300 ± 25 mA	17.0	17.5	18.0	V
Forced output voltage (program) 3/	V_{OPF2}	I_{OPF} = 300 ± 25 mA	20.0		22.0	V
Output voltage high	V_{OH}		2.4		5.25	V
Output voltage low	V_{OL}		0.0		0.45	V
V_{CC} delay time	T_{D1}	50% to 10% V_{CCP}	10	10	25	µs
V_{OUT} delay time	T_{D2}	90% V_{CCP} to 10% V_{OFF}	1.0	1.0	5.0	µs
Pulse sequence delays	$T_{D3} – T_{D8}$	See figure 5C	1.0	1.0	10	µs
V_{CC} rise time	T_{R1}	0 % to 100%	4.0	7.0	8.0	µs
V_{OUT} rise time	T_{R2}	10% to 90%	3.0	10	17	µs
V_{CC} fall time	T_{F1}	100% to 0%	2.0	4.0	10	µs
V_{OUT} fall time	T_{F2}	100% to 0%	4.0	7.0	20	µs
$\overline{CE}_2$ programming pulse width 4/	T_P	10% to 10%	5.0	10	30	µs
$\overline{CE}_2$ verify pulse width 4/	T_V	10% to 10%	5.0	5.0	10	µs
Clock pulse width (CK)	T_{WC}	50% to 50%	0.5	0.75	1.0	µs

1/ T_C = +25°C.

2/ If the overall program/verify cycle exceeds the recommended value, a 25% duty cycle must be used for V_{CCP}.

3/ V_{OPF} supply should regulate to ±0.25 V at I_{OPF}. Maximum slew rate for V_{OPF} should be 1.0 V/µs.

4/ $\overline{CE}_2$ rise time slew rate should be 1.0 V/ns maximum. $\overline{CE}_2$ fall time slew rate should be 10.0 V/ns maximum.

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TABLE IVD. Programming characteristics for circuit D.

Parameter	Symbol	Conditions 1/	Limits			Unit
			Min	Recommended	Max	
Power supply voltage	V_{CC}		6.4	6.5	6.6	V
Power supply rise time 2/	$t_{r(VCC)}$		0.2	2.0		µs
Power supply fall time 2/	$t_{f(VCC)}$		0.2	2.0		µs
V_{CC} on time 3/	t_{ON}	See programming Time diagram				
V_{CC} off time 4/	t_{OFF}					
Duty cycle for V_{CC}		$t_{ON}/(t_{OFF} + t_{ON})$			50	%
Read delay before programming	t_{dRBP}	Initial check		3.0		µs
Fuse read time	t_W 5/			1.0		µs
Delay to V_{CC} off	$t_{d(VCC)}$ 5/			1.0		µs
Delay to read after programming	t_{dRAP} 5/	Programming verification		3.0		µs
Chip select programming voltage	V_{CSP}		20.0	20.0	22.0	V
Chip select program current limit	I_{CSP}		175	180	185	mA
Input voltage low	V_{IL}		0.0	0.0	0.4	V
Input voltage high	V_{IH}		2.4	5.0	5.0	V
Delay to chip deselect	t_{dCS}			1.0		µs
Chip select pulse rise time	t_{rCS}		3.0	4.0		µs
Delay to chip select time	t_{dAP}		0.2	1.0		µs
Chip select pulse fall time	t_{fCS}		0.1	0.1	1.0	µs

See footnotes at end of table.

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TABLE IVD. Programming characteristics for circuit D – Continued.
Ramp characteristics

Parameter	Symbol	Conditions 1/	Limits			Unit
			Min	Recommended	Max	
Programming current linear point	I_{OPLP}			10	20	mA
Output programming current limits	$I_{OP(MAX)}$	Apply current ramp to selected output	155	160	165	mA
Output programming voltage limit	$V_{OP(MAX)}$		24	25	26	V
Current slew rate	SR_{IOP}	Constant after linear point	0.9	1.0	1.1	mA/µs
Blow sense voltage	V_{PS}		0.7			V
Delay to programming ramp	t_{dBP}		2.0	3.0		µs
Time to reach linear point	t_{LP}		0.2	1.0	10	µs
Program sense inhibit	t_{ss}		2.0	3.0	10	µs
Time to program fuse	t_{tp}		3.0		150	µs
Programming ramp hold time	t_{hAP}	After fuse programs	1.4	1.5	1.6	µs
Programming ramp fall time 2/	t_{flOP}			0.1	0.2	µs

1/ T_C = +25°C

2/ Rise and fall times are from 10% to 90%.

3/ Total time V_{CC} is on to program fuse is equal to or greater than the sum of all the specified delays, pulse widths and rise/fall times.

4/ t_{OFF} is equal to or greater than t_{ON}.

5/ Proceed to next address after read strobe indicates programmed cell.

TABLE IVE. Programming characteristics for circuit E – Discontinued.

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TABLE IVF. Programming characteristics for circuit F.

Parameter	Symbol	Conditions 1/	Limits			Unit
			Min	Recommended	Max	
V_{CC} required during programming	V_{CCP}		5.4	5.5	5.6	V
Rise time of program pulse to data out or program pin	t_{TLH}		0.34	0.40	0.46	V/µs
Programming voltage on program pin	V_{PP}		32.5	33	33.5	V
Output programming voltage	V_{OUT}		25.5	26	26.5	V
Programming pin pulse width ($\overline{CE}$)	t_{PP}	Chip disabled, V_{CC} = 5.5 V	----	100	180	µs
Pulse width of programming voltage	t_p		1		40	µs
Required current limit of power supply feeding program pin and output during program	I_L	V_{PP} = 33 V, V_{OUT} = 26 V, V_{CC} = 5.5 V	240		----	mA
Required time delay between disabling memory output and application of output programming pulse	T_{D1}	Measured at 10% levels	70	80	90	µs
Required time delay between removal of programming pulse and enabling memory output	T_{D2}		100			ns
Output current during verification	I_{OLV1}	Chip enabled, V_{CC} = 4.0 V	11	12	13	mA
	I_{OLV2}	Chip enabled, V_{CC} = 7.0 V	0.19	0.2	0.21	mA
Address input voltage	V_{IH}		2.4	5.0	5.5	V
	V_{IL}		0.0	0.4	0.8	V
Maximum duty cycle during automatic programming of program pin and output pin	D.C.	t_p/t_c	----	----	25	%

1/ T_C = 25°C

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TABLE IVG. Programming characteristics for circuit G .

Parameter	Symbol	Conditions 1/	Limits			Unit
			Min	Recommended	Max	
Required V_{CC} for programming	V_{CCP}		10.0	10.5	11.0	V
I_{CC} during programming	I_{CCP}	V_{CC} = 11 V			750	mA
Required output voltage for programming	V_{OP}		10.0	10.5	11.0	V
Output current while programming	I_{OP}	V_{OUT} = 11 V			20	mA
Rate of voltage change of V_{CC} or output	I_{RR}		1.0		10.0	V/µs
Programming pulse width (enabled)	PWE		9	10	11	µs
Required V_{CC} for verification	V_{CCV}		3.8	4.0	4.2	V
Maximum duty cycle for V_{CC} at V_{CCP}	MDC			25	25	%
Address set-up time	t_1		100			ns
V_{CCP} set-up time	t_2	2/	5			µs
V_{CCP} hold time	t_5		100			ns
V_{OP} set-up time	t_3		100			ns
V_{OP} hold time	t_4		100			ns

1/ T_C = +25°C.

2/ V_{CCP} setup time may be greater than 0 if V_{CCP} rises at the same rate or faster than V_{OP}.

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TABLE IVH. Programming characteristics for circuit H . 1/

Parameters	Symbol	Min	Nom	Max	Unit
Steady-state supply voltage	V_{CC}	4.75	5	5.25	V
Input voltage	V_{IH}	3	4	5	V
	V_{IL}	0	0	0.5	V
Voltage all outputs except the one to be programmed		0	0	0.5	V
Supply voltage level to program a bit	$V_{CC(pr)}$	5.75	6	6.25	V
Select or enable level to program a bit	$V_{S(pr)}$	9.75	10	11	V
Output level during interval t5	$V_{O(PR)}$	15.75	16	16.25	V
Supply voltage during verification (see step 0)	Low	4.4	4.5	4.6	V
	High	5.4	5.5	5.6	V
Time for V_{CC} to settle and to verify need to program	t_1	0	5	10	µs
Timing from V_{CC} = 6 V until chip select (enable) is at 10 V	t_2	5	5	10	µs
Timing from chip select (enable) high to start or program ramp	t_3	0.1	5	10	µs
Ramp time, output program pulse	t_4	10	15	20	µs
Duration of output program pulse	t_5	15	20	20	µs
Time from end of program pulse to chip select (enable) low	t_6	5	5	10	µs
Time from chip select (enable) low to V_{CC} = 0 V	t_7	0.1	5	5	µs
Time for cooling between bits	t_8	30	50	100	µs
Time for cooling between words	t_9	30	50		µs

1/ T_C = +25°C.

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TABLE IVI. Programming characteristics for circuit I .

Parameter	Symbol	Conditions 1/	Limits			Unit
			Min	Recommended	Max	
V_{CC} during programming	V_{CCP}		5.0		5.5	V
High level input voltage during programming	V_{IHP}		2.4		5.5	V
Low level input voltage during programming	V_{ILP}		0.0		0.45	V
Chip enable voltage during programming	V_{CEP}	$\overline{CE}$ 1 pin	14.5		15.5	V
Output voltage during programming	V_{OP}		19.5		20.5	V
Voltage on outputs not to be programmed	V_{ONP}		0		V_{CCP} + 0.3	V
Current on outputs not to be programmed	I_{ONP}				20	mA
Rate of output voltage change	$d(V_{OP})/dt$		20		250	V/µs
Rate of chip enable voltage change	$d(V_{CE})/dt$	$\overline{CE}$ 1 pin	100		1000	V/µs
Programming period	tp		50		100	µs
V_{CC} during programming verification	V_{CCL}		4.5		5.0	µs

1/ T_C = +25°C.

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TABLE IVJ. Programming characteristics for circuit J .

Parameters	Symbol	Limits 1/			Unit
		Min	Recommended	Max	
Address input voltage 2/	V_{IH}	2.4	5.0	5.0	V
	VIL	0.0	0.4	0.8	V
Programming/verify voltage to V_{CC}	V_{PH}	11.75	12.0	12.25	V
	V_{PL}	4.5	4.5	5.5	V
Programming voltage current limit with V_{PH} applied	I_{CCP}	600	600	650	mA
Voltage rise and fall time	t_r	1.0	1.0	10	µs
	t_f	1.0	1.0	10	µs
Programming delay	t_d	10	10	100	µs
Programming pulse width	t_P	100		1000	µs
Programming duty cycle	DC	----	50	90	%
Output voltage enable	V_{OPE}	10.0	10.5	11.0	V
Output voltage disable 3/	V_{OPD}	4.5	5.0	5.5	V

1/ T_C = +25°C.

2/ Address and chip select shall not be left open for V_{IH}.

3/ Disable condition shall be met with output open circuit.

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5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. PIN and compliance identifier, if applicable (see 1.2).

c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

d. Requirements for certificate of compliance, if applicable.

e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.

f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

g. Requirements for product assurance options.

h. Requirements for special lead lengths, or lead forming, if applicable. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

i. Requirement for programming the device, including processing option. The device may be programmed pre- or post-burn-in, if applicable.

j. Requirements for "JAN" marking.

k. Packaging Requirements (see 5.1)

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43218-3990.

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6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

GND ..... Ground zero voltage potential.
V_{IN} ..... Voltage level at an input terminal
V_{IC} ..... Input clamp voltage
I_{IN} ..... Current flowing into an input terminal

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.4). Longer length leads and lead forming should not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.8.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry Type	Circuit Designator	Fusible Links	CAGE Number
01 1/	76160 / Harris	A	NiCr	34371
01 1/	53S1680/Monolithic Memories	B	TiW	50364
01 1/	82S190/Signetics Corp.	C	NiCr	18324
01 1/	77S190/National	G	TiW/W	27014
02 1/	76161/Harris	A	NiCr	34371
02 1/	53S1681 / Monolithic Memories	B	TiW	50364
02, 04	82S191A/Signetics Corp.	C	NiCr	18324
02 1/	3636/Intel	E	Polysilicon	34649
02 1/	29681/Raytheon	F	NiCr	07933
02 1/	77S191/National	G	TiW/W	27014
02, 04 1/	28S166A/Texas Instruments	H	TiW	01295
02 1/	27S191/Advanced Micro Devices	I	Platinum silicide	34335
02 1/	76161/Motorola	J	NiCr	04713
03 1/	93Z510/Fairchild	D	ZVE 2/	07263
04, 02 1/	93Z511/Fairchild	D	ZVE	07263
05 1/	76165/Harris	A	NiCr	34371
05 1/	82HS195/Signetics Corp.	C	ZVE	18324

1/ This generic-industry type is no longer manufactured.
2/ Zapped vertical emitter.

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6.8 Change from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA - CC

Preparing activity:
DLA - CC

Review activities:
Army – SM, MI
Navy - AS, CG, MC, SH TD
Air Force – 03, 19, 99

(Project 5962-2006-003)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organization and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.

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