MILITARY SPECIFICATION

MICROCIRCUIT, DIGITAL, 256-BIT, SCHOTTKY, BIPOLAR,
PROGRAMMABLE READ-ONLY MEMORY (PROM), MONOLITHIC SILICON

| Inactive for new design after 24 July 1995 |
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This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, PROM microcircuits which employ thin film nichrome (NiCr) resistors, tungsten (W), titanium tungsten (TiW), or zapped vertical emitter (ZVE) as the fusible link or programming element. Two product assurance classes and a choice of case outlines and lead material and finishes are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

| Device type | Circuit |
|---|---|
| 01, 03 | 32 word / 8 bits per word PROM with open collector |
| 02, 04 | 32 word / 8 bits per word PROM with tri-state output |

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| E | GDIP1-T16 or CDIP2-T16 | 16 | Dual-in-line |
| F | GDFP2-F16 or CDFP3-F16 | 16 | Flat pack |

| Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to memory@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil |
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AMSC N/A                                                                 FSC 5962

1.3  Absolute maximum ratings.

Supply voltage range  .................................................................... -0.5 V dc to +7.0 V dc
Input voltage range  ...................................................................... -1.5 V dc at -10 mA to +5.5 V dc
Storage temperature range  ........................................................... -65° to +150°C
Lead temperature (soldering, 10 seconds) .................................... +300°C
Thermal resistance, junction to case ($\theta_{JC}$):
    Cases E and F  ........................................................................ See MIL-STD-1835  1/
Output voltage applied  .................................................................. -0.5 V dc to +$V_{CC}$
Output sink current ........................................................................ 100 mA
Maximum power dissipation ($P_D$) .................................................. 739 mW dc  2/
Maximum junction temperature ($T_J$) ............................................. +175°C  3/

1.4  Recommended operating conditions.

Supply voltage range ($V_{CC}$) .......................................................... +4.5 V dc minimum to
    +5.5 V dc maximum
Minimum high-level input voltage ($V_{IH}$) ......................................... 2.0 V dc
Maximum low-level input voltage ($V_{IL}$) ......................................... 0.8 V dc
Normalized fanout (each output) .................................................... 16 mA
Case operating temperature range ($T_C$) ....................................... -55 °C to +125 °C

2.  APPLICABLE DOCUMENTS

2.1 General.  The documents listed in this section are specified in sections 3, 4, or 5 of this specification.  This section does not include documents cited in other sections of this specification or recommended for additional information or as examples.  While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2  Government documents.

2.2.1  Specifications and Standards.  The following specifications and standards form a part of this specification to the extent specified herein.  Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

    MIL-PRF-38535   -       Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

    MIL-STD-883      -       Test Method Standard for Microelectronics.
    MIL-STD-1835    -       Interface Standard Electronic Component Case Outline

  (Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA  19111-5094.)

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1/   Heat sinking is recommended to reduce the junction temperature.

2/   Must withstand the added $P_D$ due to short circuit test (e.g. $I_{OS}$).

3/   Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions per method 5004 of MIL-STD-883.

2.3  Order of precedence.  In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence.  Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3.  REQUIREMENTS

3.1  Qualification.  Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2  Item requirements.    The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan.  The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3  Design, construction, and physical dimensions.  The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1  Terminal connections.  The terminal connections shall be as specified on figure 1.

3.3.2  Truth tables.

3.3.2.1  Unprogrammed devices.  The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2.  When required in groups A, B, or C inspection (see 4.4), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.3.2.2  Programmed devices.   The truth table for programmed devices shall be as specified by the altered item drawing.

3.3.3  Functional block diagram.  The functional block diagram shall be as specified on figure 3.

3.3.4  Case outlines.  The case outlines shall be as specified in 1.2.3.

3.4  Lead material and finish.  The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5  Electrical performance characteristics.  Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.6  Electrical test requirements.  The electrical test requirements for each device class shall be the subgroups specified in table II.  The electrical tests for each subgroup are described in table III.

3.7  Marking.  Marking shall be in accordance with MIL-PRF-38535.

3.8    Processing options.  Since the PROM is an unprogrammed device capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.8.1  Unprogrammed PROM delivered to the user.   All testing shall be verified through group A testing as defined in 3.3.2.1, table II, and table III.  It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.8.2  Manufacture-programmed PROM delivered to the user.   All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.9    Microcircuit group assignment.   The devices covered by this specification shall be in microcircuit group number 14 (see Appendix A MIL-PRF-38535.)

TABLE I.  Electrical performance characteristics.

| Test | Symbol | Conditions 1/ -55°C ≤ $T_C$ ≤ +125°C unless other wise specified | Device type | Limits Min | Limits Max | Units |
|---|---|---|---|---|---|---|
| High-level output voltage | $V_{OH}$ | $V_{CC}$ = 4.5 V, $I_{OH}$ = -2 mA, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V | 02, 04 | 2.4 | | V |
| Low-level output voltage | $V_{OL}$ | $V_{CC}$ = 4.5 V, $I_{OL}$ = 16 mA, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V | 01, 02, 03, 04 | | 0.5 | V |
| Input clamp voltage | $V_{IC}$ | $V_{CC}$ = 4.5 V, $I_{IN}$ = -10 mA, $T_C$ = +25°C | 01, 02, 03, 04 | | -1.5 | V |
| Maximum collector cut-off current | $I_{CEX1}$ | $V_{CC}$ = 5.5 V, $V_{OH}$ = 5.2 V | 01, 03 | | 100 | μA |
| High impedance (off-state) output high current | $I_{OHZ}$ | $V_{CC}$ = 5.5 V, $V_{OH}$ = 5.2 V | 02, 04 | | 40 | μA |
| High impedance (off-state) output low current | $I_{OLZ}$ | $V_{CC}$ = 5.5 V, $V_{OL}$ = 0.5 V | 02, 04 | | -40 | μA |
| High level input current | $I_{IH1}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 5.5 V | 01, 02, 03, 04 | | 50 | μA |
| | $I_{IH2}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 4.5 V , special programming pin | | | 100 | |
| Low level input current | $I_{IL}$ | $V_{CC}$ = 5.5 V,  $V_{IN}$ = 0.5 V | 01, 02, 03, 04 | -1.0 | -250 | μA |
| Short circuit output current | $I_{OS}$ | $V_{CC}$ = 5.5 V,   2/ $V_O$ = 0.0 V | 02, 04 | -10 | -100 | mA |
| Supply current | $I_{CC}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 0 V, outputs = open | 01, 02, 03, 04 | | 130 | mA |
| Propagation delay time, high to low level logic, address to output | $t_{PHL1}$ | $V_{CC}$ = 4.5 V and 5.5 V, $C_L$ = 30 pF, see figure 4 | 01, 02 | | 80 | ns |
| | | | 03, 04 | | 35 | |
| Propagation delay time, low to high level logic, address to output | $t_{PLH1}$ | $V_{CC}$ = 4.5 V and 5.5 V, $C_L$ = 30 pF, see figure 4 | 01, 02 | | 80 | ns |
| | | | 03, 04 | | 35 | |
| Propagation delay time, high to low level logic, enable to output | $t_{PHL2}$ | $V_{CC}$ = 4.5 V and 5.5 V, $C_L$ = 30 pF, see figure 4 | 01, 02 | | 50 | ns |
| | | | 03, 04 | | 25 | |
| Propagation delay time, low to high level logic, enable to output | $t_{PLH2}$ | $V_{CC}$ = 4.5 V and 5.5 V, $C_L$ = 30 pF, see figure 4 | 01, 02 | | 50 | ns |
| | | | 03, 04 | | 25 | |

1/  Complete terminal conditions shall be specified in table III.
2/  Not more than one output shall be grounded at one time.  Output shall be at high logic level prior to test.

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| Device types | 01, 02, 03, and 04 |
|---|---|
| Case outlines | E and F |
| Terminal number | Terminal symbol |
| 1 | $O_1$ |
| 2 | $O_2$ |
| 3 | $O_3$ |
| 4 | $O_4$ |
| 5 | $O_5$ |
| 6 | $O_6$ |
| 7 | $O_7$ |
| 8 | GND |
| 9 | $O_8$ |
| 10 | $A_0$ |
| 11 | $A_1$ |
| 12 | $A_2$ |
| 13 | $A_3$ |
| 14 | $A_4$ |
| 15 | $\overline{CE}$ |
| 16 | $V_{CC}$ |

FIGURE 1.  Terminal connections.

| Word | | Address | | | | |
|---|---|---|---|---|---|---|
| number | $\overline{CE}$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |
| NA | L | X | X | X | X | X |
| NA | H | X | X | X | X | X |

| Word | | DATA | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| number | $\overline{CE}$ | $O_1$ | $O_2$ | $O_3$ | $O_4$ | $O_5$ | $O_6$ | $O_7$ | $O_8$ |
| NA | L | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ | 5/ |
| NA | H | OC | OC | OC | OC | OC | OC | OC | OC |

NOTES:

1. NA = Not applicable.
2. X = Input may be high level, low level or open circuit.
3. OC = Open circuit (high resistance output).
4. Program readout can only be accomplished with enable input at low level.
5. The outputs for an unprogrammed device shall be high for circuits A and B; and shall be low for circuits C, G, and H.

FIGURE 2.  Truth table (unprogrammed).
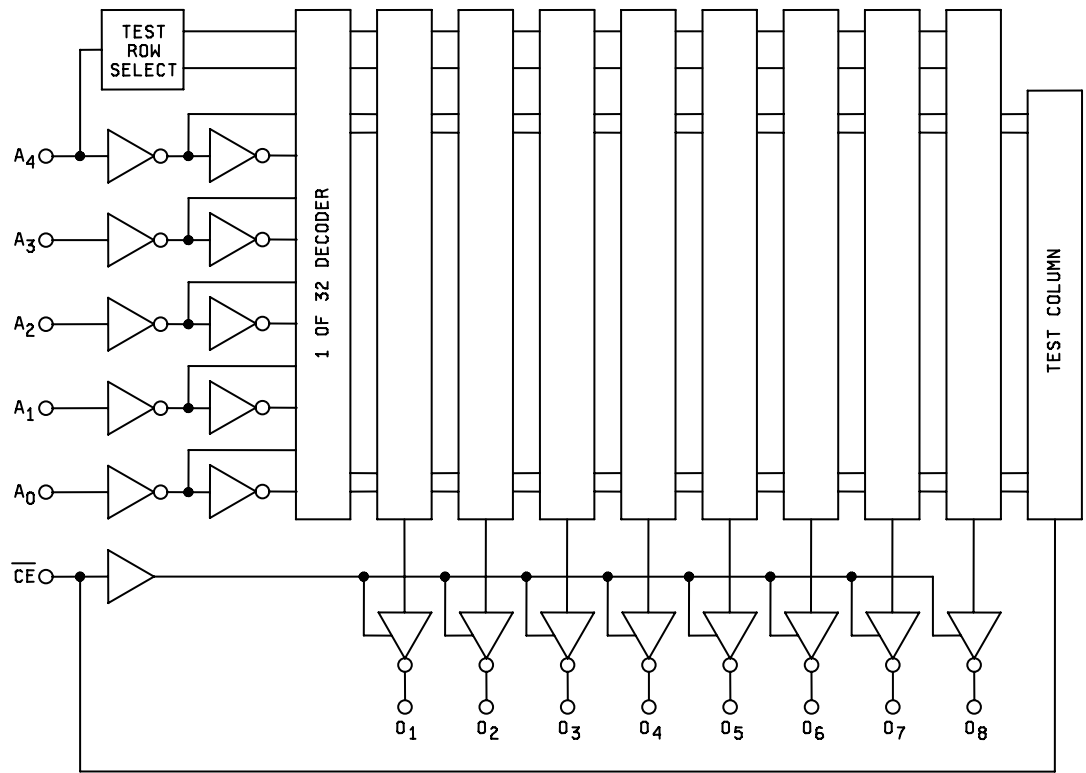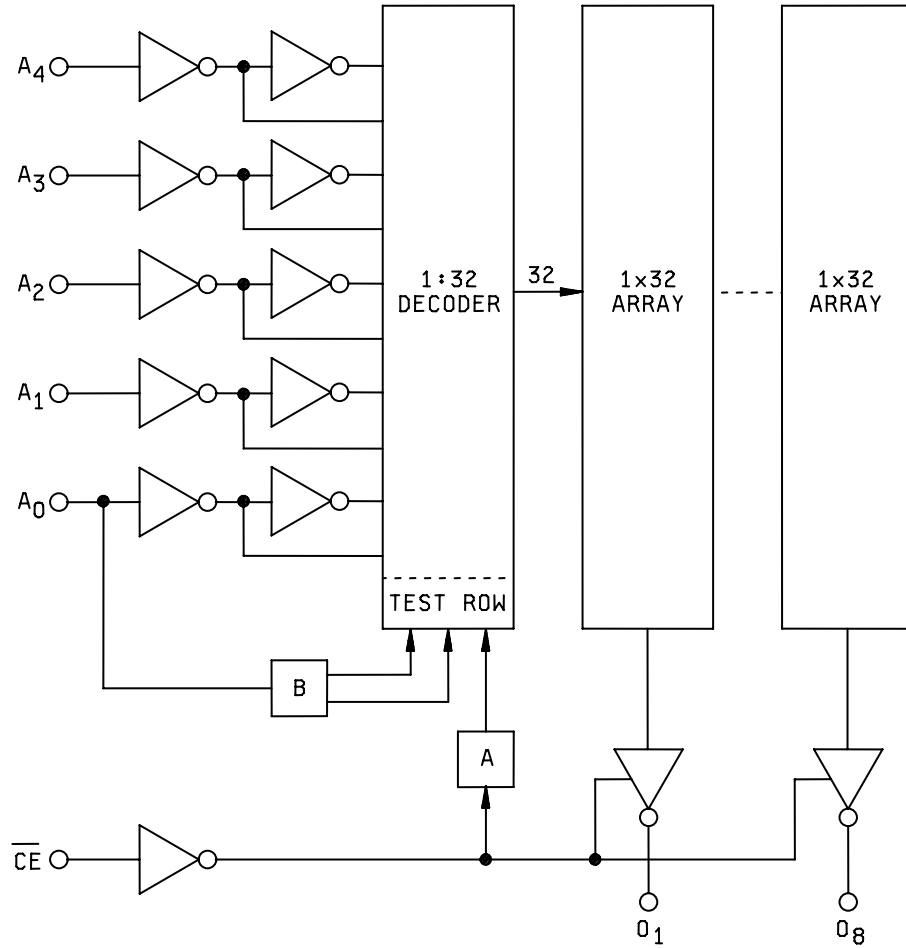
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CIRCUITS A AND B



FIGURE 3.  Functional block diagrams.

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CIRCUIT C



NOTE:  This circuit is also used as circuit H.

FIGURE 3.  Functional block diagrams – Continued.

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CIRCUIT G



FIGURE 3.  Functional block diagrams – Continued.

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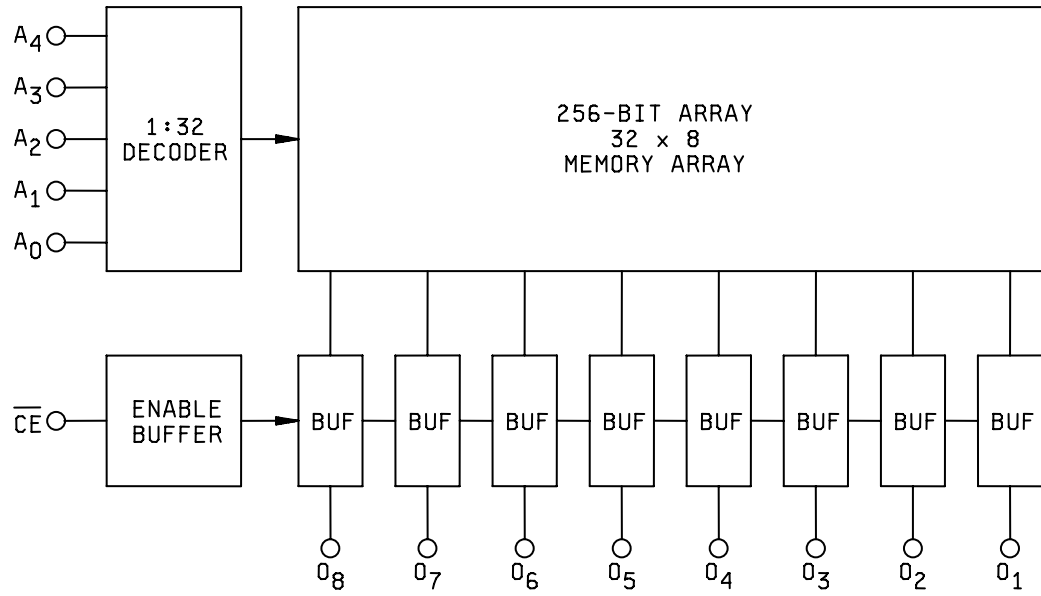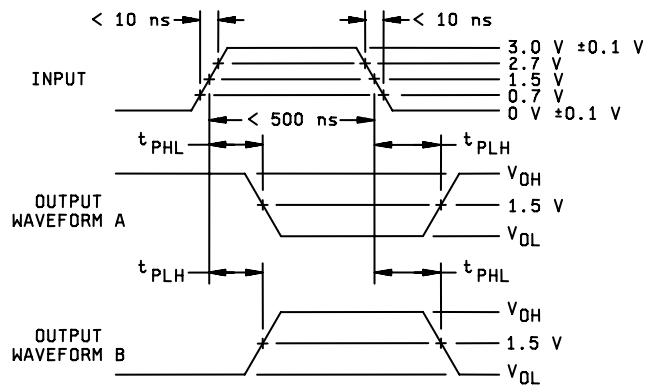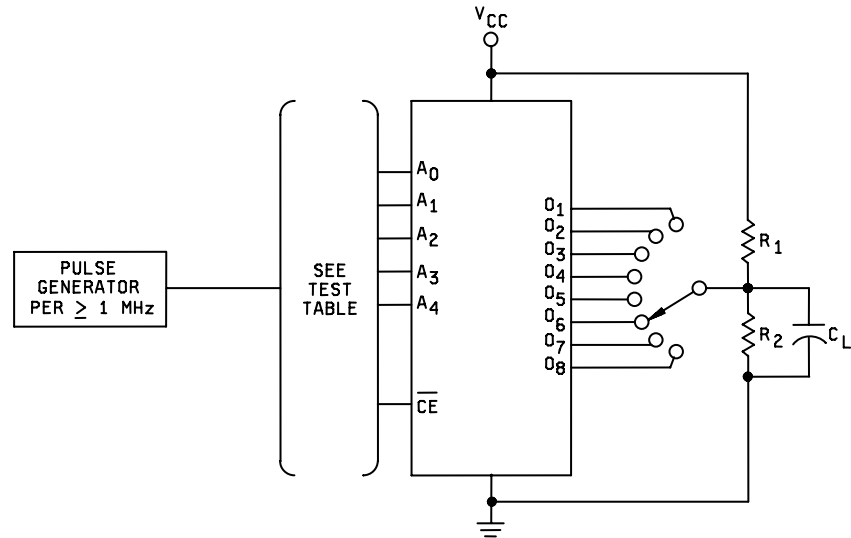
NOTES:
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. $C_L$ = 30 pF minimum, including jig and probe capacitance; $R_1$ = 330 $\Omega$ $\pm25\%$ and $R_2$ = 680 $\Omega$ $\pm20$ %.
3. Outputs may be under load simultaneously.

FIGURE 4.   Switching time test circuit.

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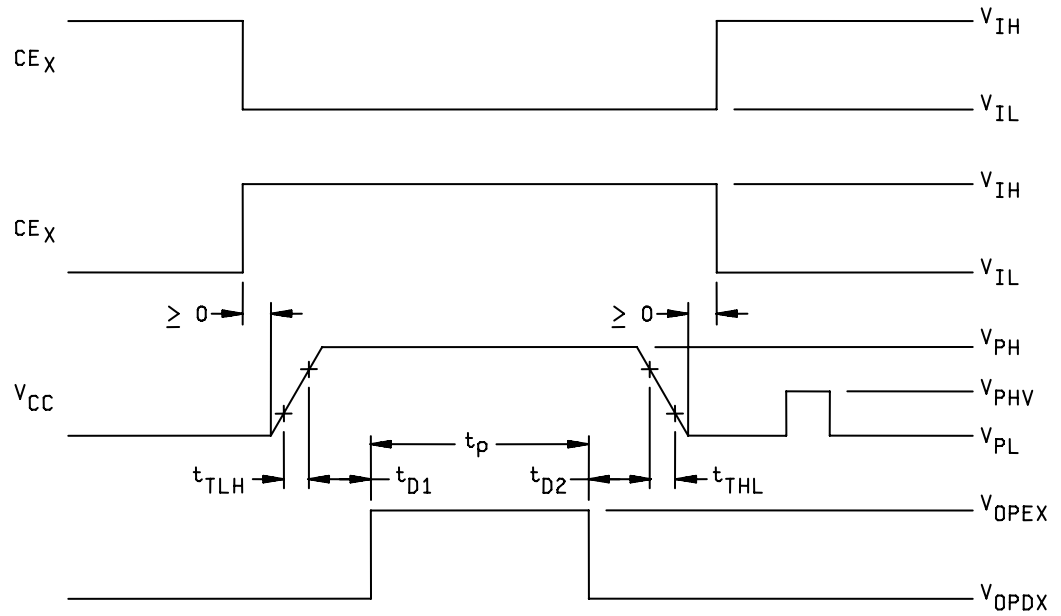
NOTE:  All other waveform characteristics shall be as specified in table IVA.

FIGURE 5A.  Typical programming voltage waveforms during programming for circuit A.

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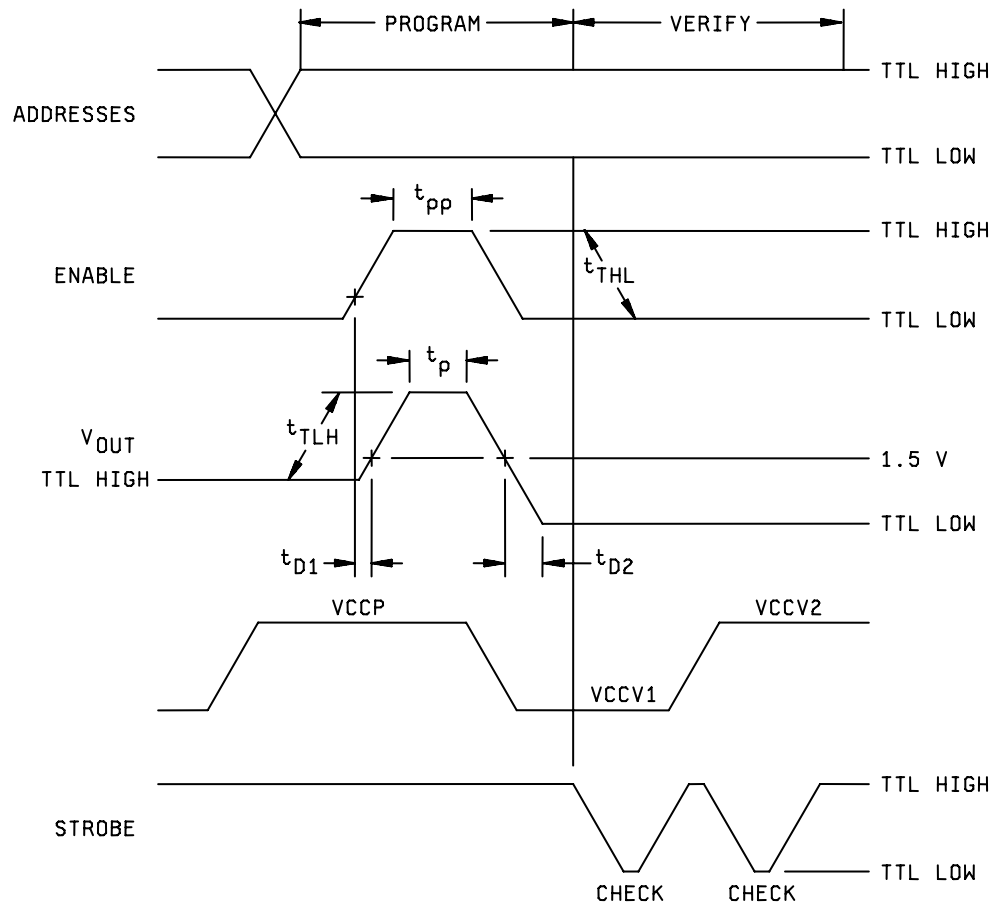
NOTES:
1.   Output load is 0.2 mA and 12 mA during 7.0 V and 4.0 V check respectively.
2.   All other waveform characteristics shall be as specified in table IVB.

FIGURE 5B.  Typical programming voltage waveforms during programming for circuit B.

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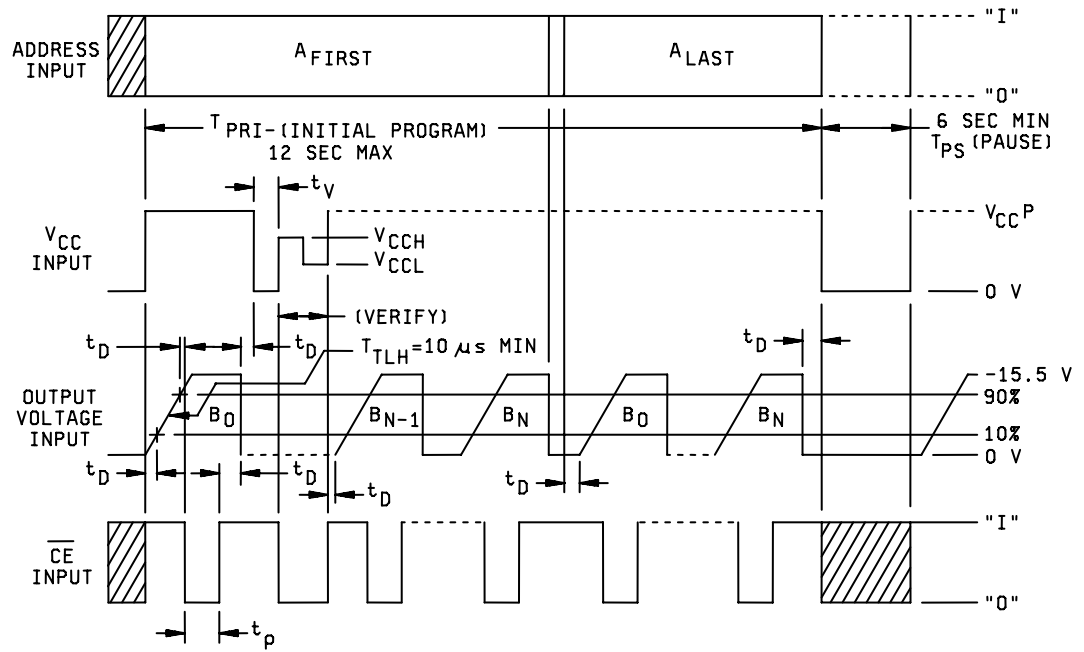
NOTE:  All other waveform characteristics shall be as specified in tables IVC.

FIGURE 5C.  Typical programming voltage waveforms during programming for circuit C.

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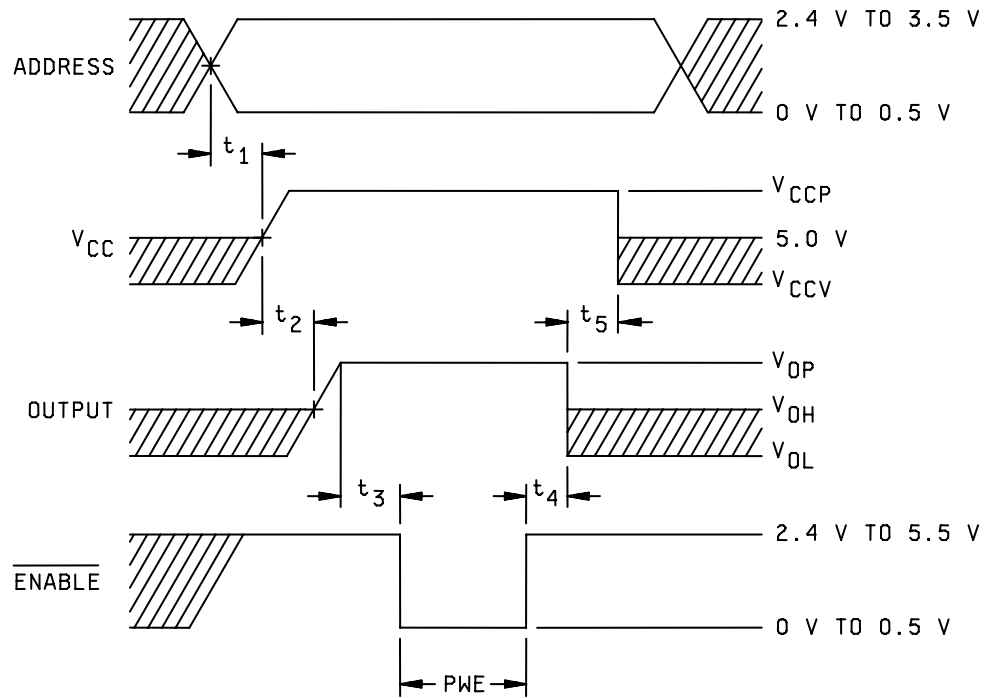
FIGURE 5D.  Typical programming voltage waveforms during programming for circuit G.
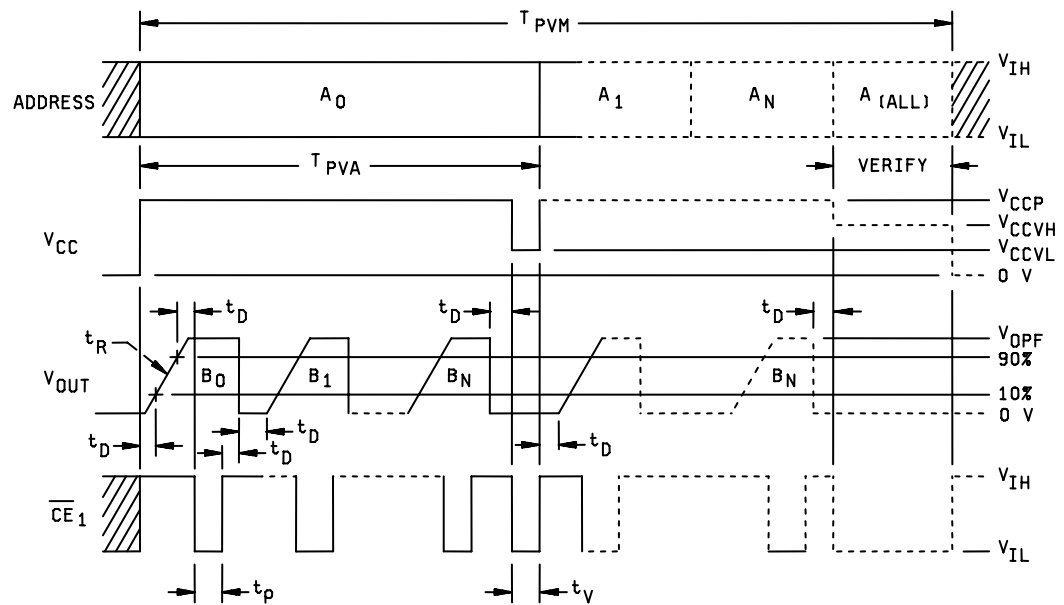
NOTES:
1. All other waveform characteristics shall be as specified in tables IVH.
2. Programming verification at both high and low $V_{CC}$ margins is optional. For convenience, verification can also be executed at the operating $V_{CC}$ limits specified in the dc characteristics.

FIGURE 5E.  Typical programming voltage waveforms during programming for circuit H.

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4. VERIFICATION

4.1  Sampling and inspection.  Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan.  The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2  Screening.  Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection.  The following additional criteria shall apply:

    a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535.  The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request.  The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

    b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

    c.  Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.

    d. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion.  The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein. Class S devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3  Qualification inspection.  Qualification inspection shall be in accordance with MIL-PRF-38535. Qualification data for subgroups 7 through 11 shall be by attributes only.

4.3.1  Qualification extension.   When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies faster device type which is manufactured identically to slower device types on this specification, then the slower device types may be qualified by conducting only group A electrical tests and any electrical specified as additional group C subgroups and submitting data in accordance with MIL-PRF-38535 (for example, groups B, C, and D tests are not required).

4.4  Technology Conformance inspection (TCI).   Technology conformance inspection shall be in accordance with MIL-PRF-38535 and as specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1  Group A inspection.  Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

    a. Electrical test requirements shall be as specified in table II herein.

    b. Subgroups 4, 5, and 6 shall be omitted.

    c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11.  Twelve devices shall be submitted to programming (see 3.3.2.1).  If more than 2 devices fail to program, the lot shall be rejected.  At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowed.

    d. For unprogrammed devices, 10 devices from the programmability sample shall be subjected to the requirements of group A, subgroups 9, 10, and 11.  If more than two total devices fail in all three subgroups, the lot shall be rejected.  At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

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TABLE II. Electrical test requirements.

| MIL-PRF-38535 test requirements | Subgroups (see table III) 1/, 2/, 3/ | |
|---|---|---|
| | Class S devices | Class B devices |
| Interim electrical parameters | 1 | 1 |
| Final electrical test parameters for unprogrammed devices | 1*, 2, 3, 7*, 8 | 1*, 2, 3, 7*, 8 |
| Final electrical test parameters for programmed devices | 1*, 2, 3, 7* 8, 9, 10, 11 | 1*, 2, 3, 7*, 8, 9, |
| Group A test requirements | 1, 2, 3, 7, 8, 9, 10, 11 | 1, 2, 3, 7, 8 9, 10, 11 |
| Group B end-point electrical parameters when using the method 5005 QCI option | 1, 2, 3, 7, 8, 9, 10, 11 | N/A |
| Group C end-point electrical parameters | 1, 2, 3, 7, 8, 9, 10, 11 | 1, 2, 3, 7, 8 |
| Group D test requirements | 1, 2, 3, 7, 8 | 1, 2, 3, 7, 8 |

1/  * indicates PDA applies to subgroups 1 and 7 (see 4.2c).
2/  Any or all subgroups may be combined when using high-speed testers.
3/  Subgroups 7 and 8 shall consist of verifying the pattern specified.


4.4.2  Group B inspection.  Group B inspection shall be in accordance with table II MIL-PRF-38535.

4.4.3  Group C inspection.  Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

   a. End-point electrical parameters shall be as specified in table II herein.

   b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535.  The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request.  The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

   c. For qualification inspection, at least 50 percent of the sample selected for testing in subgroup 1 shall be programmed (see 3.3.2).  For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the life tests.

4.4.4  Group D inspection.  Group D inspection shall be in accordance with table V of MIL-PRF-38535.  End-point electrical parameters shall be as specified in table II herein.

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TABLE III. Group A inspection for device types 01 and 03.
Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are ≥ 2.0 V, low ≤ 0.8 V).

| Subgroup | Symbol | MIL-STD-883 method | Cases E,F Test no. | 1 $O_1$ | 2 $O_2$ | 3 $O_3$ | 4 $O_4$ | 5 $O_5$ | 6 $O_6$ | 7 $O_7$ | 8 GND | 9 $O_8$ | 10 $A_0$ | 11 $A_1$ | 12 $A_2$ | 13 $A_3$ | 14 $A_4$ | 15 $\overline{CE}$ | 16 $V_{CC}$ | Measured terminal | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 $T_C$ = 25°C | $V_{IC}$ | | 1 | | | | | | | | GND | | -10mA | | | | | | 4.5V | $A_0$ | | -1.5 | V |
| | | | 2 | | | | | | | | " | | | -10mA | | | | | " | $A_1$ | | " | " |
| | | | 3 | | | | | | | | " | | | | -10mA | | | | " | $A_2$ | | " | " |
| | | | 4 | | | | | | | | " | | | | | -10mA | | | " | $A_3$ | | " | " |
| | | | 5 | | | | | | | | " | | | | | | -10mA | | " | $A_4$ | | " | " |
| | | | 6 | | | | | | | | " | | | | | | | -10mA | " | $\overline{CE}$ | | " | " |
| | $V_{OL}$ | 3007 | 7 | 16mA | | | | | | | " | | 1/ 2/ 3/ | 1/ 3/ | 1/ 3/ | 1/ 3/ | 1/ 2/ 3/ 4/ | 0.5V | | $O_1$ | | 0.5 | " |
| | | " | 8 | | 16mA | | | | | | " | | " | " | " | " | " | " | | $O_2$ | | " | " |
| | | " | 9 | | | 16mA | | | | | " | | " | " | " | " | " | " | | $O_3$ | | " | " |
| | | " | 10 | | | | 16mA | | | | " | | " | " | " | " | " | " | | $O_4$ | | " | " |
| | | " | 11 | | | | | 16mA | | | " | | " | " | " | " | " | " | | $O_5$ | | " | " |
| | | " | 12 | | | | | | 16mA | | " | | " | " | " | " | " | " | | $O_6$ | | " | " |
| | | " | 13 | | | | | | | 16mA | " | | " | " | " | " | " | " | | $O_7$ | | " | " |
| | | " | 14 | | | | | | | | " | 16mA | " | " | " | " | " | " | | $O_8$ | | " | " |
| | $I_{IL}$ | 3009 | 15 | | | | | | | | " | | 0.5V | | | | | | 5.5V | $A_0$ | -1.0 | -250 | µA |
| | | " | 16 | | | | | | | | " | | | 0.5V | | | | | " | $A_1$ | " | " | " |
| | | " | 17 | | | | | | | | " | | | | 0.5V | | | | " | $A_2$ | " | " | " |
| | | " | 18 | | | | | | | | " | | | | | 0.5V | | | " | $A_3$ | " | " | " |
| | | " | 19 | | | | | | | | " | | | | | | 0.5V | | " | $A_4$ | " | " | " |
| | | " | 20 | | | | | | | | " | | | | | | | 0.5V | " | $\overline{CE}$ | | " | " |
| | $I_{IH1}$ | 3010 | 21 | | | | | | | | " | | 5.5V | | | | | | " | $A_0$ | | 50 | " |
| | | " | 22 | | | | | | | | " | | | 5.5V | | | | | " | $A_1$ | | " | " |
| | | " | 23 | | | | | | | | " | | | | 5.5V | | | | " | $A_2$ | | " | " |
| | | " | 24 | | | | | | | | " | | | | | 5.5V | | | " | $A_3$ | | " | " |
| | | " | 25 | | | | | | | | " | | | | | | 5.5V | | " | $A_4$ | | " | " |
| | $I_{IH2}$ | " | 26 | | | | | | | | " | | | | | | | 4.5V 5/ | " | $\overline{CE}$ | | 100 | |
| | $I_{CEX}$ | " | 27 | 5.2V | | | | | | | " | | | | | | | | " | $O_1$ | | " | " |
| | | " | 28 | | 5.2V | | | | | | " | | | | | | | | " | $O_2$ | | " | " |
| | | " | 29 | | | 5.2V | | | | | " | | | | | | | | " | $O_3$ | | " | " |
| | | " | 30 | | | | 5.2V | | | | " | | | | | | | | " | $O_4$ | | " | " |
| | | " | 31 | | | | | 5.2V | | | " | | | | | | | | " | $O_5$ | | " | " |
| | | " | 32 | | | | | | 5.2V | | " | | | | | | | | " | $O_6$ | | " | " |
| | | " | 33 | | | | | | | 5.2V | " | | | | | | | | " | $O_7$ | | " | " |
| | | " | 34 | | | | | | | | " | 5.2V | | | | | | | " | $O_8$ | | " | " |
| | $I_{CC}$ | 3005 | 35 | | | | | | 5.2V | 5.2V | " | 5.2V | GND | GND | GND | GND | GND | GND | GND | $V_{CC}$ | | 130 | mA |
| 2 | Same tests, terminal conditions, and limits as for subgroup 1, except $T_C$ = 125°C and $V_{IC}$ tests are omitted. | | | | | | | | | | | | | | | | | | | | | | |
| 3 | Same tests, terminal conditions, and limits as for subgroup 1, except $T_C$ = -55°C and $V_{IC}$ tests are omitted. | | | | | | | | | | | | | | | | | | | | | | |

See footnotes at end of table.

TABLE III. Group A inspection for device types 01 and 03 – Continued.
Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are ≥ 2.0 V, low ≤ 0.8 V, or open).

| Subgroup | Symbol | MIL-STD-883 method | Cases E,F Test no. | 1 $O_1$ | 2 $O_2$ | 3 $O_3$ | 4 $O_4$ | 5 $O_5$ | 6 $O_6$ | 7 $O_7$ | 8 GND | 9 $O_8$ | 10 $A_0$ | 11 $A_1$ | 12 $A_2$ | 13 $A_3$ | 14 $A_4$ | 15 $\overline{CE}$ | 16 Vcc | Measured terminal | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 $T_C$ = 25°C | Functional test | 6/ | 36 | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | GND | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | $O_1$ | | 6/ | |
| | | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | $O_2$ | | " | |
| | | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | $O_3$ | | " | |
| | | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | $O_4$ | | " | |
| | | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | $O_5$ | | " | |
| | | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | $O_6$ | | " | |
| | | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | $O_7$ | | " | |
| | | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | " | $O_8$ | | " | |
| 8 | Same tests, terminal conditions, and limits as for subgroup 7, except $T_C$ = 125°C and -55°C. | | | | | | | | | | | | | | | | | | | | | | |
| 9 $T_C$ = 25°C | $t_{PHL1}$ | GALPAT Fig. 4 | 37 | 7/ | 7/ | 7/ | 7/ | 7/ | 7/ | 7/ | GND | 7/ | 8/ | 8/ | 8/ | 8/ | 8/ | GND | 8/ | Outputs | | 9/ | ns |
| | $t_{PLH1}$ | GALPAT Fig. 4 | 38 | " | " | " | " | " | " | " | " | " | 8/ | 8/ | 8/ | 8/ | 8/ | GND | 8/ | " | | 9/ | " |
| | $t_{PHL2}$ | Sequential Fig. 4 | 39 | " | " | " | " | " | " | " | " | " | 10/ | 10/ | 10/ | 10/ | 10/ | 10/ | 10/ | " | | 9/ | " |
| | $t_{PLH2}$ | Sequential Fig. 4 | 40 | " | " | " | " | " | " | " | " | " | 10/ | 10/ | 10/ | 10/ | 10/ | 10/ | 10/ | " | | 9/ | " |
| 10 | Same tests, terminal conditions, and limits as for subgroup 9, except $T_C$ = 125°C. | | | | | | | | | | | | | | | | | | | | | | |
| 11 | Same tests, terminal conditions, and limits as for subgroup 9, except $T_C$ = -55°C. | | | | | | | | | | | | | | | | | | | | | | |

See footnotes at end of table.

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TABLE III. Group A inspection for device types 02 and 04.
Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are ≥ 2.0 V, low ≤ 0.8 V).

| Subgroup | Symbol | MIL-STD-883 method | Cases E,F Test no. | 1 O₁ | 2 O₂ | 3 O₃ | 4 O₄ | 5 O₅ | 6 O₆ | 7 O₇ | 8 GND | 9 O₈ | 10 A₀ | 11 A₁ | 12 A₂ | 13 A₃ | 14 A₄ | 15 C̅E̅ | 16 Vcc | Measured terminal | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 Tc = 25°C | V$_{IC}$ | | 1 | | | | | | | | GND | | -10mA | | | | | | 4.5V | A₀ | | -1.5 | V |
| | | | 2 | | | | | | | | " | | | -10mA | | | | | " | A₁ | | " | " |
| | | | 3 | | | | | | | | " | | | | -10mA | | | | " | A₂ | | " | " |
| | | | 4 | | | | | | | | " | | | | | -10mA | | | " | A₃ | | " | " |
| | | | 5 | | | | | | | | " | | | | | | -10mA | | " | A₄ | | " | " |
| | | | 6 | | | | | | | | " | | | | | | | -10mA | " | C̅E̅ | | " | " |
| | V$_{OL}$ | 3007 | 7 | 16mA | | | | | | | " | | 1/ 2/ 3/ | 1/ 3/ | 1/ 3/ | 1/ 3/ | 1/ 2/ 3/ 4/ | 0.5V | " | O₁ | | 0.5 | " |
| | | " | 8 | | 16mA | | | | | | " | | " | " | " | " | " | " | " | O₂ | | " | " |
| | | " | 9 | | | 16mA | | | | | " | | " | " | " | " | " | " | " | O₃ | | " | " |
| | | " | 10 | | | | 16mA | | | | " | | " | " | " | " | " | " | " | O₄ | | " | " |
| | | " | 11 | | | | | 16mA | | | " | | " | " | " | " | " | " | " | O₅ | | " | " |
| | | " | 12 | | | | | | 16mA | | " | | " | " | " | " | " | " | " | O₆ | | " | " |
| | | " | 13 | | | | | | | 16mA | " | | " | " | " | " | " | " | " | O₇ | | " | " |
| | | " | 14 | | | | | | | | " | 16mA | " | " | " | " | " | " | " | O₈ | | " | " |
| | V$_{OH}$ | 3006 | 15 | -2.0mA | | | | | | | " | | 1/ 11/ 12/ 13/ | 1/ 11/ 12/ 13/ | 1/ 11/ 12/ 13/ | 1/ 11/ 12/ 13/ | 1/ 11/ 12/ 13/ | 1/ | " | O₁ | 2.4 | | " |
| | | " | 16 | | -2.0mA | | | | | | " | | " | " | " | " | " | " | " | O₂ | " | | " |
| | | " | 17 | | | -2.0mA | | | | | " | | " | " | " | " | " | " | " | O₃ | " | | " |
| | | " | 18 | | | | -2.0mA | | | | " | | " | " | " | " | " | " | " | O₄ | " | | " |
| | | " | 19 | | | | | -2.0mA | | | " | | " | " | " | " | " | " | " | O₅ | " | | " |
| | | " | 20 | | | | | | -2.0mA | | " | | " | " | " | " | " | " | " | O₆ | " | | " |
| | | " | 21 | | | | | | | -2.0mA | " | | " | " | " | " | " | " | " | O₇ | " | | " |
| | | " | 22 | | | | | | | | " | -2.0mA | " | " | " | " | " | " | " | O₈ | " | | " |
| | I$_{IL}$ | 3009 | 23 | | | | | | | | " | | 0.5V | 0.5V | 0.5V | 0.5V | 0.5V | 1/ | 5.5V | A₀ | -1.0 | -250 | µA |
| | | " | 24 | | | | | | | | " | | " | " | " | " | " | " | " | A₁ | " | " | " |
| | | " | 25 | | | | | | | | " | | " | " | " | " | " | " | " | A₂ | " | " | " |
| | | " | 26 | | | | | | | | " | | " | " | " | " | " | " | " | A₃ | " | " | " |
| | | " | 27 | | | | | | | | " | | " | " | " | " | " | " | " | A₄ | " | " | " |
| | | " | 28 | | | | | | | | " | | " | " | " | " | " | 0.5V | " | C̅E̅ | " | " | " |
| | I$_{IH1}$ | 3010 | 29 | | | | | | | | " | | 5.5V | 5.5V | 5.5V | 5.5V | 5.5V | | " | A₀ | | 50 | " |
| | | " | 30 | | | | | | | | " | | " | " | " | " | " | | " | A₁ | | " | " |
| | | " | 31 | | | | | | | | " | | " | " | " | " | " | | " | A₂ | | " | " |
| | | " | 32 | | | | | | | | " | | " | " | " | " | " | | " | A₃ | | " | " |
| | | " | 33 | | | | | | | | " | | " | " | " | " | 5.5V | | " | A₄ | | " | " |
| | I$_{IH2}$ | " | 34 | | | | | | | | " | | | | | | | 4.5V 4/ | " | C̅E̅ | | 100 | " |
| | I$_{OHZ}$ | | 35 | 5.2V | | | | | | | | | | | | | | 5.5V | " | O₁ | | 40 | " |
| | | | 36 | | 5.2V | | | | | | | | | | | | | " | " | O₂ | | " | " |
| | | | 37 | | | 5.2V | | | | | | | | | | | | " | " | O₃ | | " | " |
| | | | 38 | | | | 5.2V | | | | | | | | | | | " | " | O₄ | | " | " |
| | | | 39 | | | | | 5.2V | | | | | | | | | | " | " | O₅ | | " | " |
| | | | 40 | | | | | | 5.2V | | | | | | | | | " | " | O₆ | | " | " |
| | | | 41 | | | | | | | 5.2V | | | | | | | | " | " | O₇ | | " | " |
| | | | 42 | | | | | | | | | 5.2V | | | | | | " | " | O₈ | | " | " |

See footnotes at end of table.

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TABLE III. Group A inspection for devices type 02 and 04 – Continued.
Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are ≥ 2.0 V, low ≤ 0.8 V).

| Subgroup | Symbol | MIL-STD-883 method | Cases E,F Test no. | 1 $O_1$ | 2 $O_2$ | 3 $O_3$ | 4 $O_4$ | 5 $O_5$ | 6 $O_6$ | 7 $O_7$ | 8 GND | 9 $O_8$ | 10 $A_0$ | 11 $A_1$ | 12 $A_2$ | 13 $A_3$ | 14 $A_4$ | 15 $\overline{CE}$ | 16 $V_{CC}$ | Measured terminal | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 $T_C = 25°C$ | $I_{OLZ}$ | | 43 | 0.5V | | | | | | | GND | | | | | | | 5.5V | 5.5V | $O_1$ | | -40 | µA |
| | | | 44 | | 0.5V | | | | | | ″ | | | | | | | ″ | ″ | $O_2$ | | ″ | ″ |
| | | | 45 | | | 0.5V | | | | | ″ | | | | | | | ″ | ″ | $O_3$ | | ″ | ″ |
| | | | 46 | | | | 0.5V | | | | ″ | | | | | | | ″ | ″ | $O_4$ | | ″ | ″ |
| | | | 47 | | | | | 0.5V | | | ″ | | | | | | | ″ | ″ | $O_5$ | | ″ | ″ |
| | | | 48 | | | | | | 0.5V | | ″ | | | | | | | ″ | ″ | $O_6$ | | ″ | ″ |
| | | | 49 | | | | | | | 0.5V | ″ | | | | | | | ″ | ″ | $O_7$ | | ″ | ″ |
| | | | 50 | | | | | | | | ″ | 0.5V | | | | | | ″ | ″ | $O_8$ | | ″ | ″ |
| | $I_{CC}$ | 3005 | 51 | | | | | | | | | | GND | GND | GND | GND | GND | GND | ″ | $V_{CC}$ | | 130 | mA |
| | $I_{OS}$ | 3011 | 52 | GND | | | | | | | | | 1/ 11/ 12/ 13/ | 1/ 11/ 12/ 13/ | 1/ 11/ 12/ 13/ | 1/ 11/ 12/ 13/ | 1/ 11/ 12/ 13/ | 0.5V | ″ | $O_1$ | -10 | -100 | ″ |
| | | ″ | 53 | | GND | | | | | | | | ″ | ″ | ″ | ″ | ″ | ″ | ″ | $O_2$ | ″ | ″ | ″ |
| | | ″ | 54 | | | GND | | | | | | | ″ | ″ | ″ | ″ | ″ | ″ | ″ | $O_3$ | ″ | ″ | ″ |
| | | ″ | 55 | | | | GND | | | | | | ″ | ″ | ″ | ″ | ″ | ″ | ″ | $O_4$ | ″ | ″ | ″ |
| | | ″ | 56 | | | | | GND | | | | | ″ | ″ | ″ | ″ | ″ | ″ | ″ | $O_5$ | ″ | ″ | ″ |
| | | ″ | 57 | | | | | | GND | | | | ″ | ″ | ″ | ″ | ″ | ″ | ″ | $O_6$ | ″ | ″ | ″ |
| | | ″ | 58 | | | | | | | GND | | | ″ | ″ | ″ | ″ | ″ | ″ | ″ | $O_7$ | ″ | ″ | ″ |
| | | ″ | 59 | | | | | | | | | GND | ″ | ″ | ″ | ″ | ″ | ″ | ″ | $O_8$ | ″ | ″ | ″ |
| 2 | Same tests, terminal conditions, and limits as for subgroup 1, except $T_C = 125°C$ and $V_{IC}$ tests are omitted. | | | | | | | | | | | | | | | | | | | | | | |
| 3 | Same tests, terminal conditions, and limits as for subgroup 1, except $T_C = -55°C$ and $V_{IC}$ tests are omitted. | | | | | | | | | | | | | | | | | | | | | | |
| 7 $T_C = 25°C$ | Functional tests | 6/ | 60 | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | GND | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | 6/ | Outputs | | 6/ | |
| 8 | Same tests, terminal conditions, and limits as for subgroup 7, except $T_C = 125°C$ and $T_C = -55°C$. | | | | | | | | | | | | | | | | | | | | | | |
| 9 $T_C = 25°C$ | $t_{PHL1}$ | GALPAT Fig. 4 | 61 | 7/ | 7/ | 7/ | 7/ | 7/ | 7/ | 7/ | GND | 7/ | 8/ | 8/ | 8/ | 8/ | 8/ | GND | 8/ | Outputs | | 9/ | ns |
| | $t_{PLH1}$ | GALPAT Fig. 4 | 62 | ″ | ″ | ″ | ″ | ″ | ″ | ″ | ″ | ″ | 8/ | 8/ | 8/ | 8/ | 8/ | GND | 8/ | ″ | | 9/ | ″ |
| | $t_{PHL2}$ | Sequential Fig. 4 | 63 | ″ | ″ | ″ | ″ | ″ | ″ | ″ | ″ | ″ | 10/ | 10/ | 10/ | 10/ | 10/ | 10/ | 10/ | ″ | | 9/ | ″ |
| | $t_{PLH2}$ | Sequential Fig. 4 | 64 | ″ | ″ | ″ | ″ | ″ | ″ | ″ | ″ | ″ | 10/ | 10/ | 10/ | 10/ | 10/ | 10/ | 10/ | ″ | | 9/ | ″ |
| 10 | Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = 125°C$. | | | | | | | | | | | | | | | | | | | | | | |
| 11 | Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = -55°C$. | | | | | | | | | | | | | | | | | | | | | | |

See footnotes at end of table.

TABLE III.  Group A inspection – Continued.

1/  For programmed devices, select an appropriate address to acquire the desired output state, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V.

2/  For unprogrammed devices, apply 11.0 V on pins 10 ( $A_0$ ) and 14 ( $A_4$ ) for circuit A devices.

3/  For unprogrammed 02 devices ( $V_{OL}$ test ), apply 0 V on pins 10 ( $A_0$ ) through 14 ( $A_4$ ) for circuit G.

4/  For unprogrammed devices, apply 12.0 V on pin 14 ( $A_4$ ) for circuit B devices.

5/  This test may, at the manufacturer's option, be performed with $V_{IH}$ = 5.5 V (pin 15) and test limit of 50 $\mu$A maximum.

6/  The functional tests shall verify that no fuses are blown for unprogrammed devices or that the truth table specified in the altered item drawing exists for programmed devices (see table II and 3.3.2.2). All bits shall be tested.  Terminal conditions shall be as follows:

a.  Inputs: H = 3.0 V, L = 0.0 V.
b.  Outputs:  Output voltage shall be:  H $\geq$ 1.0 V and L $<$ 1.0 V.
c.  The functional tests shall be performed with $V_{CC}$ = 4.5 V and $V_{CC}$ = 5.5 V.

7/  The outputs are loaded per figure 4.

8/  GALPAT (PROGRAMMED PROM).

This program will test all bits in the array, the addressing and interaction between bits for ac performance $t_{PHL1}$ and $t_{PLH1}$ .  Each bit in the pattern is fixed by being programmed with a "H" and "L".

Description:

Step 1.  Word 0 is read.
Step 2.  Word 1 is read.
Step 3.  Word 0 is read
Step 4.  Word 2 is read.
Step 5.  Word 0 is read.
Step 6.  The reading procedure continues back and forth between word 0 and the next higher numbered word until word 255 is reached, then increments to the next word and reads back and forth as in step 1 through step 6 and shall include all words.
Step 7.  Pass execution time = ( $n^2$ + n ) x cycle time.  N = 256.
Step 8.  The GALPAT tests shall be performed with $V_{CC}$ = 4.5 V and 5.5 V.

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| Device | $t_{PHL1}$ | $t_{PLH1}$ | $t_{PHL2}$ | $t_{PLH2}$ |
|--------|-----------|-----------|-----------|-----------|
| 01, 02 | 80 ns | 80 ns | 50 ns | 50 ns |
| 03, 04 | 35 ns | 35 ns | 25 ns | 25 ns |

TABLE III.  <u>Group A inspection</u> – Continued.

<u>10</u>/  SEQUENTIAL (PROGRAMMED PROM).

This program will test all bits in the array for $t_{PHL2}$ and $t_{PLH2}$.

<u>Description</u>:

Step 1.   Each word in the pattern is tested from the enable lines to the output lines for recovery.
Step 2.   Word 0 is addressed.  Enable line is pulled high to low and low to high.  $t_{PHL2}$ and $t_{PLH2}$ are read.
Step 3.   Word 1 is addressed.  Same enable sequence as above.
Step 4.   The reading procedure continues until word 255 is reached.
Step 5.   Pass execution time = 256 x cycle time.
Step 6.   The sequential tests shall be performed with $V_{CC}$ = 4.5 V and 5.5 V.

<u>11</u>/  For unprogrammed 01, 02 devices (with date codes before 8601), apply 10.0 V to pin 10 ( $A_0$ ), apply 0.5 V to pin 11 ( $A_1$ ), and other 5.0 V on all other addresses for circuit C.

<u>12</u>/  For unprogrammed 02 devices ( $V_{OH}$ test ), with date codes before 8713, apply 0 V to pins 10 ( $A_0$ ) through 13 ( $A_3$ ), and 11.5 V to pin 14 ( $A_4$ ), with date codes of 8713 or later apply 3.0 V to pins 10 ( $A_0$ ) through 13 ( $A_3$ ), and 10.5 V to pin 14 ( $A_4$ ) for circuit G.

<u>13</u>/  For unprogrammed devices 01, 02 (with date codes of 8601 or later), 03 and 04, apply 10.0 V to pin 10 ( $A_0$ ), 0.5 V to pins 12, 13, 14, ( $A_2$, $A_3$, $A_4$ ) and 5.0 V to all other addresses for circuit C.

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4.5  <u>Methods of inspection.</u>  Methods of inspection shall be specified and as follows:

4.5.1  <u>Voltage and current.</u>  All voltages given are referenced to the microcircuit ground terminal.  Currents given are conventional and positive when flowing into the referenced terminal.

4.6  <u>Programming procedure identification.</u>  The programming procedure to be utilized shall be identified by the manufacturer's circuit designator.  The circuit designator is cross referenced in paragraph 6.6 herein with the manufacturer's symbol or CAGE number.

4.7  <u>Programming procedure for circuit A</u>.  The programming characteristics in table IVA and the following procedures shall be used for programming the device.

  a.  Connect the device in the electrical configuration for programming.  The waveforms on figure 5A and the programming characteristics in table IVA shall apply to these procedures.

  b.  Address the PROM with the binary address of the word to be programmed.  Address inputs are TTL compatible.  An open circuit shall not be used to address the PROM.

  c.  Apply $V_{PL}$ voltage to $V_{CC}$.

  d.  Bring the $\overline{CE}_X$ inputs high and the $\overline{CE}_X$ inputs low to disable the device.  The chip enables are TTL compatible.  An open circuit shall not be used to disable the device.

  e.  Disable the programming circuitry by applying a voltage of $V_{OPD}$ to the outputs of the PROM.

  f.  Raise $V_{CC}$ to $V_{PH}$ with rise time less than or equal to $t_{TLH}$.

  g.  After a delay equal to or greater than $t_{D1}$ apply only one pulse with amplitude of $V_{OPE}$ and duration of $t_p$ to the output selected for programming.  Note that the PROM is supplied with fuses intact, which generates an output high.  Programming a fuse will cause the output to go low.

  h.  Lower $V_{CC}$ to $V_{PL}$ following a delay to $t_{D2}$ from programming enable pulse applied to an output.

  i.  Enable the PROM for verification by applying $V_{IL}$ to $\overline{CE}_X$ and $V_{IH}$ to $\overline{CE}_X$.

  j.  Apply $V_{PHV}$ to $V_{CC}$ and verify bit is programmed.

  k.  Repeat steps a through j for all other bits to be programmed in the PROM.

  l.  For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

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TABLE IVA.  Programming characteristics for circuit A.

| Parameter | Symbol | Limits 1/ | | | Unit |
|---|---|---|---|---|---|
| | | Min | Recommended | Max | |
| Address input voltage  2/ | $V_{IH}$ | 2.4 | 5.0 | 5.0 | V |
| | $V_{IL}$ | 0.0 | 0.4 | 0.5 | " |
| Programming | $V_{PH}$  3/ | 10.75 | 11.0 | 11.25 | V |
| Voltage to $V_{CC}$ low | $V_{PL}$ | 0.0 | 0.0 | 1.5 | V |
| Program verify | $V_{PHV}$ | --- | 5.5 | --- | V |
| Verify voltage | $V_R$  4/ | 4.5 | 5.0 | 5.5 | V |
| Programming input low current at $V_{PH}$ | $I_{ILP}$ | --- | -300 | -600 | $\mu$A |
| Programmed voltage ($V_{CC}$) transition time | $t_{TLH}$ | 1 | 5 | 10 | $\mu$s |
| | $t_{THL}$ | 1 | 5 | 10 | " |
| Programming delay | $t_{D1}$ | 10 | 10 | 20 | $\mu$s |
| | $t_{D2}$ | 1 | 5 | 5 | " |
| Programming pulse width | $t_P$  5/ | 90 | 100 | 110 | $\mu$s |
| Programming duty cycle | PDC  6/ | --- | 30 | 60 | % |
| Output voltage Enable | $V_{OPE}$  7/ | 10.5 | 10.5 | 11.0 | V |
| Output voltage Disable | $V_{OPD}$  7/ | 0.0 | 5.0 | 5.5 | V |

During the programming the chip must be disabled for proper operation.

1/  $T_C$ = +25°C.

2/  No inputs should be left open for $V_{IH}$.

3/  $V_{PH}$ source must be capable of supplying one ampere.

4/  It is recommended that post programming dual verification be made at $V_R$ minimum and $V_R$ maximum.

5/  Note step j in programming procedure.

6/  Programming duty cycle applies to DIPs only.

7/  $V_{OPE}$ source must be capable of supplying 10 mA minimum.

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4.8  Programming procedure for circuit B.   The programming characteristics in table IVB and the following procedures shall be used for programming the devices:

a. Connect the device in the electrical configuration for programming.  The waveforms on figure 5B and the programming characteristics of table IVB shall apply to these procedures.

b. Raise $V_{CC}$ to 5.5 volts.

c. Address the PROM with binary address of the selected word to be programmed. Address inputs are TTL compatible.

d. Disable the chip by applying $V_{IH}$ to the $\overline{CE}$ input.  $\overline{CE}$ input is TTL compatible.

e. Apply the $V_{PP}$ pulse to the $\overline{CE}$ pin.  In order to insure that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse shall precede the output pin's programming pulse by $t_{D1}$ and leave after the output pin's programming pulse by $t_{D2}$ (see figure 5B).

f. Apply the $V_{OUT}$ pulse with duration of $t_P$ to the output selected for programming (see table IVB). The outputs shall be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.  Note that the PROM is supplied with fuses generating a high-level logic output.  Programming a fuse will cause the output to go to a low-level logic in the verify mode.

g. Other bits in the same word may be programmed sequentially applying $V_{OUT}$ pulses to each output to be programmed.

h. Repeat 4.8b through 4.8g for all bits to be programmed.

i. Enable the chip by applying $V_{IL}$ to the $\overline{CE}$ input and verify the program.

   Verification may check for a low output by requiring the device to sink 12 mA at $V_{CC} = 4.0$ V and 0.2 mA at $V_{CC} = 7.0$ V at $T_C = 25°C$.

j. For classes S and B devices, if any bit does not verify as programmed it shall be considered a programming reject.

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TABLE IVB.  Programming characteristics for circuit B.

| Parameter | Symbol | Conditions | Limits 1/ | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Recommended | Max | |
| Current into output during programming before the fuse has programmed | I$_{OUT1}$ | V$_{CC}$ = 5.5 V, V$_{OUT}$ = 9.0 V | | 0.1 | | mA |
| | | V$_{CC}$ = 5.5 V, V$_{OUT}$ = 25 V | | 35 | | |
| Current into output during programming after the fuse has programmed | I$_{OUT2}$ | V$_{CC}$ = 5.5 V, V$_{OUT}$ = 20 V | | 3 | | mA |
| Rise time of program pulse applied to the data out from 10% to 90% | t$_{TLH}$ | | 50 | 60 | 70 | μs |
| Chip enable ($\overline{CE}$) pin pulse width | t$_{PP}$ | Chip disabled V$_{CC}$ = 5.5 V | 80 | 95 | 110 | μs |
| Pulse width of programming voltage | t$_P$ | Chip disabled V$_{CC}$ = 5.5 V | 1 | | 40 | μs |
| Fall time of the pulse applied to the CE from 90% to 10% | t$_{THL}$ | | 50 | | 1000 | ns |
| Required time delay between disabling memory output and application of output programming pulse | t$_{D1}$ | Measured at 1.5 V levels | 70 | 80 | 90 | μs |
| Required time delay between removal of programming pulse and enabling memory output | t$_{D2}$ | Measured at 1.5 V levels | 100 | | | ns |
| V$_{CC}$ required during programming | V$_{CCP}$ | | 5.40 | 5.50 | 5.60 | V |
| Output current required during verification | I$_{OLV1}$ | T$_C$ = 25°C, V$_{CC}$ = 4.20 V chip enabled | 11 | 12 | 13 | mA |
| Output current required during verification | I$_{OLV2}$ | T$_C$ = 25°C, V$_{CC}$ = 6.0 V chip enabled | 0.19 | 0.2 | 0.21 | mA |
| Maximum duty cycle during automatic programming of enable and output pin | DC | T$_P$ / T$_C$ | | | 25 | % |
| Required programming voltage on the output pin | V$_{OUT}$ | | 20 | 20 | 26 | V |
| Required current limit of the power supply feeding the output during programming | I$_L$ | V$_{OUT}$ = 25 V, V$_{CC}$ = 5.5 0 V | 150 | | | mA |

1/  T$_C$ = +25°C.

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4.9  Programming procedure for circuit C.   The programming characteristics in table IVC and the following procedures shall apply for programming the device:

a.  Connect the device in the electrical configuration for programming.  The waveforms on figure 5C and the programming characteristics in table IVC shall apply for programming to these procedures.

b.  Terminate all device outputs with a 10 k$\Omega$ resistor to $V_{CC}$.

c.  Address the PROM with the binary address of the selected word to be programmed.  Raise $V_{CC}$ to $V_{CCP}$.

d.  After a $t_D$ delay (10 $\mu$s), apply only one $V_{OUT}$ pulse to the output to be programmed.
Program one output at a time.

e.  After a $t_D$ delay (10 $\mu$s), pulse $\overline{CE}$ input to logic "0" for a duration of $t_P$.

f.  After a $t_D$ delay (10 $\mu$s), remove the $V_{OUT}$ pulse from the programmed output.  Note that the PROM is supplied with fuses generating a low-level logic output.  Programming a fuse will cause the output to go to a high-level logic in the verify mode.

g.  Other bits in the same word may be programmed sequentially while the $V_{CC}$ input is at the $V_{CCP}$ level by applying $V_{OUT}$ pulses to each output to be programmed allowing a delay of $t_D$ between pulses as shown on figure 5C.

h.  Repeat 4.9b through 4.9g for all other bits to be programmed.

i.  To verify programming after $t_D$ (10 $\mu$s) delay, lower $V_{CC}$ to $V_{CCH}$ and apply a logic "0" level to both $\overline{CE}$ input.  The programmed output should remain in the "1" state.  Again lower $V_{CC}$ and $V_{CCL}$ and verify that the programmed output remains in the "1" state.

j.  For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVC.  <u>Programming characteristics for circuit C</u>.

| Parameter | Symbol | Conditions | Limits 1/ | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Recommended | Max | |
| Programming voltage to $V_{CC}$ | $V_{CCP}$ 1/ | $I_{CCP} = 375 \pm 75$ mA; transient or steady-state | 9.5 | 10.0 | 10.5 | V |
| Verification upper limit | $V_{CCH}$ | | 5.3 | 5.5 | 5.7 | V |
| Verification lower limit | $V_{CCL}$ | | 4.3 | 4.5 | 4.7 | V |
| Verify threshold | $V_S$ 2/ | | 0.9 | 1.0 | 1.1 | V |
| Programming supply current | $I_{CCP}$ | $V_{CCP} = +8.75 \pm 0.25$ V | 200 | 250 | 300 | mA |
| Input voltage high level "1" | $V_{IH}$ | | 2.4 | | 5.5 | V |
| Input voltage low level "0" | $V_{IL}$ | | 0 | 0.4 | 0.8 | V |
| Input current | $I_{IH}$ | $V_{IH} = +5.5$ V | | | 50 | $\mu$A |
| Input current | $I_{IL}$ | $V_{IL} = +0.4$ V | | | -500 | $\mu$A |
| Output programming voltage | $V_{OUT}$ 3/ | $I_{OUT} = 65 \pm 3$ mA, transient or steady-state | 15.0 | 15.5 | 16.0 | V |
| Output programming current | $I_{OUT}$ | $V_{OUT} = +17 \pm 1$ V | 62 | 65 | 68 | mA |
| Programming voltage transition time | $t_{TLH}$ | | 10 | | 50 | $\mu$s |
| $\overline{CE}$ programming pulse width | $t_P$ | | 300 | 400 | 500 | $\mu$s |
| Pulse sequence delay | $t_D$ | | 10 | | | $\mu$s |
| Programming duty cycle | $t_{PR}$ / $t_{PR} + t_{PS}$ | | | | 50 | % |

1/  Bypass $V_{CC}$ to GND with a 0.01 $\mu$F capacitor to reduce voltage spikes.

2/  $V_S$ is the sensing threshold of the PROM output voltage for a programmed bit.  It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

3/  Care should be taken to insure the 17 $\pm$1 V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

4.10   <u>Programming procedure for circuit G</u>.  The programming characteristics on table IVG and the following procedures shall be used for programming.

    a.  Connect the device in the electrical configuration of programming.  The waveforms on figure 5D and the programming characteristics of table IVG shall apply to these procedures.

    b.  Select the desired word by applying high or low levels to the appropriate address inputs.  Disable the device by applying a high level to one or more active low chip enable inputs.  NOTE:  Address and enable inputs must be driven with TTL logic levels during programming and verification.

    c.  Increase $V_{CC}$ from nominal to $V_{CCP}$ (10.5 $\pm$0.5 V) with a slew rate limit of $I_{RR}$ (1.0 to 10.0 V/$\mu$s).  Since $V_{CC}$ is the source of the current required to program the fuse, as well as the $I_{CC}$ for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0 volts.

    d.  Select the output where a logical high is desired by raising that output voltage to $V_{OP}$ (10.5 $\pm$0.5 V).  Limit the slew rate to $I_{RR}$ (1.0 to 10.0 V/$\mu$s).  This voltage change may occur simultaneously with the $V_{CC}$ increase to $V_{CCP}$, but must precede it.  It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time.  Outputs not being programmed must be left open or connected to a high impedance source of 20 k$\Omega$ minimum (remember that the outputs of the device are disabled at this time).

    e.  Enable the device by taking the chip enable(s) to a low level.  This is done with a pulse PWE for 10 $\mu$s.  The 10 $\mu$s duration refers to the time that the circuit (device) is enabled.  Normal input levels are used and rise and fall times are not critical.

    f.  Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing $V_{CC}$ to 5.0 V ($\pm$0.25 V).  The device must be enabled to sense the state of the outputs.  During verification, the loading of the output must be within specified $I_{OL}$ and $I_{OH}$ limits.

    g.  If the device is not to be tested for $V_{OH}$ over the entire operating range subsequent to programming, the verification of step f is to be performed at a $V_{CC}$ level of 4.0 volt ( $\pm$0.2 V ).  $V_{OH}$, during the 4 volt verification, must be at least 2.0 volts.  The 4 volt $V_{CC}$ verification assures minimum $V_{OH}$ levels over the entire operating range.

    h.  Repeat steps 4.10b through 4.10f for each bit to be programmed to a high level.  If the procedure is performed on an automatic programmer, the duty cycle of $V_{CC}$ at the programming voltage must be limited to a maximum of 25%.  This is necessary to minimize device junction temperatures.  After all selected bits are programmed, the entire contents of the memory should be verified.

    i.  For class S and B devices, if any bit does not verify as programmed it shall be considered a programming reject.

TABLE IVG.  Programming characteristics for circuit G.

| Parameter | Symbol | Conditions | Limits 1/ | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Recommended | Max | |
| Required $V_{CC}$ for programming | $V_{CCP}$ | | 10.0 | 10.5 | 11.0 | V |
| $I_{CC}$ during programming | $I_{CCP}$ | $V_{CC}$ = 11 V | | | 750 | mA |
| Required output voltage for programming | $V_{OP}$ | | 10.0 | 10.5 | 11.0 | V |
| Output current while programming | $I_{OP}$ | $V_{OUT}$ = 11 V | | | 20 | mA |
| Rate of voltage change of $V_{CC}$ or output | $I_{RR}$ | | 1.0 | | 10.0 | V/$\mu$s |
| Programming pulse width (enabled) | $P_{WE}$ | | 9 | 10 | 11 | $\mu$s |
| Required $V_{CC}$ for verification | $V_{CCV}$ | | 3.8 | 4.0 | 4.2 | V |
| Maximum duty cycle for $V_{CC}$ at $V_{CCP}$ | MDC | | | 25 | 25 | % |
| Address set-up time | $t_1$ | | 100 | | | ns |
| $V_{CCP}$ set-up time | $t_2$ | 2/ | 5 | | | $\mu$s |
| $V_{CCP}$ hold time | $t_5$ | | 100 | | | ns |
| $V_{OP}$ set-up time | $t_3$ | | 100 | | | ns |
| $V_{OP}$ hold time | $t_4$ | | 100 | | | ns |

1/  $T_C$ = +25°C.

2/  $V_{CCP}$ set-up time may be greater than 0 if $V_{CCP}$ rises at the same rate or faster than $V_{OP}$.

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4.11 <u>Programming procedure for circuit H.</u>   The programming characteristics in table IVH and the following procedures shall apply for programming the device:

   a. Connect the device in the electrical configuration for programming.  The waveforms on figure 5E and the programming characteristics in table IVH shall apply for programming to these procedures.

   b. Terminate all device outputs with a 10 k$\Omega$ resistor to $V_{CC}$.  The 10 k$\Omega$ is the pullup resistor for open collector devices.

   c. Address the PROM with the binary address of the selected word to be programmed.  Raise $V_{CC}$ to $V_{CCP}$.

   d. After a $t_D$ delay (10 $\mu$s), apply $V_{OPF}$ output to be programmed.  Program one output at a time. Note leading edge rise time restrictions.

   e. After a $t_D$ delay (10 $\mu$s), pulse $\overline{CE}$ input to logic "0" for a duration of $t_P$.

   f. After a $t_D$ delay (10 $\mu$s), remove the $V_{OPF}$ pulse from the programmed output.  Note that the PROM is supplied with fuses generating a low-level logic output.  Programming a fuse will cause the output to go to a high-level logic in the verify mode.

   g. Repeat 4.11d through 4.11f to program other bits at the same address.

   h. To verify programming of all bits at the same address, after $t_D$ delay lower $V_{CC}$ to $V_{CCVL}$ and apply a logic low level to the $\overline{CE}_X$ input.  All programmed outputs should remain in the same logic high state.

   i. After $t_D$ delay, repeat steps 4.11c through 4.11h to program and verify all other address locations.

   j. After $t_D$ delay, raise $V_{CC}$ to $V_{CCVH}$ and verify all memory locations by applying a logic low level to $\overline{CE}$ and cycling through all device addresses.

   k. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVH.  Programming characteristics for circuit H.

| Parameter | Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Recommended | Max | |
| Programming voltage to $V_{CC}$ | $V_{CCP}$ 1/ | $I_{CCP}$ = 425 ±75 mA; transient or steady-state | 8.5 | 8.75 | 9.0 | V |
| Verification upper limit | $V_{CCVH}$ | | 5.3 | 5.5 | 5.7 | V |
| Verification normal limit | $V_{CCVN}$ | | 4.75 | 5.0 | 5.25 | V |
| Verification lower limit | $V_{CCVL}$ | | 4.3 | 4.5 | 4.7 | V |
| Verify threshold | $V_S$ 2/ | | 1.4 | 1.5 | 1.6 | V |
| Programming supply current | $I_{CCP}$ | $V_{CCP}$ = +8.75 ±0.25 V | 350 | | 500 | mA |
| Input voltage high level "1" | $V_{IH}$ | | 2.4 | | 5.5 | V |
| Input voltage low level "0" | $V_{IL}$ | | 0 | | 0.8 | V |
| Input current | $I_{IH}$ | $V_{IH}$ = +5.5 V | | | 50 | μA |
| Input current | $I_{IL}$ | $V_{IL}$ = +0.4 V | | | -500 | μA |
| Forced output voltage (program) | $V_{OPF}$ 3/ | $I_{OUT}$ = 200 ±20 mA, transient or steady-state | 17 | 17.5 | 18.0 | V |
| Forced output current (program) | $I_{OPF}$ | $V_{OPF}$ = +17 ±1 V | 180 | | 220 | mA |
| Output pulse rise time | $t_{RZ}$ | | 17 | 20 | 25 | μs |
| $\overline{CE}$ programming pulse width | $t_P$ | | 10 | 10 | 25 | μs |
| Pulse sequence delay | $t_D$ | | 5 | 10 | | μs |
| Address program verify cycle | $t_{PVA}$ | | | | 1 | ms |
| Memory program verify time (continuous) | $t_{PVM}$ | | | | 20 | sec |
| Fusing attempts per link | $F_L$ | | | | 1 | cycle |

1/  Bypass $V_{CC}$ to GND with a 0.01 μF capacitor to reduce voltage spikes.

2/  $V_S$ is the sensing threshold of the PROM output voltage for a programmed bit.  It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

3/  The voltage should be maintained within specified limits during the entire fusing cycle.  For a transient current of 150 mA, limit voltage spikes to a maximum slew rate of 2 V/μs and 10 μs maximum recovery.

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5. PACKAGING

5.1 <u>Packaging requirements.</u>  For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2).  When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements.  Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command.  Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6.   NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)

6.1  <u>Intended use.</u>  Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2  <u>Acquisition requirements.</u>  Acquisition documents should specify the following:

    a.    Title, number, and date of the specification.

    b.    PIN and compliance identifier, if applicable  (see 1.2).

    c.    Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

    d.    Requirements for certificate of compliance, if applicable.

    e.    Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.

    f.    Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

    g.    Requirements for product assurance options.

    h.    Requirements for special lead lengths, or lead forming, if applicable.  Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

    i.    Requirement for programming the device, including processing option.

    j.    Requirements for "JAN" marking.

    k.    Packaging Requirements (see 5.1)

6.3  <u>Qualification.</u>  With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date.  The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification.  Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43218-3990.

6.4 <u>Superseding information</u>. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 <u>Abbreviations, symbols, and definitions.</u> The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

GND ............................................. Electrical ground (common terminal).
$I_{IN}$ ................................................ Current flowing into an input terminal.
$V_{IC}$ .............................................. Input clamp voltage.
$V_{IN}$ .............................................. Voltage level at an input terminal.

6.6 <u>Logistic support.</u> Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.8.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.7 <u>Substitutability.</u> The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

| Military device type | Generic-industry type | Circuit designator | Fusible links |
|---|---|---|---|
| 01  1/ | 7602 / Harris Semiconductor, CAGE 34371 | A | NiCr |
| 01  1/ | 5330 / Monolithic Memories, CAGE 56364 | B | NiCr |
| 02 | DM54S288 / National Semiconductor, CAGE 27014 | G | TiW / W |
| 02  1/ | 7603 / Harris Semiconductor, CAGE 34371 | A | NiCr |
| 02  1/ | 5331 / Monolithic Memories, CAGE 56364 | B | NiCr |
| 01, 03 | 82S23A / Signetics Corporation, CAGE 18324 | C | NiCr |
| 02, 04 | 82S123A / Signetics Corporation, CAGE 18324 | C | NiCr |
| 01, 03 | 82S23A / Signetics Corporation, CAGE 18324 | H  2/ | NiCr |
| 01, 03 | 82S23A/QP Semiconductor | H  2/ | ZVE |
| 02, 04 | 82S123A / Signetics Corporation, CAGE 18324 | H  2/ | NiCr |
| 02, 04 | 82S123A/QP Semiconductor | H  2/ | ZVE |

1/   This generic industry type is no longer manufactured.
2/   Updated circuit C to circuit H to reflect the current programming method.
     Contact the manufacturer for the correct programming method being used.

6.8 <u>Change from previous issue.</u>  Marginal notations are used in this revision to identify changes with respect to the previous issue.

Custodians:                                                                 Preparing activity:
   Army - CR                                                      DLA - CC
   Navy - EC
   Air Force - 11
   DLA - CC

Review activities:                                                          (Project 5962-2007-008)
   Army – SM, MI
   Navy - AS, CG, MC, SH TD
   Air Force – 03, 19, 99

NOTE:   The activities listed above were interested in this document as of the date of this document.  Since organization and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.