MIL-M-38510/9E
8 February 2005
SUPERSEDING
MIL-M-38510/9D
4 June 1980
MIL-M-0038510/9B
15 October 1973

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR TTL, SHIFT REGISTERS, MONOLITHIC SILICON

Inactive for new design after 7 September 1995.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, shift register microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535 and as specified herein.

1.2.1 Device types. The device types are as follows:

Device type	Circuit
01	4 bit right shift, left shift register
02	5 bit shift register
03	8 bit parallel out serial shift register
04	8 bit parallel load shift register
05	4 bit bidirectional shift register
06	4 bit parallel access shift register

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
A	GDFP5-F14 or CDFP6-F14	14	Flat pack
B	GDFP4-14	14	Flat pack
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat-pack

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to bipolar@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

AMSC N/A FSC 5962

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -12 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation per register, P_D 1/	
Device type 01	422 mW dc
Device type 02	400 mW dc
Device type 03	322 mW dc
Device type 04	372 mW dc
Device type 05	360 mW dc
Device type 06	372 mW dc
Lead temperature (soldering 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC})	(See MIL-STD-1835)
Junction temperature (T_J) 2/	175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage	2.0 V dc
Maximum low level input voltage	0.8 V dc
Case operating temperature range (T_C)	-55°C to 125°C
Fan out	
Device types 01, 02, 04, 05, and 06	
High logic level	20
Low logic level	10
Device type 03	
High logic level	10
Low logic level	5
Device type 01	
Low level setup time at mode control with respect to clock 1 input	35 ns minimum
High level setup time at mode control with respect to clock 2 input	35 ns minimum
Low level setup time at mode control with respect to clock 2 input	10 ns minimum
High level setup time at mode control with respect to clock 1 input	10 ns minimum
Width of clock pulse	20 ns minimum
Setup time required at serial A, B, C, D inputs	20 ns minimum
Hold time required at serial A, B, C, D inputs	5 ns minimum
Device type 02	
Minimum clock pulse width	35 ns maximum
Minimum clear pulse width	30 ns maximum
Minimum preset pulse width	30 ns maximum
Serial input setup time	30 ns minimum
Serial input hold time	0 ns minimum
Device type 03	
Minimum clock pulse width	30 ns maximum
Minimum clear pulse width	50 ns maximum
Serial setup time	15 ns minimum
Serial hold time	10 ns maximum

1/ Must withstand the added P_D due to short circuit condition (e.g. I_{OS}) at one output for 5 seconds duration.

2/ Maximum junction temperature should not be exceeded except in accordance with allowable short duration burn-in screening condition in accordance with MIL-PRF-38535.

Device type 04

Width of clock input pulse	20 ns minimum
Width of load input pulse	25 ns minimum
Clock enable setup time	30 ns minimum
Parallel input setup time	10 ns minimum
Serial input setup time	35 ns minimum
Shift setup time	45 ns minimum
Hold time at serial input	0 ns maximum
Hold time at parallel input	25 ns maximum

Device type 05

Width of clock input pulse	20 ns minimum
Width of clear input pulse	20 ns minimum
Data input setup time	20 ns minimum
Clear input setup time	25 ns minimum
Hold time at any input	7 ns minimum
Mode control setup time	30 ns minimum

Device type 06

Width of clock input pulse	16 ns minimum
Width of clear input pulse	12 ns minimum
Shift load input setup time	32 ns minimum
Data input setup time	25 ns minimum
Clear input setup time	25 ns minimum
Shift load release time	10 ns maximum
Data hold time	0 ns minimum

2.0 APPLICABLE DOCUMENT

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Truth tables and timing diagrams. The truth tables and timing diagrams shall be as specified on figure 2.

3.3.3 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.3.4 Schematic circuit. The schematic circuit shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.

3.3.5 Case outlines. Case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. Lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table 1 and apply over the full recommended case operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 5 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C unless otherwise specified	Device type	Limits		
				Min	Max	Unit
High-level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IN} = 2.0 V, I_{OH} = -400 µA	02, 03	2.4		V
		V_{CC} = 4.5 V, V_{IN} = 2.0 V, I_{OH} = -800 µA	01, 04 05, 06	2.4		V
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 16 mA, V_{IN} = 0.8 V	01, 02, 04 05, 06		0.4	V
		V_{CC} = 4.5 V, V_{IN} = 0.8 V, I_{OL} = 8 mA	03		0.4	V
High level input voltage	V_{IH}	V_{CC} = 4.5 V	All	2.0		V
Low level input voltage	V_{IL}	V_{CC} = 4.5 V	All		0.8	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -12 mA, T_C = 25° C	All		-1.5	V
High level input current at any input except mode control	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	01		40	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	01		100	µA
High level input current at mode control	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	01		80	µA
	I_{IH4}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	01		200	µA
High level input current at any input except preset	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	02		40	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	02		100	µA
High level input current at preset	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	02		200	µA
	I_{IH4}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	02		500	µA
High level input current at any input except clear	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	03		40	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	03		100	µA
High level input current at clear	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	03		80	µA
	I_{IH4}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	03		200	µA
High level input current other than load input	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	04		40	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	04		100	µA
High level input current load input	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	04		120	µA
	I_{IH4}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	04		300	µA
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	05, 06		40	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	05, 06		100	µA
Low level input current at any input except mode control	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	01	-0.4	-1.6	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$ unless otherwise specified	Device type	Limits		
Low level input current at mode control	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	01	-0.8	-3.2	mA
Low level input current at any input except preset	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	02	-0.7	-1.6	mA
Low level input current at preset	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	02	-3.0	-8.0	mA
Low level input current at any input except clear	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	03	-0.4	-1.6	mA
Low level input current at clear	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	03	-0.7	-2.6	mA
Low level input current load input	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	04	-1.2	-3.9	mA
Low level input current other than clock and load input	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	04	-0.4	-1.3	mA
Low level input current clock input	I_{IL3}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	04	-0.4	-1.6	mA
Low level input current other than S0, S1 and clock input	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	05	-0.4	-1.3	mA
Low level input current S0 and S1 input	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	05	-0.4	-1.6	mA
Low level input current clock input	I_{IL3}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	05	-0.7	-1.6	mA
Low level input current at clear input	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	06	-0.4	-1.3	mA
Low level input current other than clear and clock inputs	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	06	-0.4	-1.6	mA
Low level input current at clock input	I_{IL3}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	06	-0.7	-1.6	mA
Short-circuit output current	I_{OS}	V_{CC} = 5.5 V 1/	01	-18	-57	mA
			02, 05, 06	-20	-57	
			03	-10	-27.5	
			04	-20	-55	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Device type	Limits		
Supply current	I_{CC}	V_{CC} = 5.5 V 2/	01		72	mA
			02		68	
			04, 05, 06		63	
Supply current	I_{CC1}	V_{CC} = 5.5 V, $V_{IN(CLOCK)}$ = 0.4 V 2/	03		44	mA
	I_{CC2}	V_{CC} = 5.5 V, $V_{IN(CLOCK)}$ = 2.4 V 2/	03		54	mA
Maximum shift frequency	f_{MAX}	V_{CC} = 5.0 V, C_L = 50 pF ±10% R_L = 400 Ω ±5% (See figure 4)	01	16		MHz
Propagation delay time, low to high level from clock 1 or clock 2 to outputs	t_{PLH}			10	42	ns
Propagation delay time, high to low level from clock 1 or clock 2 to outputs	t_{PHL}			10	49	ns
Maximum clock frequency	f_{MAX}	V_{CC} = 5.0 V, C_L = 50 pF ±10% R_L = 400 Ω ±5% (See figure 5)	02	7		MHz
Propagation delay time, low to high level from clock to output	t_{PLH1}			8	56	ns
Propagation delay time, high to low level from clock to output	t_{PHL1}			8	56	ns
Propagation delay time, low to high level from preset to output	t_{PLH2}			8	59	ns
Propagation delay time, high to low level from clear to output	t_{PHL3}			8	77	ns
Maximum clock frequency	f_{MAX}	V_{CC} = 5.0 V, C_L = 50 pF ±10% R_L = 800 Ω ±5% (See figure 6)	03	18		MHz
Propagation delay time, high to low level, clear input to Q outputs	t_{PHL1}			12	63	ns
Propagation delay time, high to low level, clock input to Q outputs	t_{PHL2}			10	52	ns
Propagation delay time, low to high level, clock input to Q outputs	t_{PLH2}			10	42	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Device type	Limits		
Maximum clock frequency	f_{MAX}	V_{CC} = 5.0 V, C_L = 50 pF ±10% R_L = 400 Ω ±5% (See figure 7)	04	14		MHz
Propagation delay time, low to high level, load input to any output	t_{PLH1}			10	40	ns
Propagation delay time, high to low level, load input to any output	t_{PHL1}			11	60	ns
Propagation delay time, low to high level, clock input to any output	t_{PLH2}			6	37	ns
Propagation delay time, high to low level, clock input to any output	t_{PHL2}			10	47	ns
Propagation delay time, low to high level, H input to Q_H output	t_{PLH3}			5	27	ns
Propagation delay time, high to low level, H input to Q_H output	t_{PHL3}			11	54	ns
Propagation delay time, low to high level, H input to $\overline{Q}_H$ output	t_{PLH4}			10	41	ns
Propagation delay time, high to low level, H input to $\overline{Q}_H$ output	t_{PHL4}			10	41	ns
Maximum clock frequency	f_{MAX}	V_{CC} = 5.0 V, C_L = 50 pF ±10% R_L = 400 Ω ±5% (See figure 8)	05	18		MHz
Propagation delay time, high to low level, output from clear	t_{PHL1}			7	48	ns
Propagation delay time, low to high level output from clock	t_{PLH2}			7	36	ns
Propagation delay time, high to low level output from clock	t_{PHL2}			7	44	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Device type	Limits		
Maximum clock frequency	f_{MAX}	V_{CC} = 5.0 V, C_L = 50 pF ±10% R_L = 400 Ω ±5% (See figure 9)	06	24		MHz
Propagation delay time, high to low level output from clear	t_{PHL1}			7	34	ns
Propagation delay time, high to low level output from clock	t_{PLH2}			7	28	ns
Propagation delay time, low to high level output from clock	t_{PHL2}			7	34	ns

1/ Not more than one output should be shorted at a time.
2/ Device type:

01 - With the outputs open, mode control at 4.5 V, clock pulse applied to both clock inputs, I_{CC} is measured immediately after the application of the clock pulse.
02 - With the outputs open, presets at 4.5 V, I_{CC} is measured with the clock at ground and again with the clock at 4.5 V.
03 - I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V applied to clear.
04 - With the outputs open, serial at ground, clock, clock inhibit, and parallel inputs at 4.5 V, I_{CC} is measured by applying momentary ground, then 4.5 V to shift load prior to measurement.
05 - With all outputs open, inputs A thru D grounded, 5.5. V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested by applying clock pulse.
06 - With the outputs open, clear at 5.5 V, shift load, J, $\overline{K}$, and data inputs grounded, I_{CC} is measured by applying clock pulse.

TABLE II. Electrical test requirements.

MIL-PRF-38535 Test requirement	Subgroups (see table III)	
	Class S Devices	Class B Devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 7, 9, 10, 11	1*, 2, 3, 7, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8 9, 10, 11
Group B electrical test parameters when using the method 5005 QCI option	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3 7, 9
Group C end point electrical parameters	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3
Group D end point electrical parameters	1, 2, 3	1, 2, 3

*PDA applies to subgroup 1 (see 4.3c.).

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.4 Technology Conformance Inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5 and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End point electrical parameters shall be as specified in table II herein.

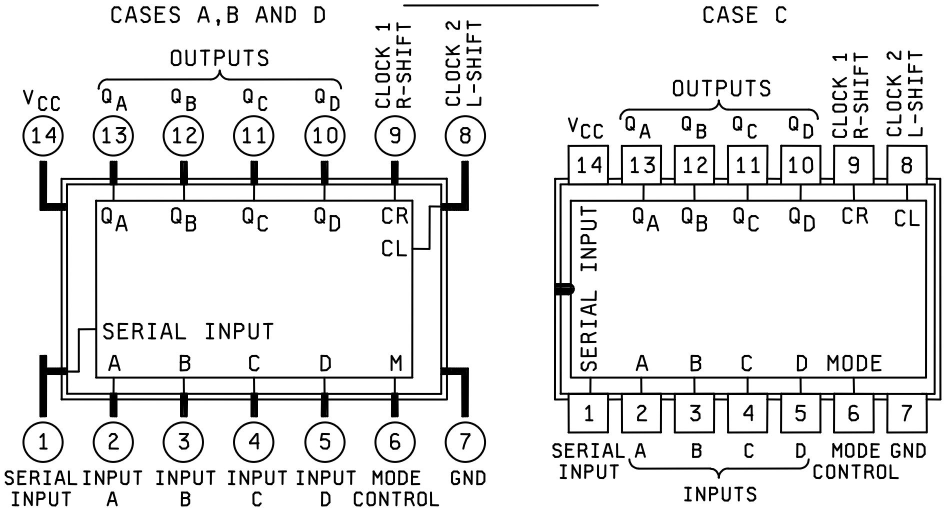
b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

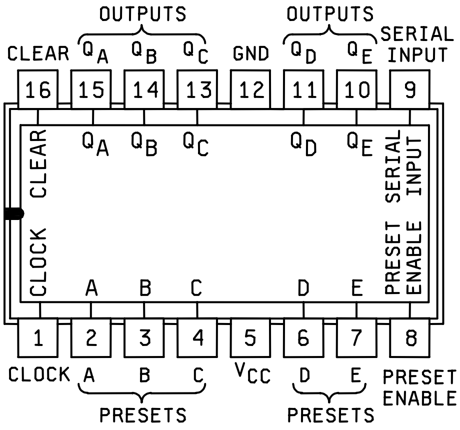
4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

DEVICE TYPE 01


CASES A,B AND D
OUTPUTS
VCC
QA
QB
QC
QD
CLOCK 1 R-SHIFT
CLOCK 2 L-SHIFT
14
13
12
11
10
9
8
CR
CL
SERIAL INPUT
A
B
C
D
M
1
2
3
4
5
6
7
SERIAL INPUT
INPUT A
INPUT B
INPUT C
INPUT D
MODE CONTROL
GND
CASE C
SERIAL INPUT
MODE
INPUTS

DEVICE TYPE 02

CASES E AND F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QB
QC
GND
QD
QE
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15
14
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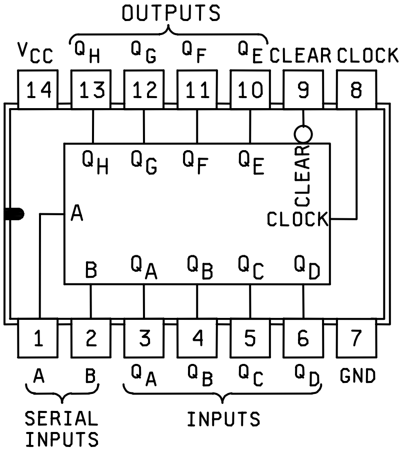
12
11
10
9
CLEAR
SERIAL INPUT
CLOCK
PRESET ENABLE
A
B
C
D
E
1
2
3
4
5
6
7
8
CLOCK
VCC
PRESET ENABLE
PRESETS
PRESETS

DEVICE TYPE 03

CASES A,B,C AND D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QG
QF
QE
CLEAR
CLOCK
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10
9
8
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B
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QB
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QD
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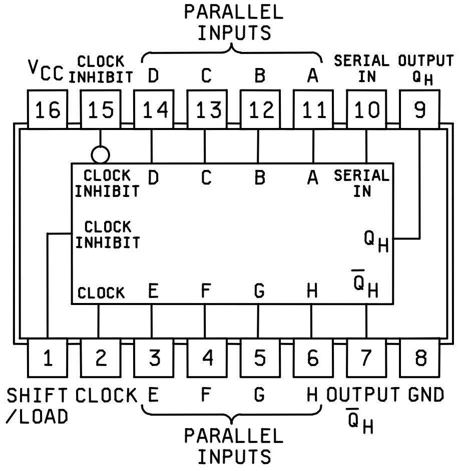
2
3
4
5
6
7
GND
SERIAL INPUTS
INPUTS

DEVICE TYPE 04

CASES E AND F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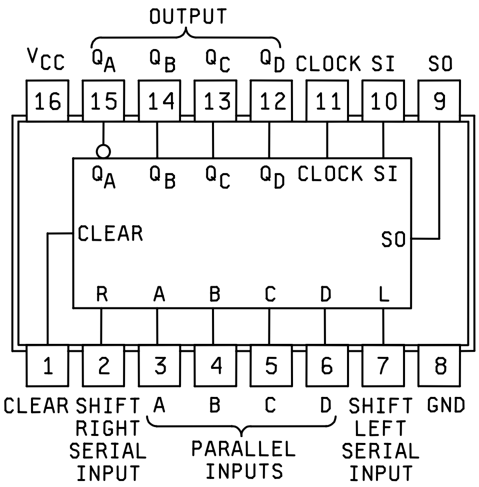
CLOCK INHIBIT
D
C
B
A
SERIAL IN
OUTPUT QH
16
15
14
13
12
11
10
9
CLOCK INHIBIT
SERIAL IN
QH
Q̄H
CLOCK
E
F
G
H
1
2
3
4
5
6
7
8
SHIFT /LOAD
CLOCK
OUTPUT Q̄H
GND
PARALLEL INPUTS

Figure 1. Terminal connections.

DEVICE TYPE 05
CASES E AND F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Q_A
Q_B
Q_C
Q_D
CLOCK
SI
SO
16
15
14
13
12
11
10
9
Q_A
Q_B
Q_C
Q_D
CLOCK
SI
CLEAR
SO
R
A
B
C
D
L
1
2
3
4
5
6
7
8
CLEAR
SHIFT RIGHT SERIAL INPUT
A
B
C
D
PARALLEL INPUTS
SHIFT LEFT SERIAL INPUT
GND

DEVICE TYPE 06
CASES E AND F

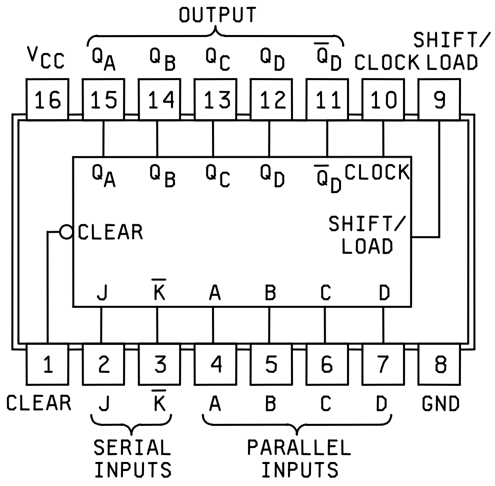

OUTPUT
V_{CC}
Q_A
Q_B
Q_C
Q_D
$\overline{Q}_D$
CLOCK
SHIFT/ LOAD
16
15
14
13
12
11
10
9
Q_A
Q_B
Q_C
Q_D
$\overline{Q}_D$
CLOCK
CLEAR
SHIFT/ LOAD
J
$\overline{K}$
A
B
C
D
1
2
3
4
5
6
7
8
CLEAR
J
$\overline{K}$
A
B
C
D
GND
SERIAL INPUTS
PARALLEL INPUTS

Figure 1. Terminal connections - Continued.

Device type 01

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS		SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D
	2 (L)	1(R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

† = Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
H = high level (steady state), L = low level (steady state), X = irrelevant (any input including transitions)
↓ = transition from high to low level, ↑ = transition from low to high level
a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C or Q_D respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C or Q_D respectively, before the most recent ↓ transition of the clock.

Device type 02

INPUTS									OUTPUTS				
CLEAR	PRESET ENABLE	PRESET					CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D	Q_E
		A	B	C	D	E							
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = high level (steady state), L = low level (steady state),
X = irrelevant (any input including transitions), ↑ = transition from low to high level
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, etc. = the level of Q_A, Q_B, etc. respectively, before the most recent ↑ transition of the clock.

Figure 2. Truth tables and timing diagrams.

Device type 03

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B…	.Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state),
X = irrelevant (any input including transitions),
↑ = transition from low to high level
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one bit shift.

Device type 04

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = high level (steady state), L = low level (steady state),
X = irrelevant (any input including transitions),
↑ = transition from low to high level
a . . . . h = the level of steady state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock.

Figure 2. Truth tables and timing diagrams – Continued.

Device type 05

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state), L = low level (steady state), X = irrelevant (any input including transitions)

↑ = transition from low to high level.

a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C or Q_D respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C or Q_D respectively, before the most recent ↑ transition of the clock.

Device type 06

INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{BO}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state), L = low level (steady state), X = irrelevant (any input including transitions)

↑ = transition from low to high level.

a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C or Q_D respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C or Q_D respectively, before the most recent ↑ transition of the clock.

Figure 2. Truth tables and timing diagrams – Continued.

Device type 01

Positive logic: Mode control = L for right shift.
Mode control = H for left shift or parallel load.

Transfer of information to the output pins occurs when the clock input goes from a logical H to a logical L.

Device type 02

Positive logic: Low input of clear sets all outputs to logical L.

Clear input is independent of clock.
Preset is independent of the clock or clear inputs

The flip-flops may be independently set to the logical H state by applying a logical H to both the preset input of the specific flip-flop and the common preset input.

Transfer of information to the output pins occurs when the clock input goes from a logical L to a logical H.

The clear input shall be a logical H and the preset input shall be at a logical L when clocking occurs.

The proper information shall appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform.

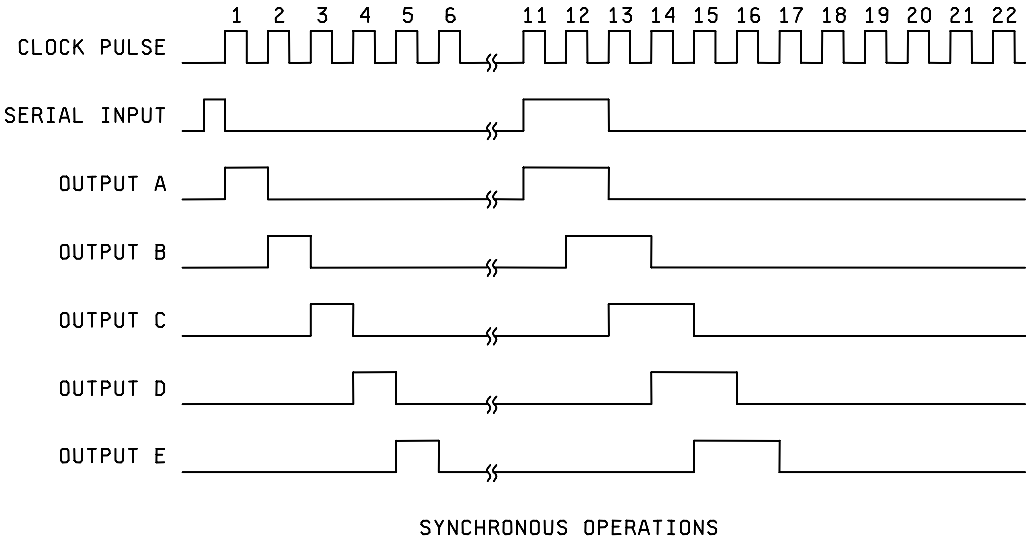
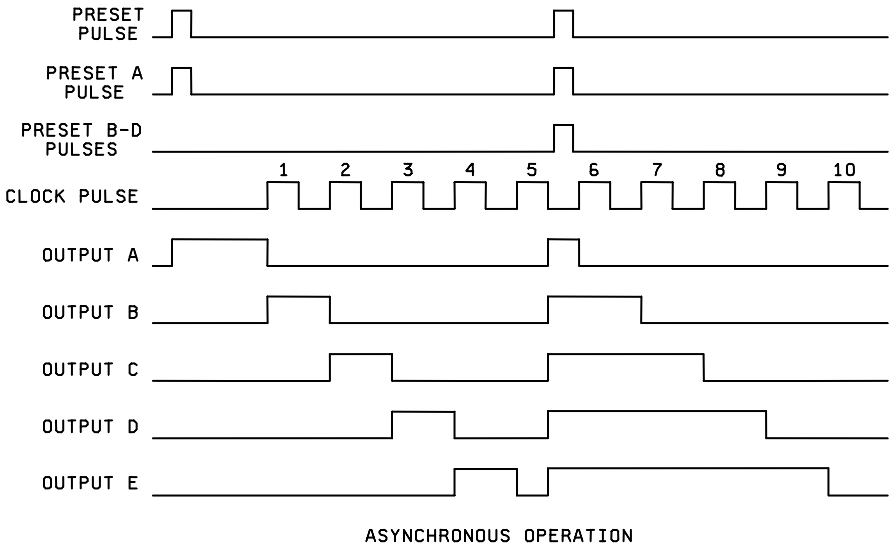

1
2
3
4
5
6
11
12
13
14
15
16
17
18
19
20
21
22
CLOCK PULSE
SERIAL INPUT
OUTPUT A
OUTPUT B
OUTPUT C
OUTPUT D
OUTPUT E
SYNCHRONOUS OPERATIONS

Figure 2. Truth tables and timing diagrams – Continued.


PRESET PULSE
PRESET A PULSE
PRESET B-D PULSES
CLOCK PULSE
1
2
3
4
5
6
7
8
9
10
OUTPUT A
OUTPUT B
OUTPUT C
OUTPUT D
OUTPUT E
ASYNCHRONOUS OPERATION

DEVICE TYPE 02
TYPICAL INPUT/OUTPUT VOLTAGE WAVEFORMS

NOTE: INPUTS NOT SHOWN ARE HELD AT LOGIC LEVEL "L".

Device type 03

SERIAL INPUTS A and B

INPUTS at t_n		OUTPUT at $t_n + 1$
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

Positive logic: t_n = bit time before clock pulse.

$t_n + 1$ = bit time after clock pulse.

Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low to high level transition of the clock input.

The clear input is asynchronous. Low level at clear input sets all outputs to logical low.

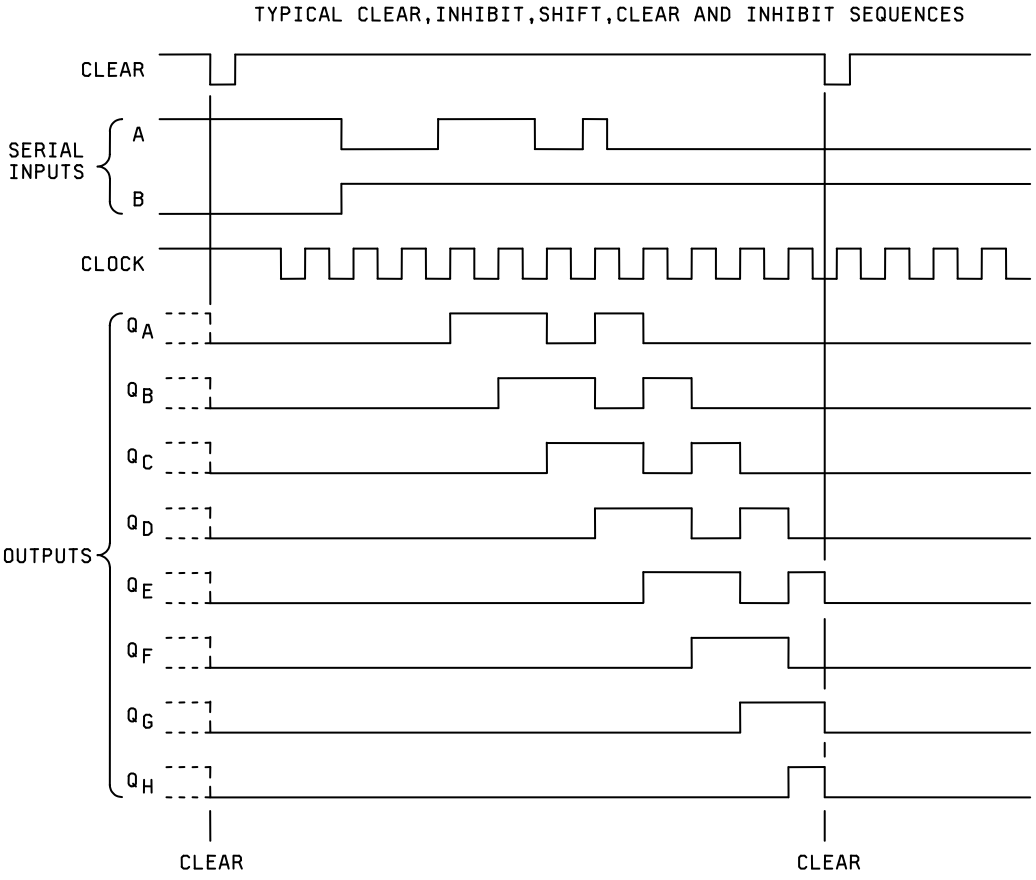

TYPICAL CLEAR,INHIBIT,SHIFT,CLEAR AND INHIBIT SEQUENCES
CLEAR
SERIAL INPUTS
A
B
CLOCK
OUTPUTS
Q_A
Q_B
Q_C
Q_D
Q_E
Q_F
Q_G
Q_H
CLEAR
CLEAR

Figure 2. Truth tables and timing diagrams – Continued.

Device type 04

Positive logic: Transfer of information to the output occurs when the clock input goes from a logical L to a logical H.

Clocking is accomplished through a 2 input positive NOR gate, permitting one input to be used as a clock inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock inhibit should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. When taken low, data at the parallel inputs are loaded directly into the register independently of the state of the clock.

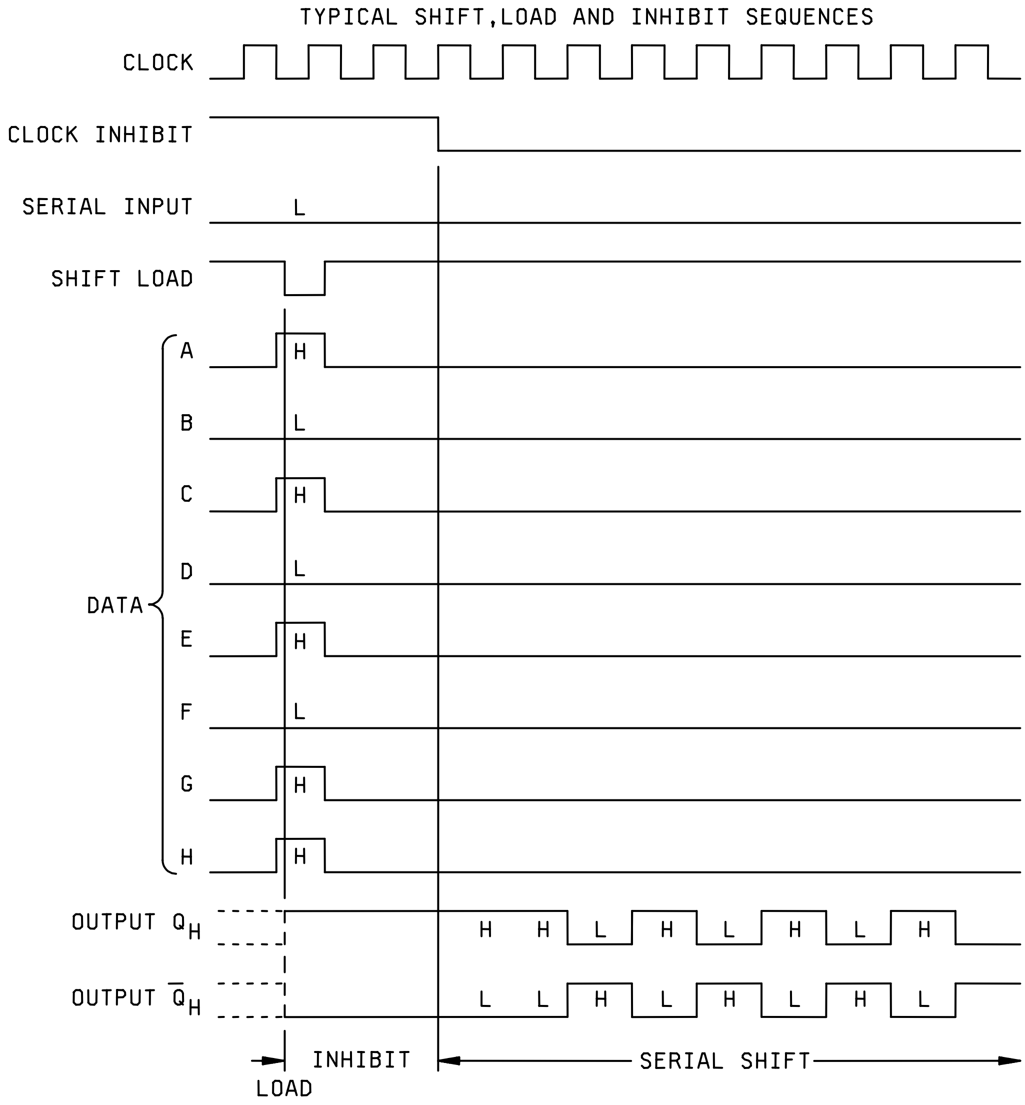

TYPICAL SHIFT,LOAD AND INHIBIT SEQUENCES
CLOCK
CLOCK INHIBIT
SERIAL INPUT
L
SHIFT LOAD
DATA
A
H
B
L
C
H
D
L
E
H
F
L
G
H
H
H
OUTPUT Q_H
H H L H L H L H
OUTPUT $\overline{Q}_H$
L L H L H L H L
INHIBIT
LOAD
SERIAL SHIFT

Figure 2. Truth tables and timing diagrams – Continued.

Device type 05

Positive logic: The register has four distinct modes of operation, namely:

	MODE CONTROL	
	S1	S0
Parallel (Broadside) Load	H	H
Shift Right (in the direction Q_A toward Q_D)	L	H
Shift Left (in the direction Q_D toward Q_A)	H	L
Inhibit Clock (do nothing)	L	L

In the parallel load mode, data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift right data input. When S0 is low S1 is high, data shifts left synchronously a new data is entered at the shift left serial input. Clocking of the flip-flops is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

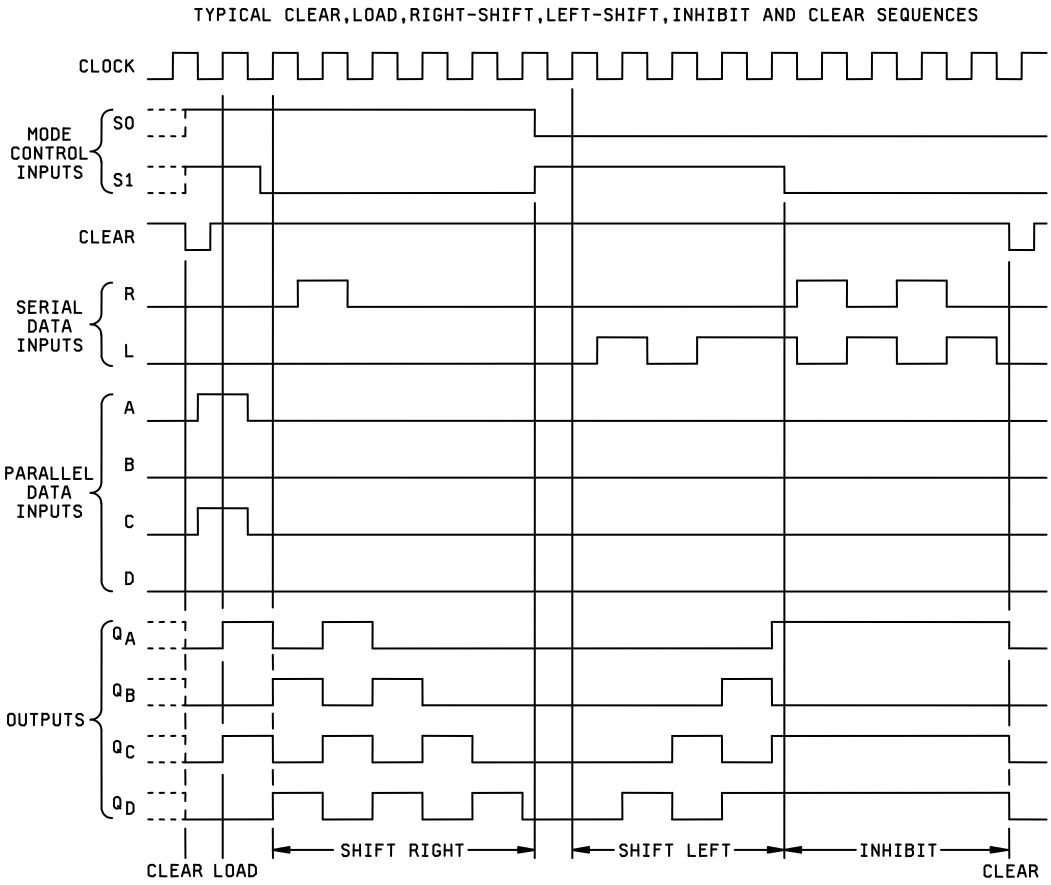

TYPICAL CLEAR,LOAD,RIGHT-SHIFT,LEFT-SHIFT,INHIBIT AND CLEAR SEQUENCES
CLOCK
MODE CONTROL INPUTS
S0
S1
CLEAR
SERIAL DATA INPUTS
R
L
PARALLEL DATA INPUTS
A
B
C
D
OUTPUTS
QA
QB
QC
QD
SHIFT RIGHT
SHIFT LEFT
INHIBIT
CLEAR
LOAD
CLEAR

Figure 2. Truth tables and timing diagrams – Continued.

Device type 06

Positive logic: The registers have two modes of operation:
Parallel (broadside) load
Shift (in direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J - $\overline{K}$ inputs. These inputs permit the first stage to perform as a J - $\overline{K}$, D-, or T-type flip-flop as shown in the truth table.

TRUTH TABLE

Inputs at t_n		Outputs at $t_n + 1$				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level, L = low level

NOTES:
1. t_n = bit time before clock pulse
2. $t_n + 1$ = bit time after clock pulse
3. Q_{An} = state of Q_{An} at t_n.

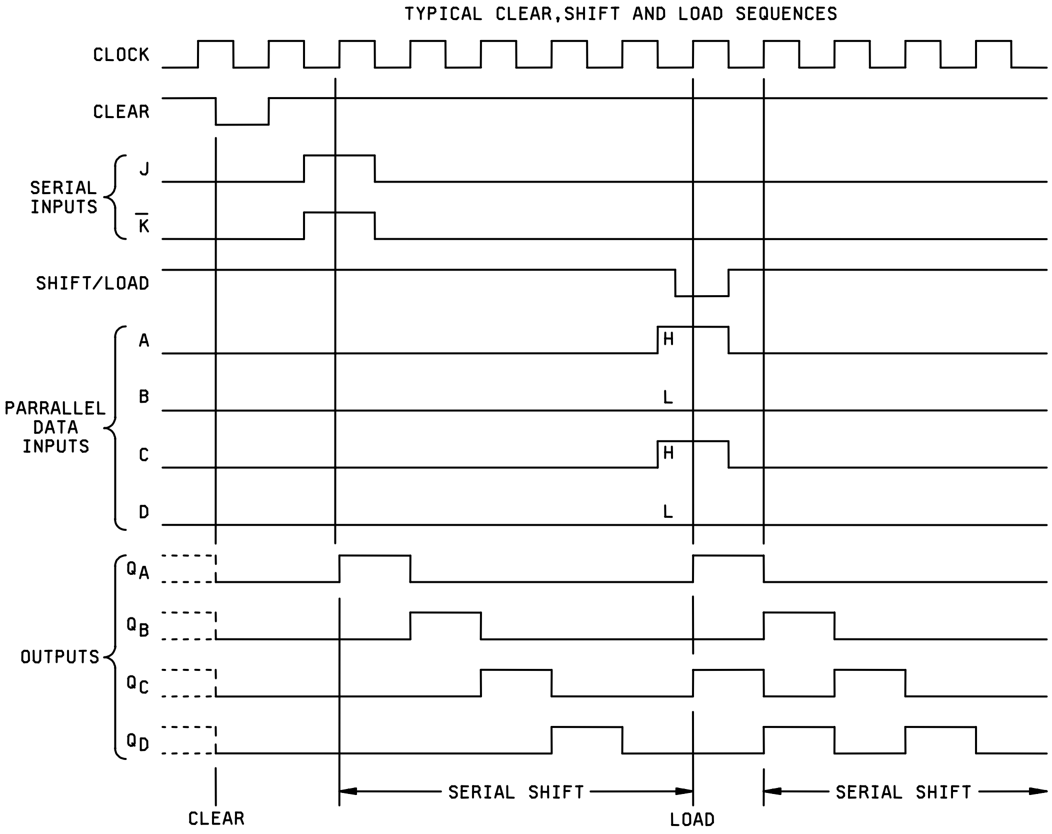

TYPICAL CLEAR,SHIFT AND LOAD SEQUENCES
CLOCK
CLEAR
SERIAL INPUTS
J
K̄
SHIFT/LOAD
PARRALLEL DATA INPUTS
A
B
C
D
H
L
H
L
OUTPUTS
QA
QB
QC
QD
SERIAL SHIFT
SERIAL SHIFT
CLEAR
LOAD

Figure 2. Truth tables and timing diagrams – Continued.

Device type 01

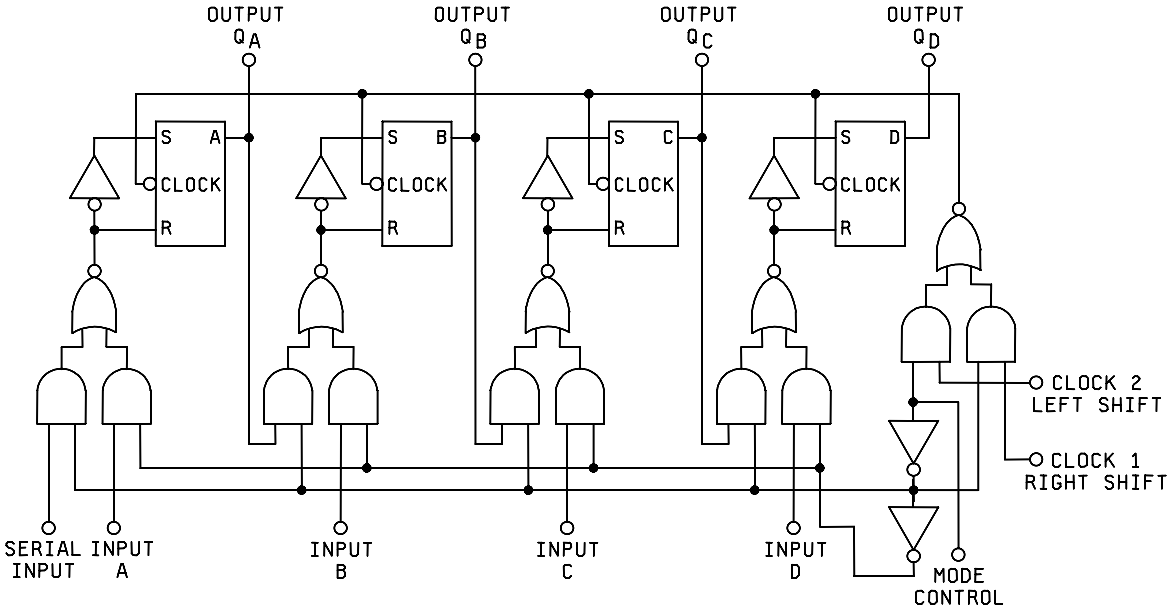
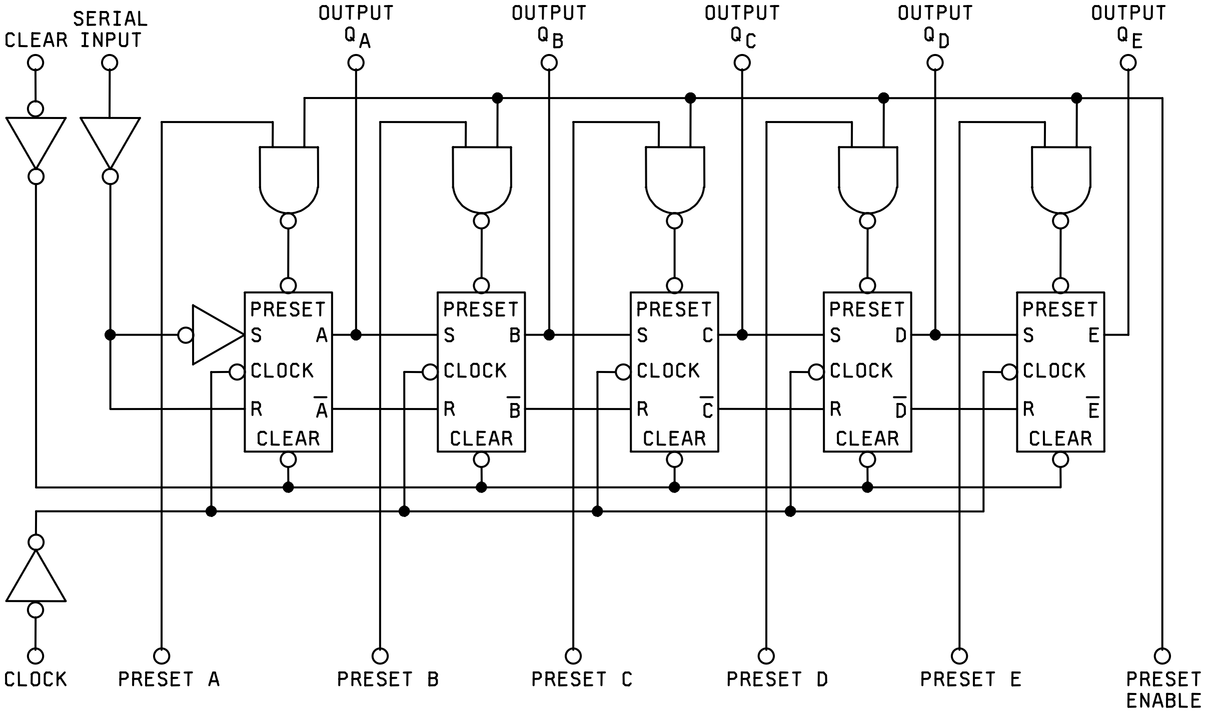

OUTPUT
Q_A
OUTPUT
Q_B
OUTPUT
Q_C
OUTPUT
Q_D
S
A
CLOCK
R
S
B
CLOCK
R
S
C
CLOCK
R
S
D
CLOCK
R
CLOCK 2
LEFT SHIFT
CLOCK 1
RIGHT SHIFT
SERIAL INPUT
INPUT A
INPUT B
INPUT C
INPUT D
MODE CONTROL

FIGURE 3. Logic diagrams.

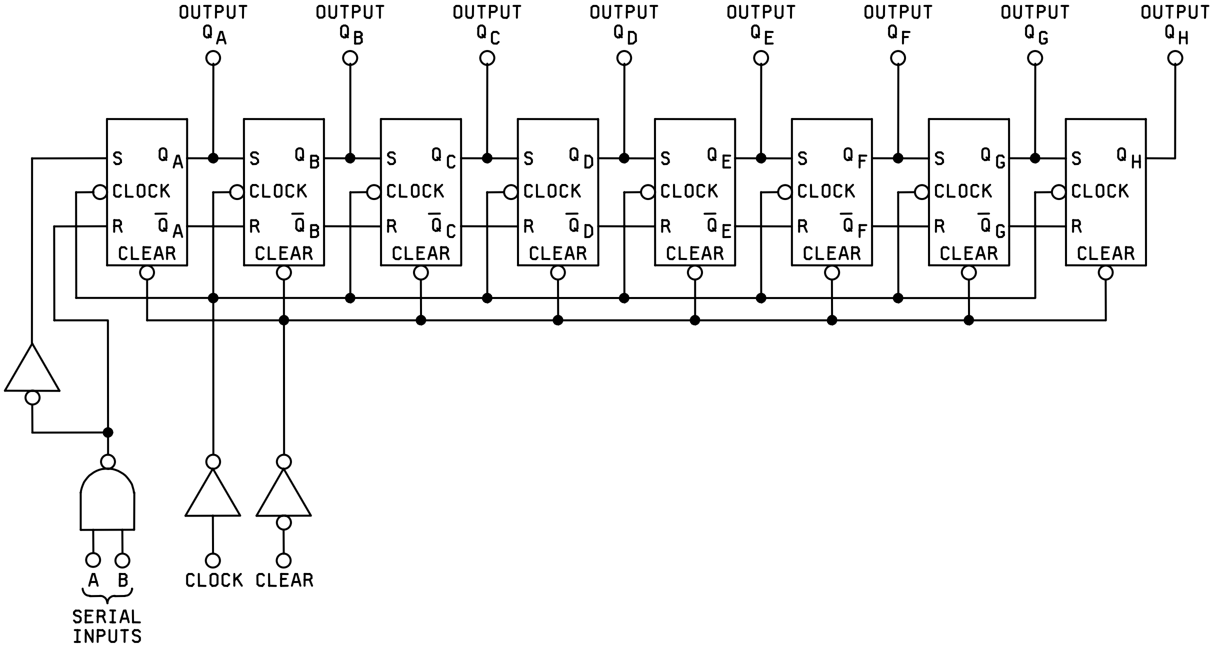
Device type 02



CLEAR
SERIAL INPUT
OUTPUT Q_A
OUTPUT Q_B
OUTPUT Q_C
OUTPUT Q_D
OUTPUT Q_E
PRESET
S
A
CLOCK
R
$\overline{A}$
CLEAR
B
$\overline{B}$
C
$\overline{C}$
D
$\overline{D}$
E
$\overline{E}$
CLOCK
PRESET A
PRESET B
PRESET C
PRESET D
PRESET E
PRESET ENABLE

FIGURE 3. Logic diagrams - Continued.

Device type 03


OUTPUT QA
OUTPUT QB
OUTPUT QC
OUTPUT QD
OUTPUT QE
OUTPUT QF
OUTPUT QG
OUTPUT QH
S QA CLOCK R Q̄A CLEAR
S QB CLOCK R Q̄B CLEAR
S QC CLOCK R Q̄C CLEAR
S QD CLOCK R Q̄D CLEAR
S QE CLOCK R Q̄E CLEAR
S QF CLOCK R Q̄F CLEAR
S QG CLOCK R Q̄G CLEAR
S QH CLOCK R CLEAR
A
B
SERIAL INPUTS
CLOCK
CLEAR

Device type 04

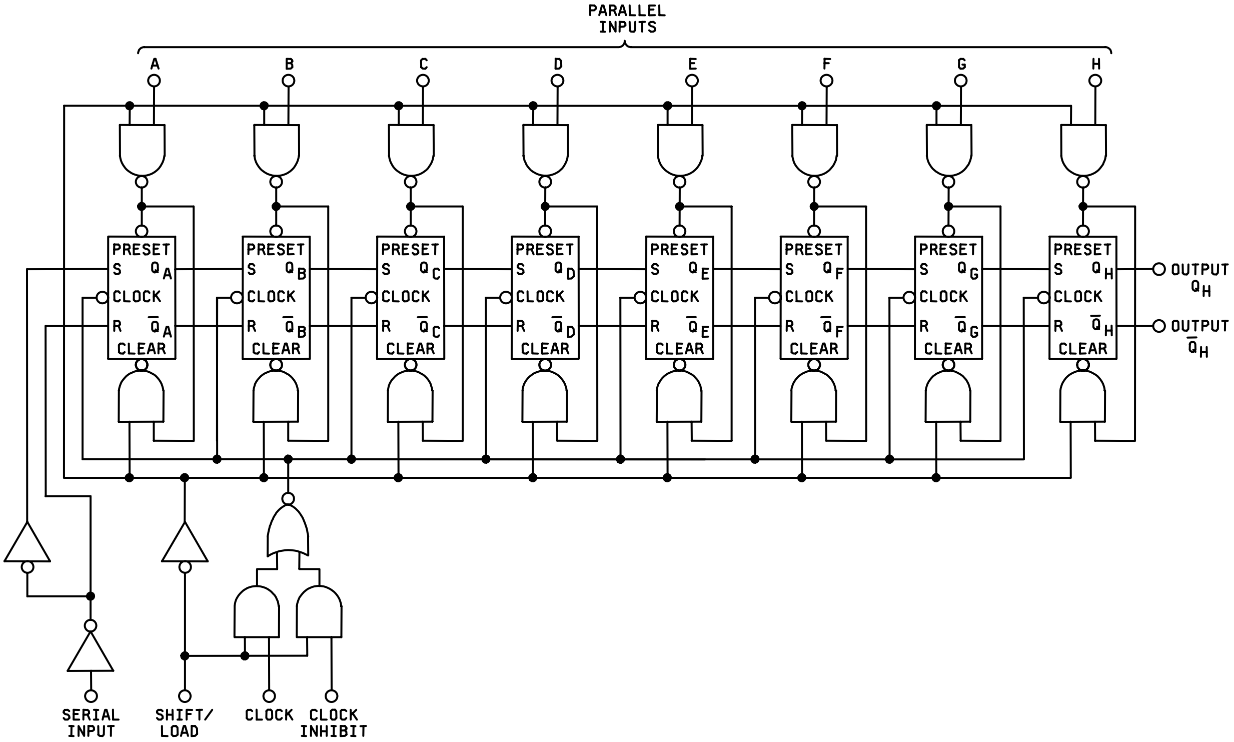

PARALLEL INPUTS
A
B
C
D
E
F
G
H
PRESET S QA CLOCK R Q̄A CLEAR
PRESET S QB CLOCK R Q̄B CLEAR
PRESET S QC CLOCK R Q̄C CLEAR
PRESET S QD CLOCK R Q̄D CLEAR
PRESET S QE CLOCK R Q̄E CLEAR
PRESET S QF CLOCK R Q̄F CLEAR
PRESET S QG CLOCK R Q̄G CLEAR
PRESET S QH CLOCK R Q̄H CLEAR
OUTPUT QH
OUTPUT Q̄H
SERIAL INPUT
SHIFT/ LOAD
CLOCK
CLOCK INHIBIT

FIGURE 3. Logic diagrams - Continued.

Device type 05

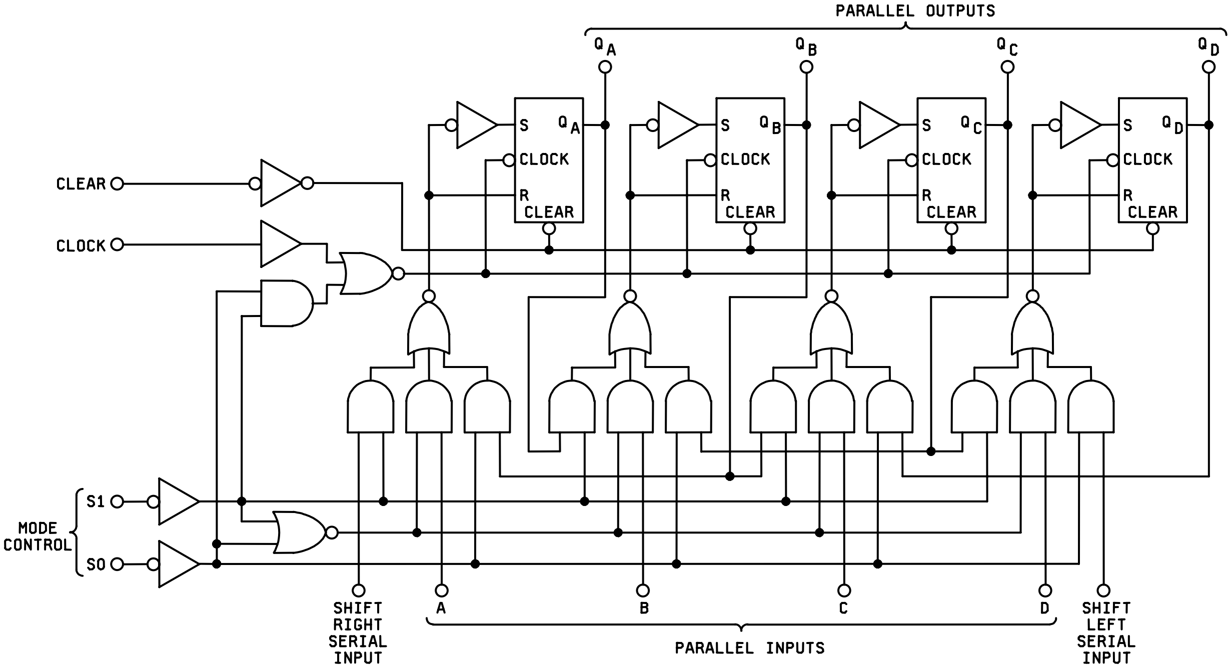

PARALLEL OUTPUTS
Q_A
Q_B
Q_C
Q_D
S
CLOCK
R
CLEAR
CLEAR
CLOCK
MODE CONTROL
S1
S0
SHIFT RIGHT SERIAL INPUT
A
B
C
D
SHIFT LEFT SERIAL INPUT
PARALLEL INPUTS

FIGURE 3. Logic diagrams - Continued.

Device type 06

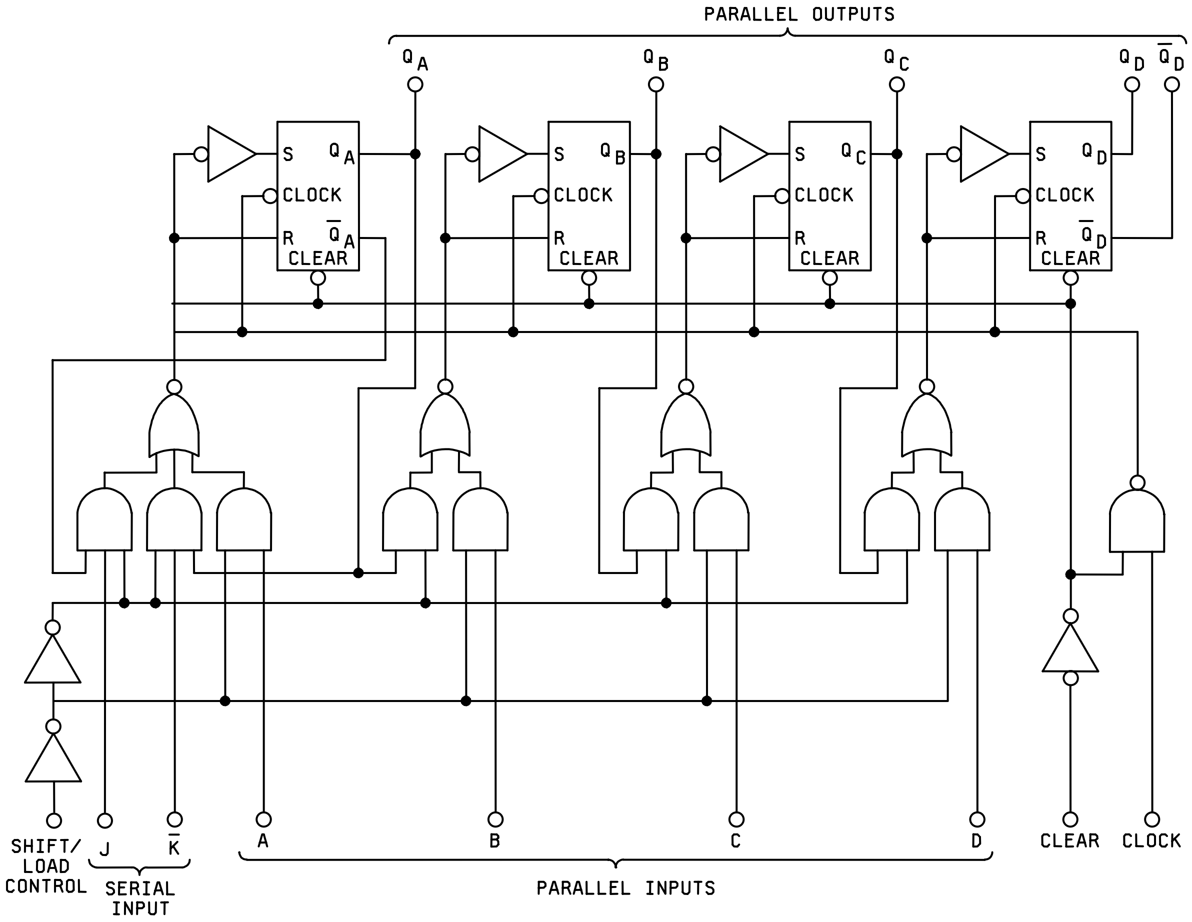
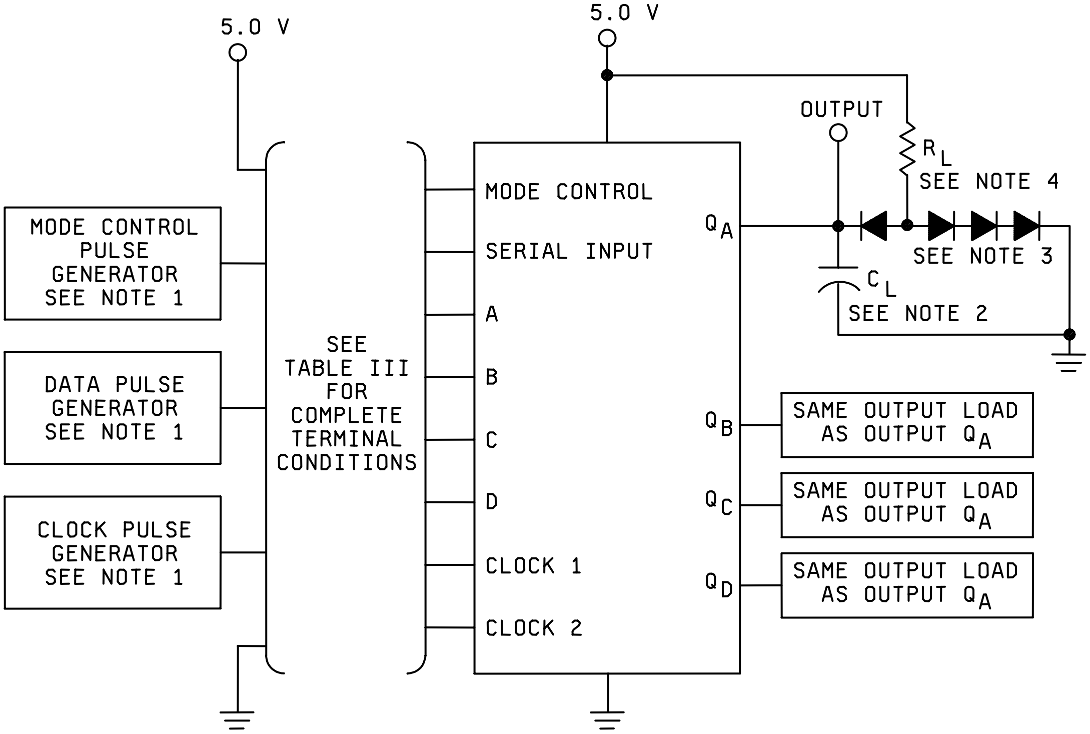

PARALLEL OUTPUTS
Q_A
Q_B
Q_C
Q_D
$\overline{Q}_D$
S
CLOCK
R
CLEAR
Q_A
$\overline{Q}_A$
Q_B
Q_C
Q_D
$\overline{Q}_D$
SHIFT/ LOAD CONTROL
J
$\overline{K}$
SERIAL INPUT
A
B
C
D
PARALLEL INPUTS
CLEAR
CLOCK

FIGURE 3. Logic diagrams - Continued.

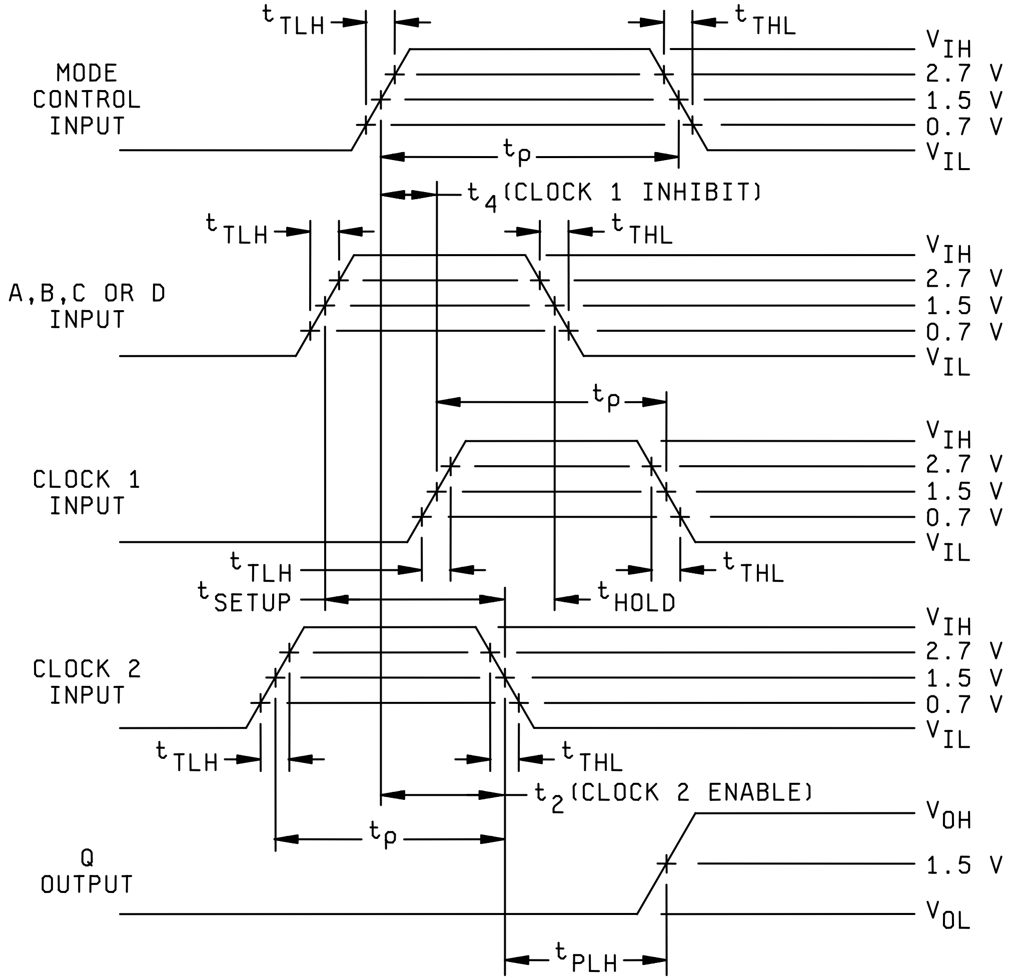

5.0 V
5.0 V
OUTPUT
R L
SEE NOTE 4
SEE NOTE 3
C L
SEE NOTE 2
MODE CONTROL PULSE GENERATOR SEE NOTE 1
DATA PULSE GENERATOR SEE NOTE 1
CLOCK PULSE GENERATOR SEE NOTE 1
SEE TABLE III FOR COMPLETE TERMINAL CONDITIONS
MODE CONTROL
SERIAL INPUT
A
B
C
D
CLOCK 1
CLOCK 2
Q A
Q B
Q C
Q D
SAME OUTPUT LOAD AS OUTPUT Q A
SAME OUTPUT LOAD AS OUTPUT Q A
SAME OUTPUT LOAD AS OUTPUT Q A

NOTES:

1. Unless otherwise specified in the notes with the individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$ V, $Z_{OUT} = 50\ \Omega$.
2. $C_L = 50$ pF minimum including jig and probe capacitance.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 400\ \Omega \pm 5\%$.

FIGURE 4. Switching test circuits and waveforms for device type 01.

MAXIMUM SHIFT FREQUENCY (f_{MAX}) AND CLOCK TO OUTPUT (t_{PLH})

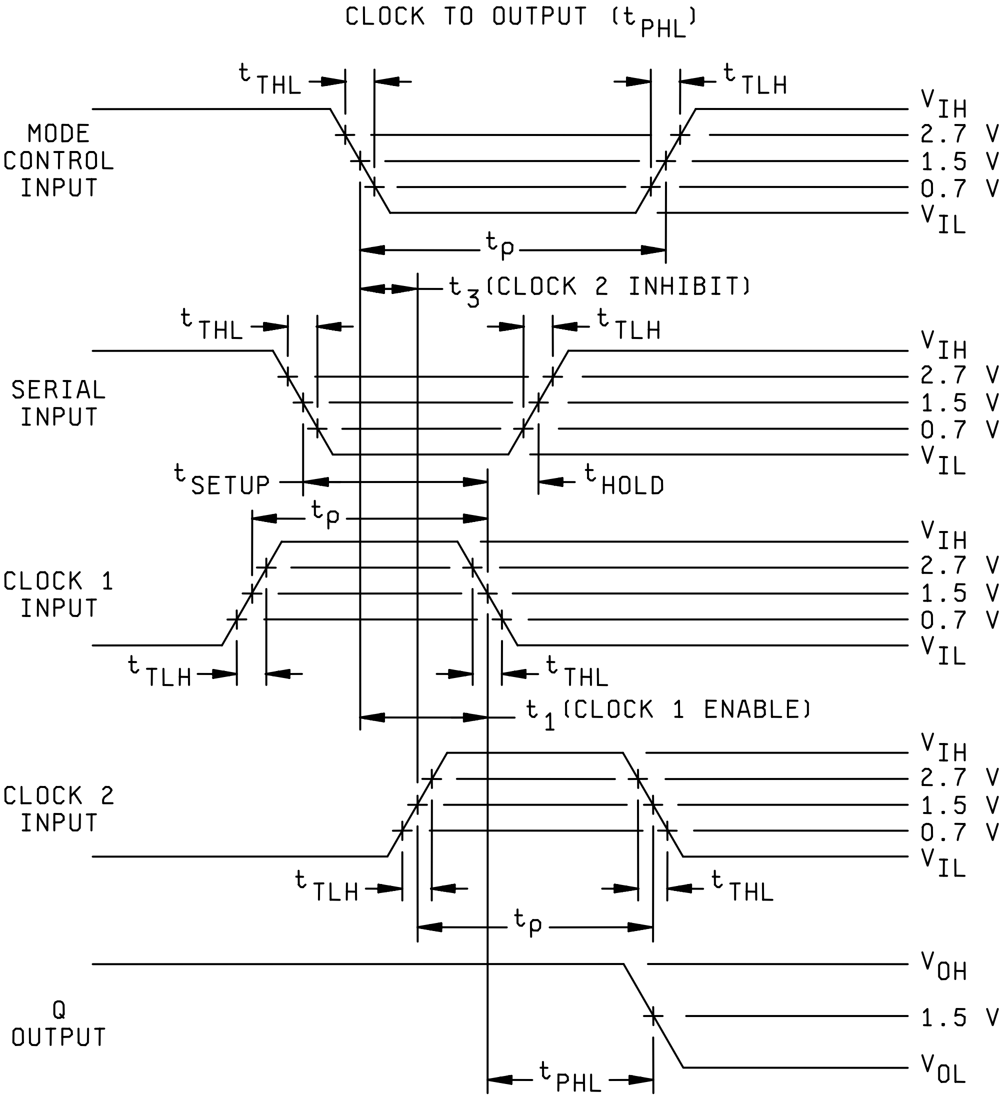


MODE CONTROL INPUT
A,B,C OR D INPUT
CLOCK 1 INPUT
CLOCK 2 INPUT
Q OUTPUT
t TLH
t THL
t P
t 4 (CLOCK 1 INHIBIT)
t SETUP
t HOLD
t 2 (CLOCK 2 ENABLE)
t PLH
V IH
2.7 V
1.5 V
0.7 V
V IL
V OH
V OL

NOTES:

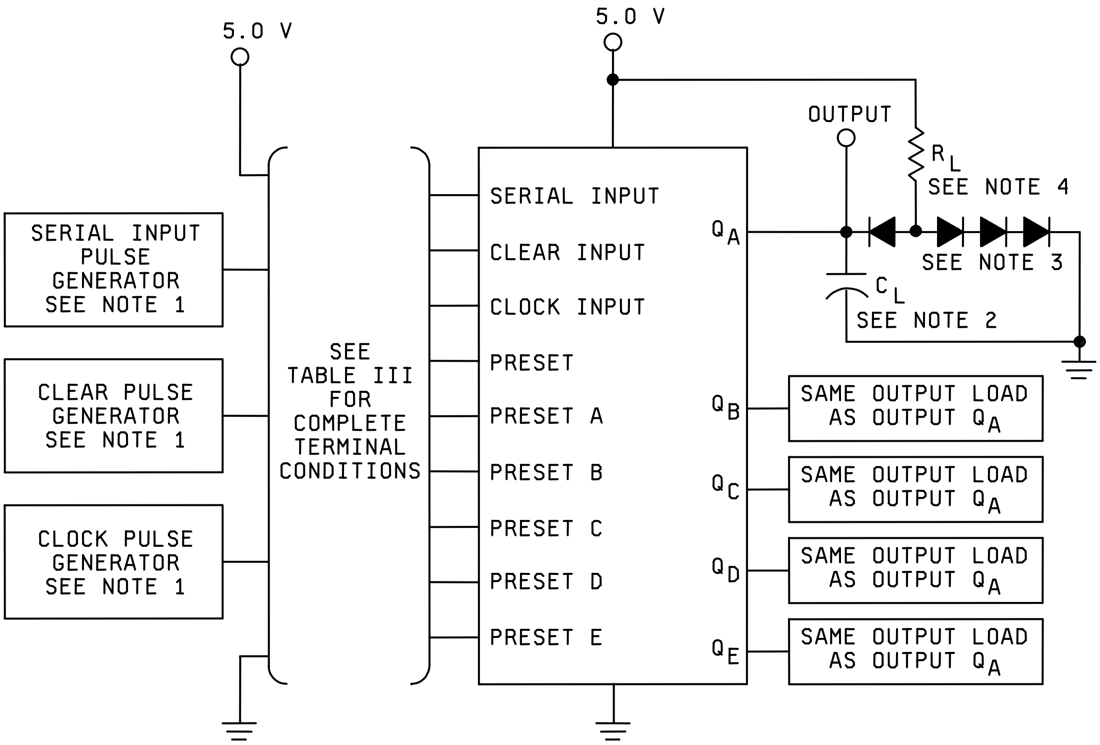
1. Mode control input characteristics: For f_{MAX}, PRR = 22 MHz at T_C = 25°C and PRR = 16 MHz at -55°C ≤ T_C ≤ 125°C. For t_{PLH}, PRR = 1 MHz, t_P = 35 ns, $t_{TLH} = t_{THL} \leq$ 10 ns.
2. A, B, C, or D input characteristics: For f_{MAX}, PRR = 11 MHz at T_C = 25°C and PRR = 8 MHz at -55°C ≤ T_C ≤ 125°C. For t_{PLH}, PRR = 500 kHz, $t_P = t_{SETUP} + t_{HOLD}$. t_{SETUP} = 20 ns, t_{HOLD} = 5 ns, $t_{TLH} = t_{THL} \leq$ 10 ns.
3. Clock 1 input characteristics: When testing f_{MAX}, PRR = 11 MHz at 25°C and PRR = 8 MHz at -55°C ≤ T_C ≤ 125°C. For t_{PLH}, PRR = 500 kHz, t_P = 20 ns minimum, $t_{TLH} = t_{THL} \leq$ 10 ns.
4. Clock 2 input characteristics: When testing f_{MAX}, PRR = 22 MHz at 25°C and PRR = 16 MHz at -55°C ≤ T_C ≤ 125°C. For t_{PLH}, PRR = 1 MHz, t_P = 20 ns minimum, $t_{TLH} = t_{THL} \leq$ 10 ns.
5. Serial input = GND.
6. Except for input under test, all other data inputs are open.

FIGURE 4. Switching test circuits and waveforms for device type 01 - Continued.


CLOCK TO OUTPUT (t_{PHL})
t_{THL}
t_{TLH}
MODE CONTROL INPUT
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
t_P
t_3 (CLOCK 2 INHIBIT)
SERIAL INPUT
t_{SETUP}
t_{HOLD}
CLOCK 1 INPUT
t_1 (CLOCK 1 ENABLE)
CLOCK 2 INPUT
Q OUTPUT
V_{OH}
V_{OL}
t_{PHL}

NOTES:
1. Mode control input characteristics: PRR = 1 MHz, t_P = 35 ns, $t_{TLH} = t_{THL} \leq 10$ ns.
2. Serial input characteristics: PRR = 500 kHz, $t_P = t_{SETUP} + t_{HOLD}$. t_{SETUP} = 20 ns, t_{HOLD} = 5 ns, $t_{TLH} = t_{THL} \leq$ 10 ns.
3. Clock 1 input characteristics: PRR = 1 MHz, t_P = 20 ns minimum, $t_{TLH} = t_{THL} \leq 10$ ns.
4. Clock 2 input characteristics: PRR = 500 kHz, t_P = 20 ns minimum, $t_{TLH} = t_{THL} \leq 10$ ns.
5. Inputs A thru D = OPEN.

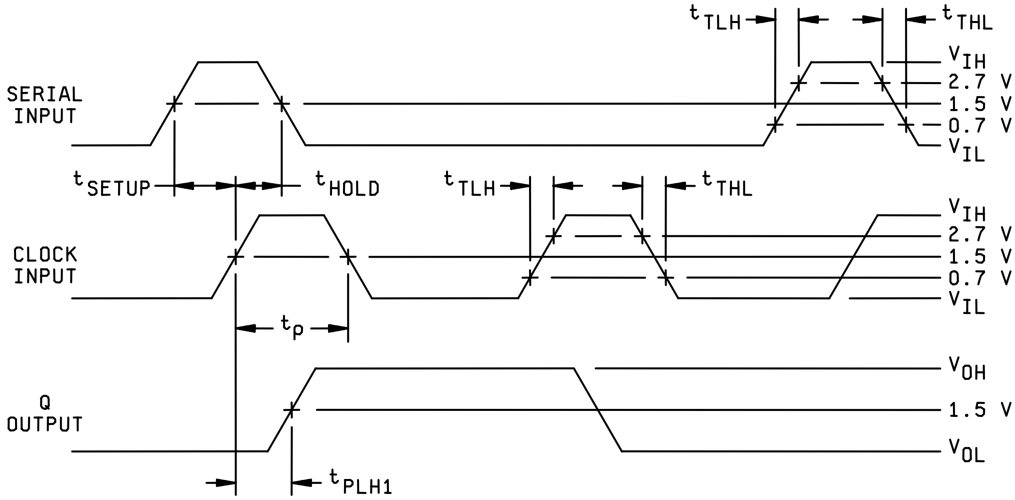
FIGURE 4. Switching test circuits and waveforms for device type 01 - Continued.


5.0 V
5.0 V
SERIAL INPUT PULSE GENERATOR SEE NOTE 1
CLEAR PULSE GENERATOR SEE NOTE 1
CLOCK PULSE GENERATOR SEE NOTE 1
SEE TABLE III FOR COMPLETE TERMINAL CONDITIONS
SERIAL INPUT
CLEAR INPUT
CLOCK INPUT
PRESET
PRESET A
PRESET B
PRESET C
PRESET D
PRESET E
Q_A
Q_B
Q_C
Q_D
Q_E
OUTPUT
R_L SEE NOTE 4
SEE NOTE 3
C_L SEE NOTE 2
SAME OUTPUT LOAD AS OUTPUT Q_A
SAME OUTPUT LOAD AS OUTPUT Q_A
SAME OUTPUT LOAD AS OUTPUT Q_A
SAME OUTPUT LOAD AS OUTPUT Q_A

NOTES:
1. Unless otherwise specified in the notes with the individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$ V, $Z_{OUT} = 50\ \Omega$.
2. $C_L = 50$ pF minimum including jig and probe capacitance.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 400\ \Omega \pm 5\%$.

FIGURE 5. Switching test circuits and waveforms for device type 02.

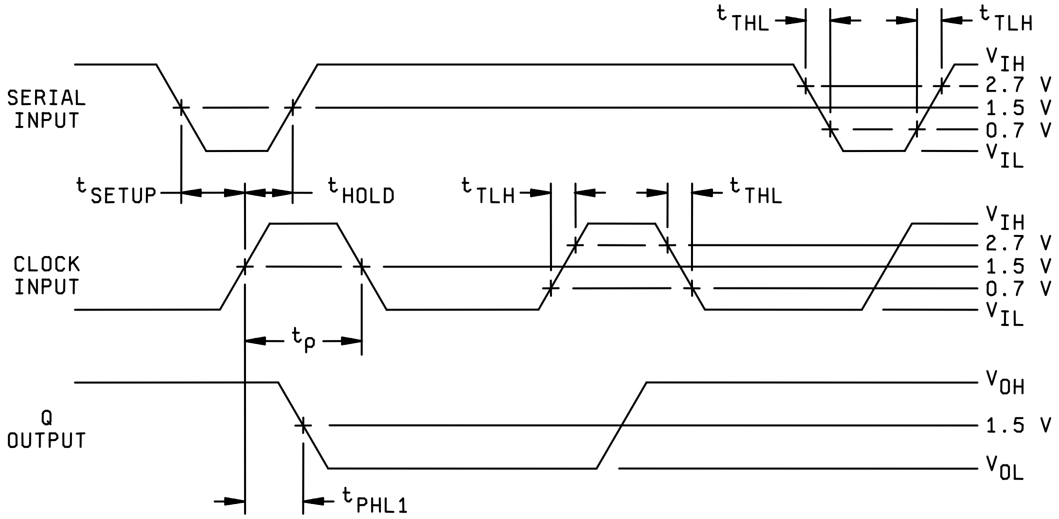
MAXIMUM CLOCK FREQUENCY (f_{MAX}) AND CLOCK TO OUTPUT (t_{PLH1})


t TLH
t THL
SERIAL INPUT
V IH
2.7 V
1.5 V
0.7 V
V IL
t SETUP
t HOLD
t TLH
t THL
CLOCK INPUT
V IH
2.7 V
1.5 V
0.7 V
V IL
t P
Q OUTPUT
V OH
1.5 V
V OL
t PLH1

NOTES:

1. Serial input characteristics: For f_{MAX}, PRR = 5 MHz at T_C = 25°C, PRR = 3.5 MHz at -55°C ≤ T_C ≤ 125°C. For t_{PLH1}, PRR = 500 kHz, $t_P = t_{SETUP} + t_{HOLD}$, t_{SETUP} = 30 ns, t_{HOLD} = 0 ns, $t_{THL} = t_{TLH} \leq 10$ ns.
2. Clock input characteristics: For f_{MAX}, PRR = 10 MHz at T_C = 25°C, PRR = 7 MHz at -55°C ≤ T_C ≤ 125°C. For t_{PLH1}, PRR = 1 MHz, t_P = 35 ns, $t_{THL} = t_{TLH} \leq 10$ ns.
3. Clear = 4.5 V, preset enable = GND, preset A thru E = OPEN.

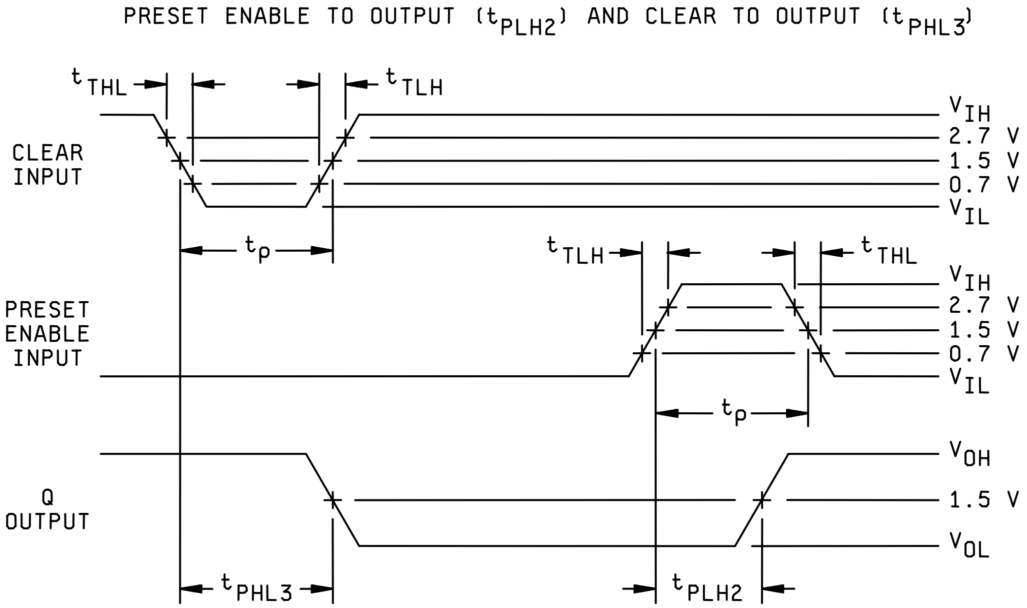
CLOCK TO OUTPUT (t_{PHL1})


t THL
t TLH
SERIAL INPUT
V IH
2.7 V
1.5 V
0.7 V
V IL
t SETUP
t HOLD
t TLH
t THL
CLOCK INPUT
V IH
2.7 V
1.5 V
0.7 V
V IL
t P
Q OUTPUT
V OH
1.5 V
V OL
t PHL1

NOTES:

1. Serial input characteristics: PRR = 500 kHz, $t_{THL} = t_{TLH} \leq 10$ ns $t_P = t_{SETUP} + t_{HOLD}$, t_{SETUP} = 30 ns, t_{HOLD} = 0 ns.
2. Clock input characteristics: PRR = 1 MHz, $t_{THL} = t_{TLH} \leq 10$ ns, t_P = 35 ns..
3. Clear = 4.5 V, preset enable = GND, preset A thru E = OPEN.

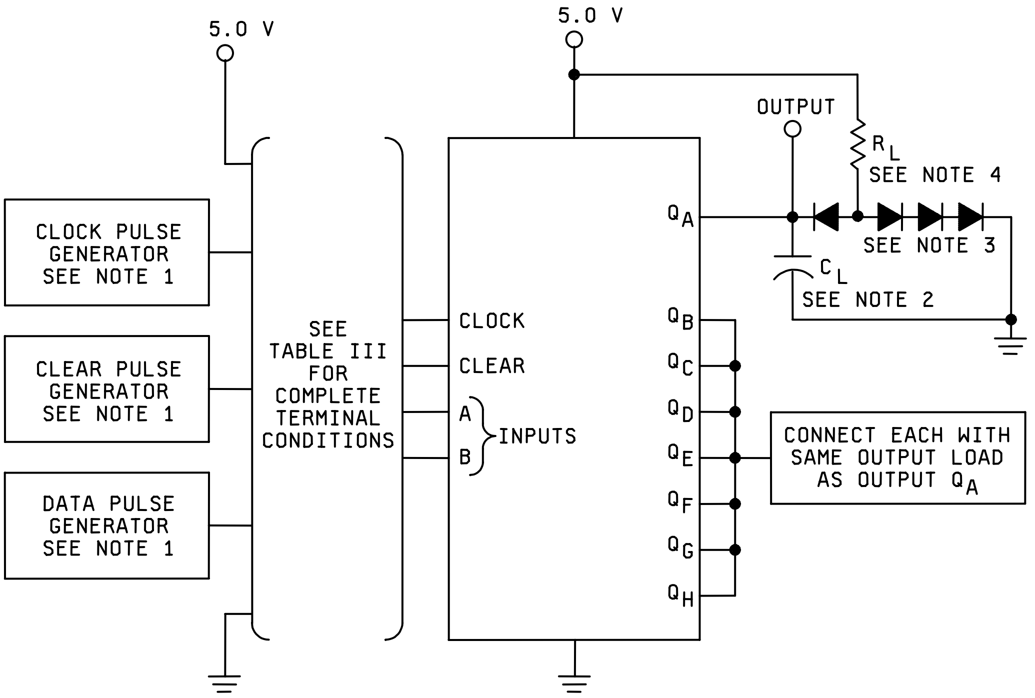
FIGURE 5. Switching test circuits and waveforms for device type 02 - Continued.


PRESET ENABLE TO OUTPUT (t_{PLH2}) AND CLEAR TO OUTPUT (t_{PHL3})
t_{THL}
t_{TLH}
CLEAR INPUT
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
t_P
PRESET ENABLE INPUT
t_{TLH}
t_{THL}
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
t_P
Q OUTPUT
V_{OH}
1.5 V
V_{OL}
t_{PHL3}
t_{PLH2}

NOTES:

1. Clear input characteristics: PRR = 1 MHz, $t_{THL} = t_{TLH} \leq 10$ ns, $t_P =$ 30 ns.
2. Preset enable characteristics: PRR = 1 MHz, $t_{THL} = t_{TLH} \leq 10$ ns, $t_P = 30$ ns..
3. Preset A thru E = 4.5 V, clock = GND, serial = OPEN.

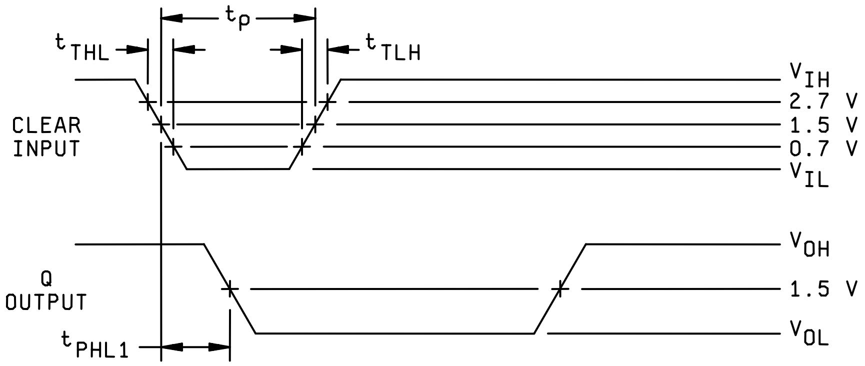
FIGURE 5. Switching test circuits and waveforms for device type 02 - Continued.


5.0 V
5.0 V
CLOCK PULSE GENERATOR SEE NOTE 1
CLEAR PULSE GENERATOR SEE NOTE 1
DATA PULSE GENERATOR SEE NOTE 1
SEE TABLE III FOR COMPLETE TERMINAL CONDITIONS
CLOCK
CLEAR
A
B
INPUTS
Q_A
Q_B
Q_C
Q_D
Q_E
Q_F
Q_G
Q_H
OUTPUT
R_L
SEE NOTE 4
SEE NOTE 3
C_L
SEE NOTE 2
CONNECT EACH WITH SAME OUTPUT LOAD AS OUTPUT Q_A

NOTES:

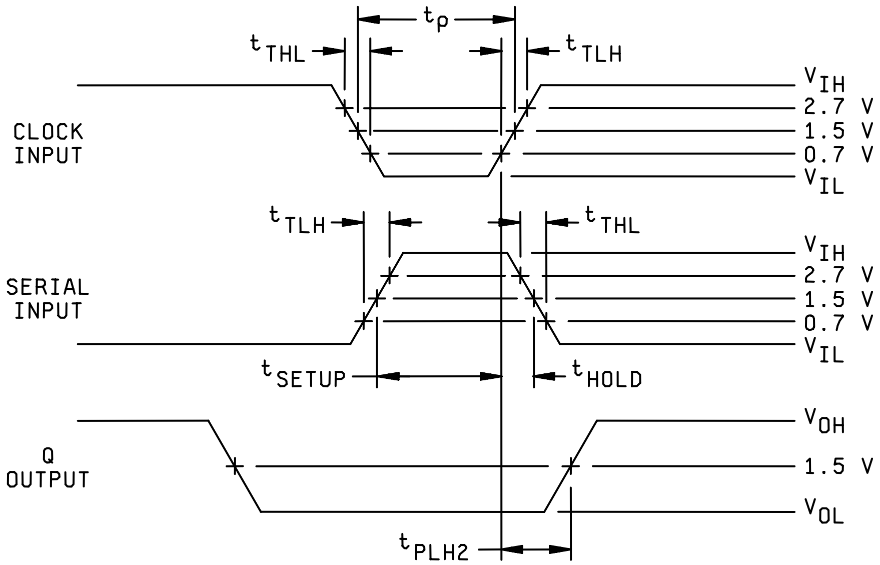
1. Unless otherwise specified in the notes with the individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$ V, $Z_{OUT} = 50\ \Omega$.
2. $C_L = 50$ pF minimum, including jig and probe capacitance.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 800\ \Omega \pm 5\%$.
5. QA outputs are illustrated in the individual waveforms. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.

FIGURE 6. Switching test circuits and waveforms for device type 03.


CLEAR INPUT TO Q OUTPUTS (t_{PHL1})
t_P
t_{THL}
t_{TLH}
CLEAR INPUT
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
Q OUTPUT
V_{OH}
1.5 V
V_{OL}
t_{PHL1}

NOTES:

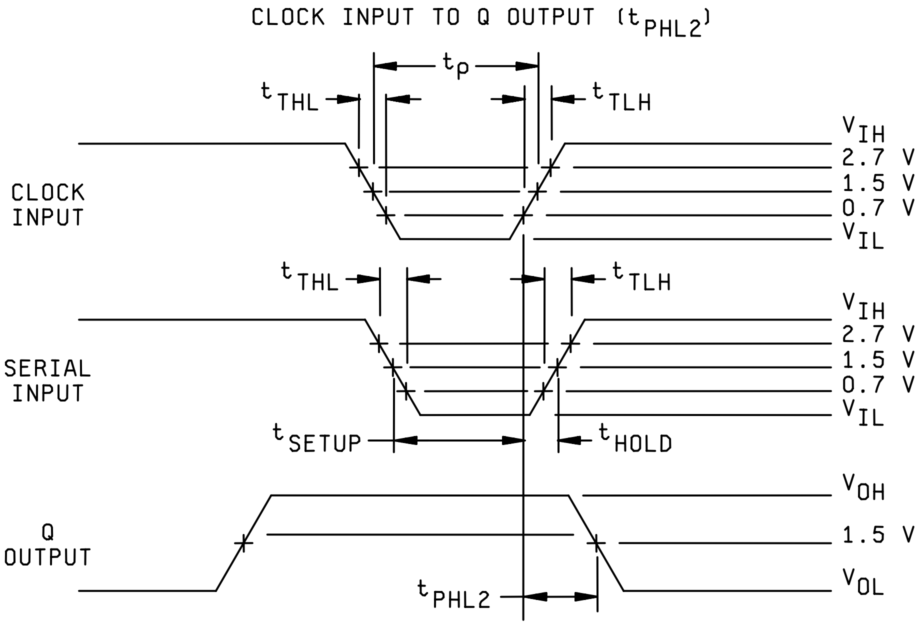
1. Clear input characteristics: PRR = 1 MHz, $t_{THL} = t_{TLH} \leq 10$ ns, $t_P = 50$ ns maximum.
2. Clock = GND, serial inputs A and B = OPEN.


MAXIMUM CLOCK FREQUENCY, (f_{MAX}) AND CLOCK INPUT TO Q OUTPUT (t_{PLH2})
t_P
t_{THL}
t_{TLH}
CLOCK INPUT
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
t_{TLH}
t_{THL}
SERIAL INPUT
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
t_{SETUP}
t_{HOLD}
Q OUTPUT
V_{OH}
1.5 V
V_{OL}
t_{PLH2}

NOTES:

1. Clock input characteristics: For f_{MAX}, PRR = 22 MHz at $T_C = 25°C$, PRR = 18 MHz at $-55°C \leq T_C \leq 125°C$. For t_{PLH2}, PRR = 1 MHz, $t_P = 30$ ns maximum, $t_{THL} = t_{TLH} \leq 10$ ns.
2. Serial input characteristics: For f_{MAX}, PRR = 11 MHz at 25°C, PRR = 9 MHz at $-55°C \leq T_C \leq 125°C$. For t_{PLH2}, PRR = 500 kHz, $t_P = t_{SETUP} + t_{HOLD}$, $t_{SETUP} = 15$ ns minimum, $t_{HOLD} = 10$ ns maximum, $t_{THL} = t_{TLH} \leq 10$ ns.
3. Clear = 4.5 V.

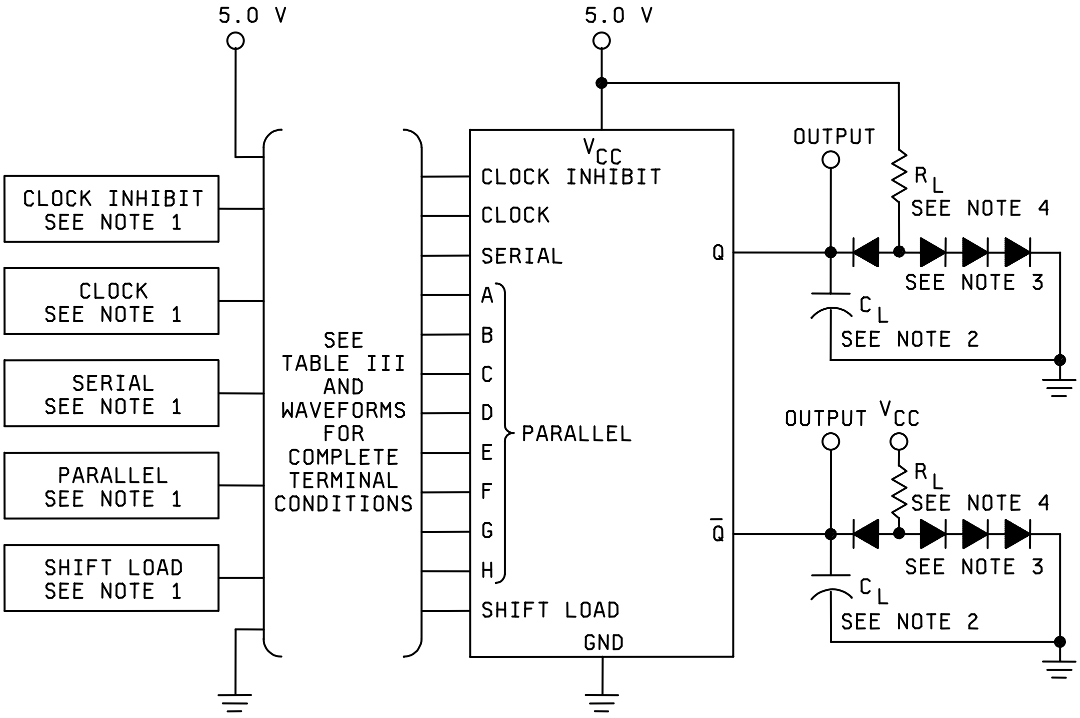
FIGURE 6. Switching test circuits and waveforms for device type 03 - Continued.


CLOCK INPUT TO Q OUTPUT (t_{PHL2})
t_P
t_{THL}
t_{TLH}
CLOCK INPUT
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
t_{THL}
t_{TLH}
SERIAL INPUT
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
t_{SETUP}
t_{HOLD}
Q OUTPUT
V_{OH}
1.5 V
V_{OL}
t_{PHL2}

NOTES:

1. Clock input characteristics: PRR = 1 MHz, $t_{THL} = t_{TLH} \leq 10$ ns, $t_P = 30$ ns maximum.
2. Serial input characteristics: PRR = 500 kHz, $t_P = t_{SETUP} + t_{HOLD}$, $t_{SETUP} = 15$ ns minimum, $t_{HOLD} = 10$ ns maximum, $t_{THL} = t_{TLH} \leq 10$ ns.
3. Clear = 4.5 V.

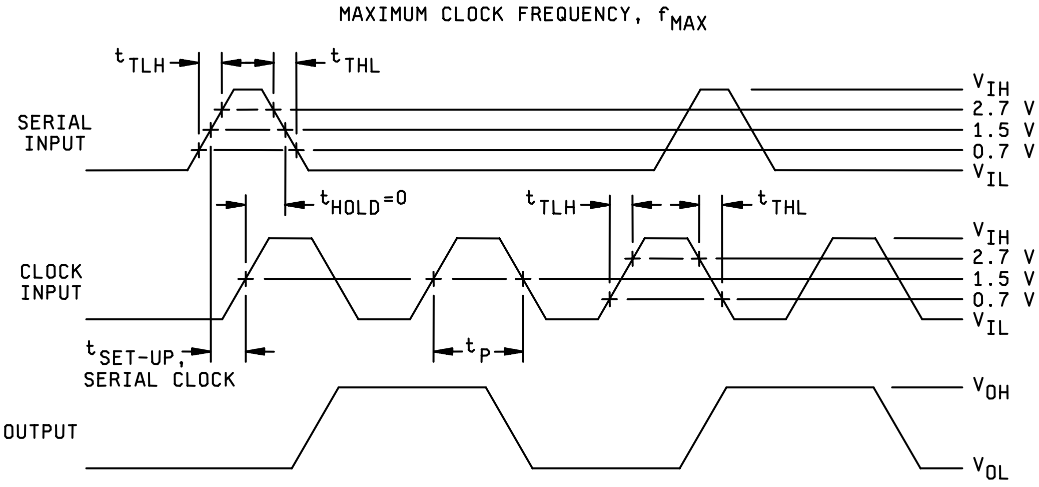
FIGURE 6. Switching test circuits and waveforms for device type 03 - Continued.


5.0 V
5.0 V
CLOCK INHIBIT SEE NOTE 1
CLOCK SEE NOTE 1
SERIAL SEE NOTE 1
PARALLEL SEE NOTE 1
SHIFT LOAD SEE NOTE 1
SEE TABLE III AND WAVEFORMS FOR COMPLETE TERMINAL CONDITIONS
VCC
CLOCK INHIBIT
CLOCK
SERIAL
A
B
C
D
E
F
G
H
PARALLEL
SHIFT LOAD
GND
Q
Q̄
OUTPUT
RL SEE NOTE 4
SEE NOTE 3
CL SEE NOTE 2
OUTPUT
VCC
RL SEE NOTE 4
SEE NOTE 3
CL SEE NOTE 2

NOTES:

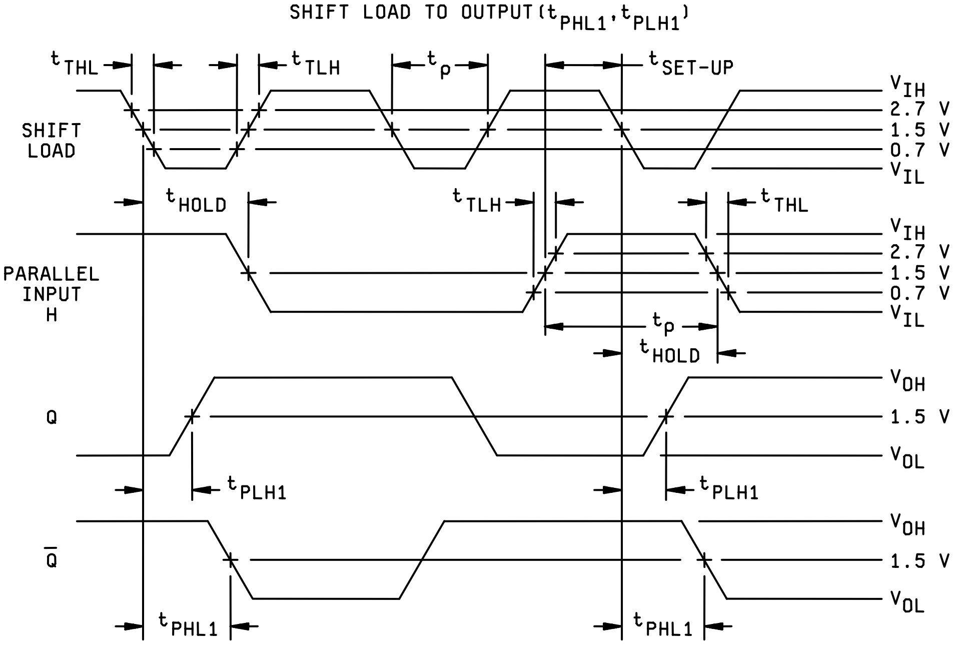
1. Unless otherwise specified in the notes with the individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$ V, $Z_{OUT} \approx 50\ \Omega$.
2. $C_L = 50$ pF minimum, including jig and probe capacitance
3. All diodes are 1N3064 or equivalent.
4. $R_L = 400\ \Omega \pm 5\%$.

FIGURE 7. Switching test circuits and waveforms for device type 04.


MAXIMUM CLOCK FREQUENCY, f_MAX
t_TLH
t_THL
SERIAL INPUT
V_IH
2.7 V
1.5 V
0.7 V
V_IL
t_HOLD=0
t_TLH
t_THL
CLOCK INPUT
t_SET-UP, SERIAL CLOCK
t_P
OUTPUT
V_OH
V_OL

NOTES:

1. Clock input characteristics: PRR = 18 MHz at T_C = 25°C, PRR = 14 MHz at -55°C ≤ T_C ≤ 125°C, $t_{THL} = t_{TLH} \leq$ 10 ns, t_P = 20 ns minimum.
2. Serial pulse characteristics: PRR = 9 MHz at T_C = 25°C, PRR = 7 MHz at -55°C ≤ T_C ≤ 125°C, $t_P = t_{SETUP} + t_{HOLD}$, t_{SETUP} = 35 ns minimum, t_{HOLD} = 0 ns, $t_{THL} = t_{TLH} \leq$ 5 ns.
3. Shift load characteristics: $t_{TLH} \leq$ 10 ns, t_{SETUP} = 45 ns.
4. Clock inhibit = GND, A through H = GND.

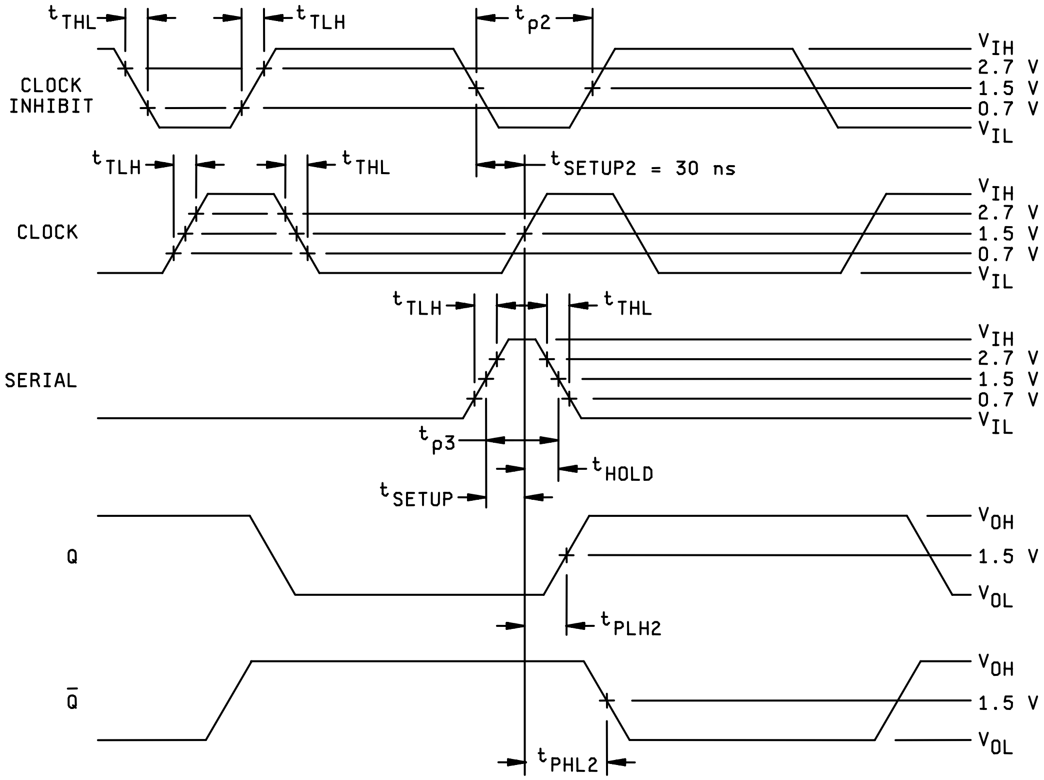

SHIFT LOAD TO OUTPUT(t_PHL1, t_PLH1)
t_THL
t_TLH
t_P
t_SET-UP
SHIFT LOAD
V_IH
2.7 V
1.5 V
0.7 V
V_IL
t_HOLD
t_TLH
t_THL
PARALLEL INPUT H
t_P
t_HOLD
Q
V_OH
1.5 V
V_OL
t_PLH1
t_PLH1
Q̄
t_PHL1
t_PHL1

NOTES:

1. Shift load characteristics: PRR = 1 MHz, t_P = 25 ns, $t_{THL} = t_{TLH} \leq$ 10 ns.
2. Parallel input characteristics: PRR = 500 kHz, $t_P = t_{SETUP} + t_{HOLD}$ = 40 ns, t_{SETUP} = 10 ns, t_{HOLD} = 30 ns , t_{THL} = ≤ 10 ns.
3. Clock = clock inhibit = GND, A through G = GND, serial = open.

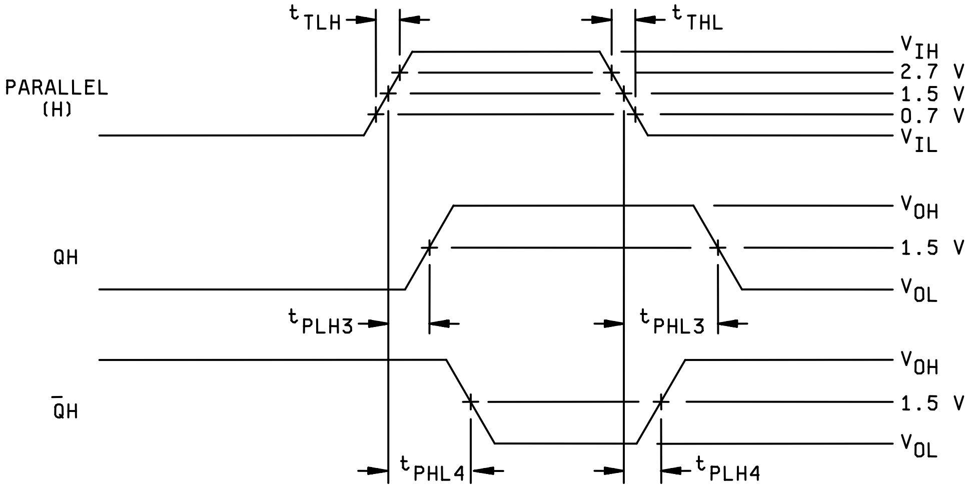
FIGURE 7. Switching test circuits and waveforms for device type 04 - Continued.

CLOCK TO OUTPUT (t_{PHL2} and t_{PLH2})


CLOCK INHIBIT
CLOCK
SERIAL
Q
Q̄
tTHL
tTLH
tp2
tSETUP2 = 30 ns
tp3
tSETUP
tHOLD
tPLH2
tPHL2
VIH
2.7 V
1.5 V
0.7 V
VIL
VOH
VOL

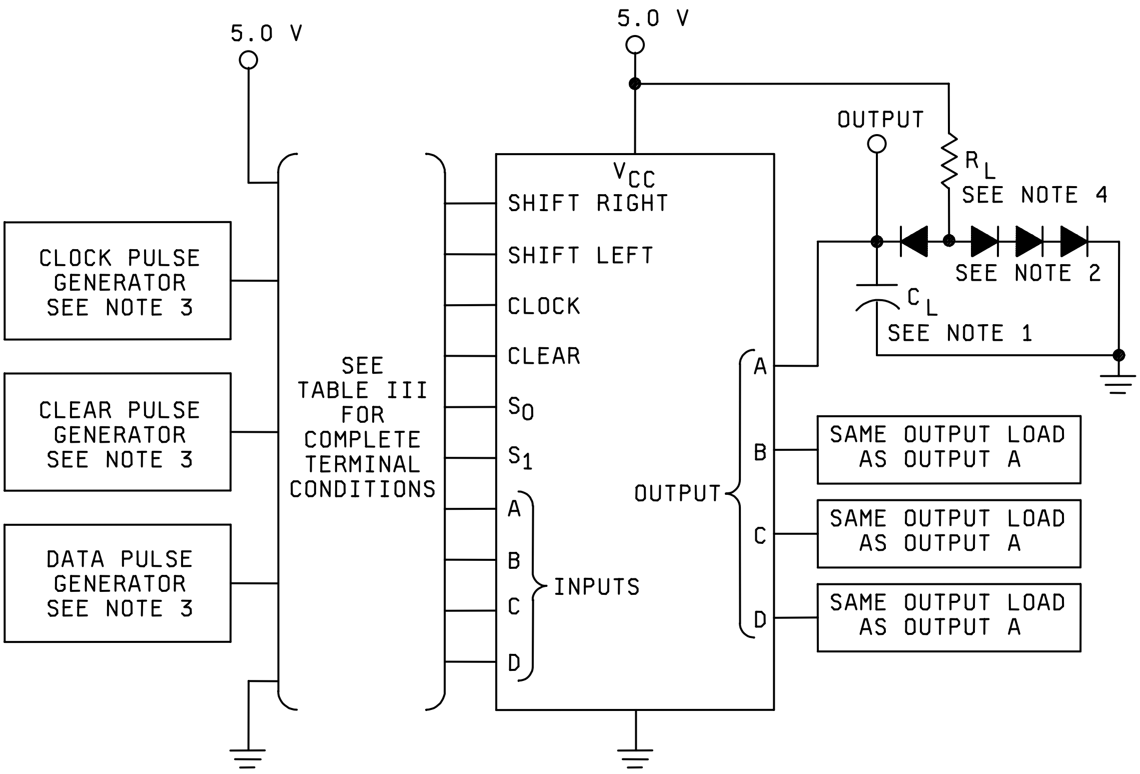
NOTES:
1. Clock inhibit characteristics: PRR = 1 MHz, t_{P2} = 50 ns, $t_{THL} = t_{TLH} \leq 10$ ns, t_{SETUP2} = 34 ns.
2. Clock pulse characteristics: PRR = 1 MHz, t_{P1} = 25 ns, $t_{THL} = t_{TLH} \leq 10$ ns.
3. Serial pulse characteristics: PRR = 500 kHz, $t_{P3} = t_{SETUP} + t_{HOLD}$, t_{SETUP} = 35 ns, t_{HOLD} = 0, $t_{THL} = t_{TLH} \leq 5$ ns.
4. Shift/load = 5.0 V.

(H) INPUT TO QH and $\overline{QH}$ OUTPUTS (t_{PHL3} and t_{PLH3}) (t_{PHL4} and t_{PLH4})


PARALLEL (H)
QH
Q̄H
tTLH
tTHL
tPLH3
tPHL3
tPHL4
tPLH4
VIH
2.7 V
1.5 V
0.7 V
VIL
VOH
VOL

NOTES:
1. (H) input characteristics: PRR = 1 MHz, 50% duty cycle, $t_{THL} = t_{TLH} \leq 10$ ns.
2. Shift/load = GND, clock inhibit = GND, serial = GND, A thru G = GND, clock = GND..

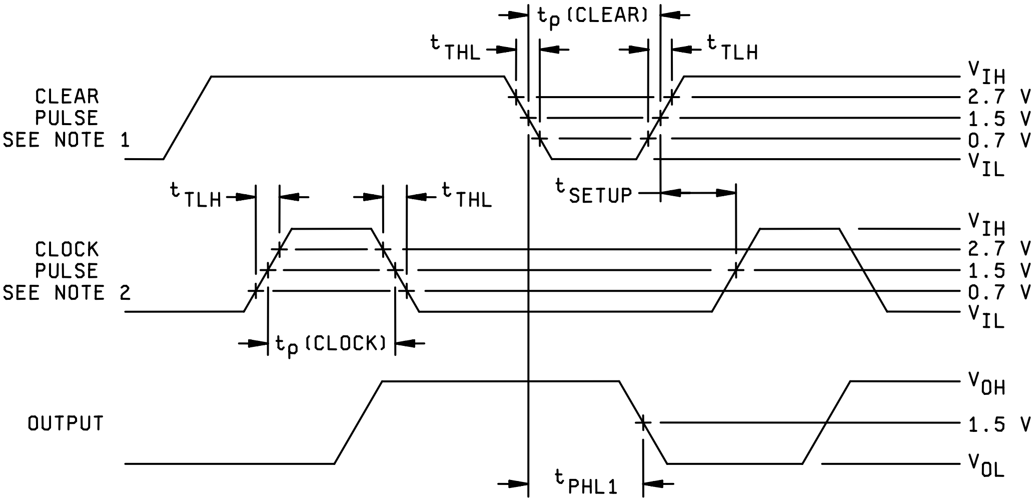
FIGURE 7. Switching test circuits and waveforms for device type 04 - Continued.


5.0 V
5.0 V
CLOCK PULSE GENERATOR SEE NOTE 3
CLEAR PULSE GENERATOR SEE NOTE 3
DATA PULSE GENERATOR SEE NOTE 3
SEE TABLE III FOR COMPLETE TERMINAL CONDITIONS
VCC
SHIFT RIGHT
SHIFT LEFT
CLOCK
CLEAR
S0
S1
A
B
C
D
INPUTS
OUTPUT
A
B
C
D
OUTPUT
RL
SEE NOTE 4
SEE NOTE 2
CL
SEE NOTE 1
SAME OUTPUT LOAD AS OUTPUT A
SAME OUTPUT LOAD AS OUTPUT A
SAME OUTPUT LOAD AS OUTPUT A

NOTES:
1. C_L = 50 pF minimum including probe and jig capacitance.
2. All diodes are 1N3064, or equivalent.
3. Unless otherwise specified in the notes associated with the individual tests, all pulse generators have the following characteristics: $Z_{OUT} \approx 50\ \Omega$, $t_{TLH} \le 7$ ns, $t_{THL} \le 7$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$.
4. $R_L = 400\ \Omega \pm 5\%$.

FIGURE 8. Switching test circuits and waveforms for device type 05.

CLEAR TO OUTPUT

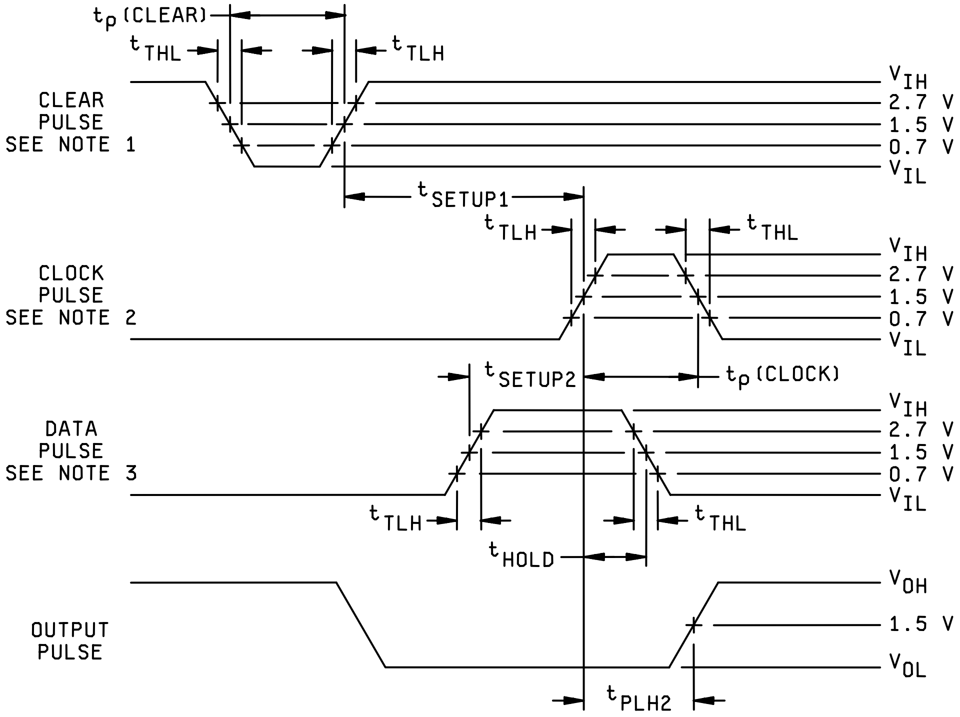


tp (CLEAR)
tTHL
tTLH
CLEAR PULSE SEE NOTE 1
VIH
2.7 V
1.5 V
0.7 V
VIL
tTLH
tTHL
tSETUP
CLOCK PULSE SEE NOTE 2
VIH
2.7 V
1.5 V
0.7 V
VIL
tp (CLOCK)
OUTPUT
VOH
1.5 V
VOL
tPHL1

NOTES:

1. The clear pulse has the following characteristics: $t_{P(CLEAR)}$ = 20 ns, t_{SETUP} = 25 ns, PRR = 1 MHz.
2. The clock pulse has the following characteristics: $t_{P(CLOCK)}$ = 20 ns, PRR = 1 MHz.

CLOCK TO OUTPUT, DATA PULSE TO PARALLEL INPUT (t_{PLH2})

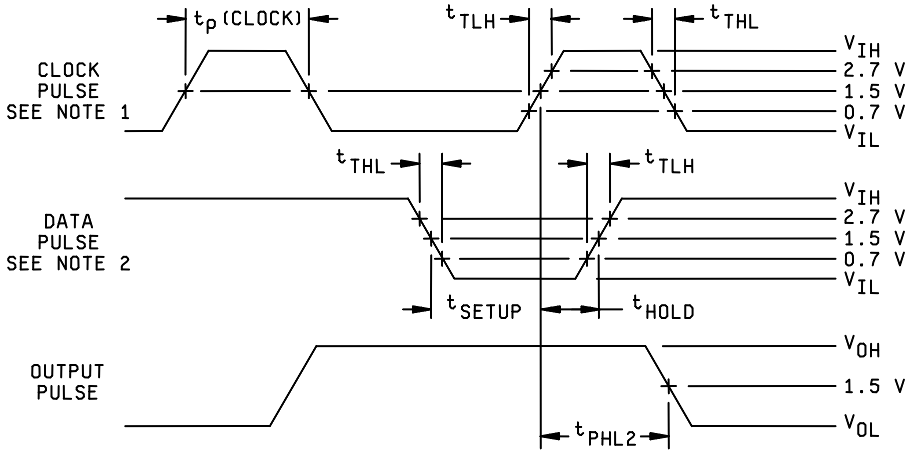


tp (CLEAR)
tTHL
tTLH
CLEAR PULSE SEE NOTE 1
VIH
2.7 V
1.5 V
0.7 V
VIL
tSETUP1
tTLH
tTHL
CLOCK PULSE SEE NOTE 2
VIH
2.7 V
1.5 V
0.7 V
VIL
tSETUP2
tp (CLOCK)
DATA PULSE SEE NOTE 3
VIH
2.7 V
1.5 V
0.7 V
VIL
tTLH
tTHL
tHOLD
OUTPUT PULSE
VOH
1.5 V
VOL
tPLH2

NOTES:

1. The clear pulse is a momentary ground, then V_{IH} is applied to the input. $t_{P(CLEAR)} \leq 75$ ns, $t_{THL} \leq 15$ ns and $t_{TLH} \leq 15$ ns, t_{SETUP} = 25 ns.
2. Clock pulse characteristics: $t_{P(CLOCK)}$ = 20 ns, PRR = 2 MHz.
3. Data pulse characteristics: $t_{P(DATA)} = t_{(SETUP2)} + t_{HOLD}$, t_{SETUP2} = 20 ns, t_{HOLD} = 7 ns, PRR = 1 MHz.

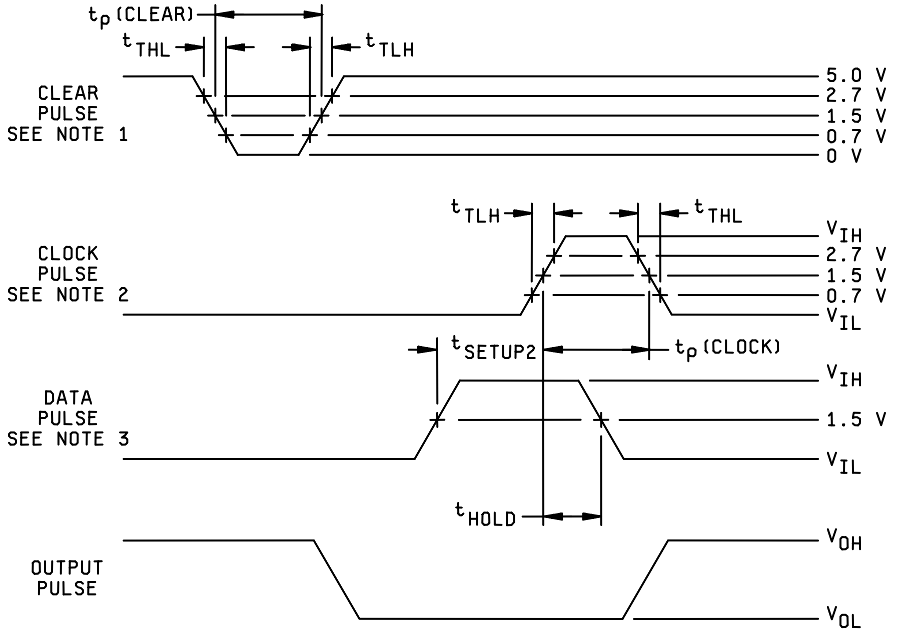
FIGURE 8. Switching test circuits and waveforms for device type 05 - Continued.


CLOCK TO OUTPUT, DATA PULSE TO PARALLEL INPUT (t_{PHL2})

t_p (CLOCK)
t_{TLH}
t_{THL}
CLOCK PULSE SEE NOTE 1
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
t_{THL}
t_{TLH}
DATA PULSE SEE NOTE 2
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
t_{SETUP}
t_{HOLD}
OUTPUT PULSE
V_{OH}
1.5 V
V_{OL}
t_{PHL2}

NOTES:

1. Clock pulse characteristics: $t_{P(CLOCK)}$ = 20 ns, PRR = 2 MHz.
2. Data pulse characteristics: $t_{P(DATA)} = t_{SETUP}$ = 20 ns, PRR = 1 MHz.

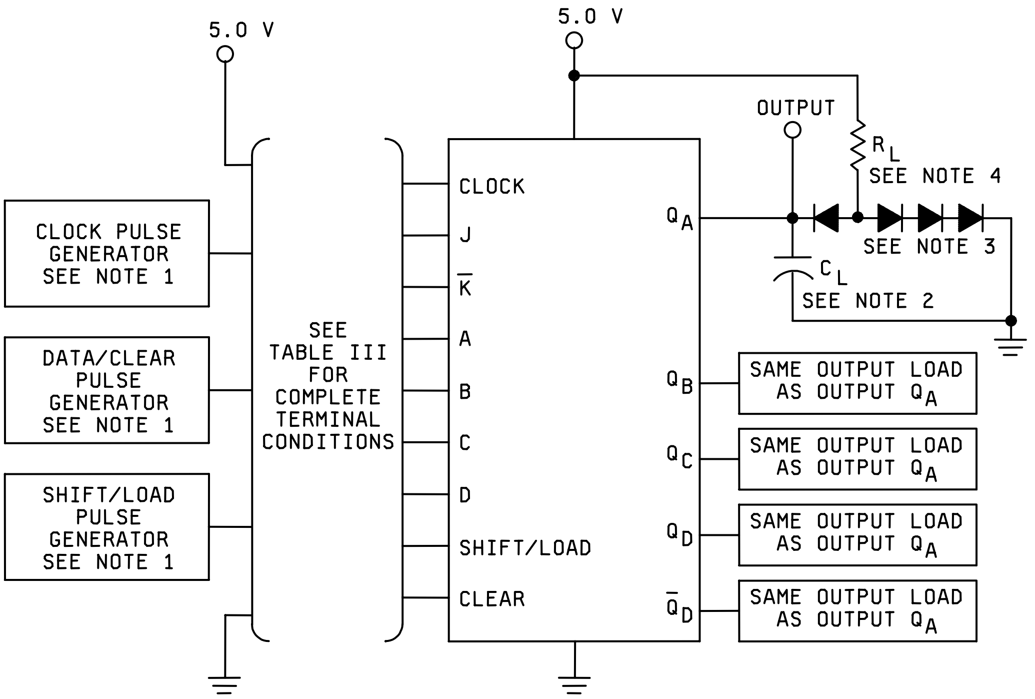

MAXIMUM CLOCK FREQUENCY (f_{MAX})

t_p (CLEAR)
t_{THL}
t_{TLH}
CLEAR PULSE SEE NOTE 1
5.0 V
2.7 V
1.5 V
0.7 V
0 V
t_{TLH}
t_{THL}
CLOCK PULSE SEE NOTE 2
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
t_{SETUP2}
t_p (CLOCK)
DATA PULSE SEE NOTE 3
V_{IH}
1.5 V
V_{IL}
t_{HOLD}
OUTPUT PULSE
V_{OH}
V_{OL}

NOTES:

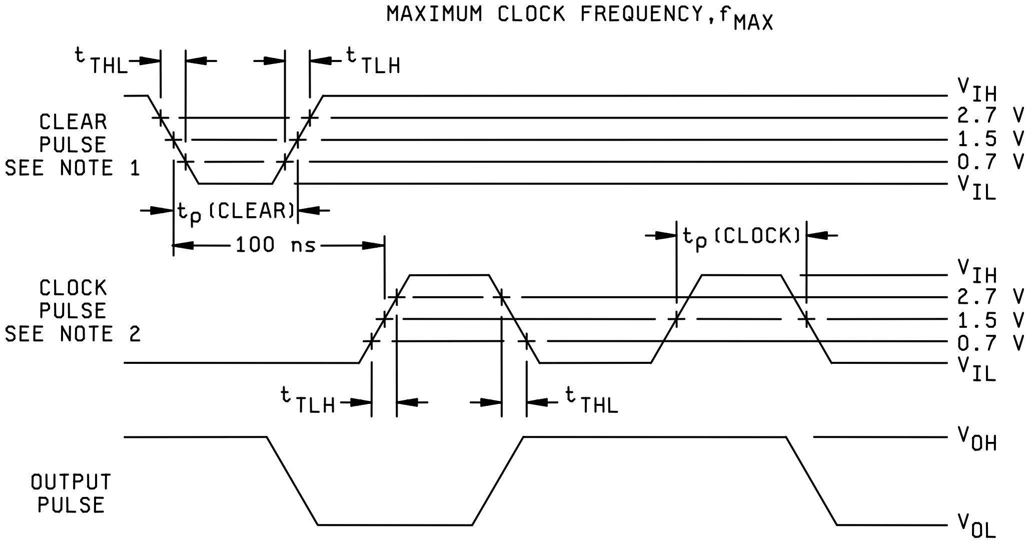
1. The clear pulse is a momentary GND, then V_{IH} is applied to the input, $t_{P(CLEAR)} \leq 20$ ns, $t_{THL} \leq 15$ ns, $t_{TLH} \leq 15$ ns.
2. Clock pulse characteristics: $t_{P(CLOCK)}$ = 20 ns, PRR = 18 MHz at -55°C ≤ T_C ≤ 125°C (22 MHz at T_C = 25°C).
3. Data pulse characteristics: $t_{P(DATA)} = t_{SETUP}$ = 20 ns, PRR = 9 MHz at -55°C ≤ T_C ≤ 125°C (11 MHz at T_C = 25°C).

FIGURE 8. Switching test circuits and waveforms for device type 05 - Continued.


5.0 V
5.0 V
CLOCK PULSE GENERATOR SEE NOTE 1
DATA/CLEAR PULSE GENERATOR SEE NOTE 1
SHIFT/LOAD PULSE GENERATOR SEE NOTE 1
SEE TABLE III FOR COMPLETE TERMINAL CONDITIONS
CLOCK
J
$\overline{K}$
A
B
C
D
SHIFT/LOAD
CLEAR
Q_A
Q_B
Q_C
Q_D
$\overline{Q}_D$
OUTPUT
R_L
SEE NOTE 4
SEE NOTE 3
C_L
SEE NOTE 2
SAME OUTPUT LOAD AS OUTPUT Q_A
SAME OUTPUT LOAD AS OUTPUT Q_A
SAME OUTPUT LOAD AS OUTPUT Q_A
SAME OUTPUT LOAD AS OUTPUT Q_A

NOTES:

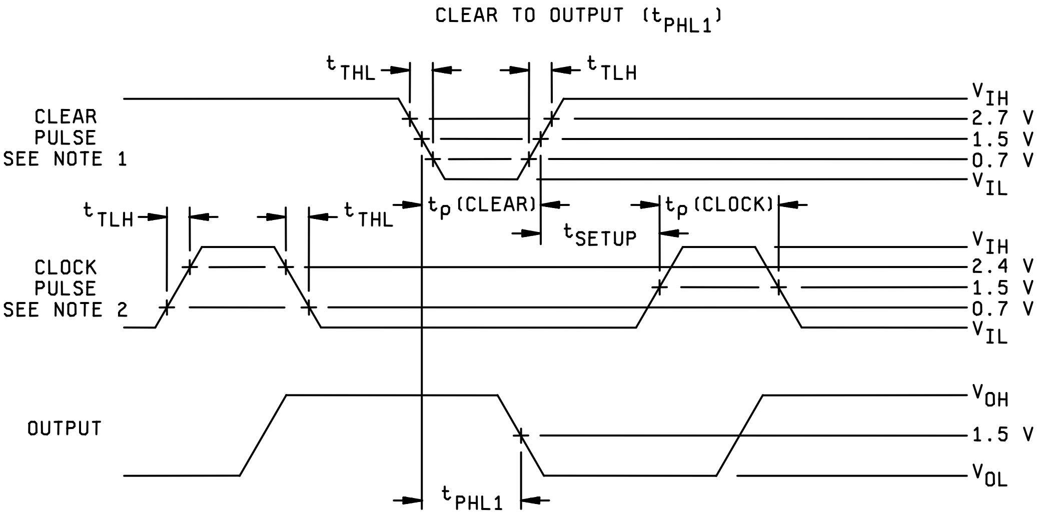
1. Unless otherwise specified in the notes with the individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 7$ ns, $t_{THL} \leq 7$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$, $Z_{OUT} \approx 50\ \Omega$.
2. $C_L = 50$ pF minimum, including jig and probe capacitance.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 400\ \Omega \pm 5\%$.


MAXIMUM CLOCK FREQUENCY, f_{MAX}
t_{THL}
t_{TLH}
CLEAR PULSE SEE NOTE 1
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
t_p (CLEAR)
100 ns
t_p (CLOCK)
CLOCK PULSE SEE NOTE 2
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
t_{TLH}
t_{THL}
OUTPUT PULSE
V_{OH}
V_{OL}

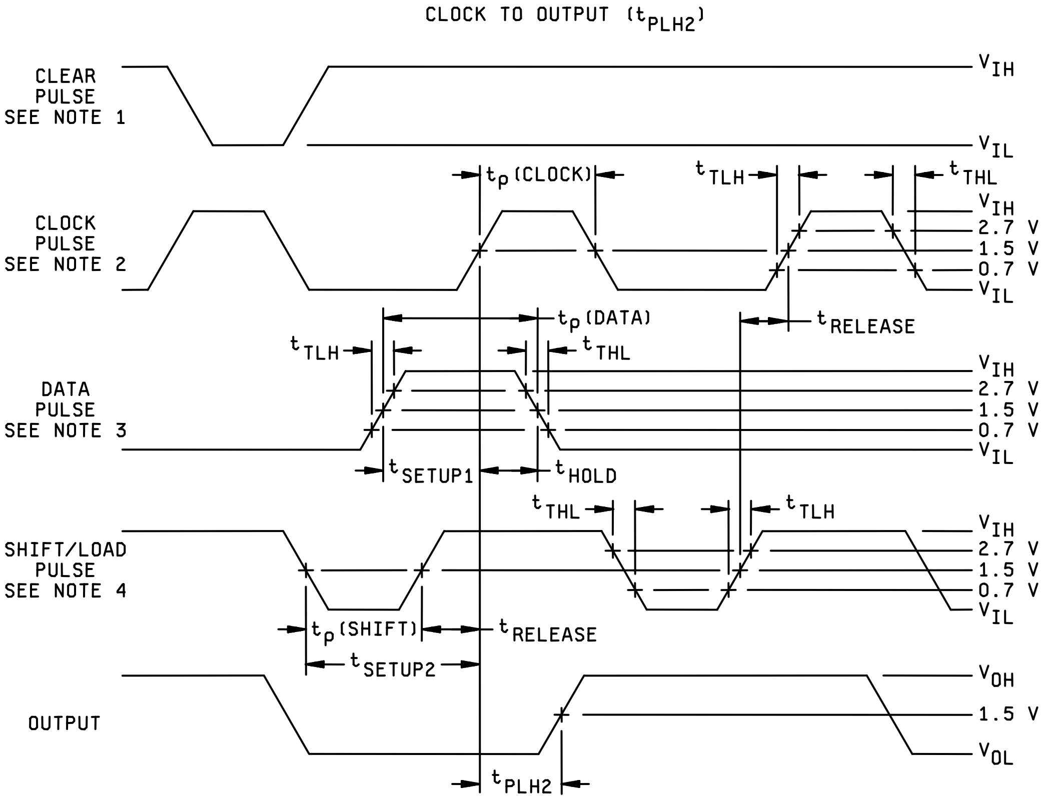
NOTES:

1. The clear pulse is a momentary GND, then V_{IH} is applied to the input. $t_{TLH} \leq 15$ ns, $t_{THL} \leq 15$ ns, $t_{P(CLEAR)} \leq 75$ ns.
2. Clock pulse characteristics: $t_{P(CLOCK)} = 16$ ns, PRR = 24 MHz at -55°C $\leq T_C \leq$ 125°C (30 MHz at T_C = 25°C), $V_{IH} = 3.0$ V minimum, V_{IL} = GND.

FIGURE 9. Switching test circuits and waveforms for device type 06.


CLEAR TO OUTPUT (t_{PHL1})
t_{THL}
t_{TLH}
CLEAR PULSE SEE NOTE 1
CLOCK PULSE SEE NOTE 2
OUTPUT
t_{TLH}
t_{THL}
t_P (CLEAR)
t_{SETUP}
t_P (CLOCK)
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
V_{IH}
2.4 V
1.5 V
0.7 V
V_{IL}
V_{OH}
1.5 V
V_{OL}
t_{PHL1}

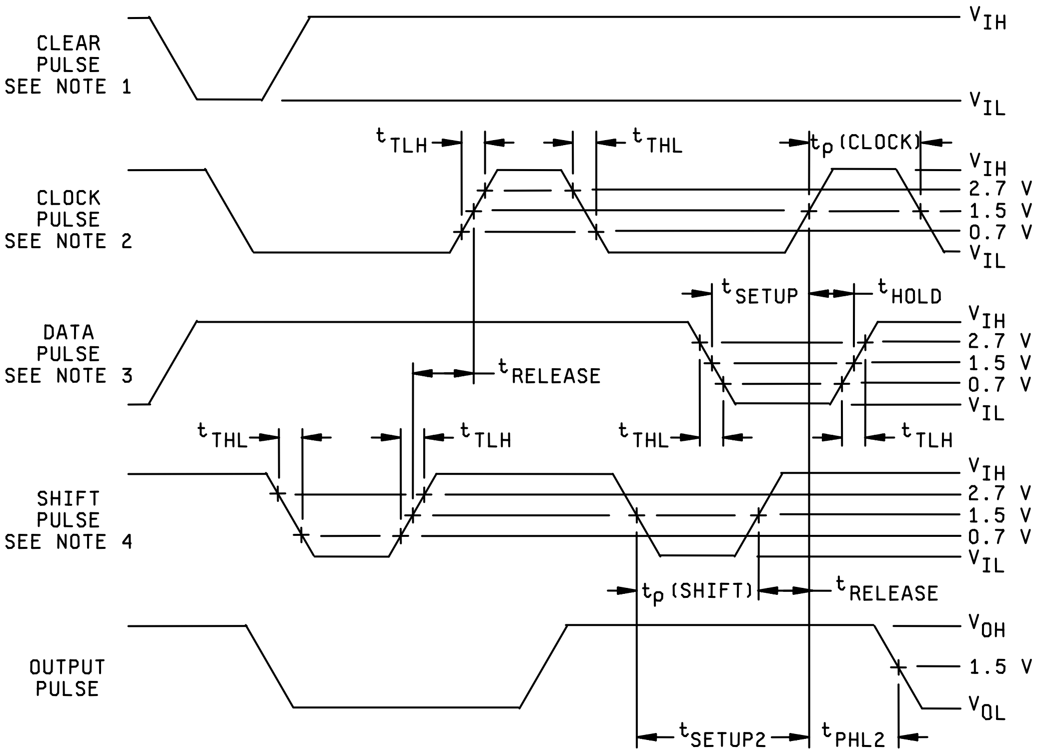
NOTES:
1. Clear pulse characteristics: $t_{P(CLEAR)}$ = 12 ns, t_{SETUP} = 25 ns, PRR = 1 MHz.
2. Clock pulse characteristics: $t_{P(CLOCK)}$ = 16 ns, PRR = 1 MHz.


CLOCK TO OUTPUT (t_{PLH2})
CLEAR PULSE SEE NOTE 1
CLOCK PULSE SEE NOTE 2
DATA PULSE SEE NOTE 3
SHIFT/LOAD PULSE SEE NOTE 4
OUTPUT
V_{IH}
V_{IL}
t_P (CLOCK)
t_{TLH}
t_{THL}
V_{IH}
2.7 V
1.5 V
0.7 V
V_{IL}
$t_{RELEASE}$
t_P (DATA)
t_{TLH}
t_{THL}
t_{SETUP1}
t_{HOLD}
t_{THL}
t_{TLH}
t_P (SHIFT)
$t_{RELEASE}$
t_{SETUP2}
V_{OH}
1.5 V
V_{OL}
t_{PLH2}

NOTES:
1. The clear pulse is a momentary GND, then V_{IH} is applied to the clear input.
2. Clock pulse characteristics: $t_{P(CLOCK)}$ = 16 ns, PRR = 2 MHz.
3. Data pulse characteristics: $t_{P(DATA)}$ = 25 ns, t_{SETUP1} = 25 ns, t_{HOLD} = 0 ns, PRR = 1 MHz.
4. Shift/Load pulse characteristics: $t_{P(SHIFT)}$ = 17 ns, $t_{RELEASE}$ = 10 ns, t_{SETUP2} = 27 ns, PRR = 2 MHz.

FIGURE 9. Switching test circuits and waveforms for device type 06 - Continued.

CLOCK TO OUTPUT (t_{PHL2})


CLEAR PULSE SEE NOTE 1
CLOCK PULSE SEE NOTE 2
DATA PULSE SEE NOTE 3
SHIFT PULSE SEE NOTE 4
OUTPUT PULSE
V_{IH}
V_{IL}
t_{TLH}
t_{THL}
t_p (CLOCK)
2.7 V
1.5 V
0.7 V
t_{SETUP}
t_{HOLD}
$t_{RELEASE}$
t_p (SHIFT)
V_{OH}
V_{OL}
t_{SETUP2}
t_{PHL2}

NOTES:
1. The clear pulse is a momentary GND, then V_{IH} is applied to the clear input.
2. Clock pulse characteristics: $t_{P(CLOCK)}$ = 16 ns, PRR = 2 MHz.
3. Data pulse characteristics: $t_{P(DATA)} = t_{SETUP} + t_{HOLD}$ = 25 ns, t_{SETUP1} = 25 ns, t_{HOLD} = 0 ns, PRR = 1 MHz.
4. Shift/load pulse characteristics: $t_{P(SHIFT)}$ = 22 ns, $t_{RELEASE}$ = 10 ns, t_{SETUP2} = 32 ns, PRR = 2 MHz.

FIGURE 9. Switching test circuits and waveforms for device type 06 - Continued.

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Min	Max	Unit
			Test No.	SI	A	B	C	D	MC	GND	CLK2	CLK1	Q_D	Q_C	Q_B	Q_A	V_{CC}				
1	V_{OH}	3006	1		2.0 V				2.0 V	GND	A 1/					-.8 mA	4.5 V	Q_A	2.4		V
T_C = 25°C	“	“	2			2.0 V			"	"	"				-.8 mA		"	Q_B	"		“
“	“	“	3				2.0 V		"	"	"			-.8 mA			"	Q_C	"		“
“	“	“	4					2.0 V	"	"	"		-.8 mA				"	Q_D	"		“
“	V_{OL}	3007	5		0.8 V				"	"	"					16 mA	"	Q_A		0.4	“
”	“	“	6			0.8 V			"	"	"				16 mA		"	Q_B		“	“
“	“	“	7				0.8 V		"	"	"			16 mA			"	Q_C		“	“
“	“	“	8					0.8 V	"	"	"		16 mA				"	Q_D		“	“
“	V_{IC}		9	-12 mA						"							"	SI		-1.5	“
“	“		10		-12 mA					"							"	A		"	“
“	“		11			-12 mA				"							"	B		"	“
“	“		12				-12 mA			"							"	C		"	“
“	"		13					-12 mA		"							"	D		"	"
“	“		14						-12 mA	"							"	MC		“	“
“	“		15							"	-12 mA						"	CLK2		“	“
“	“		16							"		-12 mA					"	CLK1		“	“
“	I_{IL1}	3009	17	0.4 V					GND	"							5.5 V	SI		2/	
“	“	“	18		0.4 V				4.5 V	"							"	A		“	
“	“	“	19			0.4 V			"	"							"	B		“	
“	“	“	20				0.4 V		"	"							"	C		“	
“	“	“	21					0.4 V	"	"							"	D		“	
“	“	“	22						"	"	0.4 V						"	CLK2		“	
“	“	“	23						GND	"		0.4 V					"	CLK1		“	
“	I_{IL2}	“	24						0.4 V	"	4.5 V						"	MC		3/	
“	I_{IH1}	3010	25	2.4 V					4.5 V	"							"	SI		40	µA
“	"	“	26		2.4 V				GND	"							"	A		"	"
“	“	“	27			2.4 V			"	"							"	B		“	“
“	“	“	28				2.4 V		"	"							"	C		“	“
“	“	“	29					2.4 V	"	"							"	D		“	“
“	“	“	30						"	"	2.4 V						"	CLK2		“	“
“	“	“	31						4.5 V	"		2.4 V					"	CLK1		“	“
“	I_{IH2}	3010	32	5.5 V					4.5 V	"							"	SI		100	"
“	"	“	33		5.5 V				GND	"							"	A		"	"
“	“	“	34			5.5 V			"	"							"	B		“	“
“	“	“	35				5.5 V		"	"							"	C		“	“
“	“	“	36					5.5 V	"	"							"	D		“	“
“	“	“	37						"	"	5.5 V						"	CLK2		“	“
“	“	“	38						4.5 V	"		5.5 V					"	CLK1		“	“

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01. - Continued
Terminal conditions (pins not designated may be H $\geq$ 2.0 V or L $\leq$ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Min	Max	Unit
			Test No.	SI	A	B	C	D	MC	GND	CLK2	CLK1	Q_D	Q_C	Q_B	Q_A	V_{CC}				
1	I_{IH3}	3010	39						2.4 V	GND	GND						5.5 V	MC		80	μA
T_C = 25°C	I_{IH4}	“	40						5.5 V	"	GND						"	MC		200	μA
“	I_{OS}	3011	41		4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	"	A					GND	"	Q_A	-18	-57	mA
“	“	“	42		"	"	"	"	"	“	"				GND		"	Q_B	"	“	“
“	“	“	43		"	"	"	"	"	“	"			GND			"	Q_C	"	“	“
"	“	“	44		"	"	"	"	"	“	"		GND				"	Q_D	"	“	“
“	I_{CCH}	3005	45		GND	GND	GND	GND	"	"	"	GND					"	V_{CC}		72	"
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = 125° C and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55° C and V_{IC} tests are omitted.																				
7	Truth	3014	46	B	B	B	B	B	A	GND	B	B	X	X	X	X	4.5 V				
T_C = 25°C	table	“	47	"	"	"	"	"	A	"	A	"	X	X	X	X	"			6/	
4/, 7/	test	“	48	"	"	"	"	"	A	"	B	"	L	L	L	L	"				
“	5/	“	49	"	"	"	"	"	B	"	"	"	"	"	"	"	"				
“	“	“	50	A	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	“	“	51	A	"	"	"	"	"	"	"	A	"	"	"	"	"				
“	"	“	52	A	"	"	"	"	"	"	"	B	"	"	"	H	"				
“	“	“	53	B	"	"	"	"	"	"	"	B	"	"	"	H	"				
“	“	“	54	B	"	"	"	"	"	"	"	A	"	"	"	H	"				
“	“	“	55	B	"	"	"	"	"	"	"	B	"	"	H	L	"				
“	“	“	56	A	"	"	"	"	"	"	"	B	"	"	H	L	"				
“	“	“	57	A	"	"	"	"	"	"	"	A	"	"	H	L	"				
“	“	“	58	A	"	"	"	"	"	"	"	B	"	H	L	H	"				
“	“	“	59	B	"	"	"	"	"	"	"	B	"	H	L	H	"				
“	“	“	60	B	"	"	"	"	"	"	"	A	"	H	L	H	"				
“	“	“	61	B	"	"	"	"	"	"	"	B	H	L	H	L	"				
“	"	"	62	A	"	"	"	"	"	"	"	B	H	L	H	L	"				
“	“	"	63	A	"	"	"	"	"	"	"	A	H	L	H	L	"				
“	“	"	64	A	"	"	"	"	"	"	"	B	L	H	L	H	"				
“	“	"	65	B	"	"	"	"	"	"	"	B	L	H	L	H	"				
“	“	"	66	"	"	"	"	"	"	"	"	A	L	H	L	H	"				
“	“	"	67	"	"	"	"	"	"	"	"	B	H	L	H	L	"				
“	“	"	68	"	"	"	"	"	"	"	"	A	H	L	H	"	"				
“	“	"	69	"	"	"	"	"	"	"	"	B	L	H	L	"	"				
“	“	"	70	"	"	"	"	"	"	"	"	A	L	H	"	"	"				
“	“	"	71	"	"	"	"	"	"	"	"	B	H	L	"	"	"				
“	“	"	72	"	"	"	"	"	"	"	"	A	H	"	"	"	"				
“	“	"	73	"	"	"	"	"	"	"	"	B	L	"	"	"	"				
“	“	"	74	"	A	"	A	"	"	"	"	B	L	"	"	"	"				

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01. - Continued

Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Min	Max	Unit
			Test No.	SI	A	B	C	D	MC	GND	CLK2	CLK1	Q_D	Q_C	Q_B	Q_A	V_{CC}				
7	Truth	3014	75	B	A	B	A	B	A	GND	B	B	L	L	L	L	4.5 V				
T_C = 25°C	table	“	76	"	A	B	A	B	"	"	A	"	"	L	"	L	"			6/	
4/, 7/	test	“	77	"	A	B	A	B	"	"	B	"	"	H	"	H	"				
“	5/	“	78	"	B	A	B	A	"	"	B	"	"	H	"	H	"				
“	“	“	79	"	B	"	B	"	"	"	A	"	"	H	"	H	"				
“	“	“	80	"	B	"	B	"	"	"	B	"	H	L	H	L	"				
“	"	“	81	"	A	"	A	"	"	"	B	"	"	L	"	L	"				
“	“	“	82	"	A	"	A	"	"	"	A	"	"	L	"	L	"				
“	“	“	83	"	A	"	A	"	"	"	B	"	"	H	"	H	"				
“	“	“	84	"	B	B	B	B	"	"	B	"	"	H	"	H	"				
“	“	“	85	"	B	B	B	B	"	"	A	"	"	H	"	H	"				
“	“	“	86	"	B	B	B	B	"	"	B	"	L	L	L	L	"				
8	Repeat subgroup 7 at T_C = +125° C and T_C = -55° C.																				
9	f_{MAX}	(Fig. 4)	87	GND					GND	GND	IN	IN	OUT				5.0 V	Q_D	11		MHz
T_C = 25°C	t_{PLH}	3003	88	"	IN				5.0 V	"	"	GND				OUT	"	Q_A	10	30	ns
“	“	(Fig. 4)	89	"		IN			"	"	"	"			OUT		"	Q_B	“	“	“
“	“	“	90	"			IN		"	"	"	"		OUT			"	Q_C	“	“	“
“	"	“	91	"				IN	"	"	"	"	OUT				"	Q_D	"	"	“
”	t_{PHL}	“	92	IN					GND	"	GND	IN				OUT	"	Q_A	“	35	“
“	“	“	93	"					"	"	"	"			OUT		"	Q_B	“	“	“
“	“	“	94	"					"	"	"	"		OUT			"	Q_C	“	“	“
”	“	“	95	"					"	"	"	"	OUT				"	Q_D	“	“	“
10	f_{MAX}	(Fig. 4)	96	GND					GND	GND	IN	IN	OUT				5.0 V	Q_D	8		MHz
T_C = 125°C	t_{PLH}	3003	97	"	IN				5.0 V	"	"	GND				OUT	"	Q_A	10	42	ns
“	“	(Fig. 4)	98	"		IN			"	"	"	"			OUT		"	Q_B	“	“	“
“	“	“	99	"			IN		"	"	"	"		OUT			"	Q_C	“	“	“
“	"	“	100	"				IN	"	"	"	"	OUT				"	Q_D	"	"	“
”	t_{PHL}	“	101	IN					GND	"	GND	IN				OUT	"	Q_A	“	49	“
“	“	“	102	"					"	"	"	"			OUT		"	Q_B	“	“	“
“	“	“	103	"					"	"	"	"		OUT			"	Q_C	“	“	“
”	“	“	104	"					"	"	"	"	OUT				"	Q_D	“	“	“
11	Same tests, terminal conditions and limits as for subgroup 10, except T_C = -55°C.																				

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V or L $\leq$ 0.8 V or open).

1/ A = normal clock pulse, except for subgroups 7 and 8 (see 4/).
2/ For device type 01, with schematics incorporating a 4 kΩ base resistor, the minimum and maximum limits shall be -0.5 and -1.4 mA, respectively. For schematics incorporating a 5 kΩ base resistor, the minimum and maximum limits shall be -0.5 and -1.4 mA, respectively. For schematics incorporating a 6 kΩ resistor, the minimum and maximum limits shall be -0.4 and -1.3 mA, respectively.
3/ For device type 01, with schematics incorporating a 4 kΩ base resistor in the mode control input circuit, the minimum and maximum limits shall be -1.4 and -3.2 mA, respectively. For schematics incorporating a 5 kΩ base resistor, the minimum and maximum limits shall be -1.0 and -2.8 mA, respectively. For schematics incorporating a 6 kΩ resistor in the mode control input circuit, the minimum and maximum limits shall be -0.8 and -2.6 mA, respectively.
4/ For subgroups 7 and 8, A = V_{CC}, B = GND, and X = indeterminate.
5/ The tests in subgroups 7 and 8 shall be performed in the sequence specified.
6/ Output voltages shall be either:
  (a) H = 2.4 V minimum and L = 0.4 V maximum when using a high speed checker double comparator or
  (b) H > 1.5 V and L < 1.5 V when using a high speed checker single comparator.
7/ Only a summary of attribute data is required.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V or L $\leq$ 0.8 V or open).

Subgroup	Symbol	MIL-	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
		STD-883 method	Test No.	CLK	P_A	P_B	P_C	V_{CC}	P_D	P_E	P EN	SI	Q_E	Q_D	GND	Q_C	Q_B	Q_A	CLR		Min	Max	Unit
1	V_{OH}	3006	1		2.0 V	2.0 V	2.0 V	4.5 V	2.0 V	2.0 V	2.0 V				GND			-.4 mA	2.0 V	Q_A	2.4		V
T_C = 25°C	“	“	2		"	"	"	"	"	"	"				"		-.4 mA		"	Q_B	"		“
“	“	“	3		"	"	"	"	"	"	"				"	-.4 mA			"	Q_C	"		“
“	“	“	4		"	"	"	"	"	"	"			-.4 mA	"				"	Q_D	"		“
“	“	“	5		"	"	"	"	"	"	"		-.4 mA		"				"	Q_E	"		“
"	V_{OL}	3007	6					"			0.8 V				"			16 mA	0.8 V	Q_A		0.4	“
“	“	“	7					"			"				"		16 mA		"	Q_B		“	“
“	“	“	8					"			"				"	16 mA			"	Q_C		“	“
“	“	“	9					"			"			16 mA	"				"	Q_D		“	“
“	"	"	10					"			"		16 mA		"				"	Q_E		"	“
“	V_{IC}	“	11	-12 mA				"							"					CLK		-1.5	“
“	“	“	12		-12 mA			"							"					P_A		"	“
“	“	“	13			-12 mA		"							"					P_B		"	“
“	“	“	14				-12 mA	"							"					P_C		"	“
“	"	"	15					"	-12 mA						"					P_D		"	"
“	"	"	16					"		-12 mA					"					P_E		"	"
“	"	"	17					"			-12 mA				"					P EN		"	"
“	“	“	18					"				-12 mA			"					SI		"	“
“	“	“	19					"							"				-12 mA	CLR		"	“
“	I_{IL1}	3009	20	0.4 V				5.5 V							"					CLK	-0.7	-1.6	mA
“	“	“	21		0.4 V			"			4.5 V				"					P_A	"	“	“
“	“	“	22			0.4 V		"			"				"					P_B	"	“	“
“	“	“	23				0.4 V	"			"				"					P_C	"	“	“
“	“	“	24					"	0.4 V		"				"					P_D	"	"	“
“	“	“	25					"		0.4 V	"				"					P_E	"	"	“
“	“	“	26					"				0.4 V			"					SI	"	"	“
“	"		27					"							"				0.4 V	CLR	"	"	“
“	I_{IL1}	“	28		4.5 V	4.5 V	4.5 V	"	4.5 V	4.5 V	0.4 V				"					P EN	-3.0	-8.0	“
“	I_{IH1}	3010	29	2.4 V				"							"					CLK		40	µA
“	“	“	30		2.4 V			"			GND				"					P_A		"	“
“	“	“	31			2.4 V		"			"				"					P_B		“	“
“	“	“	32				2.4 V	"			"				"					P_C		“	“
“	“	“	33					"	2.4 V		"				"					P_D		“	“
“	“	“	34					"		2.4 V	"				"					P_E		"	“
“	“	“	35					"				2.4 V			"					SI		"	“
“	“	“	36					"							"				2.4 V	CLR		"	“

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.

Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLK	P_A	P_B	P_C	V_{CC}	P_D	P_E	P EN	SI	Q_E	Q_D	GND	Q_C	Q_B	Q_A	CLR		Min	Max	Unit
1	I_{IH2}	3010	37	5.5 V				5.5 V							GND					CLK		100	μA
T_C = 25°C	“	“	38		5.5 V			"			GND				"					P_A		"	“
“	“	“	39			5.5 V		"			"				"					P_B		“	“
“	“	“	40				5.5 V	"			"				"					P_C		“	“
“	“	“	41					"	5.5 V		"				"					P_D		“	“
“	“	“	42					"		5.5 V	"				"					P_E		"	“
“	“	“	43					"				5.5 V			"					SI		"	“
“	“	“	44					"							"				5.5 V	CLR		"	“
"	I_{IH3}	"	45		GND	GND	GND	"	GND	GND	2.4 V				"					P EN		200	"
"	I_{IH4}	“	46		GND	GND	GND	"	GND	GND	5.5 V				"					P EN		500	“
”	I_{OS}	3011	47		4.5 V	4.5 V	4.5 V	"	4.5 V	4.5 V	4.5 V				"			GND	4.5 V	Q_A	-20	-57	mA
“	“	“	48		"	"	"	"	"	"	"				"		GND		"	Q_B	"	“	“
“	“	“	49		"	"	"	"	"	"	"				"	GND			"	Q_C	"	“	“
“	“	“	50		"	"	"	"	"	"	"			GND	"				"	Q_D	"	“	“
“	"	"	51		"	"	"	"	"	"	"		GND		"				"	Q_E	"	"	“
“	I_{CCH}	3005	52	4.5 V	"	"	"	"	"	"	"	GND			"				5.5 V	V_{CC}		68	“
“	I_{CCL}	3005	53	GND	"	"	"	"	"	"	GND	GND			"				GND	V_{CC}		68	“
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = +125° C and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55° C and V_{IC} tests are omitted.																						
7	Truth	3014	54	B	B	B	B	4.5 V	B	B	B	B	L	L	GND	L	L	L	B			2/	
T_C = 25°C	table	“	55	"	A	B	B	"	"	"	A	A	"	"	"	L	L	H	"				
1/, 4/	test	"	56	"	B	A	B	"	"	"	"	"	"	"	"	L	H	L	"				
“	3/	"	57	"	"	B	A	"	"	"	"	"	"	"	"	H	L	"	"				
“	"	"	58	"	"	"	B	"	A	"	"	"	"	H	"	L	"	"	"				
“	“	“	59	"	"	"	B	"	B	A	"	"	H	L	"	"	"	"	"				
“	“	“	60	"	"	"	B	"	B	"	B	"	L	L	"	"	"	"	"				
“	"	"	61	"	A	A	A	"	A	"	B	B	L	L	"	"	"	"	A				
“	“	“	62	"	"	"	"	"	"	"	A	A	H	H	"	H	H	H	B				
“	“	“	63	"	"	"	"	"	"	B	B	A	L	L	"	L	L	L	B				
“	“	“	64	"	"	"	"	"	"	"	B	B	"	L	"	L	L	L	A				
“	“	“	65	"	"	"	"	"	"	"	A	B	"	H	"	H	H	H	A				
“	“	“	66	"	"	"	"	"	"	"	B	A	"	H	"	H	H	H	A				
“	“	“	67	"	"	"	"	"	B	"	B	A	"	L	"	L	L	L	B				
“	"	"	68	"	"	"	"	"	B	"	B	B	"	L	"	L	L	L	A				

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLK	P_A	P_B	P_C	V_{CC}	P_D	P_E	P EN	SI	Q_E	Q_D	GND	Q_C	Q_B	Q_A	CLR		Min	Max	Unit
7	Truth	3014	69	B	A	A	A	4.5 V	B	B	A	B	L	L	GND	H	H	H	A				
T_C = 25°C	table	“	70	"	"	"	A	"	"	"	B	A	"	"	"	H	H	H	A				
1/, 4/	test	"	71	"	"	"	B	"	"	"	B	A	"	"	"	L	L	L	B				
“	3/	"	72	"	"	"	"	"	"	"	B	B	"	"	"	"	L	L	A				
“	"	"	73	"	"	"	"	"	"	"	A	B	"	"	"	"	H	H	A				
“	“	“	74	"	"	"	"	"	"	"	B	A	"	"	"	"	H	H	A				
“	“	“	75	"	"	B	"	"	"	"	B	A	"	"	"	"	L	L	B			2/	
“	"	"	76	"	"	"	"	"	"	"	B	B	"	"	"	"	"	L	A				
“	“	“	77	"	"	"	"	"	"	"	A	B	"	"	"	"	"	H	A				
“	“	“	78	"	"	"	"	"	"	"	B	A	"	"	"	"	"	H	A				
“	“	“	79	"	"	"	"	"	"	"	"	"	"	"	"	"	"	L	B				
“	“	“	80	"	"	"	"	"	"	"	"	"	"	"	"	"	"	L	A				
“	“	“	81	A	"	"	"	"	"	"	"	"	"	"	"	"	"	H	"				
“	“	“	82	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	"	83	A	"	"	"	"	"	"	"	"	"	"	"	"	H	"	"				
"	"	"	84	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	85	A	"	"	"	"	"	"	"	"	"	"	"	H	"	"	"				
"	"	"	86	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	“	"	87	A	"	"	"	"	"	"	"	"	"	H	"	"	"	"	"				
“	"	"	88	B	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	“	“	89	A	"	"	"	"	"	"	"	"	H	"	"	"	"	"	"				
“	“	“	90	B	"	A	"	"	"	"	A	B	"	"	"	"	"	"	"				
“	“	"	91	A	"	A	"	"	"	"	"	"	"	"	"	"	"	L	"				
“	“	“	92	B	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	“	“	93	A	"	"	"	"	"	"	"	"	"	"	"	"	L	"	"				
“	“	“	94	B	"	"	"	"	A	"	"	"	"	"	"	"	"	"	"				
“	“	“	95	A	"	"	"	"	A	"	"	"	"	"	"	L	"	"	"				
“	“	“	96	B	"	"	"	"	B	A	"	"	"	"	"	"	"	"	"				
“	“	“	97	A	"	"	"	"	"	A	"	"	"	L	"	"	"	"	"				
“	“	“	98	B	"	"	"	"	"	B	B	"	"	"	"	"	"	"	"				
“	“	“	99	A	A	"	"	"	"	"	"	"	L	"	"	"	"	"	"				
“	“	“	100	B	"	"	"	"	"	"	"	A	"	"	"	"	"	"	"				
“	“	“	101	A	"	"	"	"	"	"	"	A	"	"	"	"	"	H	"				
“	“	“	102	B	"	"	"	"	"	"	A	B	"	"	"	"	"	"	"				
“	"	"	103	A	"	"	"	"	"	"	A	B	"	"	"	"	H	"	"				

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H > 2.0 V or L < 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLK	P_A	P_B	P_C	V_{CC}	P_D	P_E	P EN	SI	Q_E	Q_D	GND	Q_C	Q_B	Q_A	CLR		Min	Max	Unit
7	Truth	3014	104	B	B	A	B	4.5 V	B	B	A	B	L	L	GND	L	H	H	A				
T_C = 25°C	table	“	105	A	"	A	"	"	"	"	"	"	"	"	"	H	"	L	"				
1/, 4/	test	"	106	B	"	B	A	"	"	"	"	"	"	"	"	"	"	"	"				
“	3/	"	107	A	"	"	A	"	"	"	"	"	"	H	"	"	L	"	"				
“	"	"	108	B	"	"	B	"	A	"	"	"	"	"	"	"	"	"	"				
“	“	“	109	A	"	"	"	"	A	"	"	"	H	"	"	L	"	"	"				
“	“	“	110	B	"	"	"	"	B	A	"	"	"	"	"	"	"	"	"			2/	
“	"	"	111	A	"	"	"	"	"	A	"	"	"	L	"	"	"	"	"				
“	“	“	112	B	"	"	"	"	"	B	B	"	"	L	"	"	"	"	"				
“	“	“	113	A	"	"	"	"	"	"	B	"	L	L	"	"	"	"	"				
“	“	“	114	B	"	A	"	"	A	"	A	A	L	H	"	"	H	"	"				
“	“	“	115	A	"	A	"	"	A	"	"	"	H	H	"	H	H	H	"				
“	“	“	116	B	A	B	A	"	B	A	"	"	"	H	"	"	H	"	"				
“	“	“	117	A	"	"	"	"	"	"	"	"	"	L	"	"	L	"	B				
“	"	"	118	B	"	"	"	"	"	"	"	B	"	L	"	"	L	"	A				
"	"	"	119	A	"	"	"	"	"	"	"	"	"	H	"	"	H	"	"				
"	"	“	120	B	"	A	"	"	A	"	"	"	"	H	"	"	H	"	"				
"	"	"	121	A	"	"	"	"	"	"	"	"	"	H	"	"	H	"	"				
“	"	"	122	B	"	"	"	"	"	"	B	A	L	L	"	L	L	L	B				
“	"	"	123	A	"	"	"	"	"	"	B	A	L	L	"	L	L	L	B				
8	Repeat subgroup 7 at T_C = +125° C and T_C = -55° C.																						
9	f_{MAX}	(Fig 5)	124	IN				5.0 V			GND	IN	OUT		GND				4.5 V	Q_E	5		MHz
T_C = 25°C	t_{PLH1}	3003	125	"				"			“	"			"			OUT	“	Q_A	8	40	ns
“	“	(Fig 5)	126	"				"			“	"			"		OUT		“	Q_B	“	“	“
“	“	“	127	"				"			“	"			"	OUT			“	Q_C	“	“	“
“	“	“	128	"				"			“	"		OUT	"				“	Q_D	“	“	“
”	“	“	129	"				"			“	"	OUT		"				“	Q_E	“	“	“
"	t_{PHL1}	"	130	"				"			“	"			"			OUT	“	Q_A	"	"	"
“	“	“	131	"				"			“	"			"		OUT		“	Q_B	“	“	“
“	“	“	132	"				"			“	"			"	OUT			“	Q_C	“	“	“
“	“	“	133	"				"			“	"		OUT	"				“	Q_D	“	“	“
”	“	“	134	"				"			“	"	OUT		"				“	Q_E	“	“	“

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLK	P_A	P_B	P_C	V_{CC}	P_D	P_E	P EN	SI	Q_E	Q_D	GND	Q_C	Q_B	Q_A	CLR		Min	Max	Unit
9	t_{PLH2}	3003	135	GND	4.5 V	4.5 V	4.5 V	5.0 V	4.5 V	4.5 V	IN				GND			OUT	IN	Q_A	8	42	ns
T_C = 25°C	“	(Fig 5)	136	"				"			“				"		OUT		“	Q_B	“	“	“
“	“	“	137	"				"			“				"	OUT			“	Q_C	“	“	“
“	“	“	138	"				"			“			OUT	"				“	Q_D	“	“	“
”	“	“	139	"				"			“		OUT		"				“	Q_E	“	“	“
"	t_{PHL3}	"	140	"				"			“				"			OUT	“	Q_A	"	55	ns
“	“	“	141	"				"			“				"		OUT		“	Q_B	“	“	“
“	“	“	142	"				"			“				"	OUT			“	Q_C	“	“	“
“	“	“	143	"				"			“			OUT	"				“	Q_D	“	“	“
”	“	“	144	"				"			“		OUT		"				“	Q_E	“	“	“
10	f_{MAX}	(Fig 5)	145	IN				"			GND	IN	OUT		"				4.5 V	Q_E	3.5		MHz
T_C = 125°C	t_{PLH1}	3003	146	"				"			“	"			"			OUT	“	Q_A	8	56	ns
“	“	(Fig 5)	147	"				"			“	"			"		OUT		“	Q_B	“	“	“
“	“	“	148	"				"			“	"			"	OUT			“	Q_C	“	“	“
“	“	“	149	"				"			“	"		OUT	"				“	Q_D	“	“	“
”	“	“	150	"				"			“	"	OUT		"				“	Q_E	“	“	“
"	t_{PHL1}	"	151	"				"			“	"			"			OUT	“	Q_A	"	"	"
“	“	“	152	"				"			“	"			"		OUT		“	Q_B	“	“	“
“	“	“	153	"				"			“	"			"	OUT			“	Q_C	“	“	“
“	“	“	154	"				"			“	"		OUT	"				“	Q_D	“	“	“
”	“	“	155	"				"			“	"	OUT		"				“	Q_E	“	“	“
"	t_{PLH2}	"	156	GND	4.5 V	4.5 V	4.5 V	"	4.5 V	4.5 V	IN	"			"			OUT	IN	Q_A	8	59	"
“	“	"	157	"				"			“	"			"		OUT		“	Q_B	“	“	“
“	“	“	158	"				"			“	"			"	OUT			“	Q_C	“	“	“
“	“	“	159	"				"			“	"		OUT	"				“	Q_D	“	“	“
”	“	“	160	"				"			“	"	OUT		"				“	Q_E	“	“	“
"	t_{PHL3}	"	161	"				"			“	"			"			OUT	“	Q_A	"	77	"
“	“	“	162	"				"			“	"			"		OUT		“	Q_B	“	“	“
“	“	“	163	"				"			“	"			"	OUT			“	Q_C	“	“	“
“	“	“	164	"				"			“	"		OUT	"				“	Q_D	“	“	“
”	“	“	165	"				"			“	"	OUT		"				“	Q_E	“	“	“
11	Same tests, terminal conditions and limits as for subgroup 10, except T_C = -55°C.																						

1/ For subgroups 7 and 8, A = V_{CC} and B = GND.

2/ Output voltages shall be either: (a) H = 2.4 V minimum and L = 0.4 V maximum when using a high speed checker double comparator, or
(b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.

3/ The tests in subgroups 7 and 8 shall be performed in the sequence specified.

4/ Only a summary of attributes data is required.

TABLE III. Group A inspection for device type 03.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A, B, C, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Test No.	SI_A	SI_B	Q_A	Q_B	Q_C	Q_D	GND	CLK	CLR	Q_E	Q_F	Q_G	Q_H	V_{CC}		Min	Max	Unit
1	V_{OH}	3006	1	2.0 V	2.0 V	-0.4 mA				GND	A 1/	4.5 V					4.5 V	Q_A	2.4		V
T_C = 25°C	“	“	2	"	"		-0.4mA			“	"	"					“	Q_B	"		“
“	“	“	3	"	"			-0.4 mA		“	"	"					“	Q_C	"		“
“	“	“	4	"	"				-0.4 mA	“	"	"					“	Q_D	"		“
“	“	“	5	"	"					“	"	"	-0.4 mA				“	Q_E	"		“
”	“	“	6	"	"					“	"	"		-0.4 mA			“	Q_F	"		“
“	“	“	7	"	"					“	"	"			-0.4 mA		“	Q_G	"		“
“	“	“	8	"	"					“	"	"				-0.4 mA	“	Q_H	"		“
“	V_{OL}	3007	9	0.8 V	0.8 V	8 mA				“	"	"					“	Q_A		0.4	“
“	“	“	10	"	"		8 mA			“	"	"					“	Q_B		"	“
“	“	“	11	"	"			8 mA		“	"	"					“	Q_C		"	“
“	“	“	12	"	"				8 mA	“	"	"					“	Q_D		"	“
“	"	"	13	"	"					“	"	"	8 mA				"	Q_E		"	"
“	“	“	14	"	"					“	"	"		8 mA			“	Q_F		"	"
“	"	"	15	"	"					“	"	"			8 mA		“	Q_G		"	"
“	“	“	16	"	"					“	"	"				8 mA	“	Q_H		"	“
“	V_{IC}		17	-12 mA						“							“	SI_A		-1.5	“
“	“		18		-12 mA					“							“	SI_B		"	“
“	“		19							“	-12 mA						“	CLK		"	“
“	“		20							“		-12 mA					“	CLR		"	“
“	I_{IL1}	3009	21	0.4 V	5.5 V					“							5.5 V	SI_A		7/	
“	“	“	22	5.5 V	0.4 V					“							“	SI_B			
“	“	“	23							“	0.4 V						“	CLK			
“	I_{IL2}	“	24							“		0.4 V					“	CLR		8/	
“	I_{IH1}	3010	25	2.4 V	GND					“							“	SI_A		40	µA
“	“	“	26	GND	2.4 V					“							“	SI_B		"	"
“	“	“	27							“	2.4 V						“	CLK		"	“
“	I_{IH2}	"	28	5.5 V	GND					“							“	SI_A		100	"
“	“	“	29	GND	5.5 V					“							“	SI_B		"	"
“	“	“	30							“	5.5 V						“	CLK		"	“
“	I_{IH3}	“	31							“		2.4 V					“	CLR		9/	“
“	I_{IH4}	“	32							“		5.5 V					“	CLR		10/	“

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V or L $\leq$ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A, B, C, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Test No.	SI_A	SI_B	Q_A	Q_B	Q_C	Q_D	GND	CLK	CLR	Q_E	Q_F	Q_G	Q_H	V_{CC}		Min	Max	Unit
1	I_{OS}	3011	33	4.5 V	4.5 V	GND				GND	A	4.5 V					5.5 V	Q_A	-10	-27.5	mA
T_C = 25°C	“	“	34	"	"		GND			“	"	"					“	Q_B	"	"	“
“	“	“	35	"	"			GND		“	"	"					“	Q_C	"	"	“
“	“	“	36	"	"				GND	“	"	"					“	Q_D	"	"	“
“	“	“	37	"	"					“	"	"	GND				“	Q_E	"	"	“
”	“	“	38	"	"					“	"	"		GND			“	Q_F	"	"	“
“	“	“	39	"	"					“	"	"			GND		“	Q_G	"	"	“
’‘	“	“	40	"	"					“	"	"				GND	“	Q_H	"	"	“
“	I_{CC1}	3005	41	GND	GND					“	0.4 V	B 2/					“	V_{CC}		44	“
“	I_{CC2}	3005	42	GND	GND					“	2.4 V	B					“	V_{CC}		54	“
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = +125° C and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55° C and V_{IC} tests are omitted.																				
7	Truth	3014	43	A	A	L	L	L	L	GND	A	B	L	L	L	L	4.5 V				
T_C = 25°C	table	“	44	“	“	L	“	“	“	“	A	A	“	“	“	“	“				
3/ 6/	test	"	45	“	“	L	“	“	“	“	B	“	“	“	“	“	"				
“	5/	“	46	“	“	H	“	“	“	“	A	“	“	“	“	“	“			4/	
“	"	"	47	“	“	“	“	“	“	“	B	“	“	“	“	“	“				
“	“	“	48	“	“	“	H	“	“	“	A	“	“	“	“	“	“				
“	"	"	49	“	“	“	“	“	“	“	B	“	“	“	“	“	“				
“	“	"	50	“	“	“	“	H	"	“	A	“	“	“	“	“	“				
“	“	"	51	“	“	“	“	“	"	“	B	“	“	“	“	“	“				
“	“	“	52	“	“	“	“	“	H	“	A	“	“	“	“	“	“				
“	"	"	53	“	“	“	“	“	“	“	B	“	“	“	“	“	"				
“	“	“	54	“	“	“	“	“	“	“	A	“	H	“	“	“	“				
“	“	“	55	“	“	“	“	“	“	“	B	“	“	“	“	“	“				
“	"	“	56	“	“	“	“	“	“	“	A	“	“	H	"	"	“				
“	"	"	57	“	“	“	“	“	“	“	B	“	“	“	"	"	“				
“	“	“	58	“	“	“	“	“	“	“	A	“	“	“	H	"	“				
“	“	“	59	“	“	“	“	“	“	“	B	“	“	“	“	"	“				
“	"	"	60	“	“	“	“	“	“	“	A	“	“	“	“	H	“				
“	“	“	61	B	“	“	“	“	“	“	A	“	“	“	“	"	“				
“	“	“	62	“	“	“	“	“	“	“	B	“	“	“	“	"	“				
“	"	“	63	“	“	L	“	“	“	“	A	“	“	“	“	"	“				
“	"	“	64	“	“	L	“	“	“	“	B	“	“	“	“	"	“				

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H > 2.0 V or L < 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A, B, C, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Test No.	SI_A	SI_B	Q_A	Q_B	Q_C	Q_D	GND	CLK	CLR	Q_E	Q_F	Q_G	Q_H	V_{CC}		Min	Max	Unit
7	Truth	3014	65	B	A	L	L	H	H	GND	A	A	H	H	H	H	4.5 V				
T_C = 25°C	table	"	66	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
3/ 6/	test	"	67	"	"	"	"	L	"	"	A	"	"	"	"	"	"				
"	5/	"	68	"	"	"	"	"	"	"	B	"	"	"	"	"	"			4/	
"	"	"	69	"	"	"	"	"	L	"	A	"	"	"	"	"	"				
"	"	"	70	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	71	"	"	"	"	"	"	"	A	"	L	"	"	"	"				
"	"	"	72	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	73	"	"	"	"	"	"	"	A	"	"	L	"	"	"				
"	"	"	74	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	75	"	"	"	"	"	"	"	A	"	"	"	L	"	"				
"	"	"	76	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	77	"	"	"	"	"	"	"	A	"	"	"	"	L	"				
"	"	"	78	A	"	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	79	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	80	"	"	H	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	81	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	82	"	"	"	H	"	"	"	A	"	"	"	"	"	"				
"	"	"	83	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	84	"	"	"	"	H	"	"	A	"	"	"	"	"	"				
"	"	"	85	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	86	"	"	"	"	"	H	"	A	"	"	"	"	"	"				
"	"	"	87	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	88	"	"	"	"	"	"	"	A	"	H	"	"	"	"				
"	"	"	89	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	90	"	"	"	"	"	"	"	A	"	"	H	"	"	"				
"	"	"	91	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	92	"	"	"	"	"	"	"	A	"	"	"	H	"	"				
"	"	"	93	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	94	"	"	"	"	"	"	"	A	"	"	"	"	H	"				
"	"	"	95	"	B	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	96	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	97	"	"	L	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	98	"	"	L	"	"	"	"	B	"	"	"	"	"	"				

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V or L $\leq$ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A, B, C, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Test No.	SI_A	SI_B	Q_A	Q_B	Q_C	Q_D	GND	CLK	CLR	Q_E	Q_F	Q_G	Q_H	V_{CC}		Min	Max	Unit
7	Truth	3014	99	A	B	L	L	H	H	GND	A	A	H	H	H	H	4.5 V				
T_C = 25°C	table	"	100	"	"	"	"	H	"	"	B	"	"	"	"	"	"				
3/ 6/	test	"	101	"	"	"	"	L	"	"	A	"	"	"	"	"	"				
"	5/	"	102	"	"	"	"	"	"	"	B	"	"	"	"	"	"			4/	
"	"	"	103	"	"	"	"	"	L	"	A	"	"	"	"	"	"				
"	"	"	104	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	105	"	"	"	"	"	"	"	A	"	L	"	"	"	"				
"	"	"	106	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	107	"	"	"	"	"	"	"	A	"	"	L	"	"	"				
"	"	"	108	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	109	"	"	"	"	"	"	"	A	"	"	"	L	"	"				
"	"	"	110	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	111	"	"	"	"	"	"	"	A	"	"	"	"	L	"				
"	"	"	112	"	A	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	113	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	114	"	"	H	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	115	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	116	"	"	"	H	"	"	"	A	"	"	"	"	"	"				
"	"	"	117	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	118	"	"	"	"	H	"	"	A	"	"	"	"	"	"				
"	"	"	119	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	120	"	"	"	"	"	H	"	A	"	"	"	"	"	"				
"	"	"	121	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	122	"	"	"	"	"	"	"	A	"	H	"	"	"	"				
"	"	"	123	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	124	"	"	"	"	"	"	"	A	"	"	H	"	"	"				
"	"	"	125	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	126	"	"	"	"	"	"	"	A	"	"	"	H	"	"				
"	"	"	127	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	128	"	"	"	"	"	"	"	A	"	"	"	"	H	"				
"	"	"	129	B	B	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	130	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	131	"	"	L	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	132	"	"	L	"	"	"	"	B	"	"	"	"	"	"				

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V or L $\leq$ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A, B, C, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Test No.	SI_A	SI_B	Q_A	Q_B	Q_C	Q_D	GND	CLK	CLR	Q_E	Q_F	Q_G	Q_H	V_{CC}		Min	Max	Unit
7	Truth	3014	133	B	B	L	L	H	H	GND	A	A	H	H	H	H	4.5 V				
T_C = 25°C	table	“	134	“	“	“	“	H	“	“	B	“	“	“	“	“	“				
3/ 6/	test	"	135	“	“	“	“	L	“	“	A	“	“	“	“	“	"				
“	5/	“	136	“	“	“	“	“	“	“	B	“	“	“	“	“	“			4/	
“	"	"	137	“	“	“	“	“	L	“	A	“	“	“	“	“	“				
“	“	“	138	“	“	“	“	“	“	“	B	“	“	“	“	“	“				
“	"	"	139	“	“	“	“	“	“	“	A	“	L	“	“	“	“				
“	“	"	140	“	“	“	“	“	“	“	B	“	“	“	“	“	“				
“	“	"	141	“	“	“	“	“	“	“	A	“	“	L	“	“	“				
“	“	"	142	“	“	“	“	“	“	“	B	“	“	“	“	“	“				
“	"	"	143	“	“	“	“	“	“	“	A	“	“	“	L	"	"				
“	“	“	144	“	“	“	“	“	“	“	B	“	“	“	“	"	“				
“	“	“	145	“	“	“	“	“	“	“	A	“	“	“	“	L	“				
“	"	“	146	A	A	"	“	“	“	“	A	“	“	“	“	“	“				
“	"	"	147	“	“	"	“	“	“	“	B	“	“	“	“	“	“				
“	“	“	148	“	“	H	“	“	“	“	A	“	“	“	“	“	“				
“	“	“	149	“	“	“	“	“	“	“	B	“	“	“	“	“	“				
“	"	"	150	“	“	“	H	“	“	“	A	“	“	“	“	“	“				
“	“	“	151	“	“	“	“	“	“	“	B	“	“	“	“	“	“				
“	“	“	152	“	“	“	“	H	“	“	A	“	“	“	“	“	“				
“	"	“	153	“	“	“	“	“	“	“	B	“	“	“	“	“	“				
“	“	"	154	“	“	“	“	“	H	“	A	“	“	“	“	“	“				
“	"	"	155	“	“	“	“	“	“	“	B	“	“	“	“	“	"				
“	“	“	156	“	“	“	“	“	“	“	A	“	H	“	“	“	“				
“	“	“	157	“	“	“	“	“	“	“	B	“	“	“	“	“	“				
“	"	“	158	“	“	“	“	“	“	“	A	“	“	H	“	“	“				
“	"	"	159	“	“	“	“	“	“	“	B	“	“	“	“	“	“				
“	“	“	160	“	“	“	“	“	“	“	A	“	“	“	H	“	“				
“	“	“	161	“	“	“	“	“	“	“	B	“	“	“	“	“	“				
“	"	"	162	“	“	“	“	“	“	“	A	“	“	“	“	H	“				
“	“	“	163	"	"	L	L	L	L	“	A	B	L	L	L	L	“				
8	Repeat subgroup 7 at T_C = +125° C and T_C = -55° C.																				

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V or L $\leq$ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A, B, C, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Test No.	SI_A	SI_B	Q_A	Q_B	Q_C	Q_D	GND	CLK	CLR	Q_E	Q_F	Q_G	Q_H	V_{CC}		Min	Max	Unit
9	f_{MAX}	(Fig 6)	164	IN	IN					GND	IN	4.5 V				OUT	5.0 V	Q_H	11		MHz
T_C = 25°C	t_{PHL1}	3003	165			OUT				“	GND	IN					“	Q_A	12	49	ns
“	“	(Fig 6)	166				OUT			“	"	"					“	Q_B	"	"	“
“	“	“	167					OUT		“	"	"					“	Q_C	"	"	“
“	“	“	168						OUT	“	"	"					“	Q_D	"	"	“
”	“	“	169							“	"	"	OUT				“	Q_E	"	"	“
“	“	“	170							“	"	"		OUT			“	Q_F	"	"	“
“	“	“	171							“	"	"			OUT		“	Q_G	"	"	“
“	“	“	172							“	"	"				OUT	“	Q_H	"	"	“
"	t_{PLH2}	"	173	IN	IN	OUT				“	IN	4.5 V					“	Q_A	10	30	"
“	“	"	174	"	"		OUT			“	"	"					“	Q_B	"	"	“
“	“	“	175	"	"			OUT		“	"	"					“	Q_C	"	"	“
“	“	“	176	"	"				OUT	“	"	"					“	Q_D	"	"	“
”	“	“	177	"	"					“	"	"	OUT				“	Q_E	"	"	“
“	“	“	178	"	"					“	"	"		OUT			“	Q_F	"	"	“
“	“	“	179	"	"					“	"	"			OUT		“	Q_G	"	"	“
“	“	“	180	"	"					“	"	"				OUT	“	Q_H	"	"	“
"	t_{PHL2}	"	181	"	"	OUT				“	"	"					“	Q_A	"	37	"
“	“	"	182	"	"		OUT			“	"	"					“	Q_B	"	"	“
“	“	“	183	"	"			OUT		“	"	"					“	Q_C	"	"	“
“	“	“	184	"	"				OUT	“	"	"					“	Q_D	"	"	“
”	“	“	185	"	"					“	"	"	OUT				“	Q_E	"	"	“
“	“	“	186	"	"					“	"	"		OUT			“	Q_F	"	"	“
“	“	“	187	"	"					“	"	"			OUT		“	Q_G	"	"	“
“	“	“	188	"	"					“	"	"				OUT	“	Q_H	"	"	“
10	f_{MAX}	(Fig 6)	189	IN	IN					"	"	"				OUT	"	Q_H	9		MHz
T_C = 125°C	t_{PHL1}	3003	190			OUT				“	GND	IN					“	Q_A	12	63	ns
“	“	(Fig 6)	191				OUT			“	"	"					“	Q_B	"	"	“
“	“	“	192					OUT		“	"	"					“	Q_C	"	"	“
“	“	“	193						OUT	“	"	"					“	Q_D	"	"	“
”	“	“	194							“	"	"	OUT				“	Q_E	"	"	“
“	“	“	195							“	"	"		OUT			“	Q_F	"	"	“
“	“	“	196							“	"	"			OUT		“	Q_G	"	"	“
“	“	“	197							“	"	"				OUT	“	Q_H	"	"	“

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V or L $\leq$ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A, B, C, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Test No.	SI_A	SI_B	Q_A	Q_B	Q_C	Q_D	GND	CLK	CLR	Q_E	Q_F	Q_G	Q_H	V_{CC}		Min	Max	Unit
10	t_{PLH2}	3003	198	IN	IN	OUT				GND	IN	4.5 V					5.0 V	Q_A	10	42	ns
T_C = 125°C	"	(Fig 6)	199	"	"		OUT			"	"	"					"	Q_B	"	"	"
"	"	"	200	"	"			OUT		"	"	"					"	Q_C	"	"	"
"	"	"	201	"	"				OUT	"	"	"					"	Q_D	"	"	"
"	"	"	202	"	"					"	"	"	OUT				"	Q_E	"	"	"
"	"	"	203	"	"					"	"	"		OUT			"	Q_F	"	"	"
"	"	"	204	"	"					"	"	"			OUT		"	Q_G	"	"	"
"	"	"	205	"	"					"	"	"				OUT	"	Q_H	"	"	"
"	t_{PHL2}	"	206	"	"	OUT				"	"	"					"	Q_A	"	52	"
"	"	"	207	"	"		OUT			"	"	"					"	Q_B	"	"	"
"	"	"	208	"	"			OUT		"	"	"					"	Q_C	"	"	"
"	"	"	209	"	"				OUT	"	"	"					"	Q_D	"	"	"
"	"	"	210	"	"					"	"	"	OUT				"	Q_E	"	"	"
"	"	"	211	"	"					"	"	"		OUT			"	Q_F	"	"	"
"	"	"	212	"	"					"	"	"			OUT		"	Q_G	"	"	"
"	"	"	213	"	"					"	"	"				OUT	"	Q_H	"	"	"
11	Same tests, terminal conditions and limits as for subgroup 10, except T_C = -55° C.																				

1/ A = normal clock pulse, except for subgroups 7 and 8 (see 3/).
2/ B = momentary GND, then 4.5 V to clear register prior to test, except for subgroups 7 and 8 (see 3/).
3/ For subgroups 7 and 8, A = V_{CC} and B = GND.
4/ Output voltages shall be either:
(a) H = 2.4 V minimum and L = 0.4 V maximum when using a high speed checker double comparator, or
(b) H $\geq$ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
5/ The tests in subgroups 7 and 8 shall be performed in the sequence specified.
6/ Only a summary of attributes data is required.
7/ For schematics incorporating 4.5 kΩ base resistors, the minimum and maximum limits shall be -0.6 and -1.5 mA, respectively.
For schematics incorporating 6 kΩ base resistors, the minimum and maximum limits shall be -0.4 and -1.3 mA, respectively.
8/ For device type 03, schematic circuits A, D, E and F, the minimum and maximum limits shall be -0.7 and -1.6 mA, respectively.
For schematic circuit B, the minimum and maximum limits shall be -0.8 and -2.6 mA, respectively.
For schematic circuit C, the minimum and maximum limits shall be -0.6 and -1.5 mA, respectively.
9/ For device type 03, schematics circuits A, C, D, E and F, the maximum limits shall be 40 µA. For schematic circuit B, the maximum limits shall be 80 µA.
10/ For device type 03, schematics circuits A, C, D, E and F, the maximum limits shall be 100 µA. For schematic circuit B, the maximum limits shall be 200 µA.

TABLE III. Group A inspection for device type 04.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	S/L	CLK	E	F	G	H	$\overline{Q}H$	GND	Q_H	SI	A	B	C	D	CLKI	V_{CC}		Min	Max	Unit
1	V_{OH}	3006	1	0.8 V					2.0 V		GND	-.8 mA							4.5 V	Q_H	2.4		V
T_C = 25°C	V_{OH}	3006	2	"					0.8 V	-.8 mA	"								"	$\overline{Q}H$	2.4		“
“	V_{OL}	3007	3	"					2.0 V	16 mA	"								"	$\overline{Q}H$		0.4	“
“	V_{OL}	3007	4	"					0.8 V		"	16 mA							"	Q_H		0.4	“
“	V_{IC}		5	-12 mA							"								"	S/L		-1.5	“
”	"		6		-12 mA						"								"	CLK		"	“
“	“		7								"		-12 mA						"	SI		“	“
“	“		8								"							-12 mA	"	CLKI		“	“
“	“		9								"			-12 mA					"	A		“	“
“	"		10								"				-12 mA				"	B		"	“
“	"		11								"					-12 mA			"	C		"	“
“	“		12								"						-12 mA		"	D		"	“
“	“		13			-12 mA					"								"	E		"	“
“	“		14				-12 mA				"								"	F		"	“
“	"		15					-12 mA			"								"	G		"	"
“	"		16						-12 mA		"								"	H		"	"
“	I_{IL1}	3009	17	0.4 V	4.5 V						"							4.5 V	5.5 V	S/L	-1.2	-3.9	mA
“	I_{IL2}	“	18								"		0.4 V						"	SI	-0.4	-1.3	“
“	“	“	19	4.5 V							"							0.4 V	"	CLKI	"	"	“
“	"	"	20	GND							"			0.4 V					"	A	"	"	"
“	“	“	21	"							"				0.4 V				"	B	"	“	“
“	“	“	22	"							"					0.4 V			"	C	"	“	“
“	“	“	23	"							"						0.4 V		"	D	"	“	“
“	“	“	24	"		0.4 V					"								"	E	"	"	“
“	“	“	25	"			0.4 V				"								"	F	"	"	“
“	“	“	26	"				0.4 V			"								"	G	"	"	“
“	"		27	"					0.4 V		"								"	H	"	"	“
“	I_{IL3}	“	28	4.5 V	0.4 V						"								"	CLK		6/	"

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V or L $\leq$ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	S/L	CLK	E	F	G	H	$\overline{Q}$H	GND	Q_H	SI	A	B	C	D	CLKI	V_{CC}		Min	Max	Unit
1	I_{IH1}	3010	29								GND		2.4 V						5.5 V	SI		40	µA
T_C = 25°C	“	“	30	GND							"							2.4 V	"	CLKI		"	“
“	“	“	31	5.5 V							"			2.4 V					"	A		“	“
“	“	“	32	"							"				2.4 V				"	B		“	“
“	“	“	33	"							"					2.4 V			"	C		“	“
“	“	“	34	"							"						2.4 V		"	D		"	“
“	“	“	35	"		2.4 V					"								"	E		"	“
“	“	“	36	"			2.4 V				"								"	F		“	“
“	“	“	37	"				2.4 V			"								"	G		“	“
“	“	“	38	"					2.4 V		"								"	H		"	“
“	“	“	39	GND	2.4 V						"								"	CLK		"	“
"	I_{IH2}	"	40								"		5.5 V						"	SI		100	"
"	“	“	41	GND							"							5.5 V	"	CLKI		"	“
“	“	“	42	5.5 V							"			5.5 V					"	A		“	“
“	“	“	43	"							"				5.5 V				"	B		“	“
“	“	“	44	"							"					5.5 V			"	C		“	“
“	“	“	45	"							"						5.5 V		"	D		"	“
“	“	“	46	"		5.5 V					"								"	E		"	“
“	“	“	47	"			5.5 V				"								"	F		“	“
“	“	“	48	"				5.5 V			"								"	G		“	“
“	“	“	49	"					5.5 V		"								"	H		"	“
“	“	“	50	GND	5.5 V						"								"	CLK		"	“
“	I_{IH3}	“	51	2.4 V	GND						"							GND	"	S/L		120	“
“	I_{IH4}	“	52	5.5 V	GND						"							GND	"	S/L		300	“
“	I_{OS}	3011	53	C 1/	4.5 V				4.5 V		"	GND						4.5 V	"	Q_H	-20	-55	mA
“	I_{OS}	3011	54	C 1/	4.5 V				GND	GND	"							4.5 V	"	$\overline{Q}$H	-20	-55	mA
“	I_{CC}	3005	55	C 1/	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V		"		GND	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	"	V_{CC}		63	mA
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																						
7	Truth	3014	56	B	B	B	B	B	B	H	GND	L	A	B	B	B	B	B	4.5 V		3/		
T_C = 25°C	table	“	57	A	B	B	B	B	B	"	"	"	"	B	B	B	B	"	"				
2/ 5/	test	“	58	"	A	A	A	A	A	"	"	"	"	A	A	A	A	"	"				
“	4/	“	59	"	B	A	A	A	A	"	"	"	"	A	A	A	A	"	"				

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	S/L	CLK	E	F	G	H	$\overline{Q}_H$	GND	Q_H	SI	A	B	C	D	CLKI	V_{CC}		Min	Max	Unit
7	Truth	3014	60	A	A	A	A	A	A	H	GND	L	A	A	A	A	A	B	4.5 V				
T_C = 25°C	table	“	61	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
2/ 5/	test	“	62	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	4/	“	63	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	64	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	65	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	66	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	67	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"		3/		
"	"	“	68	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	69	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	70	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	71	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	72	"	A	"	"	"	"	L	"	H	A	"	"	"	"	"	"				
"	"	“	73	"	B	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
“	"	“	74	"	A	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	“	75	"	B	"	"	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	“	76	"	A	"	"	"	"	"	"	"	A	"	"	"	"	"	"				
“	"	“	77	"	B	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	“	78	"	A	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	“	79	"	B	"	"	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	“	80	"	A	"	"	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	“	81	"	B	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
“	"	“	82	"	A	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	“	83	"	B	"	"	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	“	84	"	A	"	"	"	"	"	"	"	A	"	"	"	"	"	"				
“	"	“	85	"	B	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	“	86	"	A	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	“	87	"	B	"	"	"	"	"	"	"	A	"	"	"	"	"	"				
“	"	“	88	"	A	"	"	"	"	H	"	L	"	"	"	"	"	"	"				
"	"	“	89	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	90	"	A	"	"	"	"	"	"	"	"	"	"	"	"	A	"				
“	"	“	91	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	92	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	93	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	94	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	S/L	CLK	E	F	G	H	$\overline{Q}H$	GND	Q_H	SI	A	B	C	D	CLKI	V_{CC}		Min	Max	Unit
7	Truth	3014	95	A	B	A	A	A	A	H	GND	L	B	A	A	A	A	B	4.5 V				
T_C = 25°C	table	“	96	"	A	"	"	"	"	L	"	H	B	"	"	"	"	"	"				
2/ 5/	test	“	97	"	B	"	"	"	"	L	"	H	A	"	"	"	"	"	"				
“	4/	“	98	"	A	"	"	"	"	H	"	L	A	"	"	"	"	"	"				
"	"	“	99	"	B	"	"	"	"	H	"	L	B	"	"	"	"	"	"				
"	"	“	100	"	A	"	"	"	"	L	"	H	B	"	"	"	"	"	"				
“	"	“	101	"	B	"	"	"	"	L	"	H	A	"	"	"	"	"	"				
"	"	“	102	"	A	"	"	"	"	H	"	L	A	"	"	"	"	"	"		3/		
"	"	“	103	"	B	"	"	"	"	H	"	L	B	"	"	"	"	"	"				
"	"	“	104	"	A	"	"	"	"	L	"	H	B	"	"	"	"	"	"				
"	"	“	105	"	B	"	"	"	"	L	"	H	A	"	"	"	"	"	"				
“	"	“	106	"	A	"	"	"	"	H	"	L	A	"	"	"	"	"	"				
"	"	“	107	"	B	"	"	"	"	H	"	L	B	"	"	"	"	"	"				
"	"	“	108	"	A	"	"	"	"	L	"	H	B	"	"	"	"	"	"				
“	"	“	109	B	B	"	B	"	B	H	"	L	A	"	B	"	B	"	"				
"	"	“	110	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	111	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	112	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	113	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	114	"	A	"	"	"	"	"	"	"	"	"	"	"	"	A	"				
"	"	“	115	A	A	"	"	"	"	"	"	"	"	"	"	"	"	A	"				
"	"	“	116	"	B	"	"	"	"	"	"	"	B	"	"	"	"	B	"				
“	"	“	117	"	A	"	A	"	A	L	"	H	B	"	A	"	A	"	"				
"	"	“	118	"	B	"	"	"	"	L	"	H	A	"	"	"	"	"	"				
"	"	“	119	"	A	"	"	"	"	H	"	L	A	"	"	"	"	"	"				
“	"	“	120	"	B	"	"	"	"	H	"	L	B	"	"	"	"	"	"				
"	"	“	121	"	A	"	"	"	"	L	"	H	B	"	"	"	"	"	"				
"	"	“	122	"	B	"	"	"	"	L	"	H	A	"	"	"	"	"	"				
“	"	“	123	"	A	"	"	"	"	H	"	L	A	"	"	"	"	"	"				
"	"	“	124	"	B	"	"	"	"	H	"	L	B	"	"	"	"	"	"				
"	"	“	125	"	A	"	"	"	"	L	"	H	B	"	"	"	"	"	"				
“	"	“	126	"	B	"	"	"	"	L	"	H	A	"	"	"	"	"	"				
“	"	“	127	"	A	"	"	"	"	H	"	L	A	"	"	"	"	"	"				
"	"	“	128	"	B	"	"	"	"	H	"	L	B	"	"	"	"	"	"				
“	"	“	129	"	A	"	"	"	"	L	"	H	B	"	"	"	"	"	"				

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	S/L	CLK	E	F	G	H	$\overline{Q}_H$	GND	Q_H	SI	A	B	C	D	CLKI	V_{CC}		Min	Max	Unit
7	Truth	3014	130	A	B	A	A	A	A	L	GND	H	A	A	A	A	A	B	4.5 V				
T_C = 25°C	table	“	131	"	A	A	"	A	"	H	"	L	"	"	"	"	"	"	"				
2/ 5/	test	“	132	B	B	B	"	B	"	L	"	H	"	B	"	B	"	"	"				
“	4/	“	133	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	134	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	135	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	136	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	137	"	A	"	"	"	"	"	"	"	"	"	"	"	"	A	"		3/		
"	"	“	138	A	A	"	"	"	"	"	"	"	"	"	"	"	"	A	"				
"	"	“	139	"	B	"	"	"	"	"	"	"	B	"	"	"	"	B	"				
"	"	“	140	"	A	A	"	A	"	H	"	L	"	A	"	A	"	"	"				
“	"	“	141	"	B	"	"	"	"	H	"	L	"	"	"	"	"	"	"				
"	"	“	142	"	A	"	"	"	"	L	"	H	"	"	"	"	"	"	"				
"	"	“	143	"	B	"	"	"	"	L	"	H	"	"	"	"	"	"	"				
“	"	“	144	"	A	"	"	"	"	H	"	L	"	"	"	"	"	"	"				
"	"	“	145	"	B	"	"	"	"	H	"	L	"	"	"	"	"	"	"				
"	"	“	146	"	A	"	"	"	"	L	"	H	"	"	"	"	"	"	"				
“	"	“	147	"	B	"	"	"	"	L	"	H	"	"	"	"	"	"	"				
"	"	“	148	"	A	"	"	"	"	H	"	L	"	"	"	"	"	"	"				
"	"	“	149	"	B	"	"	"	"	H	"	L	"	"	"	"	"	"	"				
"	"	“	150	"	A	"	"	"	"	L	"	H	"	"	"	"	"	"	"				
"	"	“	151	"	B	"	"	"	"	L	"	H	"	"	"	"	"	"	"				
“	"	“	152	"	A	"	"	"	"	H	"	L	"	"	"	"	"	"	"				
"	"	“	153	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	154	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	155	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	156	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	157	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	158	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	159	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	160	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	161	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	162	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	163	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	164	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F Test No.	1 S/L	2 CLK	3 E	4 F	5 G	6 H	7 $\overline{Q}$H	8 GND	9 Q_H	10 SI	11 A	12 B	13 C	14 D	15 CLKI	16 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
7	Truth	3014	165	A	B	A	A	A	A	H	GND	L	A	A	A	A	A	B	4.5 V		3/		
T_C = 25°C	table	“	166	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
2/ 5/	test	“	167	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	4/	“	168	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	169	B	B	"	"	"	"	L	"	H	"	"	"	"	"	"	"				
"	"	“	170	A	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	171	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	172	"	B	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	“	173	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	174	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	175	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	176	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	177	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	178	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	179	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	180	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	181	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	“	182	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	183	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	“	184	B	"	"	"	"	B	H	"	L	"	"	"	"	"	"	"				
"	"	“	185	A	"	"	"	"	B	H	"	L	"	"	"	"	"	"	"				
"	"	“	186	B	"	"	"	B	A	L	"	H	"	"	"	"	"	"	"				
“	"	“	187	A	"	"	"	B	A	L	"	H	"	"	"	"	"	"	"				
8	Repeat subgroup 7 at T_C = +125° C and T_C = -55° C.																						
9	f_{MAX}	(Fig 7)	188	IN	IN	GND	GND	GND	GND		GND	OUT	IN	GND	GND	GND	GND	GND	5.0 V	Q_H	18		MHz
T_C = 25°C	t_{PLH1}	3003	189	IN	GND	GND	GND	GND	IN		"	OUT		GND	GND	GND	GND	GND	"	S/L to Q_H	6	35	ns
"	t_{PHL1}	(Fig 7)	190	IN	GND	GND	GND	GND	IN	OUT	"			GND	GND	GND	GND	GND	"	S/L to $\overline{Q}$H	7	44	"
“	t_{PLH2}	“	191	5.0 V	IN						"	OUT	IN					IN	"	CLK to Q_H	5	28	"
"	t_{PHL2}	“	192	5.0 V	IN					OUT	"		IN					IN	"	CLK to $\overline{Q}$H	6	35	"
"	t_{PLH3}	“	193	GND	GND	GND	GND	GND	IN		"	OUT	GND	GND	GND	GND	GND	GND	"	H to Q_H	5	21	"
“	t_{PHL3}	“	194	"	"	"	"	"	"		"	OUT	"	"	"	"	"	"	"	H to Q_H	7	40	"
"	t_{PLH4}	“	195	"	"	"	"	"	"	OUT	"		"	"	"	"	"	"	"	H to $\overline{Q}$H	6	31	"
"	t_{PHL4}	“	196	"	"	"	"	"	"	OUT	"		"	"	"	"	"	"	"	H to $\overline{Q}$H	6	31	"

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V or L $\leq$ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	S/L	CLK	E	F	G	H	$\overline{Q}_H$	GND	Q_H	SI	A	B	C	D	CLKI	V_{CC}		Min	Max	Unit
10	f_{MAX}	(Fig 7)	197	IN	IN	GND	GND	GND	GND		GND	OUT	IN	GND	GND	GND	GND	GND	5.0 V	Q_H	14		MHz
T_C = 125°C	t_{PLH1}	3003	198	IN	GND	GND	GND	GND	IN		"	OUT		GND	GND	GND	GND	GND	"	S/L to Q_H	10	40	ns
"	t_{PHL1}	(Fig 7)	199	IN	GND	GND	GND	GND	IN	OUT	"			GND	GND	GND	GND	GND	"	S/L to $\overline{Q}_H$	11	60	"
"	t_{PLH2}	"	200	5.0 V	IN						"	OUT	IN					IN	"	CLK to Q_H	6	37	"
"	t_{PHL2}	"	201	5.0 V	IN					OUT	"		IN					IN	"	CLK to $\overline{Q}_H$	10	47	"
"	t_{PLH3}	"	202	GND	GND	GND	GND	GND	IN		"	OUT	GND	GND	GND	GND	GND	GND	"	H to Q_H	5	27	"
"	t_{PHL3}	"	203	"	"	"	"	"	"		"	OUT	"	"	"	"	"	"	"	H to Q_H	11	54	"
"	t_{PLH4}	"	204	"	"	"	"	"	"	OUT	"		"	"	"	"	"	"	"	H to $\overline{Q}_H$	10	41	"
"	t_{PHL4}	"	205	"	"	"	"	"	"	OUT	"		"	"	"	"	"	"	"	H to $\overline{Q}_H$	10	41	"
11	Same tests, terminal conditions, and limits as for subgroup 10, except T_C = -55° C.																						

1/ C = after all other input conditions, but prior to measurement, apply momentary GND, then 4.5 V.

2/ For subgroups 7 and 8, A = V_{CC} and B = GND.

3/ Output voltages shall be either:
(a) H = 2.4 V minimum and L = 0.4 V maximum when using a high speed checker double comparator, or
(b) H $\geq$ 1.5 V and L < 1.5 V when using a high speed checker single comparator.

4/ The tests in subgroups 7 and 8 shall be performed in the sequence specified.

5/ Only a summary of attributes data is required.

6/ For device type 04, schematics incorporating a 4 kΩ base resistor in the clock input circuit, the minimum and maximum limits shall be -0.7 and -1.6 mA, respectively. For schematics incorporating a 6 kΩ base resistor in the clock input circuit, the minimum and maximum limits shall be -0.4 and -1.3 mA, respectively.

TABLE III. Group A inspection for device type 05.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLR	SR	A	B	C	D	SL	GND	S0	S1	CLK	Q_D	Q_C	Q_B	Q_A	V_{CC}		Min	Max	Unit
1	V_{OH}	3006	1	2.0 V		2.0 V	2.0 V	2.0 V	2.0 V		GND	2.0 V	2.0 V	A 1/				-0.8 mA	4.5 V	Q_A	2.4		V
T_C = 25°C	"	3006	2	"		"	"	"	"		"	"	"	"			-0.8 mA		"	Q_B	"		“
“	"	"	3	"		"	"	"	"		"	"	"	"		-0.8 mA			"	Q_C	"		“
“	"	"	4	"		"	"	"	"		"	"	"	"	-0.8 mA				"	Q_D	"		“
“	V_{OL}	3007	5	"		0.8 V	0.8 V	0.8 V	0.8 V		"	"	"	"				16 mA	"	Q_A		0.4	“
"	"	"	6	"		"	"	"	"		"	"	"	"			16 mA		"	Q_B		"	“
“	“	"	7	"		"	"	"	"		"	"	"	"		16 mA			"	Q_C		“	“
“	“	"	8	"		"	"	"	"		"	"	"	"	16 mA				"	Q_D		“	“
“	V_{IC}		9	-12 mA							"								"	CLR		-1.5	“
“	"		10		-12 mA						"								"	SR		"	“
“	"		11			-12 mA					"								"	A		"	“
“	“		12				-12 mA				"								"	B		"	“
“	“		13					-12 mA			"								"	C		"	“
“	“		14						-12 mA		"								"	D		"	“
“	"		15							-12 mA	"								"	SL		"	"
“	"		16								"	-12 mA							"	S0		"	"
“	"		17								"		-12 mA						"	S1		"	"
“	"		18								"			-12 mA					"	CLK		"	“
“	I_{IL1}	3009	19	0.4 V							"								5.5 V	CLR	-0.4	-1.3	mA
“	"	"	20		0.4 V						"		GND						"	SR	"	"	"
“	“	“	21			0.4 V					"	5.5 V	5.5 V						"	A	"	“	“
“	“	“	22				0.4 V				"	"	"						"	B	"	“	“
“	“	“	23					0.4 V			"	"	"						"	C	"	“	“
“	“	“	24						0.4 V		"	"	"						"	D	"	"	“
“	“	“	25							0.4 V	"	GND	"						"	SL	"	"	“
“	I_{IL2}	“	26								"	0.4 V							"	SO	"	7/	“
“	I_{IL2}	"	27								"		0.4 V						"	S1	"	7/	“
“	I_{IL3}	“	28	5.5 V							"			0.4 V					"	CLK	-0.7	-1.6	"

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLR	SR	A	B	C	D	SL	GND	S0	S1	CLK	Q_D	Q_C	Q_B	Q_A	V_{CC}		Min	Max	Unit
1	I_{IH1}	3010	29	2.4 V							GND								5.5 V	CLR		40	µA
T_C = 25°C	"	"	30		2.4 V						"		5.5 V						"	SR		"	“
“	"	"	31			2.4 V					"	GND	GND						"	A		"	“
“	“	"	32				2.4 V				"	"	"						"	B		"	“
“	“	"	33					2.4 V			"	"	"						"	C		"	“
“	“	"	34						2.4 V		"	"	"						"	D		"	“
“	"	"	35							2.4 V	"	5.5 V							"	SL		"	"
“	"	"	36								"	2.4 V							"	S0		"	"
“	"	"	37								"		2.4 V						"	S1		"	"
“	"	"	38								"			2.4 V					"	CLK		"	“
"	I_{IH2}	"	39	5.5 V							"								"	CLR		100	"
"	"	"	40		5.5 V						"		5.5 V						"	SR		"	“
“	"	"	41			5.5 V					"	GND	GND						"	A		"	“
“	"	"	42				5.5 V				"	"	"						"	B		"	“
“	"	"	43					5.5 V			"	"	"						"	C		"	“
“	"	"	44						5.5 V		"	"	"						"	D		"	“
“	"	"	45							5.5 V	"	5.5 V							"	SL		"	"
“	"	"	46								"	5.5 V							"	S0		"	"
“	"	"	47								"		5.5 V						"	S1		"	"
“	"	"	48								"			5.5 V					"	CLK		"	“
“	I_{OS}	3011	49	5.5 V		5.5 V	5.5 V	5.5 V	5.5 V		"	5.5 V	5.5 V	A				GND	"	Q_A	-20	-57	mA
“	"	"	50	"		"	"	"	"		"	"	"	"			GND		"	Q_B	"	"	"
“	“	“	51	"		"	"	"	"		"	"	"	"		GND			"	Q_C	"	“	“
“	“	“	52	"		"	"	"	"		"	"	"	"	GND				"	Q_D	"	“	“
“	I_{CC}	3005	53	"	5.5 V	GND	GND	GND	GND	5.5 V	"	"	"	"					"	V_{CC}		63	“
2	Same tests, terminal conditions, and limits as subgroup 1 except T_C = 125°C and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions, and limits as subgroup 1 except T_C = -55°C and V_{IC} tests are omitted.																						
7	Truth	3014	54	B 2/	B 2/	A 1/	B 2/	A 1/	B 2/	B 2/	GND	A 1/	A 1/	A 1/	L	L	L	L	5.0 V			4/	
T_C = 25°C	table	"	55	A	"	"	"	"	"	"	"	"	"	A	"	L	"	L	"				
3/ 6/	test	"	56	"	"	"	"	"	"	"	"	"	"	B	"	L	"	L	"				
“	5/	"	57	"	"	"	"	"	"	"	"	"	"	A	"	H	"	H	"				
“	"	"	58	"	"	B	A	B	A	"	"	"	"	A	"	H	"	H	"				
“	"	"	59	"	"	B	"	B	"	"	"	"	"	B	"	H	"	H	"				
“	"	"	60	"	"	B	"	B	"	"	"	"	"	A	H	L	H	L	"				

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLR	SR	A	B	C	D	SL	GND	S0	S1	CLK	Q_D	Q_C	Q_B	Q_A	V_{CC}		Min	Max	Unit
7	Truth	3014	61	A	B	A	A	A	A	B	GND	A	A	A	H	L	H	L	5.0 V				
T_C = 25°C	table	"	62	"	"	"	"	"	"	"	"	"	"	B	"	L	"	L	"				
3/ 6/	test	"	63	"	"	"	"	"	"	"	"	"	"	A	"	H	"	H	"			4/	
“	5/	"	64	"	"	"	"	"	"	"	"	B	B	A	"	"	"	"	"				
“	"	"	65	"	"	"	B	"	B	"	"	"	"	A	"	"	"	"	"				
“	"	"	66	"	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"				
“	"	"	67	"	"	"	"	"	"	"	"	"	"	A	"	"	"	"	"				
“	"	"	68	B	"	"	"	"	"	"	"	"	"	"	L	L	L	L	"				
“	"	"	69	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	"	"	70	"	"	"	A	"	"	A	"	"	"	"	"	"	"	"	"				
“	"	"	71	"	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"				
“	"	"	72	"	"	"	"	"	"	"	"	"	"	A	"	"	"	"	"				
“	"	"	73	"	"	"	"	"	"	"	"	A	"	A	"	"	"	"	"				
“	"	"	74	"	A	B	B	B	"	B	"	"	"	A	"	"	"	"	"				
“	"	"	75	"	A	"	"	"	"	"	"	"	"	B	"	"	"	"	"				
“	"	"	76	"	A	"	"	"	"	"	"	"	"	A	"	"	"	H	"				
“	"	"	77	"	B	"	"	"	"	"	"	"	"	A	"	"	"	H	"				
“	"	"	78	"	B	"	"	"	"	"	"	"	"	B	"	"	"	H	"				
“	"	"	79	"	B	"	"	"	"	"	"	"	"	A	"	"	H	L	"				
“	"	"	80	"	A	"	"	"	"	"	"	"	"	A	"	"	H	L	"				
“	"	"	81	"	A	"	"	"	"	"	"	"	"	B	"	"	H	L	"				
“	"	"	82	"	A	"	"	"	"	"	"	"	"	A	"	H	L	H	"				
“	"	"	83	"	B	"	"	"	"	"	"	"	"	A	"	H	L	H	"				
“	"	"	84	"	B	"	"	"	"	"	"	"	"	B	"	H	L	H	"				
“	"	"	85	"	B	"	"	"	"	"	"	"	"	A	H	L	H	L	"				
“	"	"	86	"	A	"	"	"	"	"	"	"	"	A	H	L	H	L	"				
“	"	"	87	"	A	"	"	"	"	"	"	"	"	B	H	L	H	L	"				
“	"	"	88	"	A	"	"	"	"	"	"	"	"	A	L	H	L	H	"				
“	"	"	89	"	B	"	"	"	"	"	"	"	"	A	L	H	L	H	"				
“	"	"	90	"	"	"	"	"	"	"	"	"	"	B	L	H	L	H	"				
“	"	"	91	"	"	"	"	"	"	"	"	"	"	A	H	L	H	L	"				
“	"	"	92	"	"	"	"	"	"	"	"	"	"	B	H	L	H	"	"				
“	"	"	93	"	"	"	"	"	"	"	"	"	"	A	L	H	L	"	"				
“	"	"	94	"	"	"	"	"	"	"	"	"	"	B	L	H	"	"	"				

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLR	SR	A	B	C	D	SL	GND	S0	S1	CLK	Q_D	Q_C	Q_B	Q_A	V_{CC}		Min	Max	Unit
7	Truth	3014	95	A	B	B	B	B	B	B	GND	A	B	A	H	L	L	L	5.0 V				
T_C = 25°C	table	"	96	"	"	"	"	"	"	"	"	"	"	B	H	"	"	"	"				
3/ 6/	test	"	97	"	"	"	"	"	"	"	"	"	"	A	L	"	"	"	"			4/	
“	5/	"	98	"	"	"	"	"	"	"	"	B	A	A	"	"	"	"	"				
“	"	"	99	"	"	"	"	"	"	A	"	"	"	A	"	"	"	"	"				
“	"	"	100	"	"	"	"	"	"	A	"	"	"	B	"	"	"	"	"				
“	"	"	101	"	"	"	"	"	"	A	"	"	"	A	H	"	"	"	"				
“	"	"	102	"	"	"	"	"	"	B	"	"	"	A	H	"	"	"	"				
“	"	"	103	"	"	"	"	"	"	B	"	"	"	B	H	"	"	"	"				
“	"	"	104	"	"	"	"	"	"	B	"	"	"	A	L	H	"	"	"				
“	"	"	105	"	"	"	"	"	"	A	"	"	"	A	L	H	"	"	"				
“	"	"	106	"	"	"	"	"	"	A	"	"	"	B	L	H	"	"	"				
“	"	"	107	"	"	"	"	"	"	A	"	"	"	A	H	L	H	"	"				
“	"	"	108	"	"	"	"	"	"	B	"	"	"	A	H	L	H	"	"				
“	"	"	109	"	"	"	"	"	"	B	"	"	"	B	H	L	H	"	"				
“	"	"	110	"	"	"	"	"	"	B	"	"	"	A	L	H	L	H	"				
“	"	"	111	"	"	"	"	"	"	A	"	"	"	A	L	H	L	H	"				
“	"	"	112	"	"	"	"	"	"	A	"	"	"	B	L	H	L	H	"				
“	"	"	113	"	"	"	"	"	"	A	"	"	"	A	H	L	H	L	"				
“	"	"	114	"	"	"	"	"	"	B	"	"	"	A	H	L	H	L	"				
“	"	"	115	"	"	"	"	"	"	"	"	"	"	B	H	L	H	L	"				
“	"	"	116	"	"	"	"	"	"	"	"	"	"	A	L	H	L	H	"				
“	"	"	117	"	"	"	"	"	"	"	"	"	"	B	"	H	L	H	"				
“	"	"	118	"	"	"	"	"	"	"	"	"	"	A	"	L	H	L	"				
“	"	"	119	"	"	"	"	"	"	"	"	"	"	B	"	"	H	L	"				
“	"	"	120	"	"	"	"	"	"	"	"	"	"	A	"	"	L	H	"				
“	"	"	121	"	"	"	"	"	"	"	"	"	"	B	"	"	"	H	"				
“	"	"	122	"	"	"	"	"	"	"	"	"	"	A	"	"	"	L	"				
“	"	"	123	B	"	"	"	"	"	"	"	"	B	B	"	"	"	L	"				
8	Repeat subgroup 7 at T_C = 125°C and T_C = -55°C.																						

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLR	SR	A	B	C	D	SL	GND	S0	S1	CLK	Q_D	Q_C	Q_B	Q_A	V_{CC}		Min	Max	Unit
9	f_{MAX}	(Fig 8)	124	B	IN	GND	GND	GND	GND	GND	GND	5.0 V	GND	IN				OUT	5.0 V	Q_A	11		MHz
T_C = 25°C	t_{PHL1}	3003	125	IN		5.0 V	5.0 V	5.0 V	5.0 V		"	"	5.0 V	"				OUT	"	CLR to Q_A	7	34	ns
"	"	(Fig 8)	126	"		"	"	"	"		"	"	"	"			OUT		"	CLR to Q_B	"	"	"
“	"	"	127	"		"	"	"	"		"	"	"	"		OUT			"	CLR to Q_C	"	"	"
“	"	"	128	"		"	"	"	"		"	"	"	"	OUT				"	CLR to Q_D	"	"	"
"	t_{PLH2}	"	129	B		IN	"	"	"		"	"	"	"				OUT	"	CLK to Q_A	"	26	"
"	"	"	130	"		5.0 V	IN	"	"		"	"	"	"			OUT		"	CLK to Q_B	"	"	"
“	"	"	131	"		5.0 V	5.0 V	IN	"		"	"	"	"		OUT			"	CLK to Q_C	"	"	"
“	"	"	132	"		5.0 V	5.0 V	5.0 V	IN		"	"	"	"	OUT				"	CLK to Q_D	"	"	"
"	t_{PHL2}	"	133	5.0 V		IN	5.0 V	5.0 V	5.0 V		"	"	"	"				OUT	"	CLK to Q_A	"	32	"
"	"	"	134	"		5.0 V	IN	5.0 V	5.0 V		"	"	"	"			OUT		"	CLK to Q_B	"	"	"
“	"	"	135	"		5.0 V	5.0 V	IN	5.0 V		"	"	"	"		OUT			"	CLK to Q_C	"	"	"
“	"	"	136	"		5.0 V	5.0 V	5.0 V	IN		"	"	"	"	OUT				"	CLK to Q_D	"	"	"
10	f_{MAX}	(Fig 8)	137	B	IN	GND	GND	GND	GND	GND	"	5.0 V	GND	IN				OUT	"	Q_A	9		MHz
T_C = 125°C	t_{PHL1}	3003	138	IN		5.0 V	5.0 V	5.0 V	5.0 V		"	"	5.0 V	"				OUT	"	CLR to Q_A	7	48	ns
"	"	(Fig 8)	139	"		"	"	"	"		"	"	"	"			OUT		"	CLR to Q_B	"	"	"
“	"	"	140	"		"	"	"	"		"	"	"	"		OUT			"	CLR to Q_C	"	"	"
“	"	"	141	"		"	"	"	"		"	"	"	"	OUT				"	CLR to Q_D	"	"	"
"	t_{PLH2}	"	142	B		IN	"	"	"		"	"	"	"				OUT	"	CLK to Q_A	"	36	"
"	"	"	143	"		5.0 V	IN	"	"		"	"	"	"			OUT		"	CLK to Q_B	"	"	"
“	"	"	144	"		5.0 V	5.0 V	IN	"		"	"	"	"		OUT			"	CLK to Q_C	"	"	"
“	"	"	145	"		5.0 V	5.0 V	5.0 V	IN		"	"	"	"	OUT				"	CLK to Q_D	"	"	"
"	t_{PHL2}	"	146	5.0 V		IN	5.0 V	5.0 V	5.0 V		"	"	"	"				OUT	"	CLK to Q_A	"	44	"
"	"	"	147	"		5.0 V	IN	5.0 V	5.0 V		"	"	"	"			OUT		"	CLK to Q_B	"	"	"
“	"	"	148	"		5.0 V	5.0 V	IN	5.0 V		"	"	"	"		OUT			"	CLK to Q_C	"	"	"
“	"	"	149	"		5.0 V	5.0 V	5.0 V	IN		"	"	"	"	OUT				"	CLK to Q_D	"	"	"
11	Same tests, terminal conditions and limits as subgroup 10, except T_C = -55°C.																						

1/ A = normal clock pulse, except for subgroup 7 and 8 (see 3/).

2/ B = momentary GND, then V_{IN} (except for subgroups 7 and 8). For subgroups 1, 2 and 3, $V_{IN} = V_{CC}$; for subgroups 9, 10 and 11, V_{IN} = 3.0 V minimum (see figure 8).

3/ For subgroups 7 and 8, A = V_{CC} and B = GND.

4/ Output voltages shall be either:
(a) H = 2.4 V minimum and L = 0.4 V maximum when using a high speed checker double comparator, or
(b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.

5/ The tests in subgroups 7 and 8 shall be performed in the sequence specified.

6/ Only a summary of attributes data is required.

7/ For device type 05, schematic circuits A and B, the minimum and maximum limits shall be -0.4 and -1.3 mA, respectively. For schematic C, the minimum and maximum limits shall be -0.7 and -1.6 mA, respectively.

TABLE III. Group A inspection for device type 06.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLR	J	$\overline{K}$	A	B	C	D	GND	SL	CLK	$\overline{Q}_D$	Q_D	Q_C	Q_B	Q_A	VCC		Min	Max	Unit
1	V_{OH}	3006	1	2.0 V			2.0 V	2.0 V	2.0 V	2.0 V	GND	0.8 V	A 1/					-0.8 mA	4.5 V	Q_A	2.4		V
T_C = 25°C	"	"	2	"			"	"	"	"	"	"	"				-0.8 mA		"	Q_B	"		“
“	"	"	3	"			"	"	"	"	"	"	"			-0.8 mA			"	Q_C	"		“
“	"	"	4	"			"	"	"	"	"	"	"		-0.8 mA				"	Q_D	"		“
“	"	"	5	"			0.8 V	0.8 V	0.8 V	0.8 V	"	"	"	-0.8 mA					"	$\overline{Q}_D$	"		“
”	V_{OL}	3007	6	"			"	"	"	"	"	"	"					16 mA	"	Q_A		0.4	“
“	“	"	7	"			"	"	"	"	"	"	"				16 mA		"	Q_B		“	“
“	“	"	8	"			"	"	"	"	"	"	"			16 mA			"	Q_C		“	“
“	"	"	9	"			"	"	"	"	"	"	"		16 mA				"	Q_D		"	“
“	"	"	10	"			2.0 V	2.0 V	2.0 V	2.0 V	"	"	"	16 mA					"	$\overline{Q}_D$		"	“
“	V_{IC}		11	-12 mA							"								"	CLR		-1.5	“
“	“		12		-12 mA						"								"	J		"	“
“	“		13			-12 mA					"								"	$\overline{K}$		"	“
“	“		14				-12 mA				"								"	A		"	“
“	"		15					-12 mA			"								"	B		"	"
“	"		16						-12 mA		"								"	C		"	"
“	"		17							-12 mA	"								"	D		"	"
“	"		18								"	-12 mA							"	SL		"	“
“	"		19								"		-12 mA						"	CLK		"	"
“	I_{IL1}	3009	20	0.4 V							"	5.5 V							5.5 V	CLR	-0.4	-1.3	mA
“	I_{IL2}	“	21	GND	0.4 V						"	5.5 V							"	J		7/	
“	“	“	22	B 2/	5.5 V	0.4 V	5.5 V				"	5.5 V	A						"	$\overline{K}$			
“	“	“	23				0.4 V				"	GND							"	A			
“	“	“	24					0.4 V			"	"							"	B			
“	“	“	25						0.4 V		"	"							"	C			
“	"	“	26							0.4 V	"	"							"	D			
“	"	"	27								"	0.4 V							"	SL			
“	I_{IL3}	“	28	5.5 V							"		0.4 V						"	CLK	-0.7	-1.6	mA

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V or L $\leq$ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLR	J	$\overline{K}$	A	B	C	D	GND	SL	CLK	$\overline{Q_D}$	Q_D	Q_C	Q_B	Q_A	V_{CC}		Min	Max	Unit
1	I_{IH1}	3010	29	2.4 V							GND								5.5 V	CLR		40	µA
T_C = 25°C	"	“	30	5.5 V	2.4 V		5.5 V				"	GND	A						"	J		"	"
“	“	“	31	GND		2.4 V					"	GND							"	$\overline{K}$		"	"
“	“	“	32				2.4 V				"	5.5 V							"	A		"	"
“	“	“	33					2.4 V			"	"							"	B		"	"
“	“	“	34						2.4 V		"	"							"	C		"	"
“	"	“	35							2.4 V	"	"							"	D		"	"
“	"	"	36								"	2.4 V							"	SL		"	"
"	"	"	37	GND							"		2.4 V						"	C LK		"	"
"	I_{IH2}	"	38	5.5 V							"								"	CLR		100	"
"	"	“	39	5.5 V	5.5 V		5.5 V				"	GND	A						"	J		"	"
“	“	“	40	GND		5.5 V					"	GND							"	$\overline{K}$		"	"
“	“	“	41				5.5 V				"	5.5 V							"	A		"	"
“	“	“	42					5.5 V			"	"							"	B		"	"
“	“	“	43						5.5 V		"	"							"	C		"	"
“	"	“	44							5.5 V	"	"							"	D		"	"
“	"	"	45								"	"							"	SL		"	"
"	"	"	46	GND							"		5.5 V						"	C LK		"	"
"	I_{OS}	3011	47	5.5 V			5.5 V	5.5 V	5.5 V	5.5 V	"	GND	A					GND	"	Q_A	-20	-57	mA
"	"	"	48	"			"	"	"	"	"	"	"				GND		"	Q_B	"	"	“
“	"	"	49	"			"	"	"	"	"	"	"			GND			"	Q_C	"	"	“
“	"	"	50	"			"	"	"	"	"	"	"		GND				"	Q_D	"	"	“
“	"	"	51	GND							"			GND					"	$\overline{Q_D}$	"	"	“
”	I_{CC}	3005	52	5.5 V	GND	GND	GND	GND	GND	GND	"	GND	A						"	V_{CC}		63	“
2	Same tests, terminal conditions, and limits as subgroup 1 except T_C = 125°C and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions, and limits as subgroup 1 except T_C = -55°C and V_{IC} tests are omitted.																						

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V or L $\leq$ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLR	J	$\overline{K}$	A	B	C	D	GND	SL	CLK	$\overline{Q_D}$	Q_D	Q_C	Q_B	Q_A	V_{CC}		Min	Max	Unit
7	Truth	3014	53	B	B	B	B	B	B	B	GND	A	A	H	L	L	L	L	5.0 V		4/		
T_C = 25°C	table	"	54	A	A	A	"	"	"	"	"	"	A	"	"	"	"	L	"				
3/ 6/	test	"	55	"	"	"	"	"	"	"	"	"	B	"	"	"	"	L	"				
"	5/	"	56	"	"	"	"	"	"	"	"	"	A	"	"	"	"	H	"				
"	"	"	57	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	58	"	"	"	"	"	"	"	"	"	A	"	"	"	H	"	"				
"	"	"	59	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	60	"	"	"	"	"	"	"	"	"	A	"	"	H	"	"	"				
"	"	"	61	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	62	"	"	"	"	"	"	"	"	"	A	L	H	"	"	"	"				
"	"	"	63	"	B	"	"	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	64	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	65	"	"	"	"	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	66	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	67	"	"	"	"	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	68	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	69	"	"	"	"	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	70	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	71	"	"	"	"	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	72	"	"	B	"	"	"	"	"	"	A	"	"	"	"	"	"				
"	"	"	73	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	74	"	"	"	"	"	"	"	"	"	A	"	"	"	"	L	"				
"	"	"	75	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	76	"	"	"	"	"	"	"	"	"	A	"	"	"	L	"	"				
"	"	"	77	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	78	"	"	"	"	"	"	"	"	"	A	"	"	L	"	"	"				
"	"	"	79	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"				
"	"	"	80	"	"	"	"	"	"	"	"	"	A	H	L	"	"	"	"				
"	"	"	81	"	"	"	A	"	A	"	"	B	A	"	"	"	"	"	"				
"	"	"	82	"	"	"	A	"	A	"	"	"	B	"	"	"	"	"	"				
"	"	"	83	"	"	"	A	"	A	"	"	"	A	"	"	H	"	H	"				
"	"	"	84	"	"	"	B	A	B	A	"	"	A	"	"	H	"	H	"				

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V or L ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLR	J	$\overline{K}$	A	B	C	D	GND	SL	CLK	$\overline{Q_D}$	Q_D	Q_C	Q_B	Q_A	V_{CC}		Min	Max	Unit
7	Truth	3014	85	A	B	B	B	A	B	A	GND	B	B	H	L	H	L	H	5.0 V				
T_C = 25°C	table	“	86	"	"	"	B	"	B	"	"	"	A	L	H	L	H	L	"				
3/ 6/	test	“	87	"	"	"	A	"	A	"	"	"	A	"	"	L	"	L	"				
“	5/	“	88	"	"	"	"	"	"	"	"	"	B	"	"	L	"	L	"				
“	“	“	89	"	"	"	"	"	"	"	"	"	A	"	"	H	"	H	"		4/		
“	“	“	90	B	"	"	"	"	"	"	"	"	B	H	L	L	L	L	"				
“	"	“	91	B	"	"	"	"	"	"	"	"	A	"	"	"	"	"	"				
“	"	"	92	B	A	A	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	"	93	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	"	"	94	B	"	"	"	"	"	"	"	A	"	"	"	"	"	"	"				
"	"	“	95	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
“	“	“	96	A	"	"	B	B	B	B	"	"	B	"	"	"	"	"	"				
“	“	“	97	A	"	"	B	B	B	B	"	"	A	"	"	"	"	H	"				
8	Repeat subgroup 7 at except T_C = 125°C and T_C = -55°C.																						
9	f_{MAX}	(Fig 9)	98	B	5.0 V	GND					GND	5.0 V	IN					OUT	5.0 V	Q_A	15		MHz
T_C = 25°C	t_{PHL1}	3003	99	IN			5.0 V	5.0 V	5.0 V	5.0 V	GND	GND	"					OUT	"	CLR to Q_A	7	30	ns
“	"	(Fig 9)	100	"			"	"	"	"	"	"	"				OUT		"	CLR to Q_B	"	"	"
“	"	"	101	"			"	"	"	"	"	"	"			OUT			"	CLR to Q_C	"	"	"
"	"	"	102	"			"	"	"	"	"	"	"		OUT				"	CLR to Q_D	"	"	"
"	t_{PHL2}	"	103	B			IN				"	IN	"					OUT	"	CLK to Q_A	"	24	"
"	"	"	104	"				IN			"	"	"				OUT		"	CLK to Q_B	"	"	"
“	"	"	105	"					IN		"	"	"			OUT			"	CLK to Q_C	"	"	"
“	"	"	106	"						IN	"	"	"		OUT				"	CLK to Q_D	"	"	"
"	t_{PHL2}	"	107	"			IN				"	"	"					OUT	"	CLK to Q_A	"	29	"
"	"	"	108	"				IN			"	"	"				OUT		"	CLK to Q_B	"	"	"
“	"	"	109	"					IN		"	"	"			OUT			"	CLK to Q_C	"	"	"
“	"	"	110	"						IN	"	"	"		OUT				"	CLK to Q_D	"	"	"

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V or L $\leq$ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	CLR	J	$\overline{K}$	A	B	C	D	GND	SL	CLK	$\overline{Q_D}$	Q_D	Q_C	Q_B	Q_A	V_{CC}		Min	Max	Unit
10	f_{MAX}	(Fig 9)	111	B	5.0 V	GND					GND	5.0 V	IN					OUT	5.0 V	Q_A	12		MHz
T_C = 125°C	t_{PHL1}	3003	112	IN			5.0 V	5.0 V	5.0 V	5.0 V	GND	GND	"					OUT	"	CLR to Q_A	7	34	ns
"	"	(Fig 9)	113	"			"	"	"	"	"	"	"				OUT		"	CLR to Q_B	"	"	"
"	"	"	114	"			"	"	"	"	"	"	"			OUT			"	CLR to Q_C	"	"	"
"	"	"	115	"			"	"	"	"	"	"	"		OUT				"	CLR to Q_D	"	"	"
"	t_{PHL2}	"	116	B			IN				"	IN	"					OUT	"	CLK to Q_A	"	28	"
"	"	"	117	"				IN			"	"	"				OUT		"	CLK to Q_B	"	"	"
"	"	"	118	"					IN		"	"	"			OUT			"	CLK to Q_C	"	"	"
"	"	"	119	"						IN	"	"	"		OUT				"	CLK to Q_D	"	"	"
"	t_{PHL2}	"	120	"			IN				"	"	"					OUT	"	CLK to Q_A	"	34	"
"	"	"	121	"				IN			"	"	"				OUT		"	CLK to Q_B	"	"	"
"	"	"	122	"					IN		"	"	"			OUT			"	CLK to Q_C	"	"	"
"	"	"	123	"						IN	"	"	"		OUT				"	CLK to Q_D	"	"	"
2	Same tests, terminal conditions, and limits as subgroup 10 except T_C = -55°C.																						

1/ A = normal clock pulse, except for subgroup 7 and 8 (see 3/).
2/ B = momentary GND, then V_{IN} except for subgroups 7 and 8. For subgroups 1, 2 and 3, $V_{IN} = V_{CC}$; for subgroups 9, 10 and 11, V_{IN} = 3.0 V minimum (see figure 11).
3/ For subgroups 7 and 8, A = V_{CC} and B = GND.
4/ Output voltages shall be either:
  (a) H = 2.4 V minimum and L = 0.4 V maximum when using a high speed checker double comparator, or
  (b) H $\geq$ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
5/ The tests in subgroups 7 and 8 shall be performed in the sequence specified.
6/ Only a summary of attributes data is required.
7/ For device type 06, schematic circuits A and B, the minimum and maximum limits shall be -0.4 and -1.3 mA, respectively. For schematic C, the minimum and maximum limits shall be -0.7 and -1.6 mA, respectively.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but it not mandatory)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.
b. PIN and compliance identifier, if applicable (see 1.2).
c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
d. Requirement for certificate of compliance, if applicable.
e. Requirements for notification of change of product or process to acquiring activity in addition to notification to the qualifying activity, if applicable.
f. Requirements for failure analysis (including required test condition of method 5003), corrective action and reporting of results, if applicable.
g. Requirements for product assurance options.
h. Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
i. Requirements for "JAN" marking.
j. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

GND .... Electrical ground (common terminal)
V_{IN} .... Voltage level at an input terminal
I_{IN} .... Current-flowing into an input terminal

6.6 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer lead lengths and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-35810 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Device type	Commercial type
01	5495
02	5496
03	54164
04	54165
05	54194
06	54195

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA - CC

Preparing activity:
DLA - CC

(Project 5962-2091)

Review activities:
Army - MI, SM
Navy - AS, CG, MC, SH, TD
Air Force - 03, 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.