HV96001

Secondary-Side, Micro-Interfaced, Flicker-Free LED Controller with Enhanced PWM and Analog Dimming

FEATURES

- Wide Input Voltage Range: 8V to 60V
- Linear (analog) Dimming:
  - With wide range of amplitude control of the LED current
- Pulse-Width Modulation (PWM) (digital) Dimming:
  - Dims down to 0.01% and lower
  - With PWM pulse width lower than 150 ns
  - PWM dimming frequency up to 20 kHz
- Flyback Converter:
  - With automatic output voltage adjustment for maintaining high system efficiency
- Boost Converter:
  - With near zero output voltage ripple for a ripple-free LED current
  - 100 Hz/120 Hz ripple rejection
  - 200 kHz fixed switching frequency
  - SEPIC topology compatible
- V_{DD} Regulator:
  - 60V input voltage/5V output voltage
  - 10 mA drive for supplying external loads
- Fault Recovery with Auto-Retry Delay Set Using Timing Capacitor
- Undervoltage Detection of:
  - V_{DD} voltage
  - Supply voltage (Flyback output voltage)
- Overvoltage Detection of:
  - LED load voltage (Boost output voltage)
- Overcurrent Detection of:
  - Load switch current
- Stuck-at-Zero Detection of:
  - DIM input signal
- Short Circuit Protection of Output with Auto-Retry Delay

APPLICATIONS

- Offline LED lighting applications featuring wide range for PWM dimming and linear dimming.

PACKAGES

- 16L VQFN, 3 mm x 3 mm
- 16L SOIC, Narrow Body

DESCRIPTION

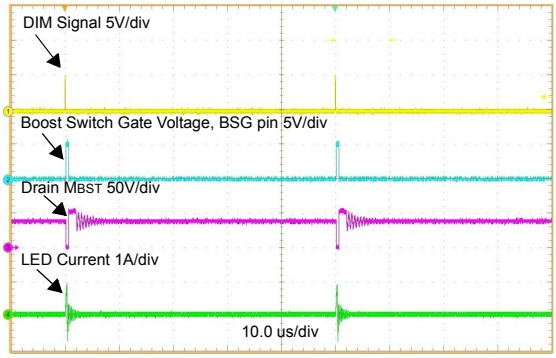
The HV96001 LED driver targets offline lighting applications requiring wide dimming capability. The device is capable of linear dimming and PWM dimming, with the PWM dimming capable of flicker-free dimming down to 0.01% level and lower.

The HV96001 is specifically adapted to LED driver designs that accommodate a wide range of the LED load voltage. The device adjusts the output voltage of the AC to DC conversion stage for maintaining a high conversion efficiency over a wide range of the LED load voltage. It also maintains a precise control over the LED current amplitude, thereby maintaining the consistent color temperature.

The adaptability of the device to wide range PWM dimming allows for a stable control of the LED current waveform for PWM dimming pulse widths down to 150 ns and lower.

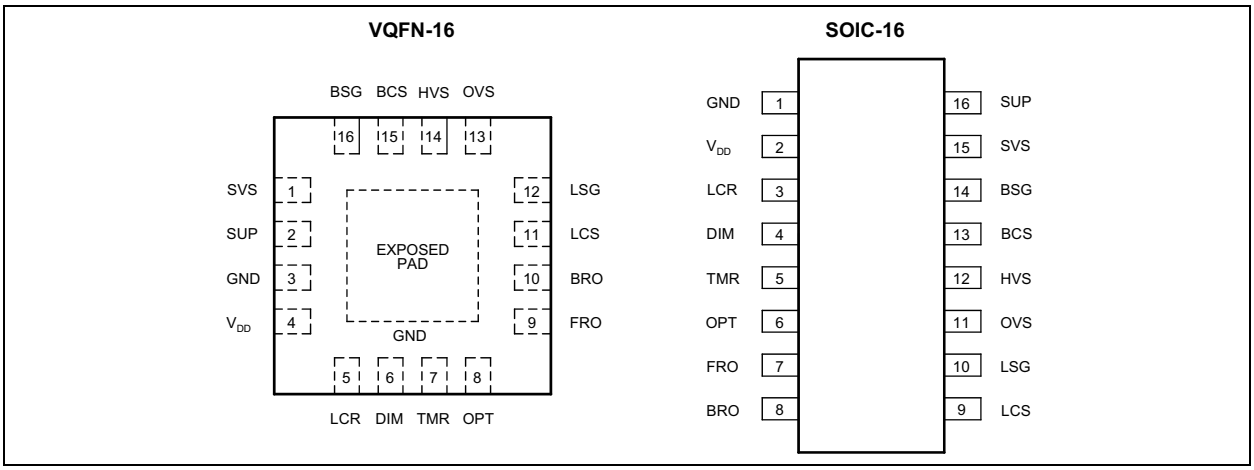
The HV96001 driver IC adjusts the flyback converter output voltage such that the boost converter (BC) operates with a small difference between the boost converter input and output voltage, also referred to as the headroom voltage. Operating the boost converter with a small headroom voltage, or, more or less equivalent, operating with a small voltage step-up ratio allows the boost converter to be physically small and operate at a higher efficiency.

The HV96001 includes two feedback regulators, the flyback regulator for control of the flyback output voltage and the boost regulator for control of the LED current amplitude. An optocoupler driver circuit drives the optocoupler, which in turn provides a control signal for driving the control input of the flyback converter.

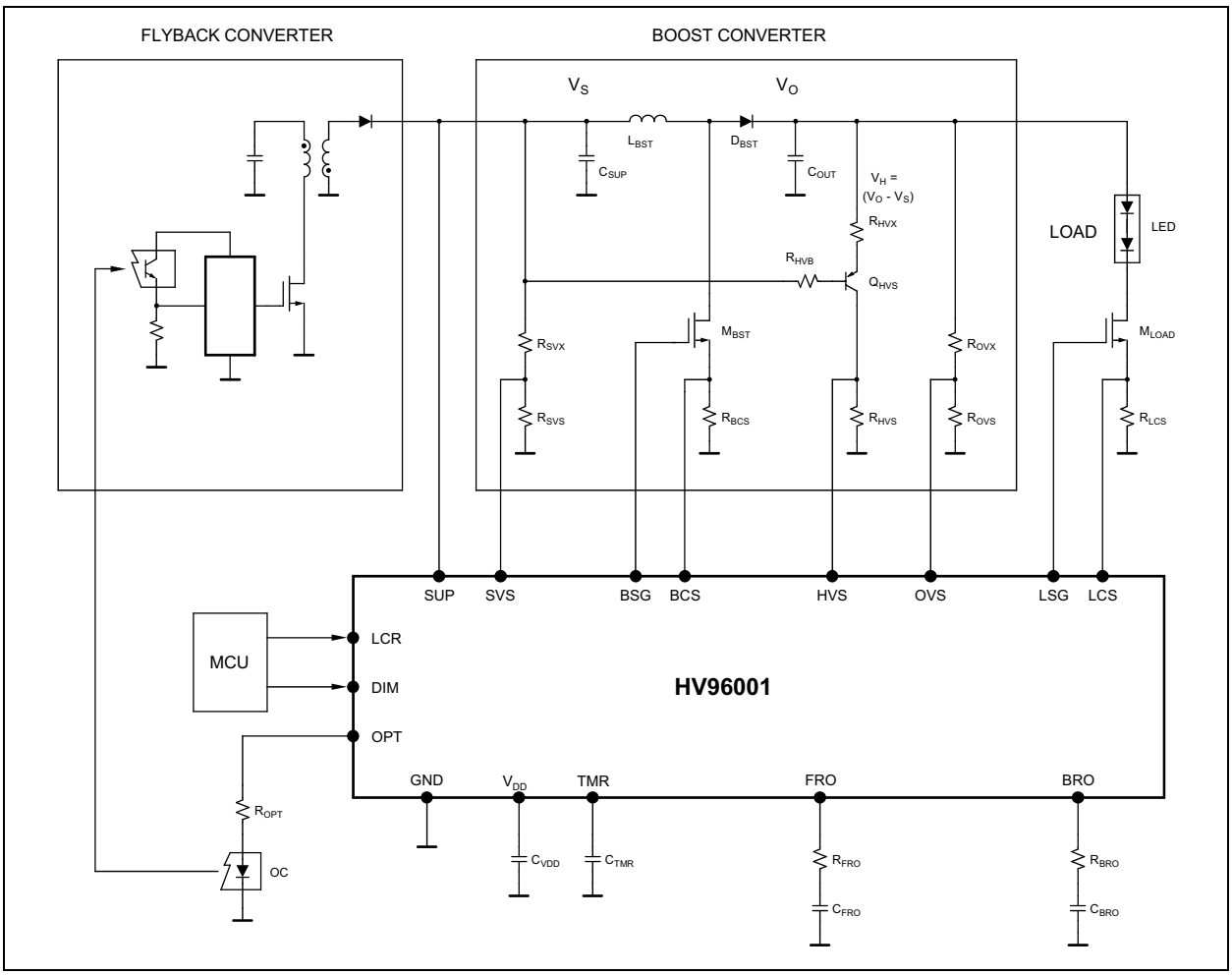


Regular Operation, 20 kHz DIM 0.3% Duty.

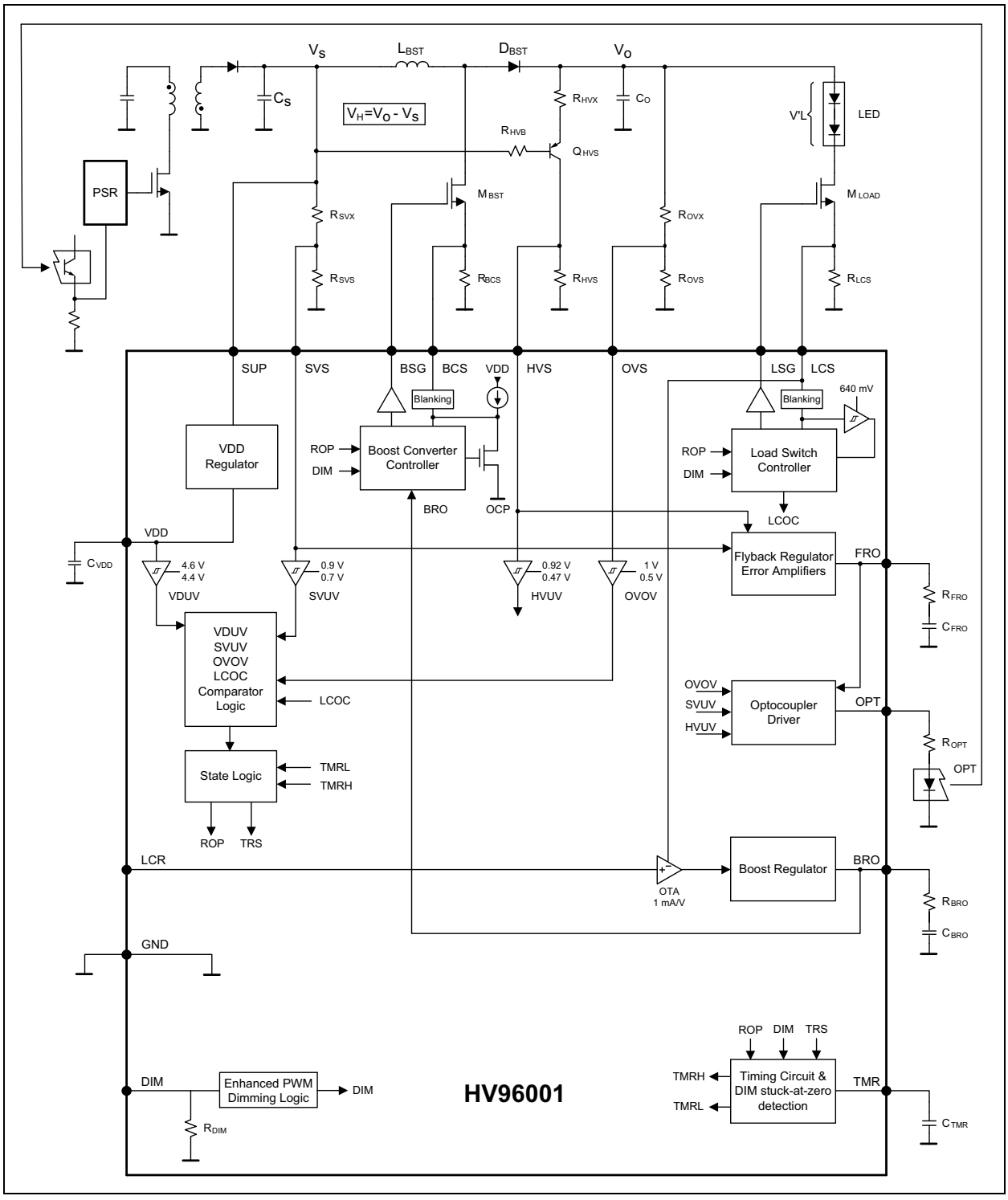
PACKAGE TYPES



TYPICAL APPLICATIONS CIRCUIT



BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

1.1 Electrical Specifications

Absolute Maximum Ratings(†)

V_{SUP} ..... -0.3V to +65V

V_{DD} ..... 0.3V to +6V

All other pin voltages ..... -0.3V to V_{DD} +0.3V

I_{ZHVS}, maximum clamp current at HVS pin ..... 2 mA

Power Dissipation at +25°C (16L VQFN) 0.24W

Power Dissipation at +25°C (16L SOIC) 0.24W

Maximum Junction Temperature ..... +150°C

Lead Soldering Temperature for 10s ..... +300°C

ESD voltage HBM (LV pin only) 2000V

ESD voltage HBM (HV pin only) (SUP) 750V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

General conditions: $T_A = T_J = 25°C$, $V_{SUP} = 8V$, $C_{VDD} = 1\ \mu F$, $C_{BSG} = 2\ nF$, $C_{LSG} = 500\ pF$, $R_{OPT} = 1\ M\Omega$, $I_{EXT} = 0\ mA$, $V_{DIM} = V_{DD} = 5V$, unless otherwise mentioned.
Boldface specifications apply over the recommended ambient temperature ($T_A = T_J$) range of -40 °C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Device Supply (SUP)						
Supply Voltage Range	V_{SUP}	**8**	—	**60**	V	
Supply Current, boost converter not switching	I_{SUP1}	—	—	1.5	mA	V_{SVS} = 1.1V, V_{HVS} = 1.1V, V_{DIM} = 0V
Supply Current, boost converter switching	I_{SUP2}	—	3.5	—		V_{SVS} = 1.1V, V_{HVS} = 1.1V, V_{DIM} = 5V
V_{DD} Supply (V_{DD})						
V_{DD} Voltage	V_{DD}	**4.85**	5.075	**5.30**	V	V_{SUP} = 8V, 60V
V_{DD} Undervoltage Lower Threshold	VL_{VDUV}	**4.2**	4.4	**4.6**		V_{DD} falling
V_{DD} Undervoltage Upper Threshold	VU_{VDUV}	—	4.6	—		V_{DD} rising, (**Note 1**)
Output Voltage Drop	VD_{VDD}	—	—	20	mV	I_{EXT} = 10 mA
External Current Draw Capacity	I_{EXT}	—	—	10	mA	
Supply Voltage Sense (SVS)						
Supply Undervoltage Lower Threshold	VL_{SVUV}	—	0.7	—	V	V_{SUP} falling, (**Note 1**)
Supply Undervoltage Upper Threshold	VU_{SVUV}	**0.85**	0.9	**1**		V_{SUP} rising
Boost Switch Gate Driver (BSG)						
Sourcing Current	$ISRC_{BSG}$	0.14	—	—	A	V_{BSG} = 0V, V_{BCS} = 0V
Sinking Current	$ISNK_{BSG}$	0.40	—	—		V_{BSG} = 5V, V_{BCS} = 2V

Note 1: Specification is obtained by characterization and is not 100% production tested.

2: Specification is for design guidance only.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

General conditions: $T_A = T_J = 25°C$, $V_{SUP} = 8V$, $C_{VDD} = 1\ \mu F$, $C_{BSG} = 2\ nF$, $C_{LSG} = 500\ pF$, $R_{OPT} = 1\ M\Omega$, $I_{EXT} = 0\ mA$, $V_{DIM} = V_{DD} = 5V$, unless otherwise mentioned.
Boldface specifications apply over the recommended ambient temperature ($T_A = T_J$) range of -40 °C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Boost Current Sense (BCS)						
Switching Frequency	F_{SW}	**180**	200	**220**	kHz	
Maximum Switch Duty	D_{MAX}	48	—	52	%	
Leading Edge Blanking Time	BT_{BCS}	**30**	—	**80**	ns	
BCS to BSG Propagation Delay	T_{BPD}	—	—	**110**		V_{BRO} = 4.8V, V_{BCS} 50 mV overdrive
Attenuation, Divider Input to Divider Output	K_{DIV}	—	10	—	V/V	
Peak Current Threshold 1	V_{BCS1}	90	130	170	mV	V_{BRO} = 1.8V
Peak Current Threshold 2	V_{BCS2}	390	410	430	mV	V_{BRO} = 4.8V
Headroom Voltage Sense (HVS)						
Clamping Voltage	VZ_{HVS}	3.70	4.3	4.9	V	I_{HVS} = 2 mA
Headroom Undervoltage Lower Threshold	VL_{HVUV}	**0.44**	0.47	**0.50**	V	V_{HVS} falling
Headroom Undervoltage Upper Threshold	VU_{HVUV}	—	0.92	—		V_{HVS} rising, (**Note 1**)
Output Voltage Sense (OVS)						
Bias Current	IOVS	—	0	—	µA	**Note 1**
Output Overvoltage Upper Threshold	VU_{OVOV}	**0.97**	1	**1.03**	V	V_{OVS} rising
Output Overvoltage Lower Threshold	VL_{OVOV}	—	0.5	—		V_{OVS} falling, (**Note 1**)
Load Switch Gate Driver (LSG)						
Output Voltage Rise Time	$TRISE_{LSG}$	—	—	100	ns	10% to 90%
Output Voltage Fall Time	$TFALL_{LSG}$	—	—	100		90% to 10%
Load Current Sense (LCS)						
Load Overcurrent Threshold	VT_{LCOC}	590	640	690	mV	V_{LCS} rising
Leading Edge Blanking Time	BT_{LCS}	600	750	900	ns	DIM rising
Boost Regulator Error Amplifier (BRO)						
Voltage Gain	VG_{BRO}	—	65	—	dB	
Transconductance	G_{BRO}	0.8	1	1.2	mA/V	
Input Offset Voltage	VOS_{BRO}	**-10**	—	**10**	mV	
Sourcing Current	$ISRC_{BRO}$	—	0.4	—	mA	V_{BRO} = 0V, V_{LCR} = 0.5V, V_{LCS} = 0V, (**Note 1**)
Sinking Current	$ISNK_{BRO}$	—	0.2	—		V_{BRO} = 4V, V_{LCR} = 0V, V_{LCS} = 0.5V, (**Note 1**)
90% Amplifier Rise Time upon DIM enable	T_{BRO}	—	50	—	µs	V_{LCS} = 0V, V_{LCR} = 100 mV, C_{BRO} = 1 nF, (**Note 1**)
Zero Switch Resistance	RZSW	—	300	—	Ω	**Note 1**
Flyback Regulator Error Amplifiers (FRO)						
Voltage Gain, low gain	VG_{FROL}	—	65	—	dB	
Transconductance, low gain	G_{FROL}	160	200	270	µA/V	
Sourcing Current, low gain	$ISRC_{FROL}$	40	90	—	µA	V_{FRO} = 0V, V_{HVS} = 1.2V
Sinking Current, low gain	$ISNK_{FROL}$	40	60	—		V_{FRO} = 5V, V_{HVS} = 0.5V
Headroom Reference Voltage, low gain	VH_{FROL}	0.95	1	1.05	V	
Voltage Gain, high gain	VG_{FROH}	—	65	—	dB	

Note 1: Specification is obtained by characterization and is not 100% production tested.
2: Specification is for design guidance only.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

General conditions: $T_A = T_J = 25°C$, $V_{SUP} = 8V$, $C_{VDD} = 1\ \mu F$, $C_{BSG} = 2\ nF$, $C_{LSG} = 500\ pF$, $R_{OPT} = 1\ M\Omega$, $I_{EXT} = 0\ mA$, $V_{DIM} = V_{DD} = 5V$, unless otherwise mentioned.
Boldface specifications apply over the recommended ambient temperature ($T_A = T_J$) range of -40 °C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Transconductance, high gain	G_{FROH}	680	860	1040	µA/V	
Sourcing Current, high gain	$ISRC_{FROH}$	180	320	—	µA	$V_{FRO} = 0V$, $V_{HVS} = 1.7V$
Minimum Supply Reference Voltage, high gain	VMS_{FROH}	0.95	1	1.05	V	
Headroom Recovery Reference Voltage, high gain	VHR_{FROH}	1.4	1.5	1.6		
Optocoupler Driver (OPT)						
Down Slope	DS	—	0.8	—	V/V	V_{OPT}/V_{FRO} (**Note 1**)
Output Voltage 1	V_{OPT1}	3.9	4.05	4.2	V	$V_{FRO} = 0V$, $I_{OPT} = 0\ mA$
Output Voltage 2	V_{OPT2}	**0.75**	0.85	**1.01**		$V_{FRO} = 4V$, $I_{OPT} = 0\ mA$
Maximum Output Current	I_{OPT}	5	—	—	mA	
Timer (TMR)						
Charge Current, DIM stuck-at-zero detection	$IDIM_{TMR}$	35	45	55	µA	
Charge Current, auto-retry delay	$IAUT_{TMR}$	4	5	6		
Timer Low Threshold Voltage	VT_{TMRL}	—	100	—	mV	V_{TMR} falling
Timer High Threshold Voltage	VT_{TMRH}	3.95	4.1	4.2	V	V_{TMR} rising
Linear Current Reference (LCR)						
LCR Bias Current	I_{LCR}	—	0	—	µA	(**Note 1**)
PWM Dimming Reference (DIM)						
DIM Bias Current	I_{DIM}	—	0	—	µA	$V_{DIM} = 0V$, (**Note 1**)
Pull Down Resistor	R_{DIM}	100	150	200	kΩ	
Minimum pulse width to start boost switching	T_{DIM}	—	75	—	ns	DIM = 400 Hz
Logic Low Threshold	V_{LO}	—	—	0.8	V	
Logic High Threshold	V_{HI}	2	—	—	V	

Note 1: Specification is obtained by characterization and is not 100% production tested.
2: Specification is for design guidance only.

1.2 Temperature Specifications

TABLE 1-2: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_{AMB}	-40	—	+125	°C	
Storage Temperature Range	T_{STO}	-65	—	+150		
Package Thermal Impedances						
Thermal Impedance Junction-to-Ambient, 16L-VQFN	$R\theta_{JAVQFN}$	—	+46	—	°C/W	
Thermal Impedance Junction-to-Case, 16L-VQFN	$R\theta_{JCVQFN}$	—	+12.5	—		
Thermal Impedance Junction-to-Ambient, 16L-SOIC	$R\theta_{JASOIC}$	—	+63	—		
Thermal Impedance Junction-to-Case, 16L-SOIC	$R\theta_{JCSOIC}$	—	+12.5	—		

2.0 TYPICAL OPERATING CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SUP} = 8V, T_A = 25°C, F_{SW} = 200 kHz.

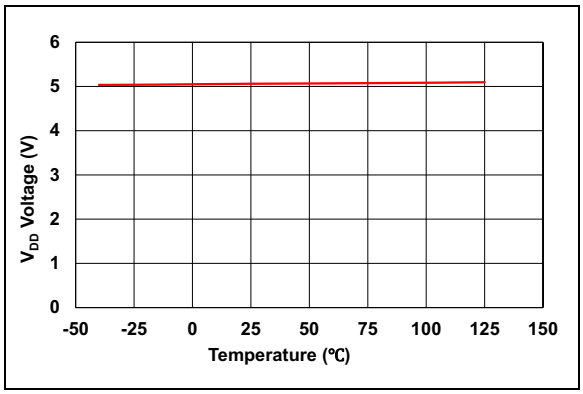


FIGURE 2-1: *V_{DD} Voltage vs. Temperature.*

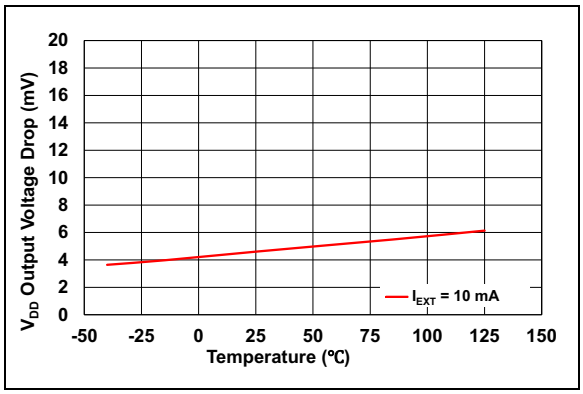


FIGURE 2-4: *V_{DD} Output Voltage Drop vs. Temperature.*

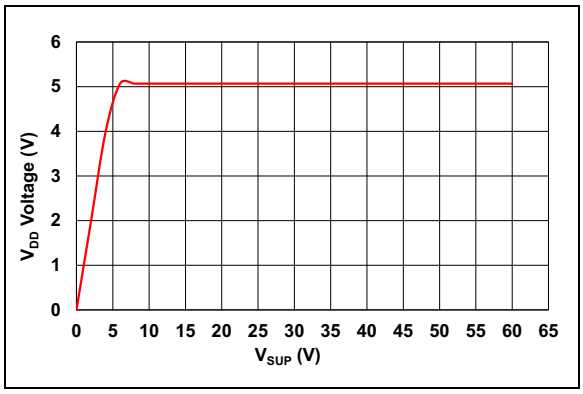


FIGURE 2-2: *V_{DD} Voltage vs. Supply Voltage.*

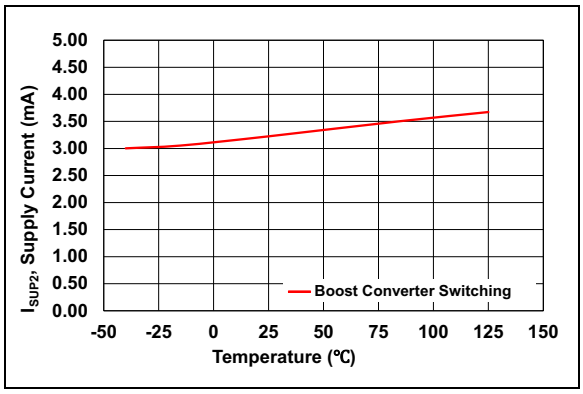


FIGURE 2-5: *Supply Current vs. Temperature (Boost Converter Switching).*

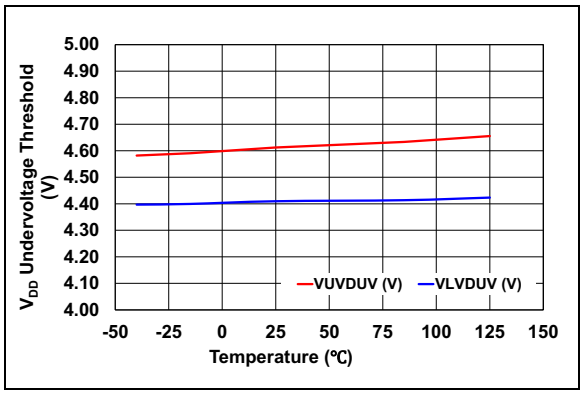


FIGURE 2-3: *V_{DD} Undervoltage Threshold vs. Temperature.*

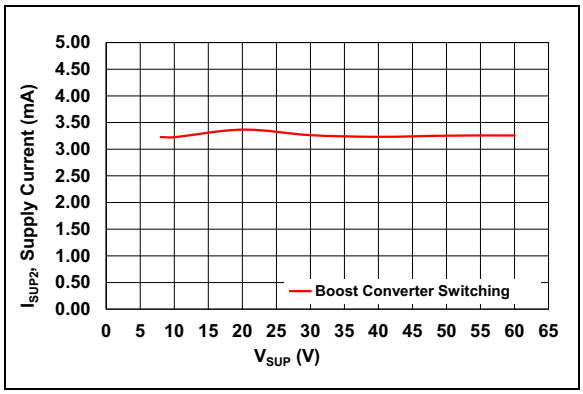


FIGURE 2-6: *Supply Current vs. Supply Voltage (Boost Converter Switching).*

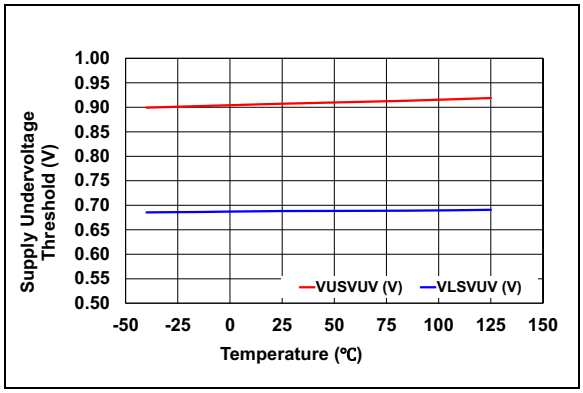


FIGURE 2-7: *Supply Undervoltage Threshold vs. Temperature.*

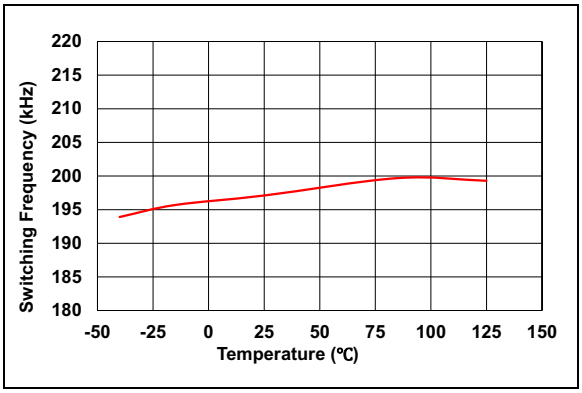


FIGURE 2-10: *Switching Frequency vs. Temperature.*

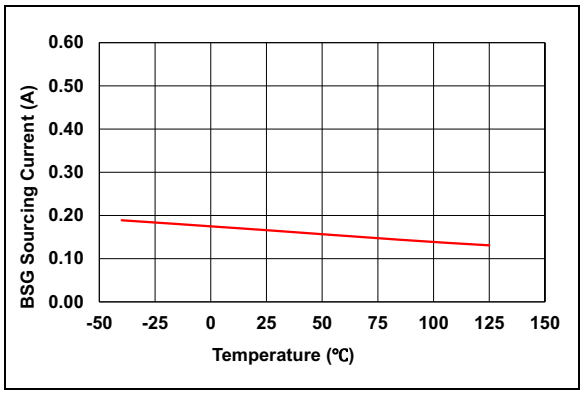


FIGURE 2-8: *BSG Sourcing Current vs. Temperature.*

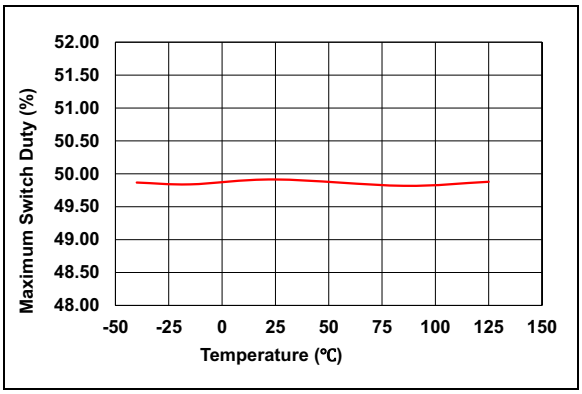


FIGURE 2-11: *Maximum Switch Duty vs. Temperature.*

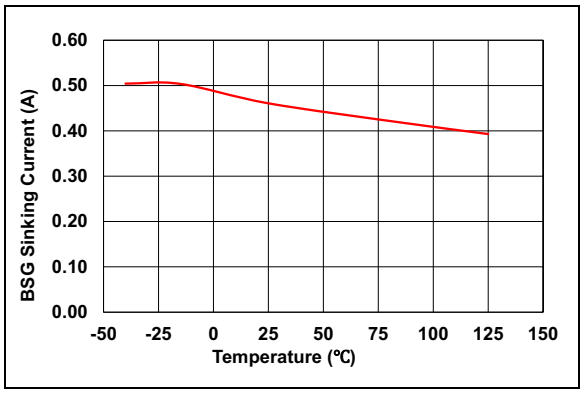


FIGURE 2-9: *BSG Sinking Current vs. Temperature.*

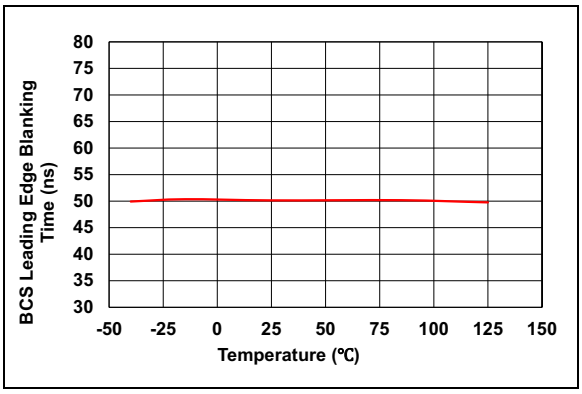


FIGURE 2-12: *BCS Leading Edge Blanking Time vs. Temperature.*

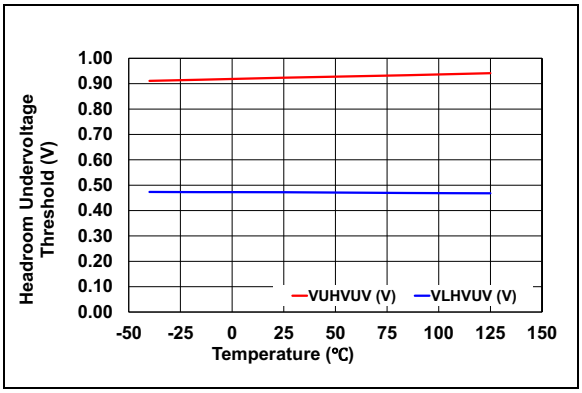


FIGURE 2-13: *Headroom Undervoltage Threshold vs. Temperature.*

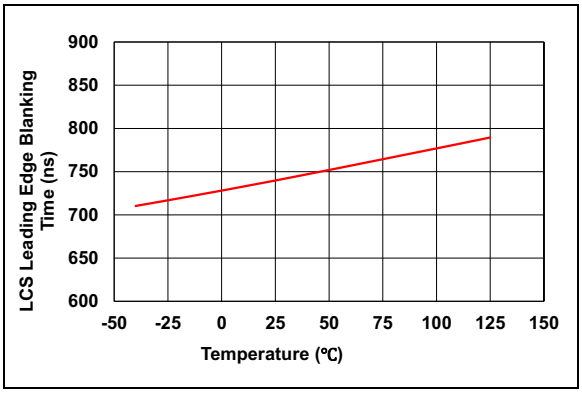


FIGURE 2-16: *LCS Leading Edge Blanking Time vs, Temperature.*

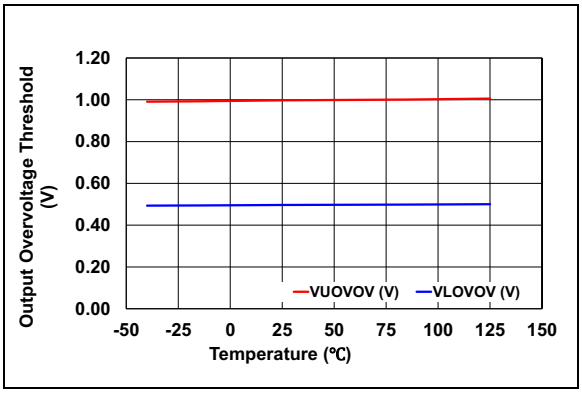


FIGURE 2-14: *Output Overvoltage Threshold vs. Temperature.*

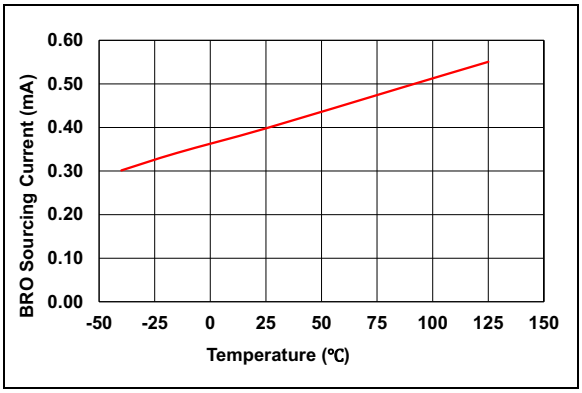


FIGURE 2-17: *BRO Sourcing Current vs. Temperature.*

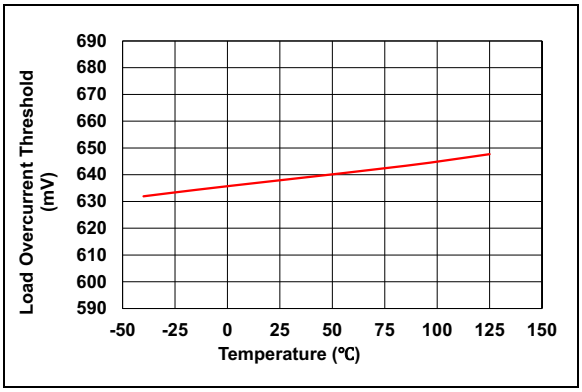


FIGURE 2-15: *Load Overcurrent Threshold vs. Temperature.*

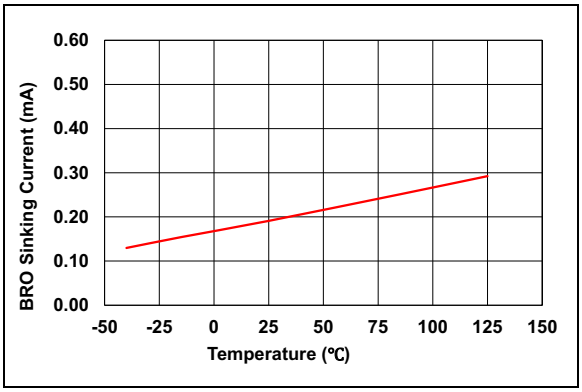


FIGURE 2-18: *BRO Sinking Current vs. Temperature.*

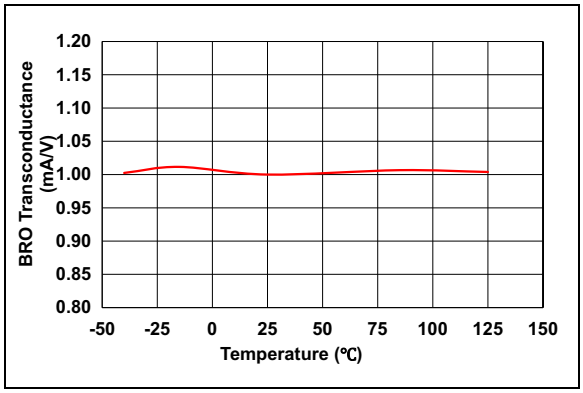


FIGURE 2-19: *BRO Transconductance vs. Temperature.*

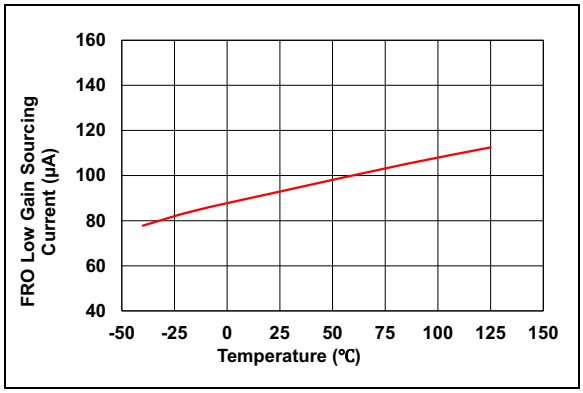


FIGURE 2-22: *FRO Low Gain Sourcing Current vs. Temperature.*

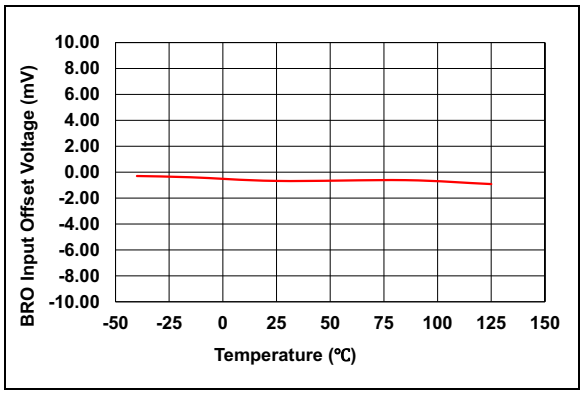


FIGURE 2-20: *BRO Input Offset Voltage vs. Temperature.*

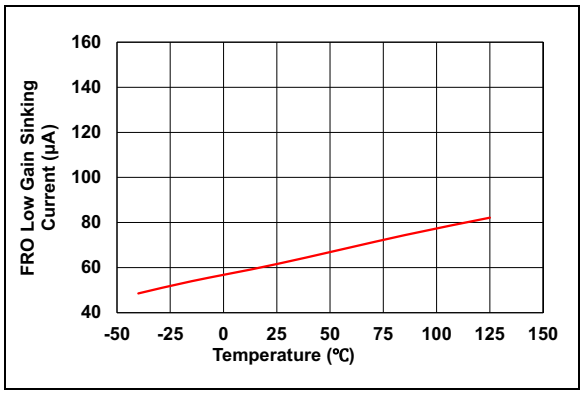


FIGURE 2-23: *FRO Low Gain Sinking Current vs. Temperature.*

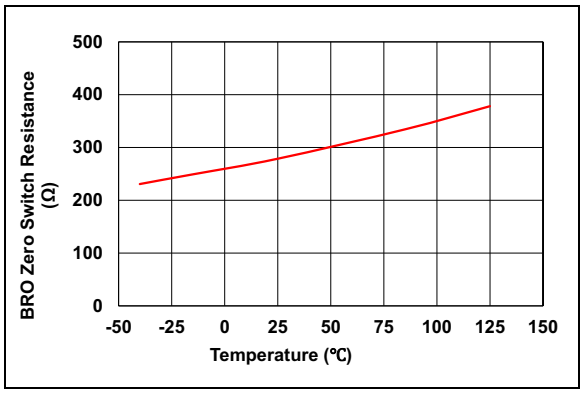


FIGURE 2-21: *BRO Zero Switch Resistance vs. Temperature.*

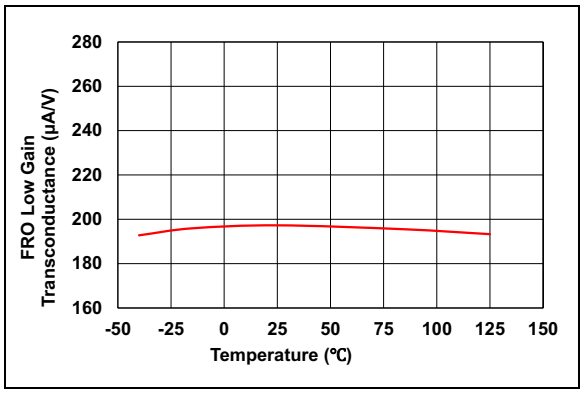


FIGURE 2-24: *FRO Low Gain Transconductance vs. Temperature.*

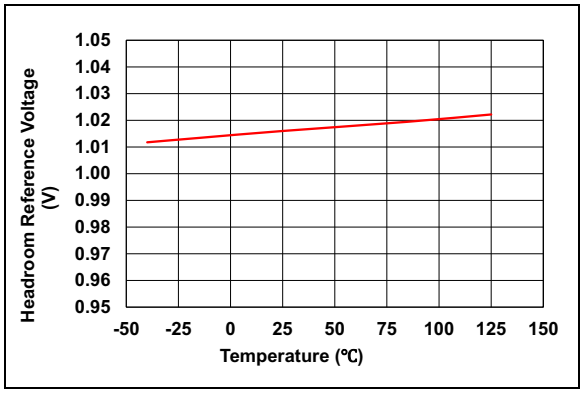


FIGURE 2-25: *Headroom Reference Voltage vs. Temperature.*

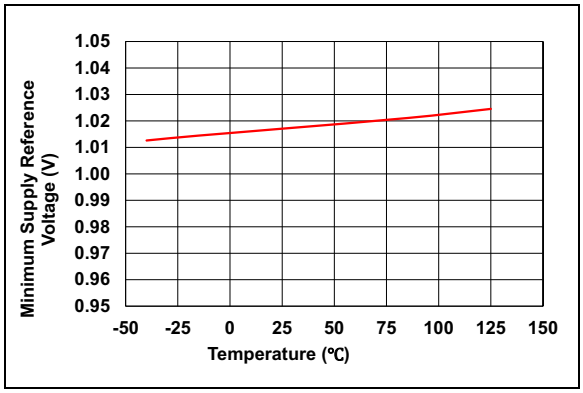


FIGURE 2-28: *Minimum Supply Reference Voltage vs. Temperature.*

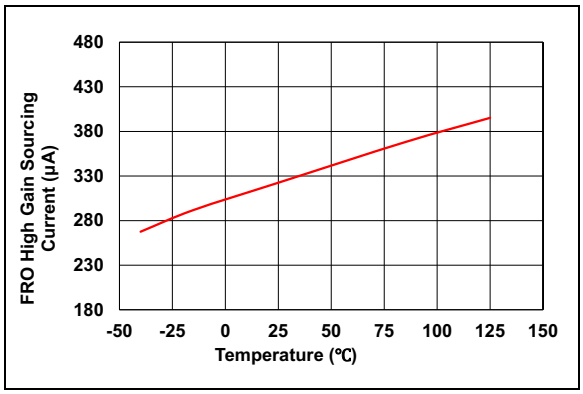


FIGURE 2-26: *FRO High Gain Sourcing Current vs. Temperature.*

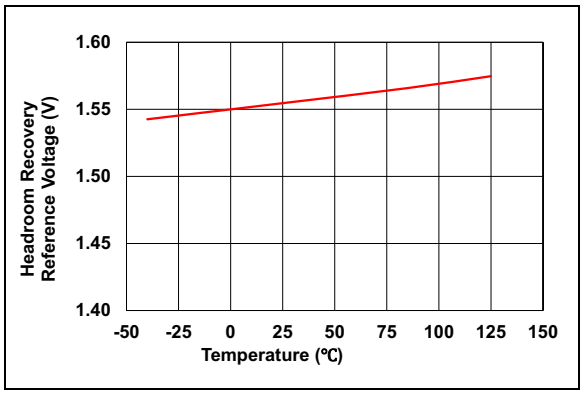


FIGURE 2-29: *Headroom Recovery Reference Voltage vs. Temperature.*

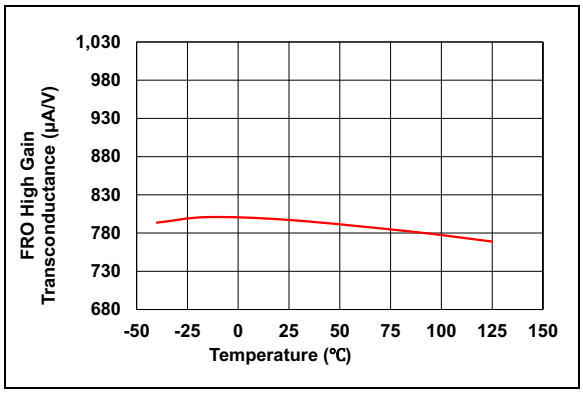


FIGURE 2-27: *FRO High Gain Transconductance vs. Temperature.*

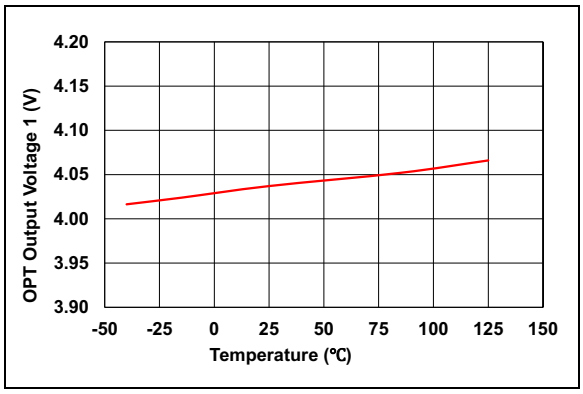


FIGURE 2-30: *OPT Output Voltage 1 vs. Temperature.*

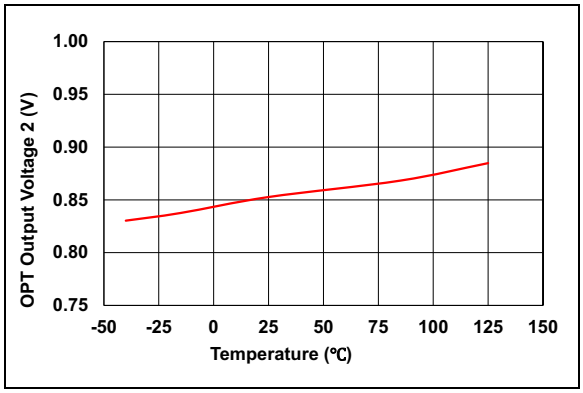


FIGURE 2-31: *OPT Output Voltage 2 vs. Temperature.*

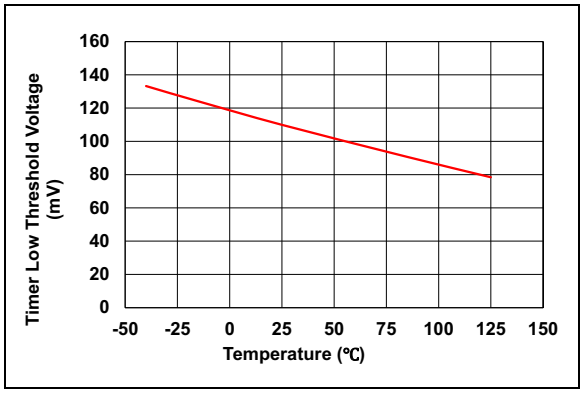


FIGURE 2-34: *Timer Low Threshold Voltage vs. Temperature.*

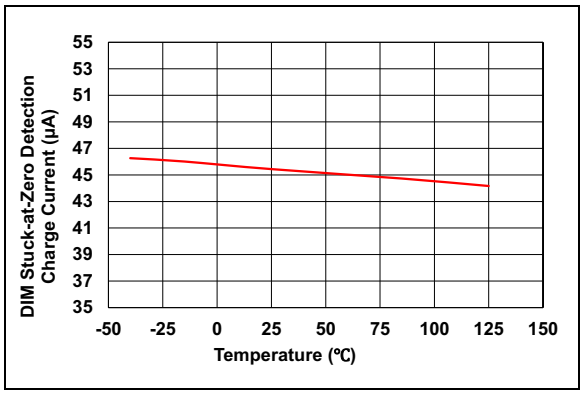


FIGURE 2-32: *DIM Stuck-at-Zero Detection Charge Current vs. Temperature.*

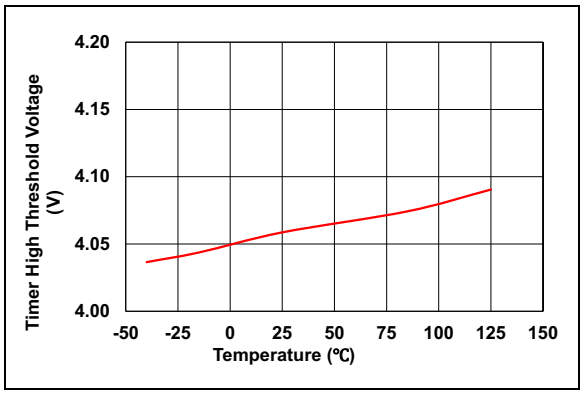


FIGURE 2-35: *Timer High Threshold Voltage vs. Temperature.*

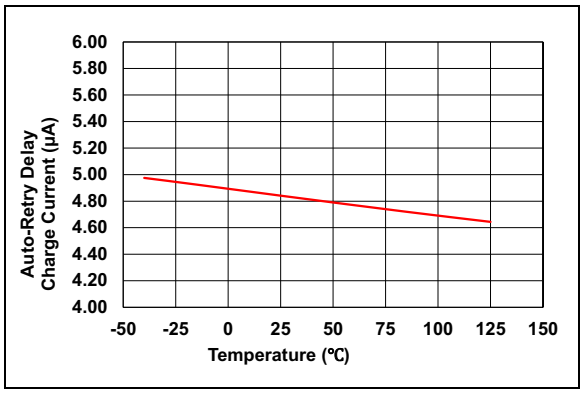


FIGURE 2-33: *Auto-Retry Delay Charge Current vs. Temperature.*

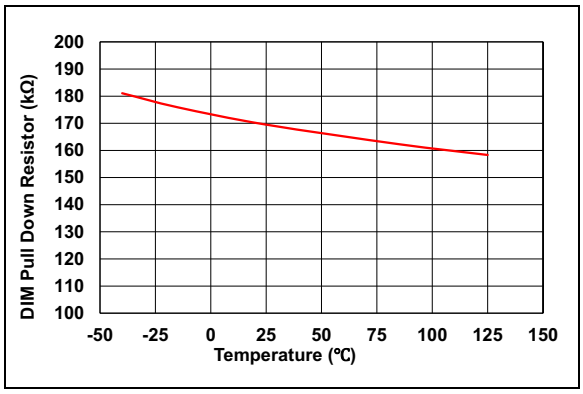


FIGURE 2-36: *DIM Pull Down Resistor vs. Temperature.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN DESCRIPTION

Pin		Name	I/O	Description
VQFN	SOIC			
1	15	SVS	—	Pin for sensing the supply voltage
2	16	SUP	—	Provides supply to the device
3	1	GND	—	Return pin
4	2	V_{DD}	—	Output pin of the V_{DD} regulator
5	3	LCR	I	LED current reference input pin
6	4	DIM	I	PWM dimming input pin
7	5	TMR	—	Timer pin
8	6	OPT	O	Output pin of the optocoupler driver
9	7	FRO	O	Output pin of the flyback regulator
10	8	BRO	O	Output pin of the boost regulator
11	9	LCS	I	Input pin to the LED current sense comparator
12	10	LSG	O	Output pin of the load switch gate driver
13	11	OVS	I	Input pin to the output overvoltage comparator
14	12	HVS	I	Input pin to the headroom voltage sense comparator
15	13	BCS	I	Pin for sensing the boost converter current
16	14	BSG	O	Output pin of the boost switch gate driver
PAD	N/A	GND	—	Return pin. Bottom side exposed pad

3.1 Supply Voltage Sense Pin (SVS)

The supply voltage sense pin voltage is proportional to the supply voltage (V_S) and is derived by the means of a resistive divider (R_{SVS}, R_{SVX}). It is the inverting input to the flyback regulator's headroom voltage recovery error amplifier and the input to the supply undervoltage comparator.

3.2 Device Supply Pin (SUP)

The supply voltage (V_S) connection, which is the output of the flyback converter and the input to the boost converter.

3.3 Ground Pin (GND)

Ground pin.

3.4 V_{DD} Regulator Output Pin (V_{DD})

The V_{DD} regulator is rated for an output voltage of 5V and an output current of 25 mA when supplied with a voltage ranging from 8V to 60V.

3.5 LED Current Reference Pin (LCR)

The LED current reference pin is the noninverting input to the boost regulator error amplifier with a maximum level of the linear current reference to be 400 mV.

3.6 PWM Dimming Pin (DIM)

In regular operation, the DIM signal may be either continuously high, or continuously low, or a square wave signal of a given frequency and duty. The suggested PWM dimming frequency is 400 Hz.

3.7 Timer Pin (TMR)

The timer pin voltage is the output of the timing circuitry. This voltage determines the condition asserted by the timer voltage comparator.

3.8 Optocoupler Driver Pin (OPT)

The optocoupler drive pin output voltage provides a control signal for driving the control input of the flyback converter.

3.9 Flyback Regulator Output Pin (FRO)

The voltage at the flyback regulator output pin is converted into a voltage for driving the optocoupler, by the optocoupler driver circuit.

3.10 Boost Regulator Output Pin (BRO)

The boost regulator output pin provides an output signal for control of the boost converter output voltage and output current.

3.11 LED Current Sense Pin (LCS)

The LED current sense pin is the input to the LED overcurrent comparator in the load switch controller.

3.12 Load Switch Gate Driver Pin (LSG)

The load switch gate driver pin is the output of the load switch controller, which drives the load side MOSFET.

3.13 Output Voltage Sense Pin (OVS)

The output voltage sense pin is the input to a comparator that monitors the output overvoltage condition. The voltage at the OVS pin is proportional to the output voltage (V_O) and is derived by means of a resistive divider (R_{OVS}, R_{OVX}).

3.14 Headroom Voltage Sense Pin (HVS)

The headroom voltage sense pin is the noninverting input to the flyback regulator's headroom voltage error amplifier and minimum supply error amplifier. It is also the input to the headroom undervoltage comparator.

3.15 Boost Current Sense Pin (BCS)

The boost current sense pin provides the inductor current sense signal, which is the input to the boost converter controller.

3.16 Boost Switch Gate Driver Pin (BSG)

The boost switch gate driver pin is the output of the boost converter controller, which drives the boost converter's MOSFET.

4.0 FUNCTIONAL DESCRIPTION

4.1 Introduction

The HV96001 LED driver IC is targeted at offline lighting applications requiring wide dimming range and galvanic isolation. It is particularly adapted to wide range PWM dimming, featuring stable control of the LED current waveform for PWM dimming pulse widths down to 150 ns.

A HV96001 based LED driver includes a flyback converter, a boost converter and a load switch, as shown in the typical applications circuit diagram. This driver architecture allows negligible LED current ripple, high conversion efficiency over a wide range of LED load voltage and a fast response to change in dimming parameters.

The boost converter steps up the flyback converter output voltage to a near zero ripple voltage. The load switch in series with the LED load provides fine control over the LED current pulse width and provides overcurrent protection.

The HV96001 driver IC adjusts the flyback converter output voltage such that the boost converter operates with a small difference between boost converter input and output voltage, also known as the headroom voltage. Operating the boost converter with a small headroom voltage, or, more or less equivalent, operating with a small voltage step-up ratio allows the boost converter to be physically small. This further allows both the flyback converter and the boost converter to operate at a high efficiency over a wide range of the LED load voltage.

4.2 Regulator Architecture

The HV96001 includes two feedback regulators, the flyback regulator for control of the flyback output voltage and the boost regulator for control of the LED current amplitude.

An optocoupler driver circuit translates the flyback regulator output voltage into a voltage for driving an optocoupler, which in turn provides a control signal for driving the control input of the flyback converter.

The device includes logic controls, in part implemented as finite state machines, for mode control of various functions, and a timer with an external timing capacitor for timing the auto-retry delay and the trigger delay of the DIM stuck-at-zero detection.

4.2.1 FLYBACK REGULATOR

The flyback regulator provides a reference signal for controlling flyback converter output power, and, thereby, controlling flyback converter output voltage and boost converter headroom voltage. The regulator includes three transconductance error amplifiers and a gain network being a series RC-network (R_{FRO}, C_{FRO}) attached to ground.

4.2.1.1 Headroom Voltage Error Amplifier

The headroom voltage error amplifier is responsible for maintaining the target boost converter headroom voltage, the target being set by an external divider network.

The headroom voltage error amplifier dominates the flyback regulator response when the driver operates in Steady state or near Steady state.

The headroom reference voltage (VH_{FROL}) is internally set to 1V.

4.2.1.2 Minimum Supply Voltage Error Amplifier

The minimum supply voltage error amplifier is responsible for maintaining the flyback converter output voltage at a given minimum level, the minimum supply voltage level being set by an external divider network.

The supply voltage error amplifier dominates the flyback regulator response when the flyback converter output voltage is less than a given minimum level, the minimum level necessary for efficient operation of the boost converter.

The reference voltage for the minimum supply voltage error amplifier (VMS_{FROH}) is set to 1V.

4.2.1.3 Headroom Voltage Recovery Error Amplifier

The headroom voltage recovery error amplifier is generally active when a sudden and large increase in LED load power occurs, which causes an excess drop in flyback converter output voltage and excess increase in headroom voltage.

The headroom voltage recovery error amplifier dominates the regulator response when the headroom voltage is one and a half times larger than the target headroom voltage level. The excess headroom voltage is corrected by a fast increase in flyback regulator output voltage.

The reference voltage for the headroom recovery error amplifier (VHR_{FROH}) is set to 1.5V.

4.2.2 BOOST REGULATOR

The boost regulator provides an output signal for control of the boost converter output voltage and output current.

More precisely, the boost regulator output drives a FET follower having a high-impedance input, the follower output driving a resistive voltage divider with an attenuation factor of ten times, the attenuator output driving the control input of the boost converter, and the control input providing the target level of the boost

inductor current peak amplitude required for operating a boost converter with a Current-mode control method.

4.2.2.1 Control Amplifier

The boost regulator includes a typical configuration of an error amplifier and a gain network, the error amplifier being a transconductance amplifier and the gain network being a series RC-network (R_{BRO}, C_{BRO}) attached to ground. The amplifier is active during the regular operation mode of the driver and is otherwise shorted to ground during start-up and Fault mode.

4.2.2.2 Dimmed Operation

The boost regulator circuit is adapted to the needs of PWM dimming at very narrow pulse widths.

The output stage of the error amplifier is disconnected from the boost regulator (BRO) node when DIM is low and reconnected when DIM is high. Doing so effectively puts the regulator into a Sleep mode when DIM is low.

Dimming at narrow pulse widths imposes the need for high-speed circuitry and low parasitics in terms of leakage current and charge injection, whether injected internally to the IC or externally.

4.2.2.3 High-Speed Circuitry

One aspect is the speed of response of all components within the LED current control loop to a change of state of the DIM signal, one component being the error amplifier output stage switch.

All components that are part of the control loop need to establish voltage and current levels fast. These components include:

- The load switch and associated gate driver,
- The LED current sense (feedback) network, and
- The error amplifier and associated disconnect switch.

Note that a slow responding load switch or slow responding current sense network can cause significant LED current regulation error. Lag in establishing the LED current and a lag in establishing the LED current sense signal causes the true level of the LED current to be underreported. Accordingly, the control loop will command a larger than required LED current to compensate.

4.2.2.4 Leakage Current and Charge Injection

Leakage current and charge injection at the output side of the error amplifier, whether originated from within the HV96001 device or from external circuitry, can cause significant voltage drift at the boost regulator output node when the DIM signal is low for an extended time period. The drift can be substantial when the DIM duty is small.

Leakage is one reason for giving the error amplifier a large transconductance, as operating at a higher current level will reduce the impact of leakage current and charge injection.

4.2.2.5 DIM Stuck-at-Zero Condition

The DIM stuck-at-zero condition detects the presence of a prolonged DIM low condition, which can lead to a large drift in the boost regulator output voltage. The occurrence of a DIM stuck-at-zero condition is to cause a restart of the LED driver with an auto-retry delay.

4.3 Driver Modes

LED driver operation can be characterized by one of the three modes:

4.3.1 START-UP

The start-up of the LED driver is primarily concerned with establishing the flyback converter output voltage at a minimum supply voltage level, the level being set by an external voltage divider.

During start-up, the flyback converter is more or less under control of the flyback regulator first error amplifier, which is responsible for maintaining the flyback converter output voltage at a minimum given level.

The boost converter and the load switch are turned off and the boost regulator output is connected to ground.

4.3.2 REGULAR OPERATION

The LED driver transitions to regular operation when the flyback converter output voltage reaches the given minimum supply voltage level. The boost converter, boost regulator and the load switch are enabled. The boost converter and the load switch turn on when the DIM signal is high and turn off when the DIM signal is low.

When the LED load power is steady or is changing slowly, the action of the flyback regulator headroom voltage error amplifier suffices to keep the boost converter headroom voltage at a given level.

The timer resets when the DIM signal is high and runs for timing the DIM stuck-at-zero detection when the DIM signal is low. During regular operation, a current of 45 µA is sourced towards the timer (TMR) pin for timing the DIM stuck-at-zero condition.

When the LED load power makes a sudden and large increase, the flyback converter output voltage drops and thus the boost headroom voltage rises. As a consequence, when the headroom voltage rises above one and a half times the target headroom voltage, it triggers the action of the headroom voltage recovery error amplifier, which then quickly raises the flyback converter output voltage to return the headroom voltage to the target level.

When the LED load power makes a sudden and large decrease, the flyback converter output voltage may rise to such an extent that the headroom voltage becomes too low for regular operation. A loss of headroom voltage to half its target level triggers the headroom undervoltage comparator, which in turn shuts the flyback converter down to keep the headroom voltage from dropping even further. The comparator releases the shutdown action when the headroom voltage returns to 90% of the target level.

4.3.3 FAULT

The driver transitions to the Fault mode when certain abnormal conditions occur during either start-up or regular operation.

In Fault mode, the boost converter and the load switch are turned off, and the boost regulator gain setting network is discharged to ground. The flyback converter continues operation being under control of the three error amplifiers of the flyback regulator.

The course of action taken upon entering Fault mode depends on the condition encountered, as shown in the State Transitions diagram. The five Fault conditions are as follows:

4.3.3.1 V_{DD} Undervoltage Fault (VDUV)

A V_{DD} undervoltage condition is treated as a Fault when it occurs during a later part of start-up or during regular operation. This Fault is followed by an immediate driver restart.

The driver enters into Fault mode when the V_{DD} voltage falls below the V_{DD} undervoltage lower threshold (VL_{VDUV}) voltage of 4.4V and restarts when the V_{DD} voltage crosses the V_{DD} undervoltage upper threshold (VU_{VDUV}) voltage of 4.6V.

4.3.3.2 Supply Undervoltage Fault (SVUV)

A supply undervoltage condition is treated as a Fault when it occurs during regular operation. This Fault is followed by an immediate driver restart.

The driver enters into Fault mode when the voltage at the supply voltage sense (SVS) pin falls below the supply undervoltage lower threshold (VL_{SVUV}) voltage of 0.7V and restarts when the voltage at the SVS pin crosses the supply undervoltage upper threshold (VU_{SVUV}) voltage of 0.9V.

4.3.3.3 LED Overcurrent Fault (LCOC)

An LED overcurrent condition is treated as a Fault when it occurs during either start-up or regular operation. The driver remains in Fault mode as long as the condition persists. Once the condition is cleared, the driver restarts after an auto-retry delay.

The driver enters into Fault mode when the voltage at the load current sense (LCS) pin crosses 640 mV. As long as the LED overcurrent condition is present, the driver remains in the Fault mode and transitions to the Auto-Retry Delay mode when the condition clears. A current of 5 µA is sourced for timing the auto-retry delay. Finally, the driver restarts when the timer capacitor voltage reaches the high-voltage condition, thereby signaling the end of the auto-retry period.

The auto-retry delay period is determined by the size of the timing capacitor, the magnitude of the charging current and the timer high threshold (VT_{TMRH}) voltage.

For reference, a timing capacitor of 0.22 µF with a charging current of 5 µA and a timer high threshold of 4.1V corresponds to a Fault timer delay of approximately 180 ms.

Note that the timer charging current can assume one of two values. The charging current is 5 µA during auto-retry delay timing and 45 µA during regular operation, where the DIM stuck-at-zero timing is activated when the DIM signal is low.

4.3.3.4 Output Overvoltage Fault (OVOV)

An output overvoltage condition (boost converter output overvoltage/LED load overvoltage) is treated as a Fault when it occurs during either start-up or regular operation. The driver remains in Fault mode as long as the condition persists. Once the condition is cleared, the driver restarts after an auto-retry delay.

The driver enters into Fault mode when the voltage at the output voltage sense (OVS) pin rises above the output overvoltage upper threshold (VU_{OVUV}) voltage of 1V and restarts after an auto-retry delay when the voltage at the OVS pin falls below the output overvoltage lower threshold (VL_{OVOV}) voltage of 0.5V.

4.3.3.5 DIM Stuck-at-Zero Fault

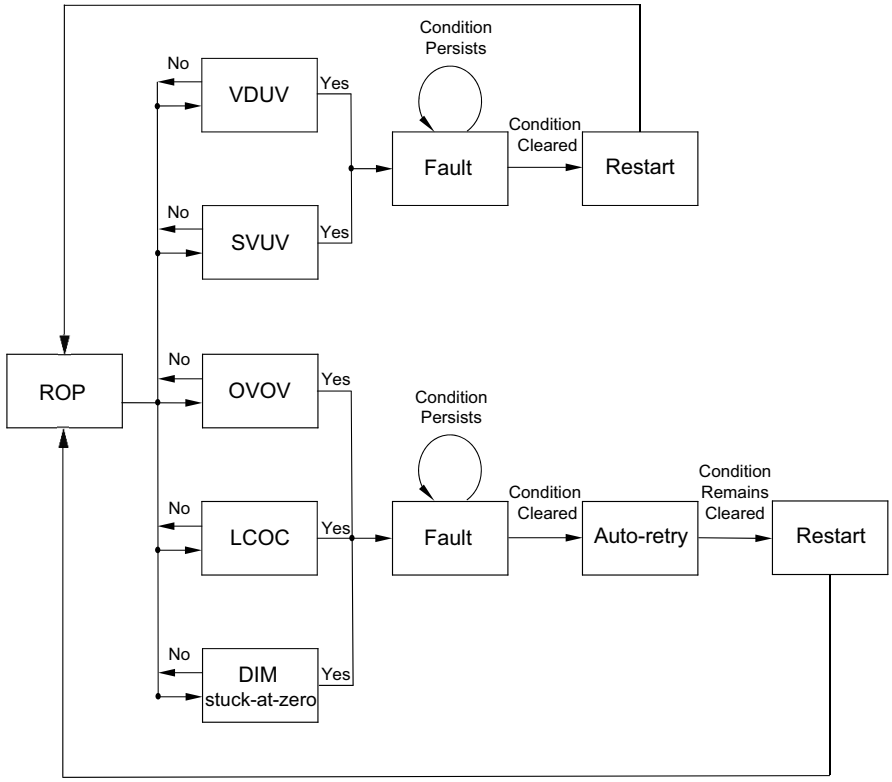
A DIM stuck-at-zero condition is treated as a Fault when it occurs during regular operation.

A prolonged period of a low DIM signal may cause the boost regulator output voltage to drift to an inappropriate value, due to circuit leakage currents acting on the gain setting network and the error amplifier being disconnected.

The DIM stuck-at-zero condition is asserted when the DIM signal remains low for a period equal to one tenth the auto-retry delay. Upon detection of the condition, regular operation is terminated, the Fault mode is activated, and a new start-up is initiated after an auto-retry delay.

4.3.4 SHORT CIRCUIT PROTECTION

When the output enters into short-circuit condition, the device turns off and enters into Auto-Retry Delay mode. Once the short-circuit condition is cleared, the device turns on after an auto-retry delay.



Legend:

ROP	=	Regular Operation
VDUV	=	V_{DD} Undervoltage
SVUV	=	Supply Voltage Undervoltage
OVOV	=	Output Voltage Overvoltage
LCOC	=	LED Current Overcurrent
DIM	=	PWM Dimming Signal

FIGURE 4-1: *State Transitions Diagram.*

4.4 Optocoupler Driver

The optocoupler driver circuit translates the flyback regulator output signal into a signal for driving the optocoupler input circuit. The optocoupler circuit in turn provides an output signal for driving the control input of the flyback controller device.

A rising flyback regulator reference signal translates into a falling optocoupler drive signal.

The optocoupler driver circuit includes logic for the immediate shutdown of the flyback converter when either of the following occur:

- Boost converter output overvoltage, and
- Headroom undervoltage during regular operation of the driver.

A shutdown of the flyback converter corresponds with driving the optocoupler input circuit with the full V_{DD} voltage.

The HV96001 optocoupler drive circuit generates the drive voltage (V_{OPT}) for the optocoupler LED. The drive voltage establishes an optocoupler input current or optocoupler LED current (I_{OPT}), which can be approximated by Equation 4-1.

EQUATION 4-1:

$$(V_{OPT} - V_{LED}) = (I_{OPT} \times R_{OPT})$$

Where:

$$V_{LED} \approx 0.8V \text{ to } 1.3V$$

Note that, generally, the optocoupler LED is unresponsive to a drive voltage lower than 0.8V to 1.3V, the LED being a diode having a forward voltage drop. Also note that the LED forward voltage (V_{LED}) is not a constant but varies with the production lot, LED current amplitude (I_{OPT}) and with temperature.

The optocoupler driver adjusts the optocoupler drive voltage as shown in Equation 4-2.

EQUATION 4-2:

$$V_{OPT} = 4.05 - (0.8 \times V_{FRO})$$

Corresponding with:
$V_{OPT} = 4.05V$ *when* $V_{FRO} = 0V$
$V_{OPT} = 0.85V$ *when* $V_{FRO} = 4V$

The lower output voltage level of 0.85V corresponds to zero LED drive current.

4.5 Dimming

The HV96001 provides the following two inputs for control of the LED current:

- The LED Current Reference (LCR), and
- The PWM Dimming Reference (DIM)

4.5.1 LED CURRENT REFERENCE

The LED current amplitude (I_{LED}), the LED current reference voltage (V_{LCR}) and the LED current sense resistor (R_{LCS}) are related by Equation 4-3.

EQUATION 4-3:

$$I_{LED} = \frac{V_{LCR}}{R_{LCS}}$$

The maximum level of the linear current reference is 500 mV.

The LED overcurrent threshold is a typical of 640 mV, giving a 140 mV margin between the maximum reference level and the LED overcurrent comparator trip level.

4.5.2 PWM DIMMING REFERENCE

The PWM dimming reference (DIM) exercises immediate control over:

- The boost converter
- The load switch
- The boost regulator error amplifier
- The timer

Ultrasonic PWM dimming frequencies may be used to advantage where the emission of audible noise is a concern.

Note, it is neither necessary nor desirable to run the boost converter when the DIM signal is low as the demand for LED load current is zero.

4.6 Boost Power Circuit

The power circuit consists of an inductor, a controlled switch, a current sense resistor and a diode. The current sense resistor provides a current sense signal for regulating the peak amplitude of the boost inductor current.

The inductor current ramps up when the switch is on, thereby transferring energy from the source to the inductor, and ramps down when the switch is off, thereby transferring energy from both the inductor and the source to the load.

The HV96001 boost converter is generally operated with small headroom voltage, that is, with a small voltage difference between source and load voltage. Such operation corresponds to operation with a small voltage step-up ratio and to operation with a small duty.

The small step-up ratio is advantageous as it results in a small converter size and high efficiency operation of the boost converter. A small difference between boost converter input and output voltage implies that the boost inductor can be small for a given target amplitude of the inductor current ripple. A typical target for the peak-to-peak inductor current ripple is 30% of the average inductor current.

Since the nominal step-up ratio is small, the maximum duty can be limited to 50%. A maximum duty of 50% limits the voltage step-up ratio to a factor of two, which is more than adequate for the intended application.

The 50% duty limit offers the benefit of dispensing with the need for slope compensation circuitry, which is typically required when operating in Current-mode at duties exceeding 50%.

4.7 Boost Controller

Current-mode control provides for simple control loop dynamics and for inherent inductor and switch overcurrent protection.

The Current-mode control principle terminates switch conduction when the boost inductor current reaches a given peak current reference level. The boost converter limits the switch duty to 50%. Given the 50% duty limit, switch conduction is also terminated when the 50% duty is reached, whichever occurs earlier. The 50% duty limit avoids duty operation in a region where sub-harmonic oscillation of the inductor peak current can occur.

4.7.1 OSCILLATOR

The oscillator generates switching cycles of constant frequency and period when the boost converter is enabled.

The oscillator operates at a fixed frequency of 200 kHz.

The oscillator starts with a fresh switching cycle at the rising edge of the DIM signal and stops operation on the falling edge of the DIM signal.

The oscillator includes a current source and a capacitor for generating the oscillator ramp voltage. A switch and comparator circuit discharge the capacitor at the end of the switching cycle when the oscillator ramp voltage reaches the end of cycle threshold voltage. When the DIM signal goes high, the discharge switch and the comparator circuit are enabled, thereby causing an immediate discharge of the oscillator capacitor and the start of a fresh switching cycle.

4.7.2 PEAK CURRENT COMPARATOR

The peak current comparator indicates whether the inductor current sense signal (V_{BCS}) exceeds the peak current reference signal. And the peak current reference signal is derived from the boost regulator output voltage (V_{BRO}) by means of a FET follower and an attached voltage divider with an attenuation ratio of 10. The boost regulator output voltage operates at a significantly higher voltage level of 4V and above.

The input voltages to the comparator, the peak current reference and the inductor current sense operate at a maximum level of 400 mV. The low level is required to limit sense resistor power dissipation and to limit the impact of the sense resistor voltage waveform on the gate drive waveform.

EQUATION 4-4:

$$V_{BRO} = (V_{BCR} \times 10) + 0.8V$$

Where:

V_{BRO} = *Output Voltage at Boost Regulator Output Pin*

V_{BCR} = *Boost Converter Current Reference*

$$V_{BRO} = (V_{BCS} \times 10) + 0.8V$$

In Steady state condition, $V_{BCR} = V_{BCS}$

V_{BCS} = *Output Voltage at Boost Current Sense Pin*

$0.8V$ = *Internal Voltage Follower V_{GS} Drop*

4.7.3 LEADING EDGE BLANKING

The peak comparator input signal or the output of the peak current comparator is to be ignored for a given period at the leading edge of the gate pulse, the period known as the leading edge blanking delay.

To enable small duty operation, leading edge blanking delay should not be excessive and gate charging should occur fast.

4.8 Logic Inputs

The HV96001 logic operates on the following logic inputs:

4.8.1 POWER-ON RESET (POR)

The Power-on Reset condition indicates that adequate V_{DD} voltage is present for the reset of the state logic. Note that spurious turn-on of the boost converter switch and the load switch gate is to be avoided during start-up.

4.8.2 V_{DD} UNDERVOLTAGE (VDUV)

A V_{DD} undervoltage condition indicates that the V_{DD} voltage is inadequate for enabling all HV96001 circuit functions.

The V_{DD} undervoltage (VDUV) condition is monitored with a voltage comparator having hysteresis.

The comparator asserts the condition when the V_{DD} voltage falls below 4.4V and de-asserts the condition when the V_{DD} voltage rises above 4.6V.

4.8.3 SUPPLY UNDERVOLTAGE (SVUV)

A supply undervoltage condition indicates that the supply voltage is insufficient for the first start of the boost converter.

The supply undervoltage (SVUV) condition is monitored with a voltage comparator having hysteresis.

The comparator asserts the condition when the voltage at the supply voltage sense (SVS) pin falls below 0.7V and de-asserts the condition when the voltage at the SVS pin rises above 0.9V.

The supply voltage sense pin voltage is proportional to the supply voltage (V_S) and is derived by means of an external resistive divider (R_{SVS}, R_{SVX}). The supply voltage and the supply voltage sense voltage are related by Equation 4-5.

EQUATION 4-5:

$$V_{SVS} = V_S \times \left(\frac{R_{SVS}}{R_{SVX} + R_{SVS}}\right)$$

4.8.4 HEADROOM UNDERVOLTAGE (HVUV)

The headroom undervoltage (HVUV) condition calls for the unconditional turn off of the flyback converter so that no danger exists of the supply voltage reaching or exceeding the LED load operating voltage.

When the headroom is close to the target value, that is, when the headroom voltage is 90% of the target level, the headroom undervoltage condition is cleared and the flyback converter is switched on again.

Shutdown of the flyback converter because of headroom undervoltage is only relevant when an adequate supply voltage is present.

The headroom undervoltage (HVUV) condition is monitored with a voltage comparator having hysteresis.

The comparator asserts the condition when the voltage at the headroom voltage sense (HVS) pin falls below 0.47V and de-asserts the condition when the voltage at the HVS pin rises above 0.92V.

The headroom voltage sense pin voltage is the input to the headroom voltage error amplifier and the HVS pin voltage is derived with the aid of an external sense network (R_{HVS}, R_{HVX}, R_{HVB}) and the bipolar transistor (Q_{HVS}). The sense voltage can be approximated by the relation shown in Equation 4-6.

EQUATION 4-6:

$$V_{HVS} = R_{HVS} \times \left(\frac{V_{HVX}}{R_{HVX}}\right)$$

Where:

$$V_H = (V_O - V_S)$$

$$V_{HVX} \approx (V_H - V_{QVS})$$

$$V_{QVS} \approx 0.7V$$

The resistor (R_{HVB}), which is located in series with the base of the transistor (Q_{HVS}) is one method of protecting the base-emitter junction of the transistor from a large reverse breakdown current, should the base-emitter voltage become reverse biased inadvertently.

The headroom voltage may inadvertently assume a large negative value if the boost inductor or the boost diode is missing from the boost converter power circuit.

The HV96001 includes an internal clamp circuit, capable of limiting the HVS pin voltage to 5V and is rated for a clamping current of 2 mA at 5V.

4.8.5 OUTPUT OVERVOLTAGE (OVOV)

Output overvoltage can occur for many reasons, one being a poorly adjusted control loop of the flyback regulator, and two being a sudden LED open circuit condition.

The output overvoltage (OVOV) condition is monitored with a voltage comparator having hysteresis.

The comparator asserts the condition when the voltage at the output voltage sense (OVS) pin rises above 1V and de-asserts the condition when the voltage at the OVS pin falls below 0.5V.

The output voltage sense voltage is proportional to the output voltage (V_O) and is derived by means of an external resistive divider (R_{OVS}, R_{OVX}).

The output voltage and the output voltage sense voltage are related as shown in Equation 4-7.

EQUATION 4-7:

$$V_{OVS} = V_O \times \left(\frac{R_{OVS}}{R_{OVX} + R_{OVS}}\right)$$

Tolerance

The tolerance of the comparator upper trip level is specified at 3%. Assuming a voltage divider tolerance of 1%, the overall trip tolerance results in 4%.

For reference, 4% of 60V corresponds to 2.4V. Accordingly, the nominal overvoltage trip setting can be set as high as 57.6V.

When assuming the LED forward voltage tolerance of 5%, the nominal operating voltage of the LED load is limited to 55.4V. Assuming a 10% tolerance, the nominal LED load voltage is limited to 52.9V.

4.8.6 LED OVERCURRENT (LCOC)

A possible cause for an LED overcurrent situation is a blown FET or the opening of the current sense resistor.

Should LED overcurrent occur, then the load switch is turned off immediately and state logic transitions to the Fault mode.

The LED overcurrent (LCOC) condition is monitored with a voltage comparator and an associated leading edge blanking circuit.

The comparator asserts the condition when the voltage at the LED current sense (LCS) pin rises above 640 mV.

The sense voltage is proportional to the LED current and is derived by means of a current sense resistor (R_{LCS}), which is connected in the FET source circuit.

Leading Edge Blanking

A leading edge blanking circuit prevents premature tripping of the comparator on account of the leading edge spike of the current sense signal at the turn-on of the load switch. The spike is associated with a relatively large transient current required for charging the FET gate capacitance and for discharging the FET drain capacitance.

The blanking time is specified at 600 ns minimum. The discharge of the load switch drain node may require relatively high current as the equivalent capacitance at the drain node may be more than usual due to relatively large capacitance loading of a LED load and associated wiring.

Hence, a relatively large blanking time is specified for the leading edge blanking circuit of the load switch overcurrent comparator.

4.8.7 TIMER LOW VOLTAGE (TMRL)

A timer low output voltage condition indicates that the timer capacitor is reset to zero.

The timer low output voltage condition is monitored by a voltage comparator.

The comparator asserts the condition when the voltage at the timer pin is less than 100 mV.

4.8.8 TIMER HIGH VOLTAGE (TMRH)

A timer high output voltage condition indicates that the timer has timed out.

The timer high output voltage condition is monitored by a voltage comparator.

The comparator asserts the condition when the voltage at the timer pin rises above 4.1V.

4.9 Logic Outputs

The state logic generates the following logic outputs:

4.9.1 REGULAR OPERATION (ROP)

This enables the boost converter, the load switch, the boost regulator error amplifier output and the DIM stuck-at-zero switch to ground at the timer pin.

4.9.2 TIMER RESET (TRS)

This turns on the timer Reset switch.

4.10 V_{DD} Regulator

The V_{DD} regulator is rated for an output voltage of 5V and an output current of 25 mA when supplied with a voltage ranging from 8V to 60V.

Regulator Stability

Should an external V_{DD} capacitor be necessary in the design of a stable V_{DD} regulator, then the capacitance should not exceed 100 nF.

Linear Regulator Dissipation

The use of an external preregulator or the use of a dedicated supply circuit for powering the HV96001 is suggested for situations that may cause excess V_{DD} regulator dissipation.

Current Draw

The V_{DD} regulator delivers current to the internal control circuits, the boost switch gate and the load switch gate driver circuits, the optocoupler driver output circuit and the external control circuits.

4.10.1 INTERNAL CONTROL CIRCUITS

The current draw of internal control circuits should not exceed 2 mA.

4.10.2 EXTERNAL CONTROL CIRCUITS

The current draw of external control circuits should not exceed 10 mA.

4.10.3 GATE DRIVER CIRCUITS

The combined current draw of the boost FET gate circuit and the dimming switch gate circuit should not exceed 5 mA.

Gate drive current is a function of FET gate charge and operating frequency.

The operating frequency of the dimming switch is set by the frequency of the PWM dimming signal. The operating frequency of the boost FET is 200 kHz.

4.10.4 OPTOCOUPLER DRIVER CIRCUITS

The optocoupler driver output current should not exceed 5 mA.

4.11 TYPICAL WAVEFORMS

4.11.1 NO DIMMING, 50V LED LOAD

The figure below shows basic waveforms of start-up and regular operation without PWM dimming, that is, DIM signal continuously high.

Note that the HV96001 LED-based driver can be given a wide output voltage range, that is, wide range of the LED load operating voltage, such as the 20V to 50V range. A figure for operation at 20V and a figure for operation at 50V are included.

Figure 4-2 corresponds to operation at 50V, the flyback converter, thereby operating near its maximum power level in Steady state.

The curves are referenced to their position (0, y) in Figure 4-2, each being described below.

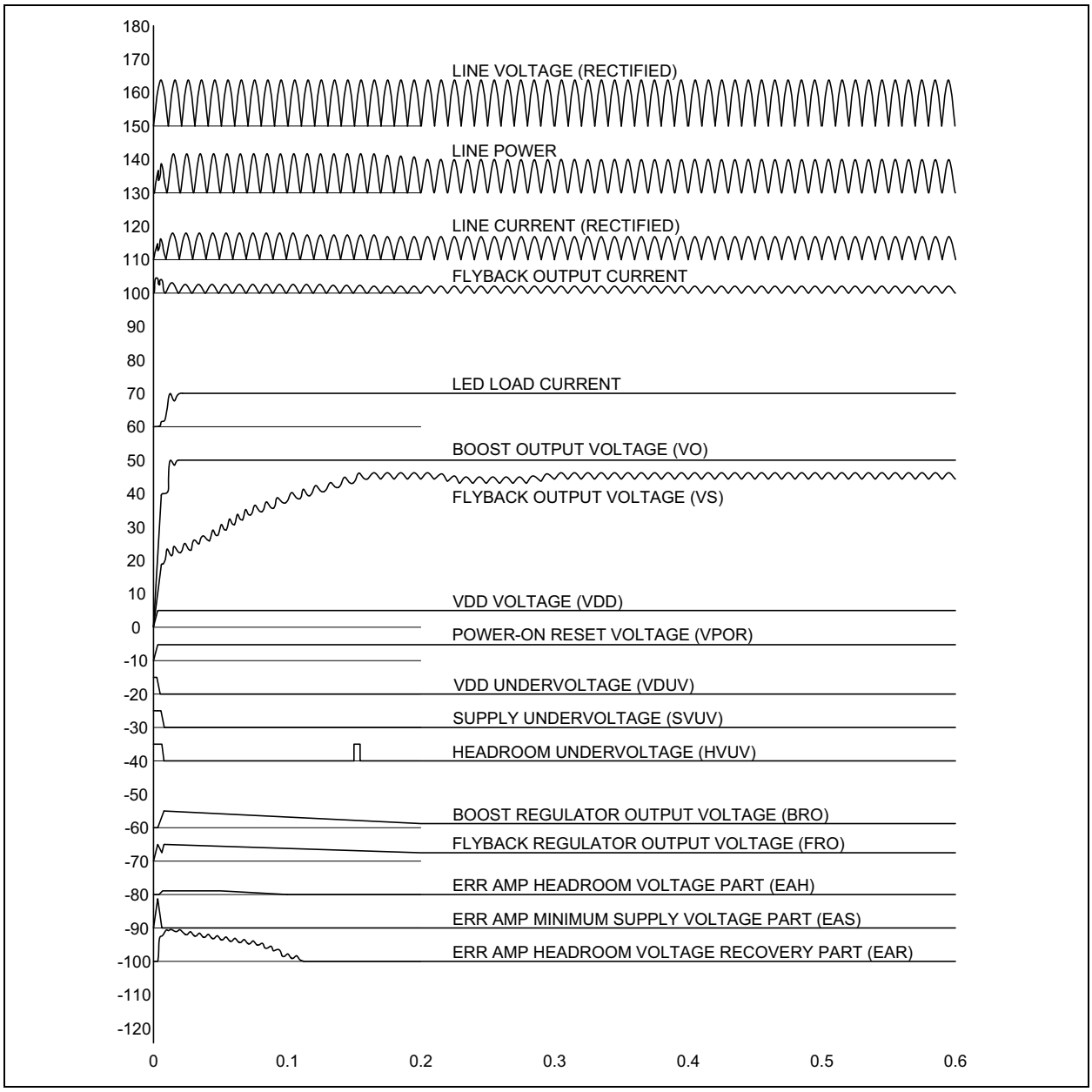


FIGURE 4-2: *No Dimming, 50V LED Load.*

4.11.1.1 Rectified Line Voltage (0, 150)

Shown is the voltage waveform at the load side of the rectifier bridge.

The flyback converter waveforms correspond to a flyback converter operating with high-power factor.

4.11.1.2 Line Power (0, 130)

Shown is the power as drawn from the AC line, that is, the input power of the flyback converter. The power oscillates between zero and twice the average power at twice the line frequency (100 or 120 Hz). Line power amplitude is modulated by the output voltage of the flyback regulator.

4.11.1.3 Rectified Line Current (0, 110)

The shape of the rectified line current resembles the shape of the rectified line voltage conforming to high-power factor operation. As with the line power, line current amplitude is modulated by the flyback regulator output voltage.

4.11.1.4 Flyback Output Current (0, 100)

The flyback output current is indicative of the pulsating nature of AC power delivery. The large ripple amplitude leads to a relatively large ripple on the flyback converter output voltage.

4.11.1.5 LED Load Current (0, 60)

The LED load current appears when the boost converter output voltage reaches the LED load operating voltage.

The LED current exhibits very little ripple due to the high bandwidth of the boost regulator, keeping the LED current and boost output voltage near constant despite the relatively high ripple of the boost converter input voltage (flyback converter output voltage).

4.11.1.6 Boost Converter Output Voltage (0, 0)

The boost converter output voltage, at first, follows the rise of the flyback converter output voltage by way of the boost diode. Once the boost converter is enabled, the boost converter output voltage rises quickly and settles at the level required for operating the LED load at the target LED current level.

4.11.1.7 Flyback Output Voltage (0, 0)

The flyback converter output voltage shows high ripple content due to the high ripple content of the flyback converter output current.

First, the flyback output voltage rises to the minimum supply voltage level. Next, the boost converter turns on and the flyback converter output voltage rises to a voltage (45V), which is equal to the boost converter output voltage (50V) less the target headroom voltage (5V).

4.11.1.8 V_{DD} Voltage (0, 0)

The V_{DD} voltage follows the rise of the flyback converter output voltage less the internal voltage drop of the internal V_{DD} regulator and settles at the V_{DD} voltage regulation level (5V).

4.11.1.9 Power-on Reset Voltage (0, -10)

The Power-on Reset voltage signal goes high at the moment when the V_{DD} voltage reaches about 1V.

4.11.1.10 V_{DD} Undervoltage (0, -20)

The V_{DD} undervoltage signal goes low at the moment when the V_{DD} voltage reaches 4.6V.

4.11.1.11 Supply Undervoltage (0, -30)

The supply undervoltage signal goes low at the moment when the flyback converter output voltage reaches the minimum target level (15V).

4.11.1.12 Headroom Undervoltage (0, -40)

The headroom undervoltage signal goes low at the moment when the boost converter headroom voltage reaches 90% of the headroom voltage target level.

Headroom undervoltage occurs at approximately the 0.18 second mark as the flyback converter output voltage temporarily overshoots. The headroom undervoltage condition leads to a temporary shutdown of the flyback converter.

4.11.1.13 Boost Regulator Output Voltage (0, -60)

The boost regulator output voltage programs the peak current level of the boost converter and is seen to rise to a high level at the moment where the boost converter turns on. As soon as the LED current reaches the target value, the regulator output drops back.

4.11.1.14 Flyback Regulator Output Voltage (0, -70)

The flyback regulator output programs the power level of the flyback converter and is seen to command a high power level at start-up of the driver. The power level drops somewhat when Steady state operation is reached.

4.11.1.15 Flyback Regulator Error Amplifier Outputs (0, (-80, -90, -100))

It can be seen that all three error amplifiers play a part.

At the very start, a high regulator output voltage is produced through the action of the minimum supply voltage error amplifier. As soon as the boost converter starts and significant headroom voltage is produced, the headroom voltage recovery error amplifier keeps the power at a high level. Once the headroom voltage establishes the target value, the flyback converter power level is regulated by the output current of the headroom voltage error amplifier, this amplifier having a lower gain, a gain which is appropriate for maintaining high-power factor operation in Steady state.

4.11.2 NO DIMMING, 20V LED LOAD

Note that the 20V LED load voltage gives a much faster start-up when compared to 50V LED load voltage.

The flyback converter power level is significantly lower in Steady state operation, as shown in Figure 4-3.

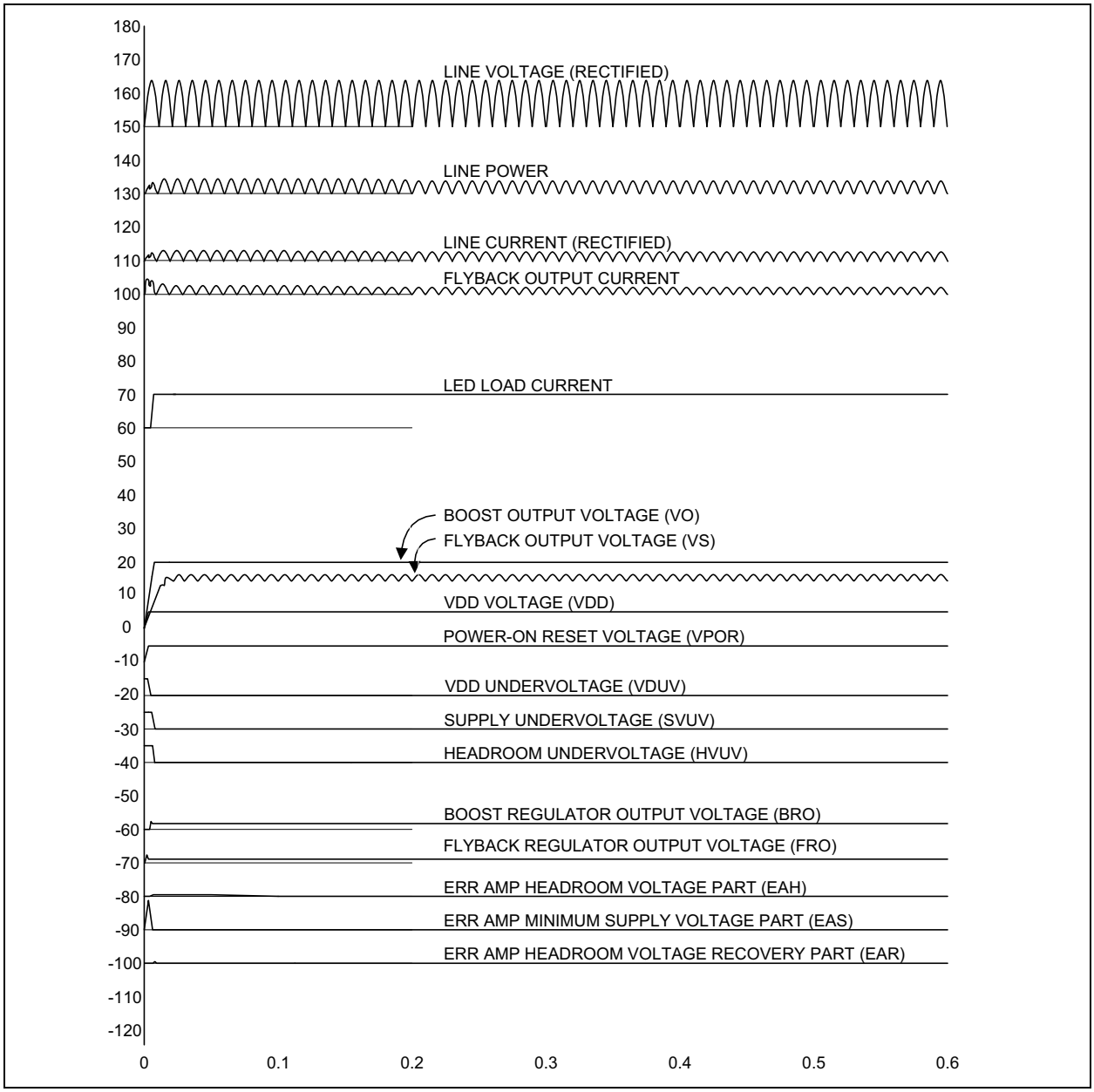


FIGURE 4-3: *No Dimming, 20V LED Load.*

4.11.3 DIMMING, 50V LED LOAD

Figure 4-4 shows PWM dimming operation.

The DIM signal switches from full-on (100%) to PWM dimming at 10% duty, and switches back to full-on. In practice, such large changes in duty may not be utilized, but rather gradual change in duty.

The stepwise change from 100% dimming to 10% dimming causes the flyback converter output voltage to rise, thereby triggering the headroom undervoltage condition several times, while the flyback regulator is gradually reducing the flyback power level. The flyback power level eventually settles into a lower value, which corresponds to dimming at 10% duty.

Whereas not clearly visible at the scale of this drawing, the voltage waveform of the timer voltage exhibits a sawtooth shape during part of each PWM dimming cycle, the shape ramping from zero when the DIM signal goes low and resetting to zero when the DIM signal goes high.

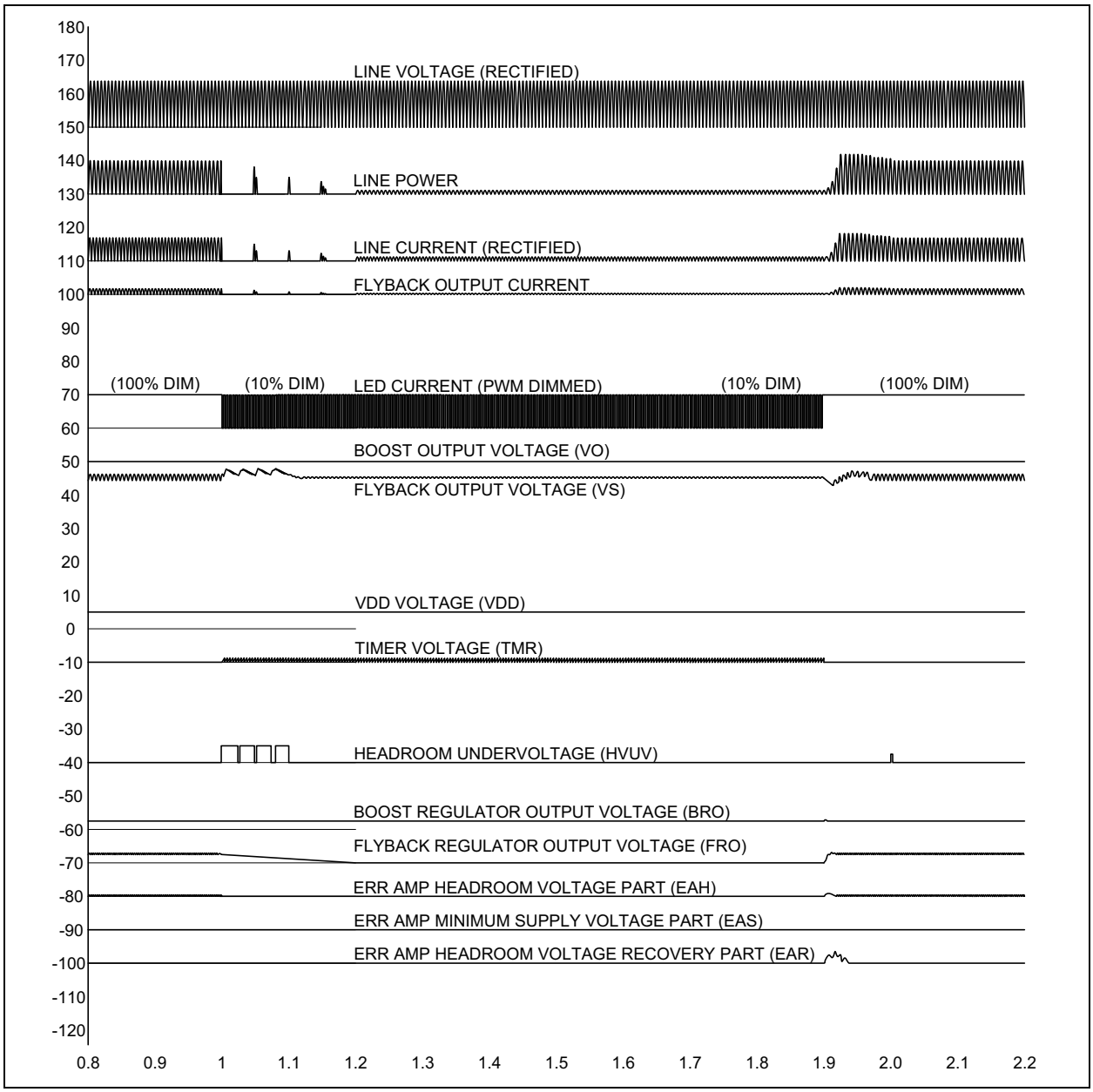


FIGURE 4-4: *Dimming, 50V LED Load.*

4.11.4 DIMMING DETAIL

Figure 4-5 shows waveforms corresponding to a transition from 100% to 10% PWM dimming.

It can be seen that the flyback converter turns off when headroom undervoltage occurs. The headroom undervoltage signal goes high when the headroom voltage drops below 50% of the target headroom voltage.

The flyback converter turns back on when the headroom voltage has risen to 90% of the target headroom voltage.

The figure shows the action of the DIM stuck-at-zero detection in greater detail. Timer voltage ramps up whenever the DIM signal is low and is reset when the DIM signal is high. Should the timer voltage reach 4.1V, then the driver transitions from regular operation mode to Fault mode.

Note that the amplitude of the timer voltage was enlarged to make the ramp clearly visible in Figure 4-5.

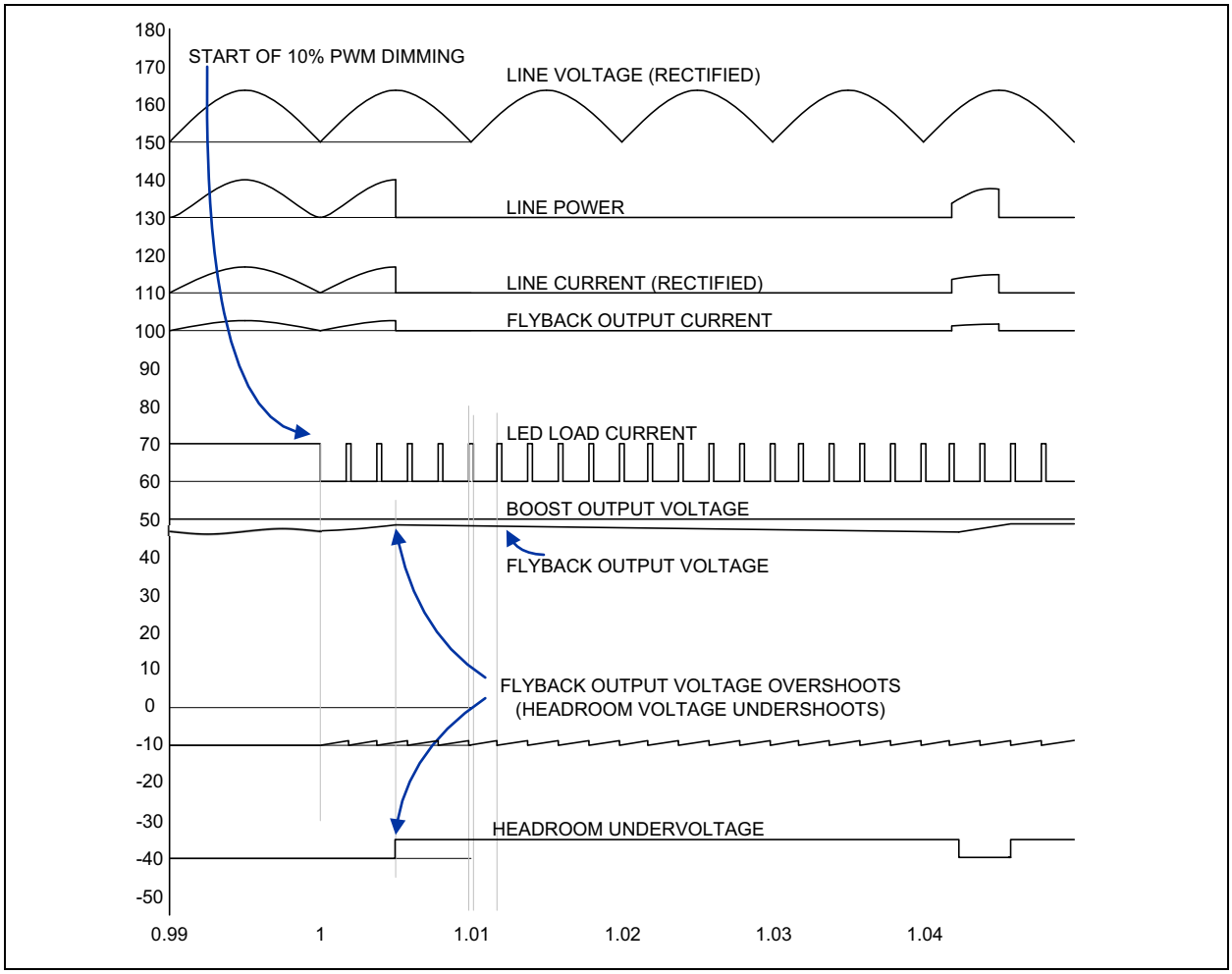


FIGURE 4-5: *Dimming Detail.*

4.12 Performance Curves

Note: Unless otherwise indicated, V_{OUT} = 50V, I_{LED} = 1A, T_A = +25°C, F_{SW} = 200 kHz.

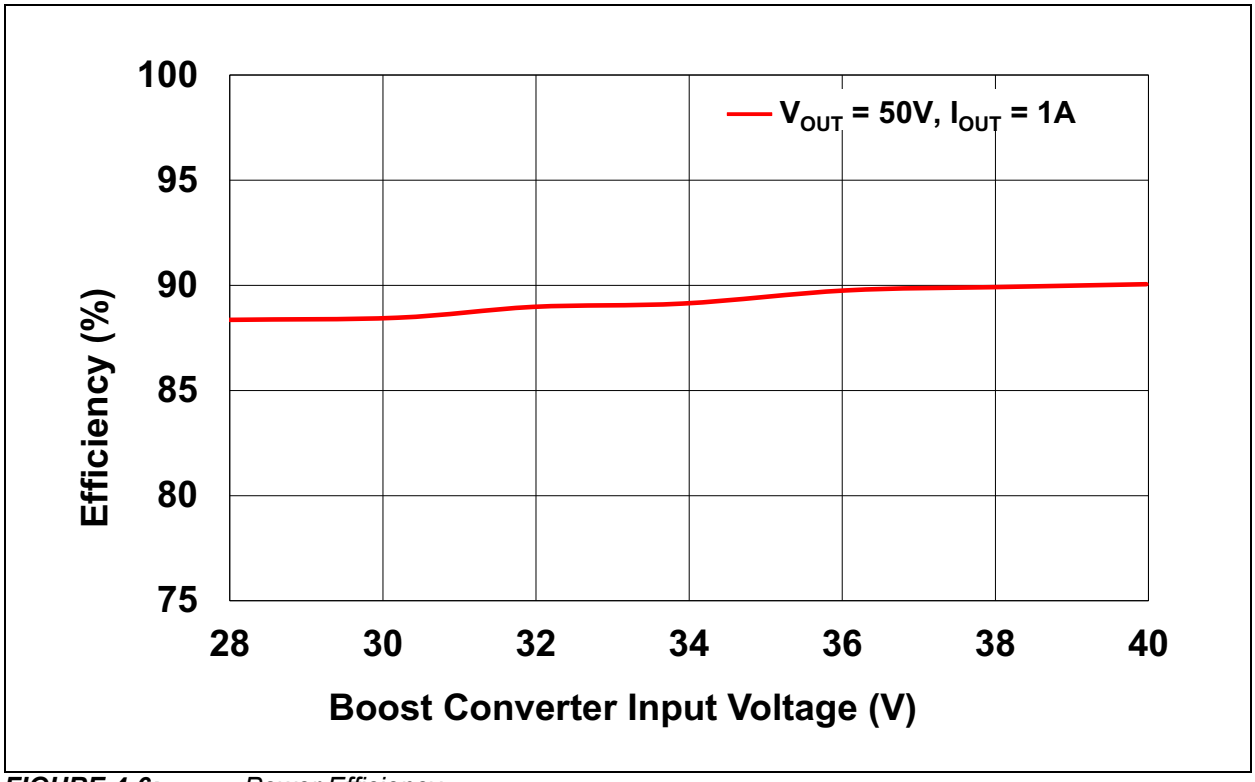


FIGURE 4-6: *Power Efficiency.*

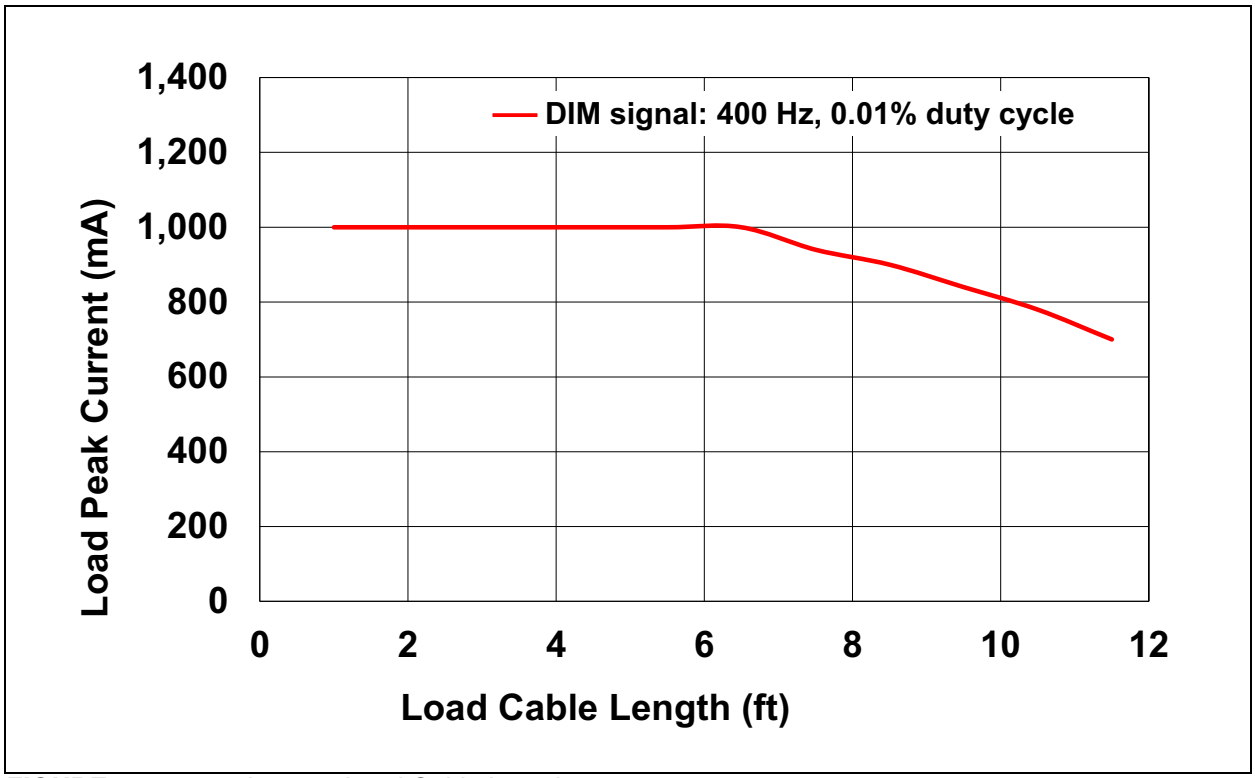


FIGURE 4-7: *I_{LED} vs. Load Cable Length.*

4.13 Functional Waveforms

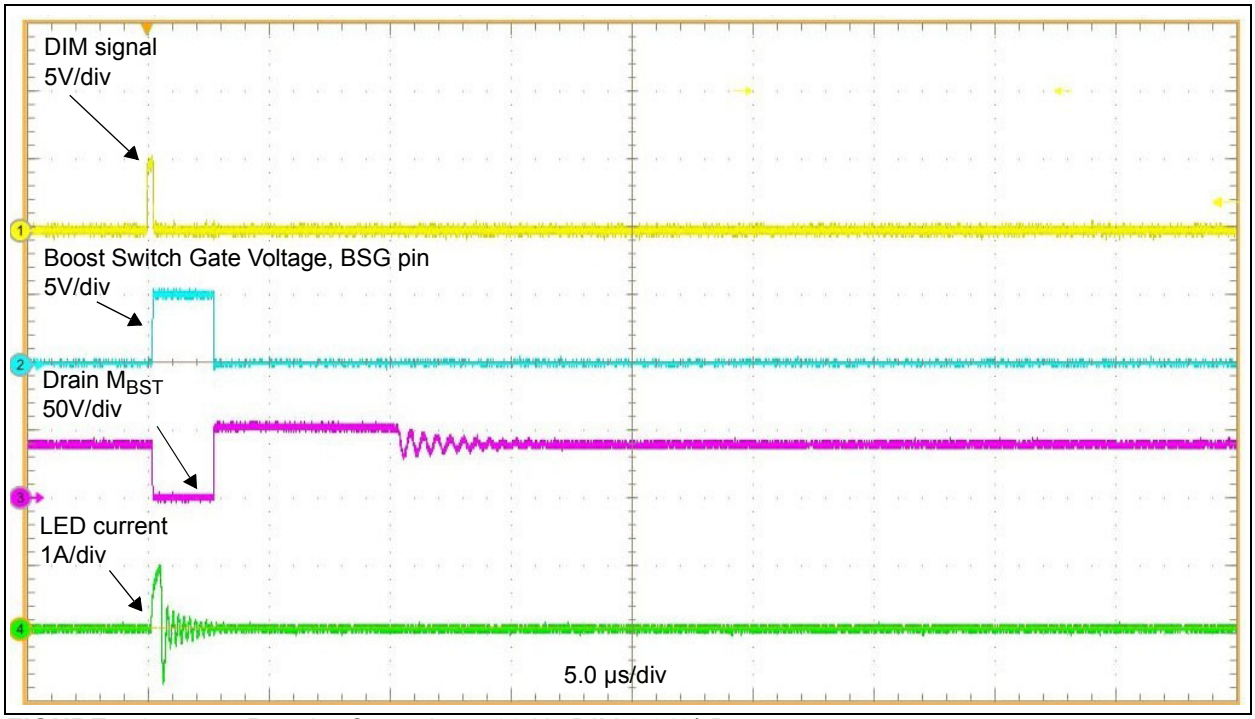


FIGURE 4-8: *Regular Operation, 400 Hz DIM 0.01% Duty.*

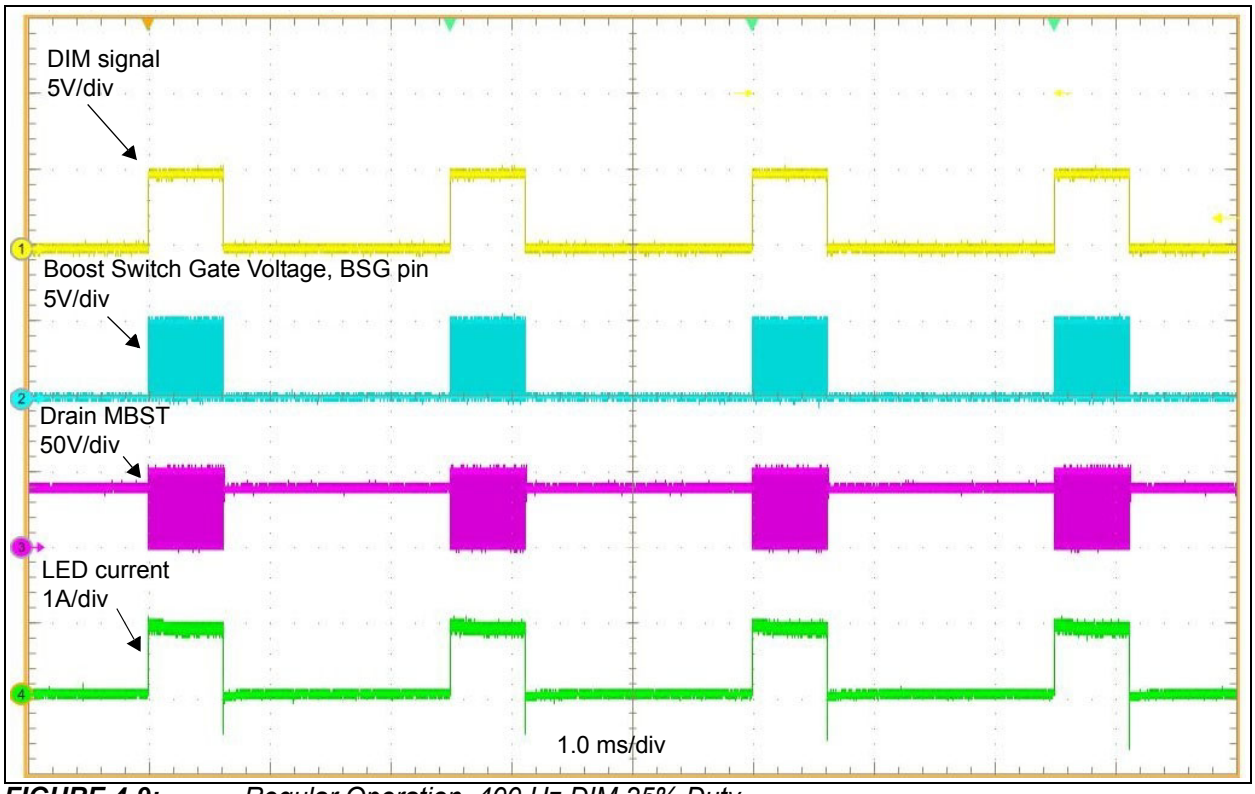


FIGURE 4-9: *Regular Operation, 400 Hz DIM 25% Duty.*

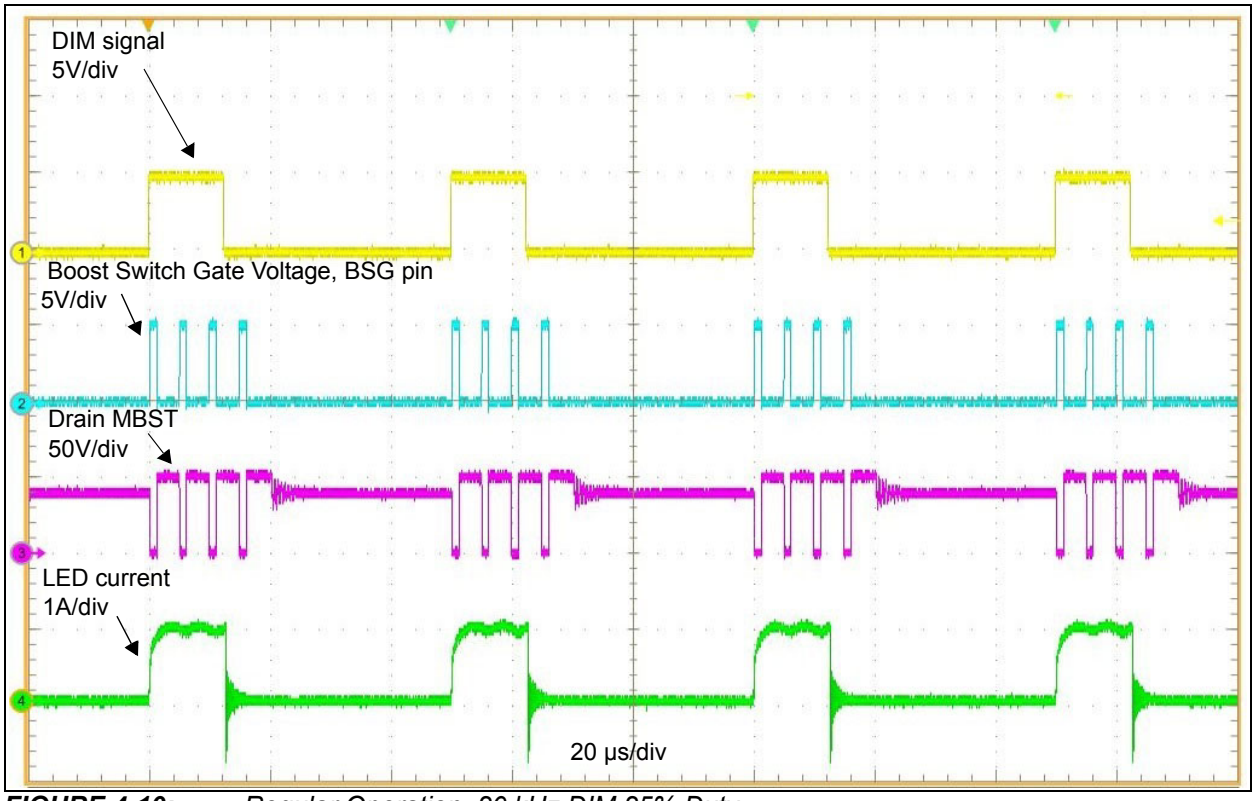


FIGURE 4-10: *Regular Operation, 20 kHz DIM 25% Duty.*

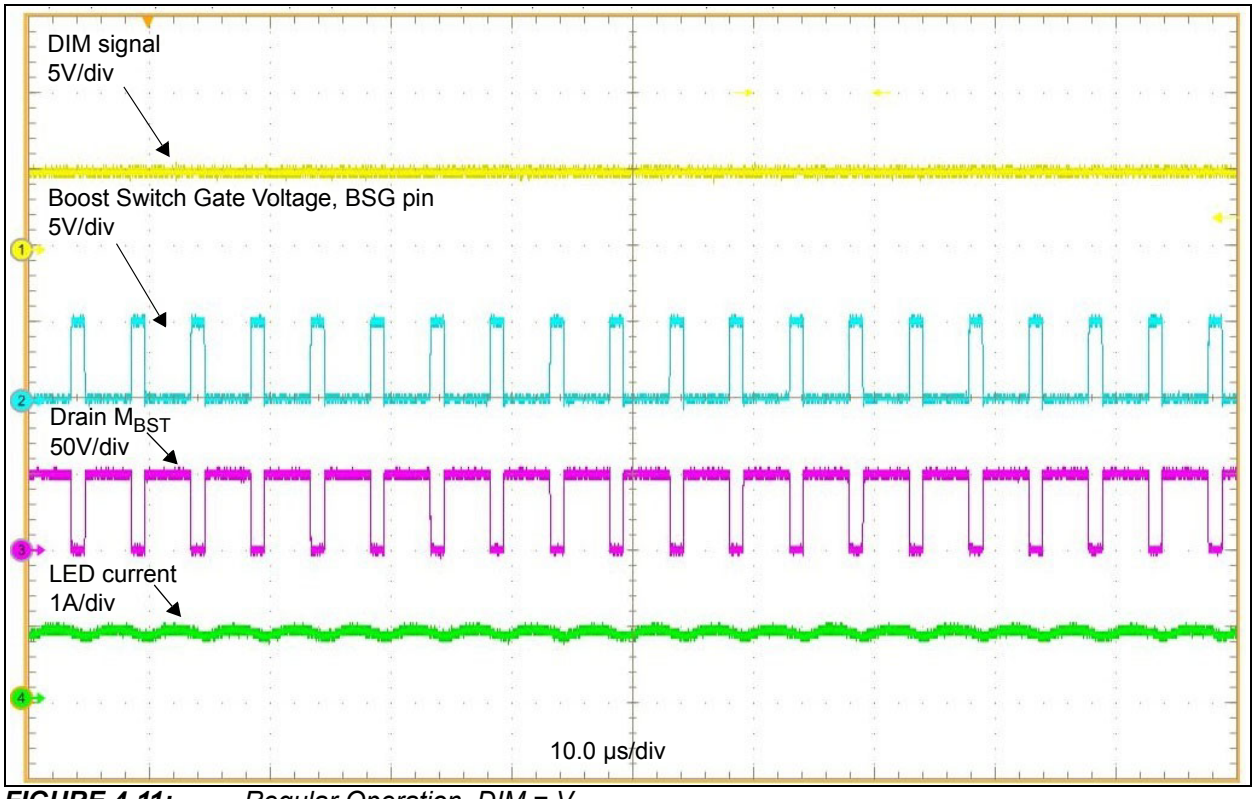


FIGURE 4-11: *Regular Operation, DIM = V_{DD}.*

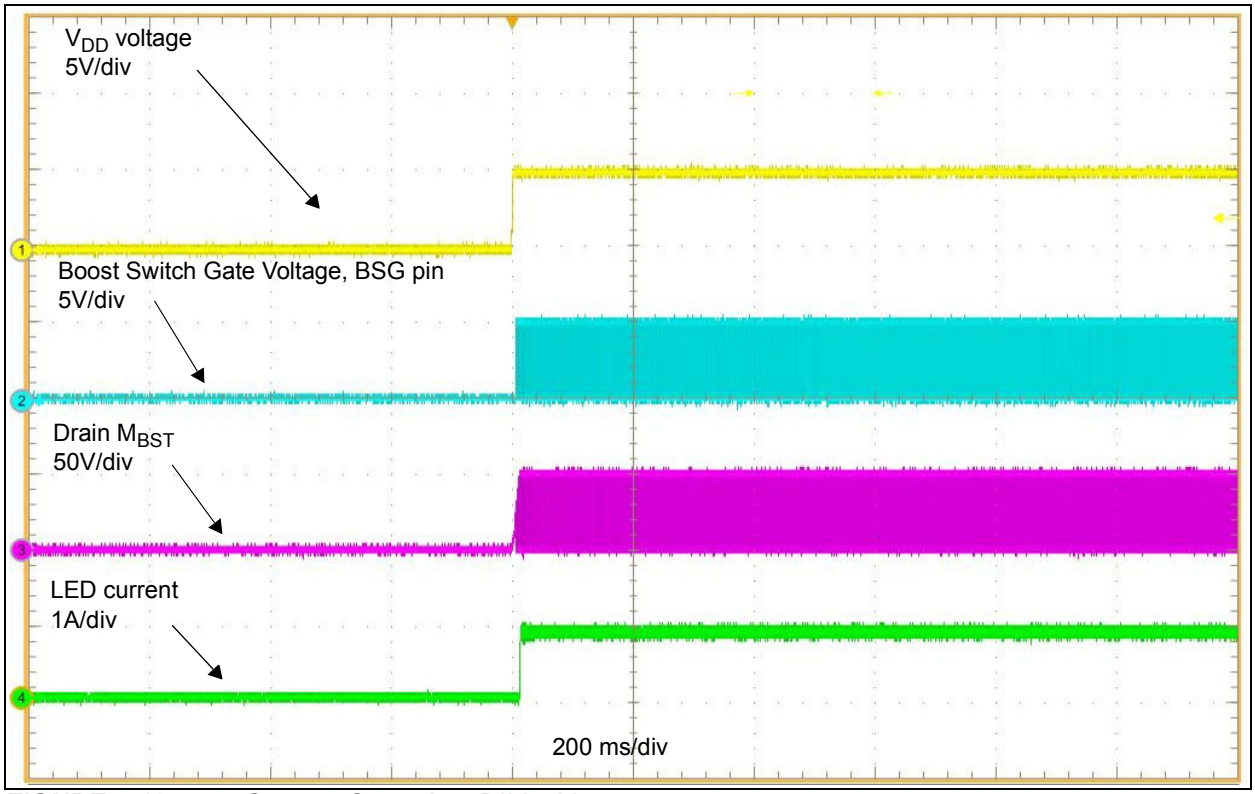


FIGURE 4-12: *Start-up Operation, DIM = V_{DD}.*

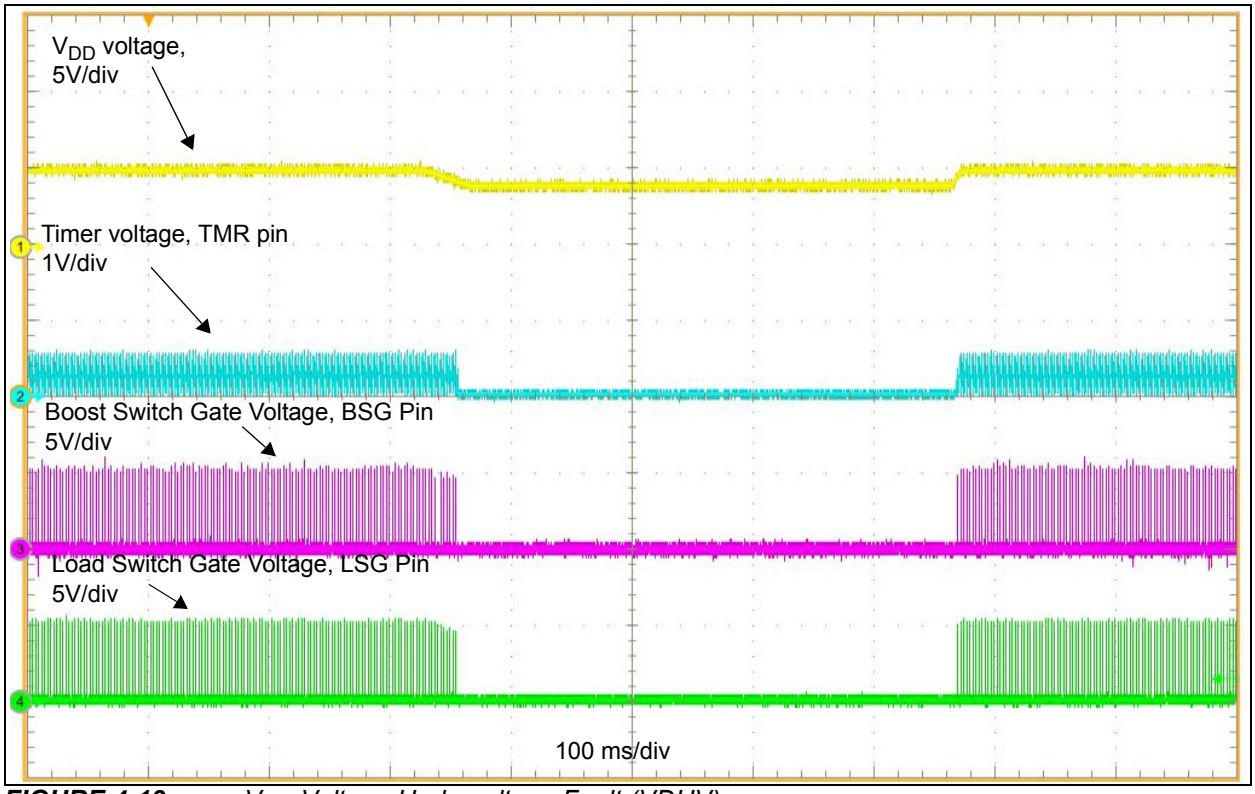


FIGURE 4-13: *V_{DD} Voltage Undervoltage Fault (VDUV).*

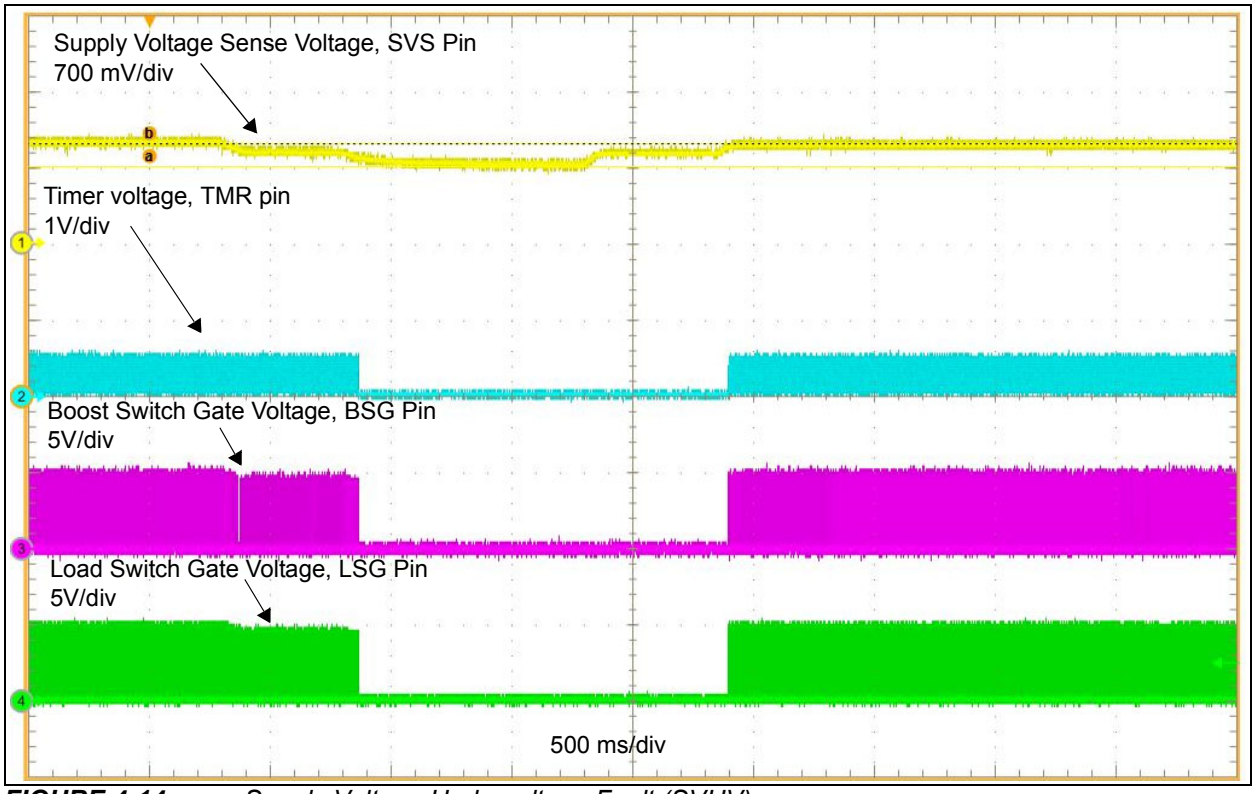


FIGURE 4-14: *Supply Voltage Undervoltage Fault (SVUV).*

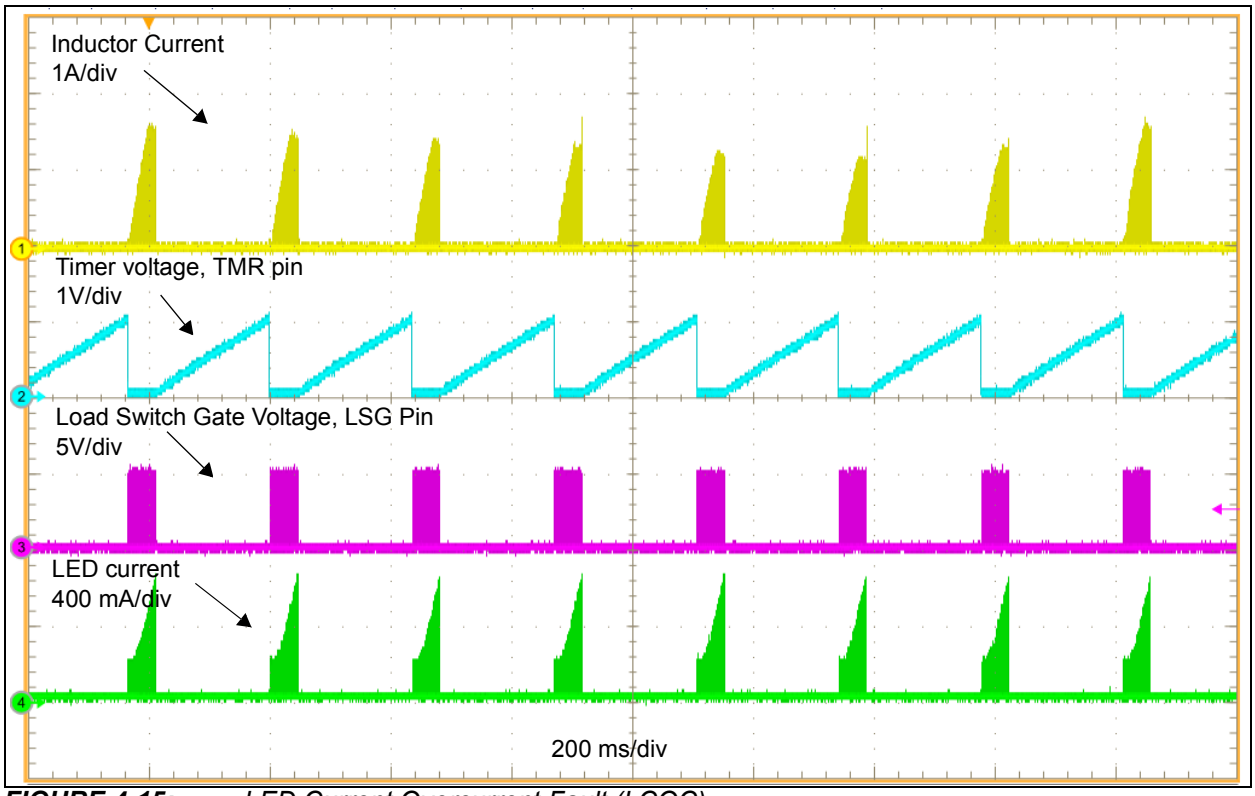


FIGURE 4-15: *LED Current Overcurrent Fault (LCOC).*

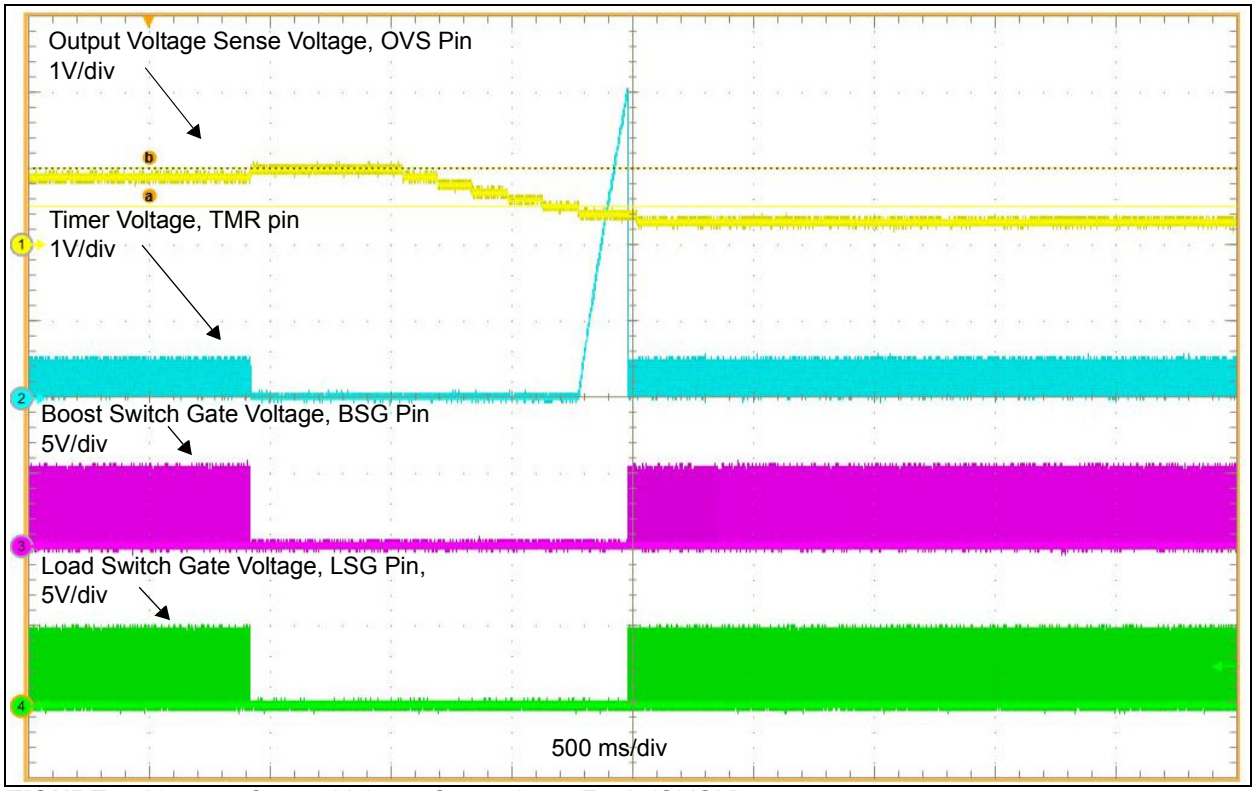


FIGURE 4-16: *Output Voltage Overvoltage Fault (OVOV).*

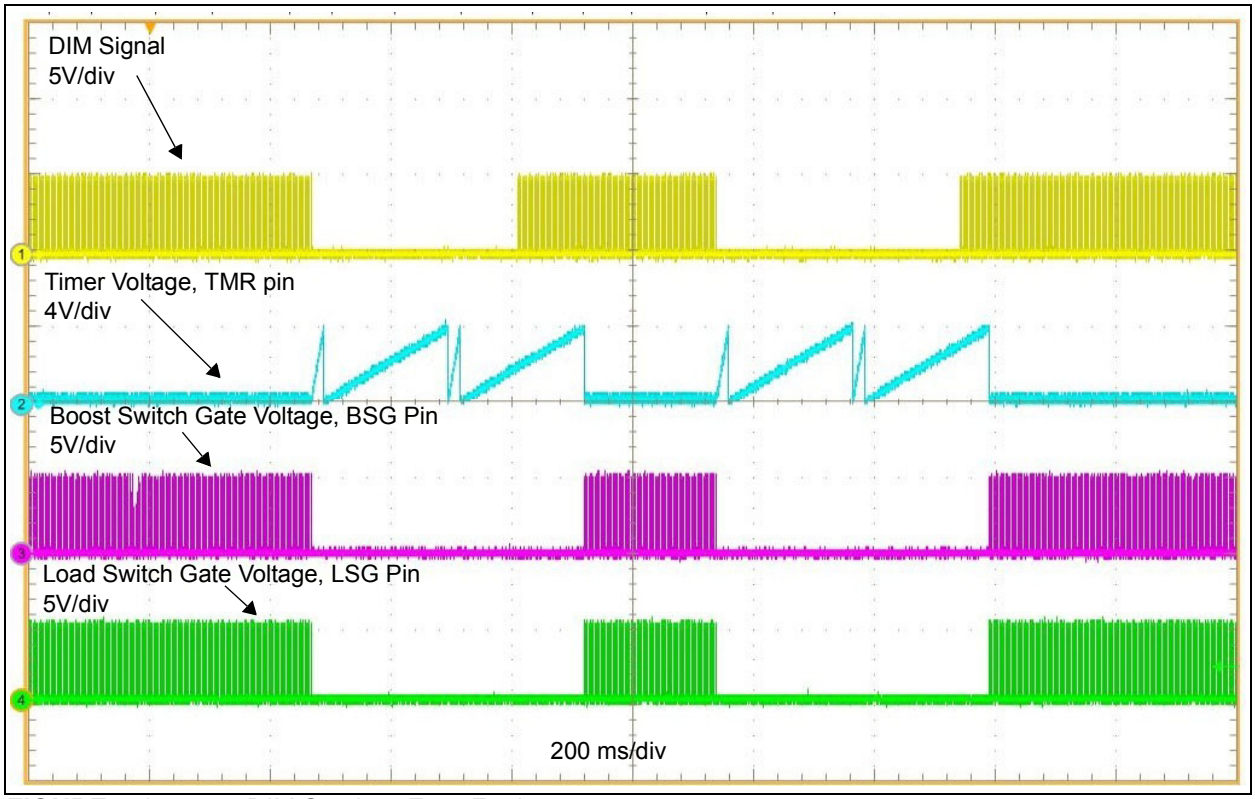


FIGURE 4-17: *DIM Stuck-at-Zero Fault.*

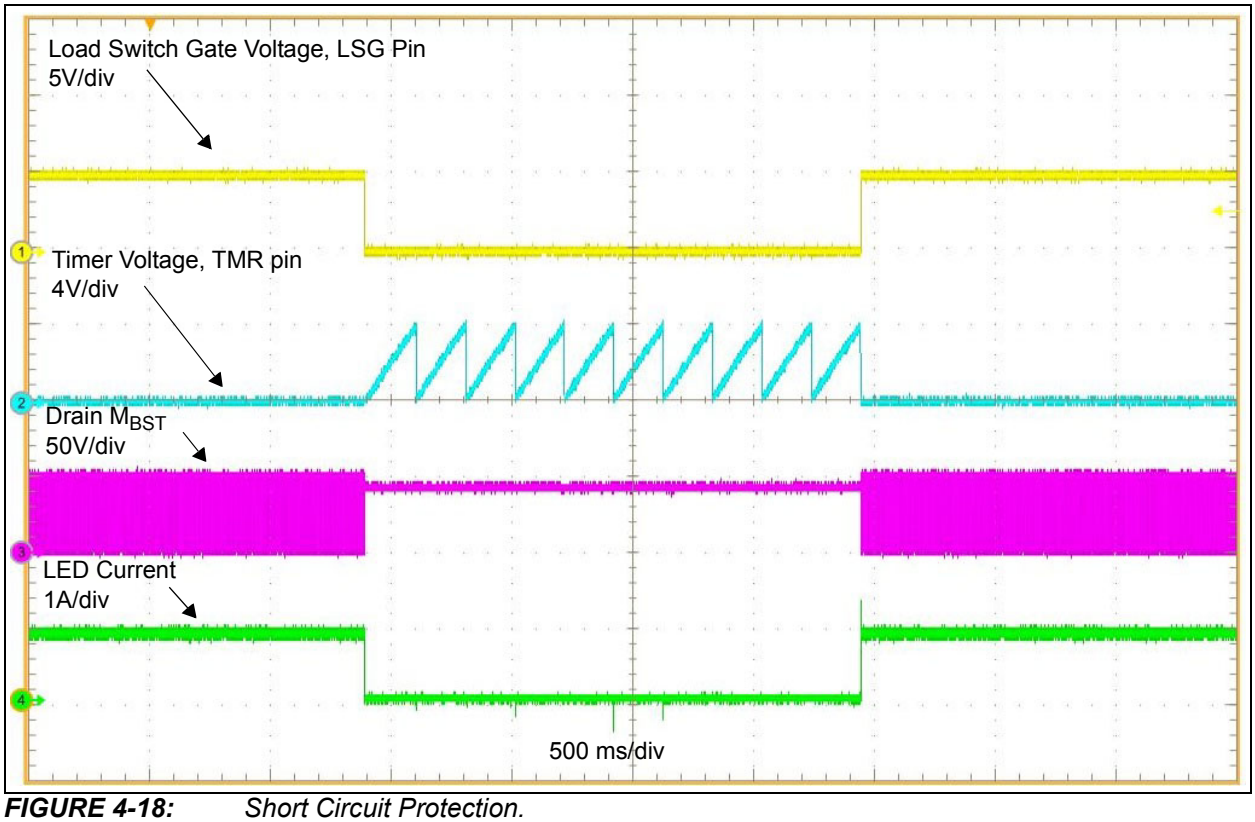


FIGURE 4-18: *Short Circuit Protection.*

5.0 APPLICATION INFORMATION

5.1 Selection of Components

5.1.1 BOOST INDUCTOR SELECTION

Values for inductance, peak and RMS currents are required to select the inductor. The input voltage, output voltage, switching frequency and the inductance value determine the peak-to-peak inductor current ripple. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value, and therefore, a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 30% of the average output current. The inductance value is calculated by Equation 5-1.

EQUATION 5-1:

$$L = \frac{(V_O \times (1-D) \times D)}{(\Delta I_L \times F_{SW})}$$

Where:

F_{SW} = *Switching Frequency*

V_O = *Boost Converter Output Voltage*

D = *Duty Cycle* $= \frac{(V_O - n \times V_{IN})}{V_O}$

n = *Efficiency of Boost Converter*

ΔI_L = *Inductor Ripple Current* $= 30\% \times I_{OUT}$

I_{OUT} = *Average Output Current*

V_{IN} = *Boost Converter Input Voltage*

For a selected inductor, the inductor current ripple is given by Equation 5-2.

EQUATION 5-2:

$$\Delta I_L = \frac{V_{IN} \times D}{L \times F_{SW}}$$

The peak inductor current can be found using Equation 5-3.

EQUATION 5-3:

$$I_{L(PK)} = I_{OUT} + \frac{\Delta I_L}{2}$$

The saturation current of the inductor at the highest operating temperature must be rated higher than the peak inductor current calculated in Equation 5-3.

The RMS inductor current is calculated using Equation 5-4 and is used to calculate the I^2R losses in the inductor.

EQUATION 5-4:

$$I_{L(RMS)} = \sqrt{\left[D \times \left[I_{L(PK)}^2 + (I_{L(PK)} - \Delta I_L)^2 + (I_{L(PK)} \times (I_{L(PK)} - \Delta I_L))\right]\right]}$$

Maximizing efficiency requires the proper selection of the core material while minimizing the DC resistance or the winding resistance of the inductor. The DC resistance must be minimized but this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be significant. The core loss information is usually available at the supplier of the magnetic components.

The power dissipated in the inductor can be calculated by Equation 5-5.

EQUATION 5-5:

$$P_{INDUCTOR} = I_{L(RMS)}^2 \times DCR$$

Where:

DCR = *DC Resistance of the Inductor*

5.1.2 OUTPUT (BOOST) CAPACITOR SELECTION

The type of output capacitor is usually determined by its equivalent series resistance (ESR) value. Voltage and RMS current capability are two other important factors in the selection of the output capacitor. The ESR of the output capacitor is usually the main cause of the output ripple. It also affects the control loop from a stability point of view. The maximum value of the ESR can be calculated using Equation 5-6.

EQUATION 5-6:

$$ESR_{C_{OUT}} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_L}$$

Where:

$\Delta V_{OUT(PP)}$ = *Peak-to-Peak Output Voltage Ripple*

The calculation shown in Equation 5-7 can be used to calculate the minimum value of the output capacitor.

EQUATION 5-7:

$$C_{OUT} = \frac{I_{OUT} \times D}{F_{SW} \times \Delta V_{OUT(PP)}}$$

The RMS current of the output capacitor can be calculated by Equation 5-8.

EQUATION 5-8:

$$I_{C_{OUT(RMS)}} = I_{OUT} \times \sqrt{\frac{D}{1-D}}$$

5.1.3 INPUT CAPACITOR SELECTION

For a required input voltage ripple, the minimum value of the input capacitor that should be used is calculated by Equation 5-9.

EQUATION 5-9:

$$C_{IN} = \frac{\Delta I_L}{8 \times F_{SW} \times \Delta V_{IN(PP)}}$$

Where:

$\Delta V_{IN(PP)}$ = *Peak-to-Peak Input Voltage Ripple*

To protect the IC from inductive spikes or any overshoot, a larger value of input capacitance may be required.

5.1.4 POWER MOSFET SELECTION

To ensure safe operation, the drain-to-source voltage rating of the MOSFET must be at least 20% greater than the maximum switch node voltage. This voltage, along with the RMS current rating, can be calculated using Equation 5-10 and Equation 5-11.

EQUATION 5-10:

$$V_{DS} \geq 1.5 \times V_{OUT(MAX)}$$

Where:

$V_{OUT(MAX)}$ = *Maximum Output Voltage*

EQUATION 5-11:

$$I_{POWER\ MOSFET(RMS)} = I_{OUT} \times \frac{\sqrt{D}}{1-D}$$

The current rating of the MOSFET is recommended to be at least 10% higher than the calculated value in Equation 5-11. Selecting a MOSFET with a lower gate charge will help minimize the gate drive and switching losses. The package of the MOSFET must be selected taking into account the total converter losses, ambient operating temperature and the maximum allowable temperature.

5.1.5 RECTIFIER DIODE SELECTION

The diode's reverse breakdown voltage must be at least equal to the drain-to-source voltage rating of the MOSFET. The current rating of the diode should exceed the current calculated in Equation 5-12.

EQUATION 5-12:

$$I_D = I_L \times (1-D) = I_{OUT}$$

The package of the diode must be selected in such a way that it is able to dissipate power such that it does not exceed the maximum allowable temperature.

5.1.6 BOOST CURRENT SENSE RESISTOR SELECTION

The output of the boost regulator is V_{BRO} and its limits are $0 < V_{BRO} < 5V$. The boost regulator must go through transient response during dimming off-to-on transient and replenish the V_{BRO}. The V_{BRO} at full brightness in Steady state should be set at around 2V to allow enough headroom for faster transient response, maintain peak LED current pulse at Steady state full brightness level, and achieve better dimmed output current accuracy.

The equation calculation of V_{BRO} is:

EQUATION 5-13:

$$V_{BRO} = \left[I_{OUT} + \frac{V_{IN}}{2L \times F} \left(\frac{V_{OUT} - n \times V_{INB}}{V_{OUTB}} \right) \right] \times R_{BCS} \times 10 + 0.8V$$

Where:

V_{BRO} = *Output Voltage for Boost Regulator*
V_{INB} = *Boost Stage Input Voltage*
V_{OUTB} = *Boost Stage Output Voltage*
I_{OUTB} = *Output Current (LED Load Current)*
n = *Effieiency of the Boost Converter*
R_{BCS} = *Boost Current Sense Resistor*

Using the upper expression by imposing wanted V_{BRO} (2-2.5V) value for regulator in Steady state, then results R_{BCS} expression.

EQUATION 5-14:

$$R_{BCS} = \frac{V_{BRO} - 0.8V}{\left[I_{OUTB} + \frac{V_{INB}}{2L \times F} \left(\frac{V_{OUT} - n \times V_{INB}}{V_{OUTB}} \right) \right] \times 10}$$

Example: for V_{BRO} = 2.5V, I_{OUTB} = 0.4A, V_{INB} = 40V, V_{OUTB} = 45V, n = 0.85, f = 200 kHz, L = 68 µH, results R_{BCS} = 0.473 ohms and we can choose 0.5 ohms.

This equation is true for Steady state regulation.

5.1.7 BOOST REGULATOR AND FLYBACK REGULATOR COMPENSATION NETWORK COMPONENTS SELECTION

Equation 5-15 and Equation 5-17 can be used to calculate the compensation components associated with the boost regulator output.

EQUATION 5-15:

$$R_{BRO} = \frac{2R_{BCS} \times (R_{LCS} + R_{OB}) \times (\pi f_C R_{OB} C_{OB})}{(125(1 - D_B)R_{OB} \times R_{LCS} \times g_m)}$$

Where:

- R_{BCS} = *Boost Current Sense Resistor*
- R_{LCS} = *LED Load Current Sense Resistor*
- R_{OB} = *LED Load Equivalent Resistance*
- f_C = *Crossover Frequency of the Control Loop of the Boost Regulator, $f_C = f_{RHPZ}/3$*
- C_{OB} = *Output Boost Capacitor Value*
- g_m = *Transconductance of Boost Regulator BRO*

EQUATION 5-16:

$$C_{BRO} = \frac{6L}{R_{BRO} \times R_{OB}(1 - D_B)^2}$$

Where:

- R_{BRO} = *Boost Compensation Network Resistor*
- R_{OB} = *LED Load Equivalent Resistance*
- L = *Boost Inductor Inductance*
- D_B = *Boost Regulator Duty Cycle*

Equation 5-17 and Equation 5-18 can be used to calculate the compensation components associated with the flyback regulator output.

EQUATION 5-17:

$$C_{FRO} = \frac{3M \times \frac{L_{PRI}}{N_{P2S}^2} \times D_{FMAX}}{R_{FRO} \times \frac{V_{OUTF}}{I_{OUTF}} \times (1 - D_{FMAX})^2}$$

Where:

- M = *Ratio of Flyback Converter Crossover Frequency to the Flyback Compensation Network Zero Frequency*
- L_{PRI} = *Transformer Primary Inductance*
- N_{P2S} = *Transformer Turn Ratio Primary to Secondary*
- D_{FMAX} = *Flyback Converter Maximum Duty Ratio at $V_{IN(MIN)}$*
- R_{FRO} = *Flyback Regulator Compensation Network Resistor*
- V_{OUTF} = *Output Voltage of the Flyback Converter*
- I_{OUTF} = *Output Current of the Flyback Converter*

EQUATION 5-18:

$$R_{FRO} = \frac{C_{OUTF} \times R_{OUTF}}{2 \times C_{FRO}}$$

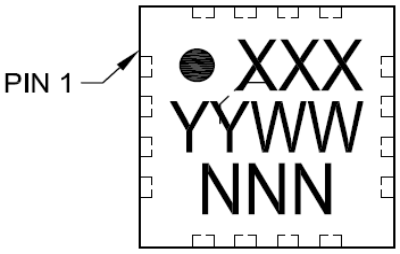
Where:

- C_{OUTF} = *Flyback Converter Output Capacitor*
- R_{OUTF} = *Flyback Converter Equivalent Output Resistor*
- C_{FRO} = *Flyback Regulator Compensation Network Capacitor*

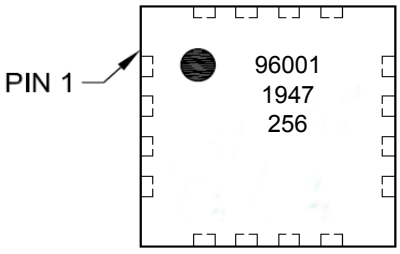
6.0 PACKAGING INFORMATION

Package Marking Information

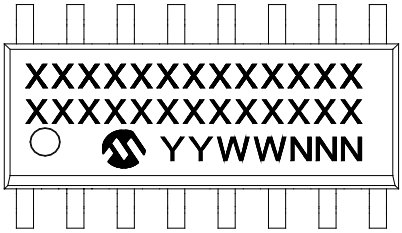
16-Lead VQFN (3x3 mm)



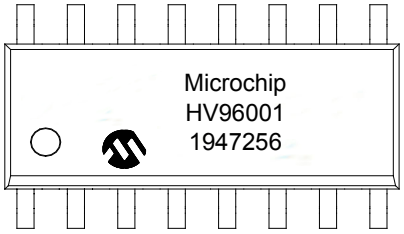
Example:



16-Lead SOIC (Narrow Body)

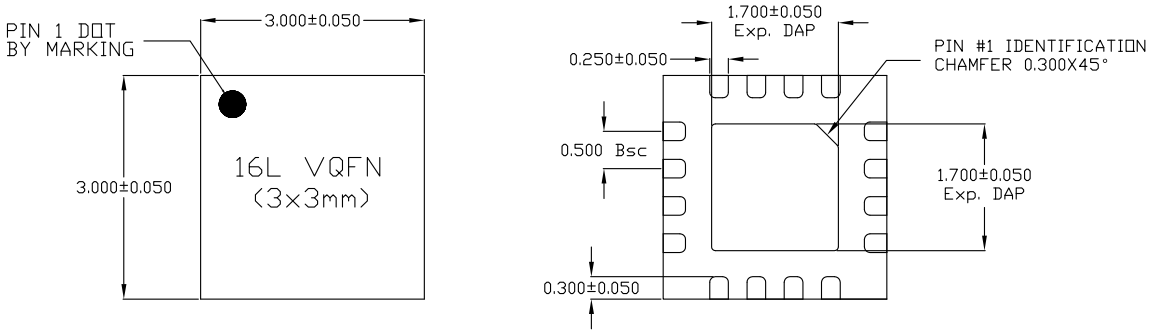


Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.



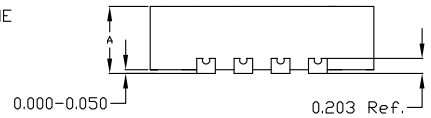
TOP VIEW

BOTTOM VIEW

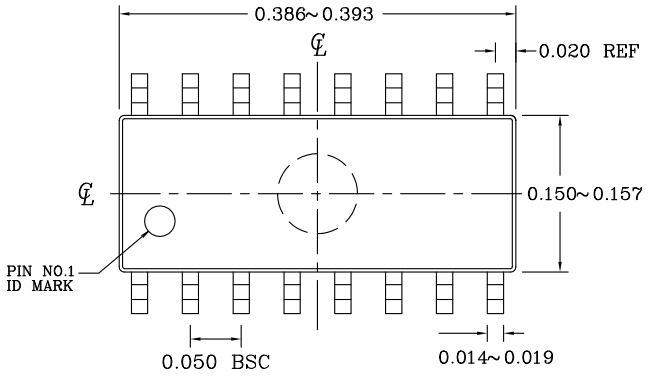
NOTE:

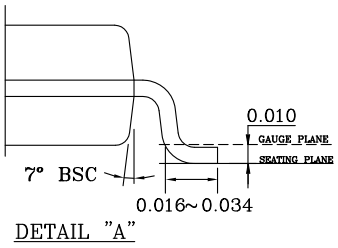
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

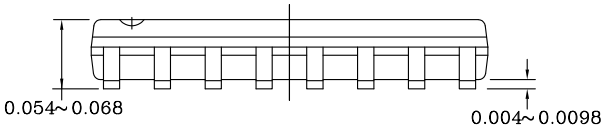
		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

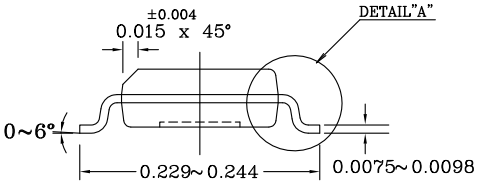


SIDE VIEW









NOTE:

1. LEAD COPLANARITY SHOULD BE 0 TO 0.004" MAX.
2. PACKAGE SURFACE FINISHING: VDI 24~27 (DUAL)
   PACKAGE SURFACE FINISHING: VDI 13~15 (16L SOIC(NB) MATRIX)
3. ALL DIMENSION EXCLUDING MOLD FLASHES.
4. THE LEAD WIDTH, B TO BE DETERMINED AT 0.0075"
   FROM THE LEAD TIP.

APPENDIX A: REVISION HISTORY

Revision A (January 2020)

- Original release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	HV96001	Secondary-Side, Micro-Interfaced, Flicker-Free LED Controller with Enhanced PWM and Analog Dimming
Temperature Range:	E =	-40°C to +125°C
Package:	D7X =	Plastic Small Outline
	NFA =	Very Thin Quad Flatpack No-Leads

Examples:

a) HV96001-E/D7X: Extended temperature, 16LD SOIC

b) HV96001-E/NFA: Extended temperature, 16LD VQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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