HV7358

16-Channel, 3-Level HV Ultrasound Transmitter with Built-in Transmit Beamformer

Features

- 16-Channel with Active Return to True Zero
- Up to ±80V Output Voltage and ±1.6A Output Current
- Programmable Output Current: 0.3A, 0.5A, 1.0A and 1.6A
- -40 dB Second Harmonic at 5 MHz, ±70V, 5-Cycle
- Built-in T/R Switch, Damper and Protection Diodes
- Built-in Linear Regulators for Floating Gate Driver
- Internal Low Jitter Phase-Locked Loop (PLL) Clock Multiplier for TX_{CH} Clock
- 30 MHz to 80 MHz Input Clock Frequency in PLL Mode
- 30 MHz to 200 MHz Input Clock Frequency (in Non-PLL Mode) over Low-Voltage Differential Signaling (LVDS) Connection
- PLL Frequency Integer Multiplier x1, x2, x3, x4, x5, x6, x8
- Internal Clock Frequency (f_C), up to 200 MHz to Allow a 5 ns Delay Resolution
- Ensured Synchronize Internal Transmit Clock Across Devices in the Same Phase
- PLL Circuit can be Bypassed and Shut Down to Reduce the Power Consumption
- Built-in Active Bleeder Circuit on V_{PP} and V_{NN} for Rapid Capacitor Discharging to Reduce the Time Required for Transmit Voltage Adjustment
- Configurable 12-Bit Delay for Beamform per Channel
- Stores up to Four TX_{CH} Patterns with the Optional Local t_{OFF} Counter, Allowing the TX_{CH} Apodization Use of the Pulse-Width Modulator (PWM)
- TX_{CH} Patterns, up to 255 Pulses with Programmable Pulse Width and Frequency
- Programmable Continuous Wave (CW) Frequency Divide Ratio, from 1 to 255 of the Input Clock Frequency
- Set-and-Go Feature in CW Mode Reduces the Digital Cross-Coupled Noise on PCB
- High-Speed LVDS SPI, Typical 200 MHz Operation Allows Fast Device Programming
- SPI Group Broadcast Mode for Fast Data Writing
- Two-Wire I^2C Interface for Control and Status Reading
- 13 mm x 13 mm TFBGA Package with 0.8 mm Pitch

Applications

- Medical Portable Notebook Size and Trolley Size Ultrasound Imaging System
- NDT Ultrasound Pulsers and Industrial Use
- HV Pulse Pattern Generators

General Description

The HV7358 is a 16-Channel, 3-Level HV ultrasound transmitter with built-in digital beamformer. Each channel is capable of swinging up to ±80V with an active discharge back to 0V. The outputs can source and sink more than 1.6A to achieve fast output rise and fall times. The active discharge is also capable of ±1.6A for a fast return to ground. The HV7358 additionally features the programmable output current. The output current can be programmed via the I^2C Interface. All 16 channels have built-in output protection diodes and clamp diodes. The HV7358 features 16 Integrated T/R switches, a receive damping circuit and an active RTZ circuit. The active RTZ circuit has a typical R_{ON} of 300Ω. The active RTZ circuit activates to discharge the transmitter's output internal node when the transmit burst ends.

The gate drivers for the output MOSFETs are powered by built-in linear floating regulators referenced to V_{PP} and V_{NN}. This direct coupling topology of the gate drivers eliminates the need for the gate driver and floating power supply circuit.

The HV7358 features an internal low-jitter PLL clock multiplier for generating the delay clock for the built-in digital beamformer. The clock input has to accept an LVDS differential system clock with frequencies from 30 MHz (min.) to 80 MHz (max.) in PLL mode and a frequency from 30 MHz (min.) to 200 MHz (max.) in Non-PLL mode. The clock multiplier is programmable by x1, x2, x3, x4, x5, x6 and x8, and the maximum delay clock frequency can be up to 200 MHz, allowing incremental delays down to 5 ns. This feature eliminates the need for the power-hungry external clock synthesizer/multiplier to generate the high-frequency delay clock from the system/sampling clock. The transmitter outputs are synchronized with the delay clock to reduce phase noise.

Package Type

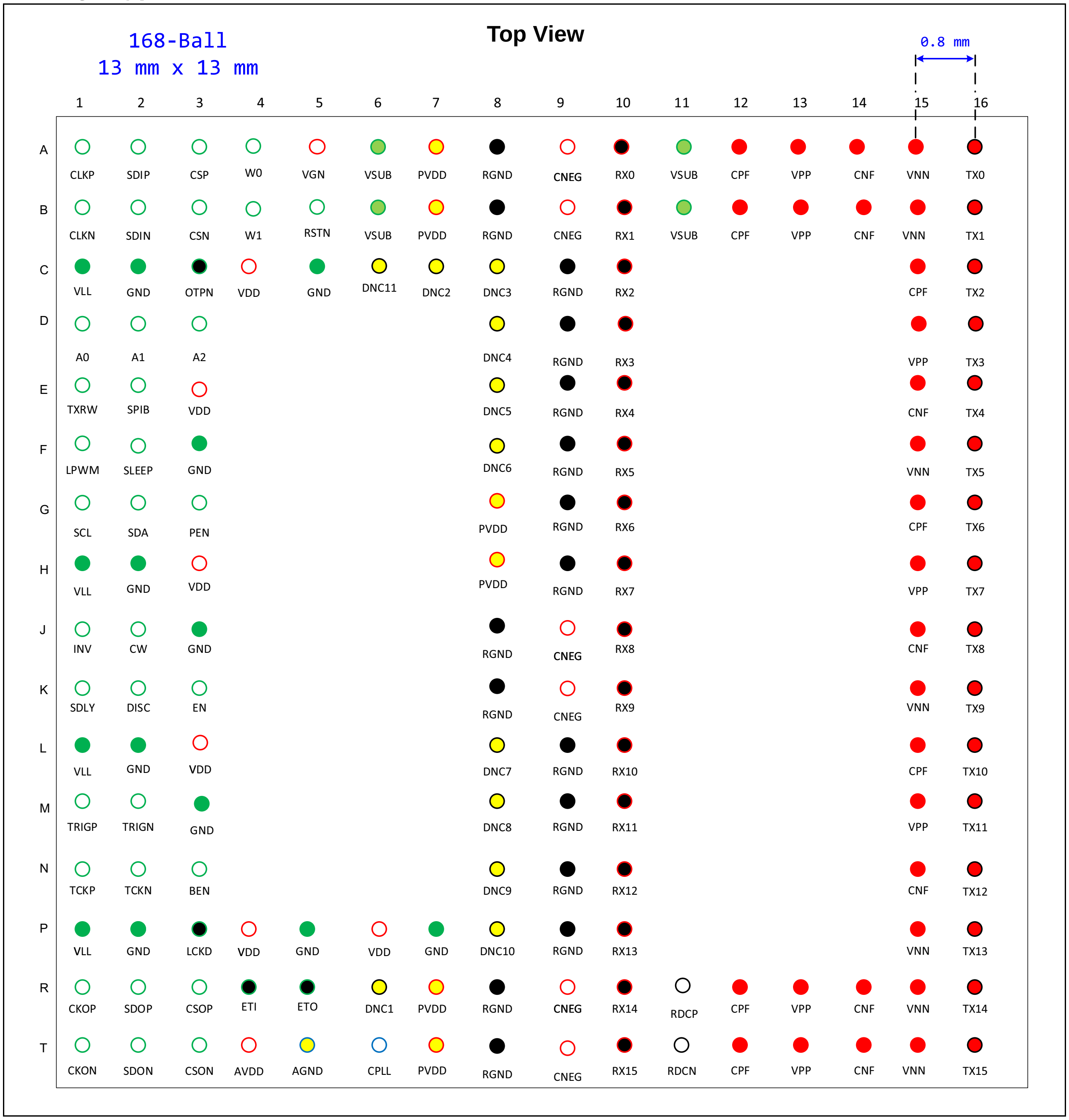
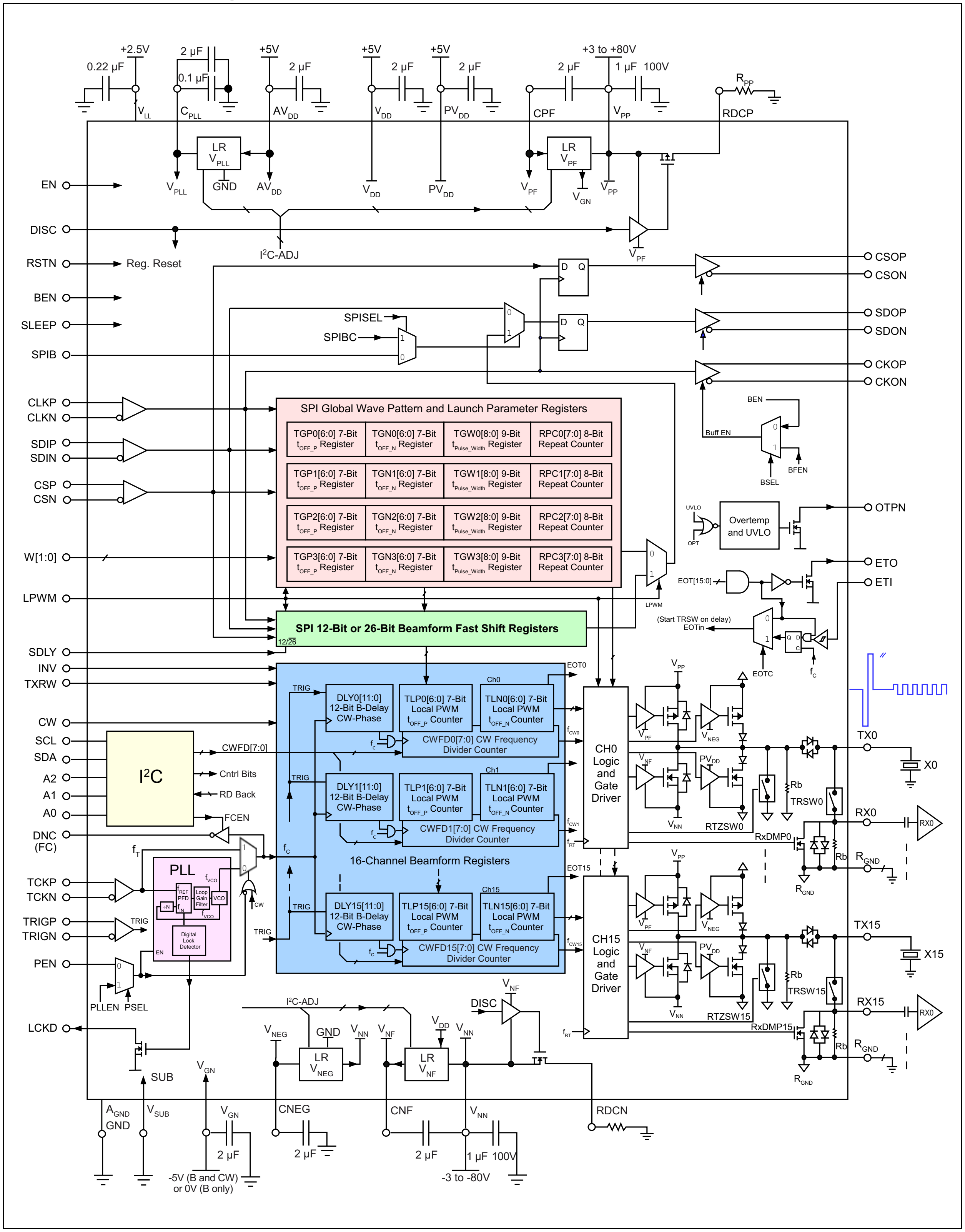


FIGURE 1: *HV7358 Pin Configuration.*

The 168-lead TFBGA, with an outline 13 mm x 13 mm body, 1.2 mm (max.) height and 0.8 mm pitch package, is available.

Note that the backside of the die bias voltage, V_{SUB}, must be connected to ground (0V, GND). Because this package is mounted onto a 4 x 4 inch, 4-layer, 1 oz copper PCB, the maximum allowable power dissipation is about 4W. The maximum junction temperature is lower than +130°C and the package has an ambient temperature of +55°C.

Functional Block Diagram



Typical Applications

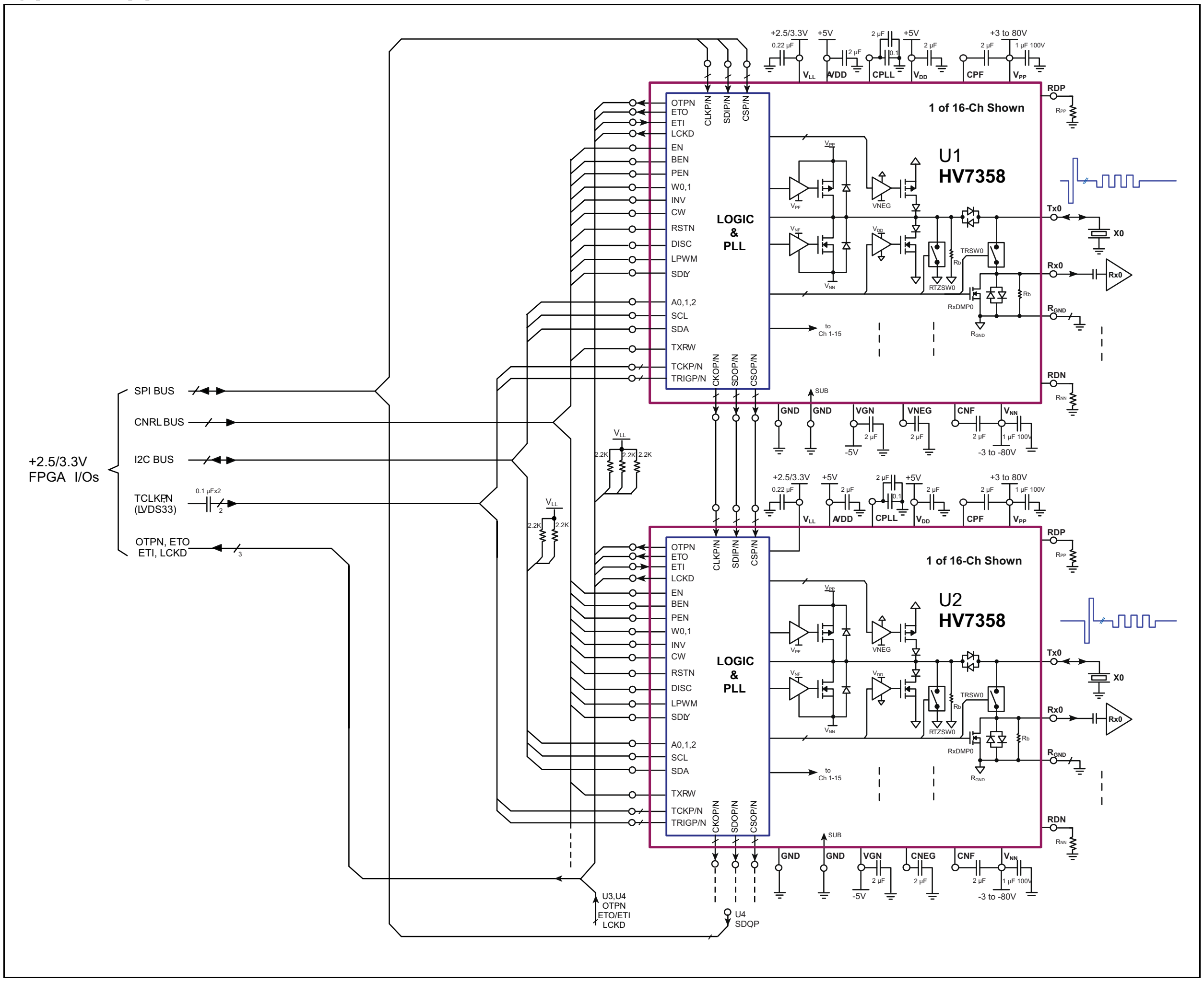


FIGURE 2: Multiple HV7358 Devices are Working Together as a 64-Channel Pulser and Beamformer. For More Details about Daisy-Chained SPI Connections, see Figure 4-2 and the Associated Discussion.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Substrate (V_{SUB}, connect to GND) 0V
All Logic I/O and CLK Pins .... -0.5V to +5.5V
Logic Voltage (V_{LL} pin has diode to V_{DD} and AV_{DD}) .... -0.5V to +5.5V
Low-Voltage Positive PLL Supply .... -0.5V to +5.5V
Low-Voltage Positive Supply .... -0.5V to +5.5V
Low-Voltage Positive RTZ Supply .... -0.5V to +5.5V
V_{GN} Negative Power Supply .... -5.5V to +0.5V
V_{NEG} Regulator Bypass Cap .... -5.5V to +0.5V
V_{PLL} Regulator Bypass Cap .... -0.5V to +5.5V
V_{PP} Power Supply .... -1V to +85V
V_{NN} Power Supply .... -85V to -1V
RDCP V_{PP} Rail Bleed Switch(2) .... -1V to +82V
RDCP V_{NN} Rail Bleed Switch(2) .... -82V to + -1V
TX_{CH} Pin Voltage (no load and all switches off) .... -85V to +85V
RX_{CH} Pin to GND Voltage (at I_{RX} = ±500 mA DC) .... ±0.7V to ±1.4V
Operating Ambient Temperature Range(1) .... 0°C to +85°C
Storage Temperature Range(1) .... -55°C to +150°C
Junction Temperature(1) .... +125°C
High-Voltage Pins HBM (TX0~15, RX0~15, V_{PP}, V_{NN}, CPF, CNF, RDCP, RDCN pins)(1,3) .... -0.75 kV to +0.75 kV
Low-Voltage Pins HBM(1,3) .... -2 kV to +2 kV
Power Dissipation 5W
Thermal Resistance Junction to Ambient(2,4) .... 15.5°C/W
Thermal Resistance Junction to PCB(2,4) .... 3°C/W
Thermal Resistance Junction to Case(2,4) .... 2°C/W

Note 1: The design must try to meet the complete range of operating conditions, unless otherwise stated.

2: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

3: This device is not required for CDM or MM ESD tests.

4: EIA/JESSD51-9, 102 mm x 114 mm x 1.6 mm PCB, Horizontal Still Air, 56 Thermal Vias, T_A = +55°C, T_J = +125°C.

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

OPERATING SUPPLY VOLTAGES

Unless otherwise specified: V_{LL} = +2.5V, AV_{DD} = V_{DD} = +5.0V, V_{PP} = +80V, V_{NN} = -80V, V_{GN} = -5.0V, V_{SUB} = 0V, EN = PEN = BEN = 1, T_A = 0° to +85°C

Parameters	Sym.	Min.	Typ.	Max.	Unit	Conditions
Positive Logic Supply	V_{LL}	**2.375**	**2.50**	**3.625**	V	
Positive Low-Voltage PLL Supply	AV_{DD}	**4.75**	**5.0**	**5.25**	V	AV_{DD}, PV_{DD} and V_{DD} must have separated bypass cap to GND when they are connected to the same +5V
Positive Low-Voltage RTZ Supply	PV_{DD}	**4.75**	**5.0**	**5.25**	V	
Positive Low-Voltage Supply	V_{DD}	**4.75**	**5.0**	**5.25**	V	
Negative Voltage Supply	V_{GN}	**-5.25**	**-5.0**	**-4.75**	V	B mode and CW mode
		—	**0**	—		V_{GN} = 0 (B mode only)
Positive V_{PP} Voltage Supply	V_{PP}	**3.0**	—	**8.0**	V	In CW mode
		8.0	—	**80**		In B mode
Negative V_{NN} Voltage Supply	V_{NN}	**-8.0**	—	**-3.0**		In CW mode
		-80	—	**-8.0**		In B mode

Note: The device is not ensured to function outside the operating range.

POWER-UP AND POWER-DOWN SEQUENCES

Powering up/down in any arbitrary sequence will not cause any damage to the device. The powering up/down sequences are only recommended in order to minimize possible inrush current.

Step	Power-up Description	Step	Power-Down Description
1	V_{LL} On with Logic Signal Low	1	EN = 0 and the Logic Control Signal goes to Low
2	AV_{DD}, PV_{DD}, V_{DD} and V_{GN} On	2	V_{PP} and V_{NN} Off
3	V_{PP} and V_{NN} On	3	AV_{DD}, VP_{DD}, V_{DD} and V_{GN} Off
4	EN = 1 and Logic Control Signal Active	4	V_{LL} Off

Note: The HV7358 is a high-voltage CMOS I^2C with multiple supply rails. It is highly recommended to add a Schottky diode at each voltage rail to GND, with 2~3A and sufficient BV, on the same PCB device(s) in mounted. Only one set of such diodes is needed per PCB.

ELECTRICAL SPECIFICATIONS

Electrical Specifications: V_{LL} = +2.5V, AV_{DD} = V_{DD} = +5V, V_{PP} = +80V, V_{NN} = -80V, V_{GN} = -5V, V_{SUB} = 0V, EN = 1, SPIB = BEN = 0, T_A = +25°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
V_{LL} Quiescent Current	I_{LLQ}	—	2.0	7.0	µA	EN = PEN = 0, f_{TCK} = f_{CLK} = 0 MHz
AV_{DD} Quiescent Current	I_{AVDDQ}	—	0.5	5.0		
V_{DD} Quiescent Current	I_{DDQ}	—	58	75		
PV_{DD} Quiescent Current	I_{PVDDQ}	—	6.0	15		
V_{GN} Quiescent Current	I_{GNQ}	-5.0	-2.2	—		
V_{PP} Quiescent Current	I_{PPQ}	—	2.0	8.0		
V_{NN} Quiescent Current	I_{NNQ}	-14	-7.0	—		
V_{LL} Current at Chip Enabled	I_{LLEN}	—	0.01	0.1	mA	EN = 1, PEN = 0, f_{TCK} = f_{CLK} = 0 MHz
AV_{DD} Current at Chip Enabled	I_{AVDDEN}	—	0.3	1.5		
V_{DD} Current at Chip Enabled	I_{DDEN}	—	1.35	3.0		
PV_{DD} Current at Chip Enabled	I_{PVDDEN}	—	0.2	1.5		
V_{GN} Current at Chip Enabled	I_{VGNEN}	-1.5	-0.2	—		
V_{PP} Current at Chip Enabled	I_{PPEN}	—	0.1	1.0		
V_{NN} Current at Chip Enabled	I_{NNEN}	-0.75	-0.67	—		
AV_{DD} Current with PLL and Buffer Enabled	I_{AVDD_PLL}	—	4.7	8.0	mA	EN = PEN = BEN = 1, f_{TCK} = 40 MHz, f_C = 160 MHz(1)
V_{LL} CW Current	I_{LLCW}	—	3.0	10	mA	TX_{CH} one-channel output 5 MHz, continuous, no loads, CW = 1, CWOC = 1, V_{PP}/V_{NN} = ±5V(1)
AV_{DD} CW Current	I_{AVDDCW}	—	0.5	2.0		
V_{DD} CW Current	I_{DDCW}	—	8.0	15		
PV_{DD} CW Current	I_{PVDDCW}	—	1.45	5.0		
V_{GN} CW Current	I_{GNCW}	-10	-4.6	—	mA	TX_{CH} one-channel output 5 MHz, continuous, no loads, CW = 1, CWOC = 1, V_{PP}/V_{NN} = ±5V(1)
V_{PP} CW Current	I_{PPCW}	—	13	18		
V_{NN} CW Current	I_{NNCW}	-18	-10.5	—		

Note 1: Characterized only; not 100% tested in production.

TABLE 1-1: TX_{CH} OUTPUT P-CHANNEL MOSFET ON V_{PP}

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
B mode Output Current, BOC = `00b`	I_{OUT_P}	—	0.9	—	A	V_{PP} = +25V, R_L = 1Ω to GND, 20 ns pulse width at D% = 0.1%(1)
B mode Output Current, BOC = `01b`		—	0.6	—		
B mode Output Current, BOC = `10b`		—	0.3	—		
B mode Output Current, BOC = `11b`		—	0.15	—		
B mode Output Current, BOC = `00b`		—	1.6	—		V_{PP} = +80V, R_L = 1Ω to GND, 20 ns pulse width at D% = 0.1%(1)
B mode Output Current, BOC = `01b`		—	1.1	—		
B mode Output Current, BOC = `10b`		—	0.6	—		
B mode Output Current, BOC = `11b`		—	0.3	—		
On-Resistance B mode, BOC = `00b`	R_{ONB_P}	—	12	—	Ω	I_{SD} = 100 mA(1)
On-Resistance, CW = `1`, CWOC = `0`	R_{ONCW_P}	—	36	—		At V_{PP} = +5V(1)
On-Resistance, CW = `1`, CWOC = `1`		—	50	—		

Note 1: Characterized only; not 100% tested in production.

TABLE 1-2: TX_{CH} OUTPUT N-CHANNEL MOSFET ON V_{NN}

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
B mode Output Current, BOC = `00b`	I_{OUT_N}	—	-1.0	—	A	V_{NN} = -25V, R_L = 1Ω to GND, 20 ns pulse width at D% = 0.1%(1)
B mode Output Current, BOC = `01b`		—	-0.7	—		
B mode Output Current, BOC = `10b`		—	-0.36	—		
B mode Output Current, BOC = `11b`		—	-0.18	—		
B mode Output Current, BOC = `00b`		—	-1.6	—		V_{NN} = -80V, R_L = 1Ω to GND, 20 ns pulse width at D% = 0.1%(1)
B mode Output Current, BOC = `01b`		—	-1.0	—		
B mode Output Current, BOC = `10b`		—	-0.5	—		
B mode Output Current, BOC = `11b`		—	-0.3	—		
On-Resistance B mode, BOC = `11b`	R_{ONB_N}	—	10.5	—	Ω	I_{SD} = 100 mA(1)
On-Resistance, CW = `1`, CWOC = `0`	R_{ONCW_N}	—	42	—		At V_{NN} = -5V(1)
On-Resistance, CW = `1`, CWOC = `1`		—	59	—		

Note 1: Characterized only; not 100% tested in production.

TABLE 1-3: TX_{CH} DAMPING P-CHANNEL MOSFET ON GND

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
B mode Output Current, BOC = `00b`	I_{OUT_PDMP}	—	1.7	—	A	R_L = 1Ω, TX_{CH} to V_{NN} = -25V, 20 ns pulse width at D% = 0.1%(1)
B mode Output Current, BOC = `01b`		—	1.2	—		
B mode Output Current, BOC = `10b`		—	0.6	—		
B mode Output Current, BOC = `11b`		—	0.3	—		
B mode Output Current, BOC = `00b`		—	2.3	—		R_L = 1Ω, TX_{CH} to V_{NN} = -80V, 20 ns pulse width at D% = 0.1%(1)
B mode Output Current, BOC = `01b`		—	1.5	—		
B mode Output Current, BOC = `10b`		—	0.8	—		
B mode Output Current, BOC = `11b`		—	0.4	—		
On-Resistance	R_{ON_PDMP}	—	8.1	—	Ω	I_{SD} = 100 mA(1)

Note 1: Characterized only; not 100% tested in production.

TABLE 1-4: TX_{CH} DAMPING N-CHANNEL MOSFET ON GND

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
B mode Output Current, BOC = `00b`	I_{OUT_NDMP}	—	-1.6	—	A	R_L = 1Ω, TX_{CH} to V_{PP} = +25V, 20 ns pulse width at D% = 0.1%(1)
B mode Output Current, BOC = `01b`		—	-1.0	—		
B mode Output Current, BOC = `10b`		—	-0.5	—		
B mode Output Current, BOC = `11b`		—	-0.3	—		
B mode Output Current, BOC = `00b`		—	-2.3	—		R_L = 1Ω,TX_{CH} to V_{PP} = +80V, 20 ns pulse width at D% = 0.1%(1)
B mode Output Current, BOC = `01b`		—	-1.5	—		
B mode Output Current, BOC = `10b`		—	-0.8	—		
B mode Output Current, BOC = `11b`		—	-0.4	—		
On-Resistance	R_{ON_NDMP}	—	4.2	—	Ω	I_{SD} = 100 mA(1)

Note 1: Characterized only; not 100% tested in production.

TABLE 1-5: RTZ AUTO-BLEED AND V_{PP}/V_{NN} SUPPLY RAIL BLEED SWITCHES

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
RTZSW On-Resistance	R_{RTZSW}	—	190	—	Ω	I_{SD} = ±1.0 mA(1)
Bleed Resistor to GND per Channel(1)	R_b	—	17	—	kΩ	
RTZSW Off Withstand Voltage	V_{RTZSW}	-80	—	+80	V	I_{SW} = ±100 µA(1)
RDCP Switch Output Current	I_{RDCP}	—	5.8	—	mA	V_{PP} = +80V(1)
RDCN Switch Output Current	I_{RDCN}	—	-6.0	—		V_{NN} = -80V(1)
Voltage of RDCP	V_{RDCP}	0	—	+82	V	$I_{RDCP/N}$ = ±0.6$A_{(PK)}$(1)
Voltage of RDCN Bleed Pin for V_{NN}	V_{RDCN}	-82	—	0		
Suggested Bleed Resistor Value to GND for RDCP and RDCN Pins	R_{DCP}	—	1.0	—	kΩ	An external resistor (0.25W) for pin to GND suggested(2)
	R_{DCN}	—	1.0	—		

Note 1: Characterized only; not 100% tested in production.
2: Design guidance only.

TABLE 1-6: TX_{CH} OUTPUT ISOLATION DIODES AND BLEED RESISTOR

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Diode Forward Voltage	V_F	—	1.2	—	V	I_{FM} = 300 mA
Forward Continuous Current(1)	I_{FM}	—	300	—	mA	
Peak Forward Pulse Current	I_{FSM}	—	3.0	—	A	PW = 50 ns(1)
Total Capacitance of Diode Pair	C_T	—	3.5	—	pF	At 1 MHz, 1 dBm, 0V DC(1)

Note 1: Characterized only; not 100% tested in production.

TABLE 1-7: TRSW AND RXDMP SWITCHES

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
TRSW Analog Switch-On Resistor	R_{TRSW}	—	17	22	Ω	I_{TRSW} = ±1 mA(1)
TRSW Off Withstand Voltage	V_{TRSW}	-80	—	+80	V	I_{SW} = ±100 µA(1)
RX_{CH} to GND Protection Diode	V_F	—	±0.8	±1.2	V	I_F = ±20 mA(1)
RXDMP Switch-On Resistance	R_{RXDMP}	—	15	—	Ω	I_{SD} = ±1 mA(1)
RX_{CH} Bleed Resistor to GND(1)	R_b	—	17	—	kΩ	
RX_{CH} Pin to GND Capacitance	C_{RXG}	—	—	7.0	pF	At 1 MHz, 1 dBm, 0V DC(2)

Note 1: Characterized only; not 100% tested in production.
2: Design guidance only.

TABLE 1-8: BUILT-IN VOLTAGE LINEAR REGULATORS

Unless otherwise specified: V_{LL} = +2.5V, AV_{DD} = V_{DD} = +5V, V_{PP} = +80V, V_{NN} = -80V, V_{GN} = -5V, V_{SUB} = 0V, EN = 1, PEN = BEN = 0, T_A = +25°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output P-Channel Gate Drive Voltage Referenced to V_{PP}	V_{PF}	-4.9	-5.0	-5.1	V	$(V_{GN} – V_{PP})$ < -8.0V
Output N-Channel Gate Drive Voltage Referenced to V_{NN}	V_{NF}	5.1	5.0	5.3	V	$(V_{DD} – V_{NN})$ > +8.0V
Output P-Channel Gate Drive Voltage Referenced to GND	V_{NEG}	-5.1	-5.0	-4.9	V	CW = 0
Output PLL Voltage Referenced to GND	V_{PLL}	4.4	4.6	4.8	V	PEN = 1
Dropout Voltage of $(V_{PP} – V_{GN})$	V_{DOPF}	—	3.5	—	V	100 mA load, drop to 95% at worst case(1)
Dropout Voltage of $(V_{DD} – V_{NN})$	V_{DONF}	—	3.5	—	V	
Dropout Voltage of $(V_{NEG} – V_{NN})$	V_{DONEG}	—	1.36	—	V	10 mA load, drop to 95% at worst case(1)
Dropout Voltage of $(AV_{DD} – V_{PLL})$	V_{DOPLL}	—	0.31	—	V	1 mA load, drop to 95% at worst case(1)

Note 1: Characterized only; not 100% tested in production.

TABLE 1-9: LOGIC INPUTS CHARACTERISTICS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Rise/Fall Time of Input Logic Signals	t_{rf}	—	—	3.5	ns	10% to 90% at pin(s)(2)
Input Logic Low Voltage(1)	V_{IL}	0	—	0.2 V_{LL}	V	
Input Logic High Voltage(1)	V_{IH}	0.8	—	V_{LL}	V	
Input Logic Low Current	I_{IL}	-0.1	—	—	µA	
Input Logic High Current	I_{IH}	—	—	1.0	µA	
Input Capacitance(2)	C_{IN}	—	2.0	3.0	pF	
EN Switching On Time	t_{EN}	—	300	—	µs	50% EN rise to TX_{CH} ready(2)
EN Switching Off Time		—	300	—	ns	50% EN fall to TX_{CH}, all output FETs on HV rails are off(1)
Internal Reset Signal Width(2)	t_{RST}	100	—	150	ns	
Reset Input Low Time(1)	t_{RSTN}	100	—	—	ns	

Note 1: Characterized only; not 100% tested in production.
2: Design guidance only.

TABLE 1-10: OVERTEMPERATURE AND UNDERVOLTAGE PROTECTIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
OTP Output Maximum Pull-up	V_{OH}	—	—	5.25	V	
OTP Output Low Maximum Voltage	V_{OL}	—	—	0.1	V	At 100 µA
		—	—	0.4	V	At 4 mA
OTP Output High Current	I_{OFF}	—	—	10	µA	0° to +125°C, at 5.25V pull-up(1)
Thermal Shutdown Trip Point	T_{TRIP}	+135	—	+155	°C	OTP = H when thermal shutdown occurs(1)
Thermal Shutdown Hysteresis	T_{HYS}	—	40	—		
V_{DD} Ok Voltage	V_{DDUVON}	3.9	4.2	4.5	V	External power supply inputs(1)
V_{DD} UVLO Trip Voltage	$V_{DDUVOFF}$	3.7	3.95	4.3		
V_{LL} Ok Voltage	V_{LLUVON}	1.65	1.75	1.85		
V_{LL} UVLO Trip Voltage	$V_{LLUVOFF}$	1.5	1.6	1.7		
V_{PLL} Ok Voltage	$V_{PLLUVON}$	—	3.8	—		+4.5V LR for PLL circuit(1)
V_{PLL} UVLO Trip Voltage	$V_{PLLUVOFF}$	—	3.3	—		
V_{NEG} Ok Voltage	V_{NGUVON}	—	–4.0	—		-5V LR for RTZ P-FET gate drive circuit(1)
V_{NEG} UVLO Trip Voltage	$V_{NGUVOFF}$	—	–4.4	—		
$V_{PP\text{-}PF}$ Ok Voltage	$V_{PP\text{-}PFON}$	—	–3.4	—	V	Floating ±5V LRs for HV P-FET and N-FET gate drive circuit
$V_{PP\text{-}PF}$ UVLO Trip Voltage	$V_{PP\text{-}PFOFF}$	—	–3.8	—		
$V_{NF\text{-}NN}$ Ok Voltage	$V_{NF\text{-}NNON}$	—	3.8	—		
$V_{NF\text{-}NN}$ UVLO Trip Voltage	$V_{NF\text{-}NNOFF}$	—	3.4	—		

Note 1: Characterized only; not 100% tested in production.

TABLE 1-11: SWITCH TIMING CHARACTERISTICS

Unless otherwise specified: V_{LL} = +2.5V, AV_{DD} = V_{DD} = +5V, V_{PP} = +80V, V_{NN} = -80V, V_{GN} = -5V, V_{SUB} = 0V, EN = 1, PEN = BEN = 0, T_A = +25°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
SDI Valid to CLK Setup Time(1)	t_1	2.0	—	—	ns	
CLKP to SDI Data Hold Time(1)	t_2	2.0	—	—	ns	
CLK High Time % of $1/f_{CLK}$(1)	t_3	45	—	55	%	
CLK Low Time % of $1/f_{CLK}$(1)	t_4	45	—	55	%	
CSN Minimum High Time Between SPI Words	t_5		3-cycle		CLK	Designed for f_{CLK} = 200 MHz(2)
CLKP Rise to CSN Rise(1)	t_6	—	2.0	—	ns	
CSON Fall to CLKP Rise(1)	t_7	—	2.0	—	ns	
SDOP Delay from CLKP Rise	t_8	—	2.0	3.0	ns	SPIB = 0, 3 pF Load(1)
CSN Rise to CLK Rise(1)	t_9	—	2.0	—	ns	
CSN Rise to TXRW or to SPIB(2)	t_{10}		9-cycle		TCK	
CLK Start, TXRW, SPIB to CSN Fall(2)	t_{11}	—	200	—	ns	
SDIP to SDOP Delay	t_{12}	—	10	—	ns	SPIB = 1, 3 pF Load(1)
TXRW Rise to CLKP Rise Edge(1)	t_{13}	—	6.0	—	ns	
TX_{CH} Ready Latency after TXRW = 1(2)	t_{14}		12-cycle		TCK	
SPI or I^2C Ready after TXRW = 0(2)	t_{15}		2-cycle		TCK	
TRIG Rise to CLK Rise Setup Time	t_{16}		0.5-cycle		ns	
W0 or W1 Pin Ready to TXRW Rise Time	t_{17}		3-cycle		ns	
W0 or W1 Pin Holdup Time	t_{18}		3-cycle		ns	
TRIG High Time(2)	t_{19}		6-cycle		TCK	
TXRW Rise to TRIG Rise Time	t_{20}		3-cycle		ns	
CW Pin Changing to TXRW Rise Time	t_{21}		3-cycle		ns	Mode changing time(2)
ETO High to TXRW High or Low Time	t_{22}	2.0	—	10	ns	
Minimum TXRW Low Time	t_{23}	—	1.2	—	µs	Must wait for the TRSW to completely turn off(2)
This Chip ETO Change Time(1)	t_{24}	—	45	—	ns	
f_C Clock Cycles before ETO Rise(1)	t_{25}		11-cycle		TCK	
ETI High to f_C Clock Rise Setup Time(1)	t_{26}		0.5-cycle		ns	
Minimum TCK Cycles after ETI Rise	t_{27}		TRDLY[4:0] + (6-cycle)		TCK	Stop TCK for power saving in RX_{CH} time(2)
Minimum TCK Cycles before TXRW = 0	t_{28}		6-cycle		TCK	
Delay Finish to TX_{CH} Launch Latency Time(2)	$t_{Latency}$		5-cycle		TCK	
SPI Data Clock Resynchronization Time(2)	t_{Sync}		32-cycle		CLK	
Second Harmonic Distortion	HD2	—	-43	-40	dB	HD2 at 5 MHz, 5-cycle pulse inversion, ±70V, in 100 µs appart, 220 pF/2.5k Load. The t_r, t_f, t_{dr}, t_{df} values, at ±70V, 220 pF //2.5k Load.
Output Rise Time from 0V to V_{PP}	t_r	—	12	14	ns	
Output Fall Time from 0V to V_{NN}	t_f	—	12	14	ns	
Output Rise Time from V_{NN} to V_{PP}	t_{r2}	—	24	26	ns	
Output Fall Time from V_{PP} to V_{NN}	t_{f2}	—	24	26	ns	
Propagation Delay Rise Time 1	t_{dr}	—	20	—	ns	
Propagation Delay Fall Time 1	t_{df}	—	20	—	ns	
Delay Time Matching	Δt_d	—	±1.0	—	ns	P to N, channel to channel matching in IC, at ±70V, 220 pF //2.5k Load(1)

Note 1: Characterized only; not 100% tested in production.

2: Design guidance only.

TABLE 1-12: SPI AND I^2C I/O CHARACTERISTICS

Unless otherwise specified: V_{LL} = +2.5V, AV_{DD} = V_{DD} = +5V, V_{PP} = +80V, V_{NN} = -80V, V_{GN} = -5V, V_{SUB} = 0V, EN = 1, T_A = +25°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
LVDS Differential Input: CLKP/N, SDIP/N, CSP/N and TRIGP/N Pins						
SPI LVDS Clock I/O Frequency	f_{CLK}	30	—	200	MHz	
SPI LVDS Clock Input Duty Cycle[(1)]	D%	45	50	55	%	
AC Differential Sensitivity	V_{SNS}	150	200	—	mV	P-P at 200 MHz[(1)]
AC Common-Mode Voltage[(1)]	V_{CMAC}	1	—	1.4	V	
DC Common-Mode Voltage	V_{REF}	$V_{LL}/2 - 0.2$	$V_{LL}/2$	$V_{LL}/2 + 0.2$	V	
CLK Input Offset Voltage[(1)]	V_{OFFSET}	—	30	—	mV	
LVDS DC Input Differential Voltage	V_{ID}	100	350	600	mV	Same as FPGA I/O
CLK Input Resistance	R_{IN_CLK}	—	5.0	—	kΩ	
CLK Input Capacitance[(2)]	C_{IN_CLK}	—	4.0	—	pF	
CLK Input Bias Current	I_{BIAS_CLK}	—	1.0	—	mA	At input 200 mVp-p
LVDS Differential Output: CKOP/N, SDOP/N and CSOP/N Pins						
LVDS DC Output Differential Voltage	V_{OD}	300	500	—	mV	R_T = 100Ω, termination resistor at the P to N LVDS input pins[(2)]
LVDS DC Output Common-Mode Voltage	V_{OCM}	$V_{LL}/2 - 0.2$	$V_{LL}/2$	$V_{LL}/2 + 0.2$	V	
LVDS Output High Voltage for P&N Pins	V_{OH}	—	1.38	1.6	V	
LVDS Output Low Voltage for P&N Pins	V_{OL}	0.9	1.03	—	V	
Output Current for P&N Pins	I_{O_LVDS}	±3.0	±3.5	±5.0	mA	
Output Rise Time	t_{RO}	—	1.5	—	ns	
Output Fall Time	t_{FO}	—	1.5	—	ns	
CKOP/N Output Clock Duty Cycle	$D\%_{CKO}$	49.5	50	50.5	%	At 200 MHz[(2)]
Output Rise Propagation Delay	t_{DRO}	—	1.5	2.0	ns	CKOP 50% to CKN 50%[(2)]
Output Fall Propagation Delay	t_{DFO}	—	1.5	2.0	ns	
BEN Enable Time	t_{BEN}	—	0.7	1.0	ns	BEN 50% to CLK
CKO, SDO and CSO Logic High	V_{OHO}	1.95	—	—	V	
CKO, SDO and CSO Logic Low	V_{OLO}	—	—	0.35	V	

Note 1: Characterized only; not 100% tested in production.

2: Design guidance only.

3: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

4: The maximum $t_{HD,DAT}$ only has to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

5: A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement of a $t_{SU,DAT}$ of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line, t_{Rmax} + $t_{SU,DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification), before the SCL line is released.

6: The maximum t_F for the SDA and SCL bus lines of 300 ns is longer than the specified maximum t_{of} for the output stages, 250 ns. This allows series protection resistors (Rs) to be connected between the SDA/SCL pins and the SDA/SCL bus lines.

7: I/O pins of Fast mode devices must not obstruct the SDA and SCL lines if V_{LL} is switched off.

TABLE 1-12: SPI AND I²C I/O CHARACTERISTICS (CONTINUED)

Unless otherwise specified: V_{LL} = +2.5V, AV_{DD} = V_{DD} = +5V, V_{PP} = +80V, V_{NN} = -80V, V_{GN} = -5V, V_{SUB} = 0V, EN = 1, T_A = +25°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Fast I²C Interface I/O: SDA and SCL Pins						
Low-Level Input Voltage	V_{IL}	-0.5	—	0.3 * V_{LL}	V	
High-Level Input Voltage	V_{IH}	0.7 * V_{LL}	—	0.5 + V_{LL}	V	
Hysteresis of Schmitt Trigger Inputs[(2)]	V_{hys}	0.05 * V_{LL}	—	—	V	
Pulse Width of Spikes (which must be by the input filter suppressed)[(1)]	t_{SP}	0	—	50	ns	
Low-Level Output Voltage (open-drain or open-collector)	V_{OL6}	0	—	0.6	V	I_{SINK} = 6 mA[(1)]
Output Fall Time from V_{IHmin} to V_{ILmax} with a bus capacitance of 10 pF to 400 pF, I = 6 mA[(1)]	t_{of6}	20	—	250[(6)]	ns	
Input Current	I_i	-10[(7)]	—	10[(7)]	µA	0.4V to 2.8V
I/O Capacitance[(2)]	C_i	—	—	10	pF	
SCL Clock Frequency	f_{SCL}	—	—	400	kHz	
Bus Free Time, Stop to Start	t_{BUF}	1.3	—	—	µs	
Hold Time (Repeated) Start Condition	$t_{HD,STA}$	0.6	—	—	µs	After this period, 1st
Low Period of the SCL Clock	t_{LOW}	1.3	—	—	µs	
High Period of the SCL Clock	t_{HIGH}	0.6	—	—	µs	
Setup Time (Repeated) Start Condition	$t_{SU,SAT}$	0.6	—	—	µs	
Data Hold Time	$t_{HD,DAT}$	0[(3)]	—	0.9[(4)]	µs	Cbus compatible
Setup Time for Stop Condition	$t_{SU,STO}$	0.6	—	—	µs	
Data Setup Time	$t_{SU,DAT}$	100[(5)]	—	—	ns	
Rise Time of SDA or SCL	t_R	20	—	300	ns	
Fall Time of SDA or SCL	t_F	20	—	300	ns	
Capacitive Load for SDA or SCL	C_b	—	—	400	pF	

Note 1: Characterized only; not 100% tested in production.

2: Design guidance only.

3: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

4: The maximum $t_{HD,DAT}$ only has to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

5: A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement of a $t_{SU,DAT}$ of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line, t_{Rmax} + $t_{SU,DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCL line is released.

6: The maximum t_F for the SDA and SCL bus lines of 300 ns is longer than the specified maximum t_{of} for the output stages, 250 ns. This allows series protection resistors (Rs) to be connected between the SDA/SCL pins and the SDA/SCL bus lines.

7: I/O pins of Fast mode devices must not obstruct the SDA and SCL lines if V_{LL} is switched off.

TABLE 1-13: TX_{CH} CLOCK AND PLL AC/DC CHARACTERISTICS

Over operating conditions unless otherwise specified: V_{LL} = +2.5V, AV_{DD} = V_{DD} = +5V, V_{GN} = -5V, V_{PP} = +80V, V_{NN} = -80V, EN = 1, T_A = +25°C						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
V_{PLL} Regulator Output Voltage	V_{CPLL}	4.37	4.50	4.64	V	±3%, T_A = 5° to +75°C
PEN = 1 PLL Current Consumption	I_{VPLL}	—	5.0	8.0	mA	V_{CPLL} = 4.50V(2)
PEN = 0 PLL Current Consumption		—	—	3.0	µA	
Input Clock Frequency in Non-PLL mode	f_{TCK}	30	—	200	MHz	PEN = LCKD = 0(2)
Input Clock Frequency in PLL mode		30	—	80	MHz	PEN = LCKD = 1(2)
Clock Output Duty Cycle(2)	D%	45	50	55	%	
VCO Frequency Range	f_{VCO}	160	240	250	MHz	At pin DNC1(1)
VCO Frequency Range Ratio (fmax/fmin)(2)	r_{fvco}	—	1.56	—	—	
Lock Time	t_{LOCK}	—	300	500	µs	f_{REF} = 80 to 96 MHz jump(1)
Bandwidth of PLL Loop	BW	—	1.0	—	MHz	In design now(2)
f_{VCO} Frequency Divider	N	1	—	8	—	Integer number: 1,2,3,4,5,6, 8(1)
Output f_C Clock Integrated RMS Jitter	t_J	—	15	20	ps	f_{VCO} = 240 MHz, f_{TCK} = 80 MHz(2)
Output f_C Clock Integrated RMS Jitter	t_{JS}	—	15	—	ps	f_{VCO} = 240 MHz, f_{TCK} = 80 MHz w/1%, 10 kHz V_{CPLL} change(2)
Static Phase Error, 500 µs after LCKD = 1	E_{PH}	—	±50	±100	ps	f_{VCO} = 240 MHz, f_{TCK} = 80 MHz(2)
Worst-Case Phase Jump Relock Time	t_{PJ}	—	—	10	µs	f_{VCO} = 240 MHz, f_{TCK} = 80MHz(2)

Note 1: Characterized only; not 100% tested in production.

2: Design guidance only.

TABLE 1-14: TRSW AND RXDMP SWITCHES SWITCHING TIMING AND SPIKE VOLTAGES

Over operating conditions unless otherwise specified: V_{LL} = +2.5V, AV_{DD} = V_{DD} = +5V, V_{GN} = -5V, V_{PP} = +80V, V_{NN} = -80V, EN = 1, T_A = +25°C						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TRSW Switch-On Fixed Propagation Delay	t_{TRSW}	—	200	—	ns	Addition to TRDLY<4:0>[1]
TRSW Switch-On Programmable Delay		8	—	288	$1/f_C$	TRDLY<4:0> value[1]
TRSW Switch-Off Delay Time		—	1.0	1.2	µs	TXRW fall to TRSW off, before TX_{CH} next launch[1]
RTZSW Switch-On Delay Time	t_{RTZSW}	8	—	288	$1/f_C$	TRDLY<4:0> I^2C register value[1]
RTZSW Switch-Off Delay Time		—	105	—	ns	TXRW fall to RTZSW off[1]
RXDMP Damp Switch-On Delay Time	t_{RXDMP}	—	15.2	—	ns	TXRW fall to RXDMP on[1]
RXDMP Damp Switch-Off Delay Time		—	1.1	—	µs	TRSW on to RXDMP off[1]
TX_{CH} Output Frequency Range in B mode	f_{OUT}	—	30	40	MHz	100Ω resistor load[1]
TRSW Turn-On Spike Voltage at TX_{CH} Pins	V_{TRSW_ON}	—	80	110	mVpk	TX_{CH} 50Ω load to GND[1]
TRSW Turn-Off Spike Voltage at TX_{CH} Pins	V_{TRSW_OFF}	-90	-70	—		
RXDMP Turn-On Spike Voltage at RX_{CH} Pins	V_{RXDMP_ON}	—	45	60		RX_{CH} 300 load to GND[1]
RXDMP Turn-Off Spike Voltage at RX_{CH} Pins	V_{RXDMP_OFF}	-70	-60	—		

Note 1: Characterized only; not 100% tested in production.

TABLE 1-15: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_O	0	—	+85	°C	
Storage Temperature Range	T_A	-55	—	+150	°C	
Junction Temperature	T_J	—	+125	—	°C	
Package Thermal Resistances						
Thermal Resistance Junction to Ambient	θ_{JA}	—	+16.5	—	°C/W	JEDEC (2S2P) 4-Lead PCB, 114.3 mm x 76.2 mm x 1.6 mm, T_A = +85°C
Thermal Resistance Junction to PCB	θ_{JB}	—	+4.5	—	°C/W	
Thermal Resistance Junction to Case Top	θ_{JC}	—	+2.3	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: V_{IN} = 12V, AV_{CC} = DV_{CC} = 5V, T_A = +25°C unless otherwise specified.

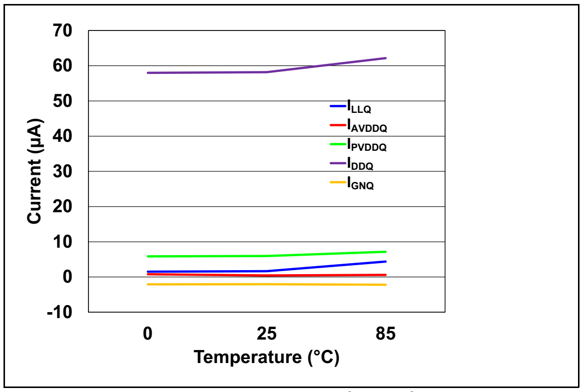


FIGURE 2-1: *LV Supply Quiescent Current vs. Temperature (±70V, 5 MHz, 5 Cycles, PRF 2.5 kHz).*

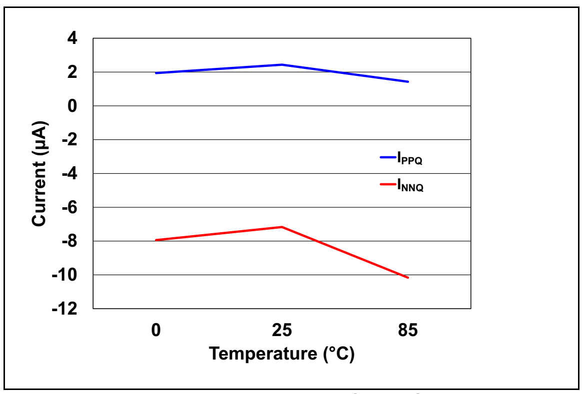


FIGURE 2-2: *HV Supply Quiescent Current vs. Temperature (±70V, 5 MHz, 5 Cycles, PRF 2.5 kHz).*

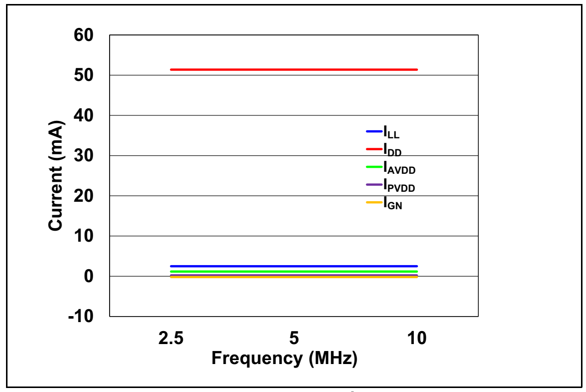


FIGURE 2-3: *LV Supply Current vs. TX Frequency (±70V, 5 Cycles, PRF 2.5 kHz).*

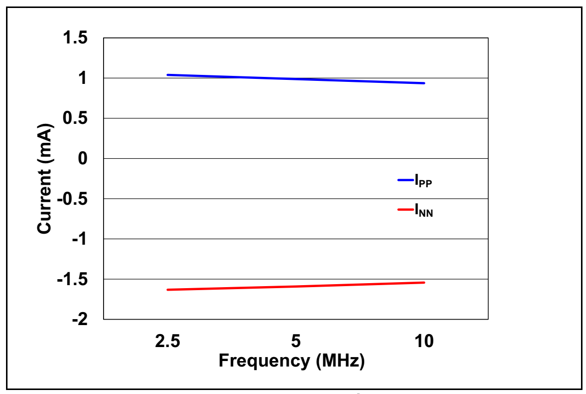


FIGURE 2-4: *HV Supply Current vs. TX Frequency (±70V, 5 Cycles, PRF 2.5 kHz).*

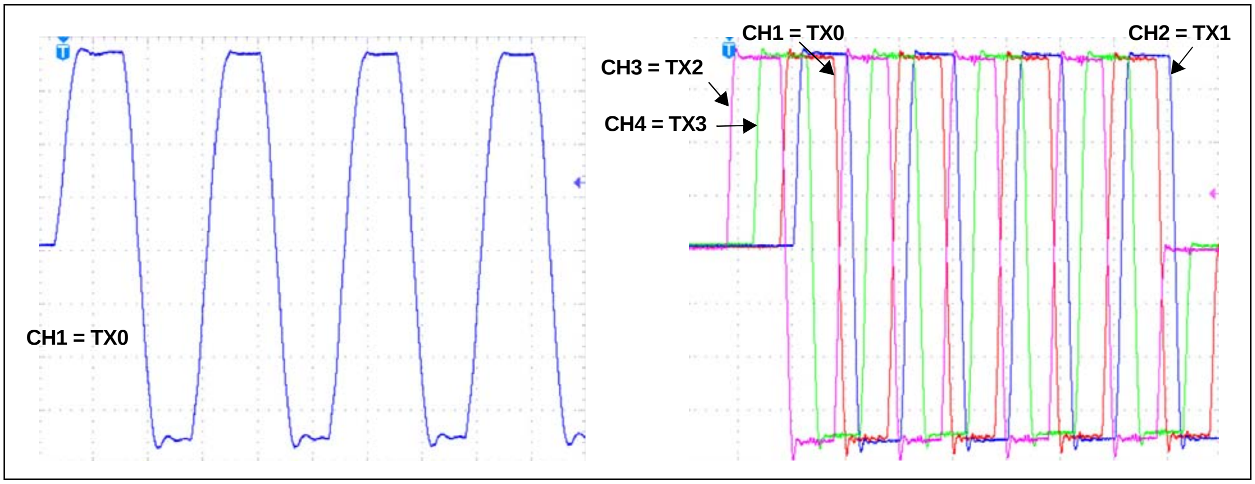


FIGURE 2-5: *Typical Output Waveforms in B Mode Non-RTZ.*

Note:	V_{LL} = +2.5V, AV_{DD} = V_{DD} = PV_{DD} = +5V, V_{GN} = -5V, V_{PP} = +75V, V_{NN} = -75V. Load = 330 pF//2.5 kΩ, 5 MHz and 10 MHz Non-RTZ, BOC[1:0] = `00b`, 200 ns delay between each channel. T_A = +25°C.

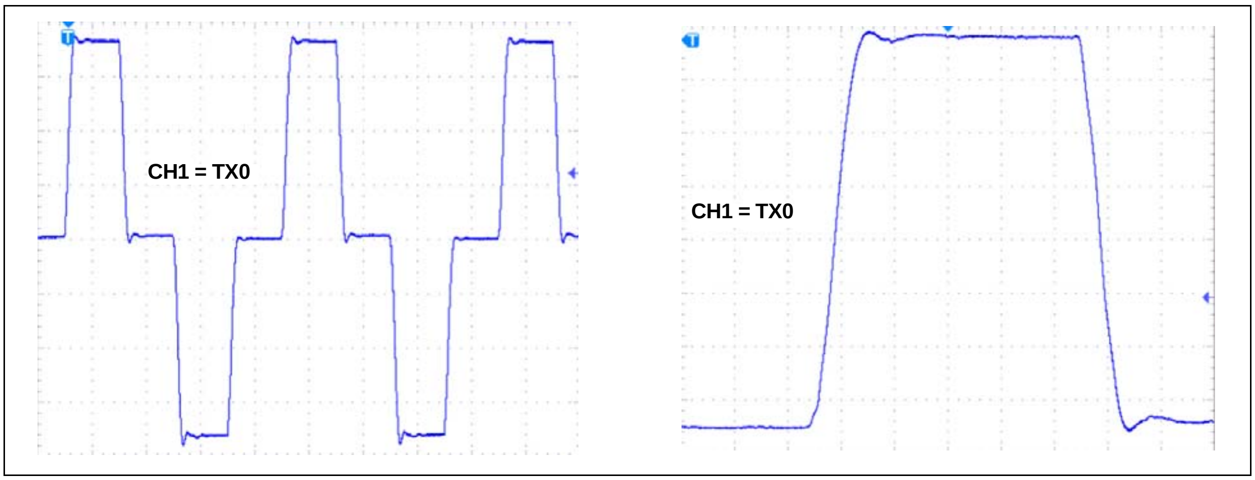


FIGURE 2-6: *Typical Output Waveforms in B Mode RTZ.*

Note:	V_{LL} = +2.5V, AV_{DD} = V_{DD} = PV_{DD} = +5V, V_{GN} = -5V, V_{PP} = +75V, V_{NN} = -75V. Load = 330 pF//2.5 kΩ, 5 MHz RTZ with t_r/t_f measurements, BOC[1:0] = `00b`. T_A = +25°C.

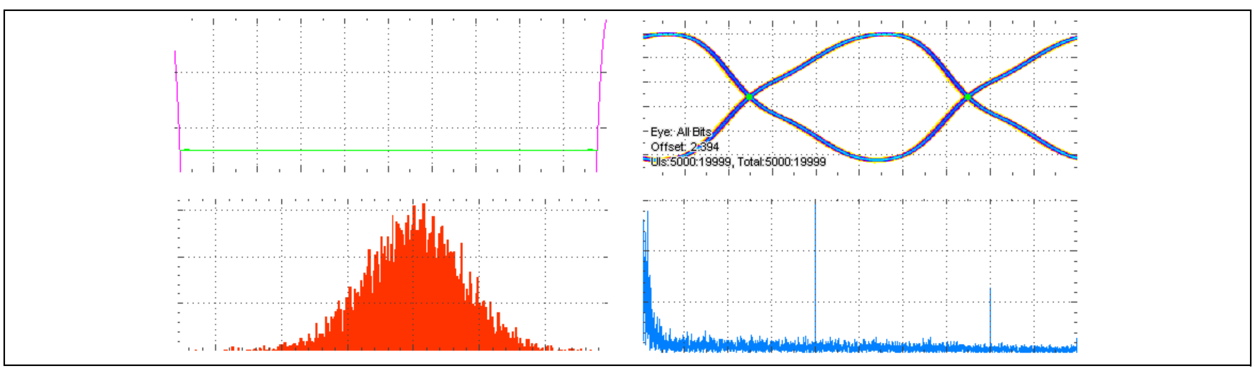


FIGURE 2-7: *Typical B Mode Output Jitter with PLL Enabled.*

Note:	V_{LL} = +2.5V, AV_{DD} = V_{DD} = PV_{DD} = +5V, V_{GN} = -5V, V_{PP} = +15V, V_{NN} = -15V. Load = 330 pF//2.5 kΩ, f_{CLK} = 40 MHz, N = `100b`, f_C = 200 MHz, f_{TX} = 5 MHz, PEN = `1`, BOC[1:0] = `00b`. T_A = +25°C.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION

HV7358	Symbol	Description
C1, H1, L1, P1	V_{LL}	Logic Circuit Power Supply Pin: 0.22 µF ceramic cap to GND per pin.
T4	AV_{DD}	Positive Power Supply Pin for Logic and PLL: +5V, 0.1 µF + 1 µF ceramic caps to GND per pin.
C4, E3, H3, L3, P4, P6	V_{DD}	Positive Voltage Supply Input Pins: +5V, 1 µF ceramic cap to GND per pin.
A7, B7, G8, H8, R7, T7	PV_{DD}	Positive Voltage Supply Input Pins for the RTZ N-Gate Drive: +5V, 1 µF ceramic cap to GND per pin.
A13, B13, D15, H15, M15, R13, T13	V_{PP}	TX_{CH} Positive Power Supply: +3V to +80V, 2 µF ceramic X7R cap to GND per pin.
A15, B15, F15, K15, P15, R15, T15	V_{NN}	TX_{CH} Negative Power Supply: -3V to -80V, 2 µF ceramic X7R cap to GND per pin.
A12, B12, C15, G15, L15, R12, T12	CPF	Internal V_{PF} Gate Drive Voltage Linear Regulator Output Bypass Cap: 2 µF 10V to V_{PP} per pin.
A14, B14, E15, J15, N15, R14, T14	CNF	Internal V_{NF} Gate Drive Voltage Linear Regulator Output Bypass Cap: 2 µF 10V to V_{NN} per pin.
T5	A_{GND}	PLL Circuit Ground and 0V.
C2, C5, F3, H2, J3, L2, M3, P2, P5, P7	GND	Circuit Ground and 0V.
A8, B8, C9, D9, E9, F9, G9, H9, J8, K8, L9, M9, N9, P9, R8, T8	R_{GND}	The TX_{CH} and RX_{CH} Signal Return Grounds (0V): R_{GND} must connect to the GND plane on the PCB.
A5	V_{GN}	-5V Power Supply Input Pins: Must add an X7R 2 µF bypass cap to GND per pin. V_{GN} can be connected to GND when V_{PP} > 10V and V_{NN} < -10V for B mode only.
A9, B9, J9, K9, R9, T9	CNEG	Internal V_{NEG} Gate Drive Voltage Linear Regulator Output Bypass Cap: 2 µF to GND per pin.
T6	C_{PLL}	Internal V_{PLL} Linear Voltage Regulator Output Bypass Cap: 0.1 µF and 2 µF to GND if the built-in PLL functions are used. It can be disabled if EN = 1 and PEN = 0 to save power dissipation.
K3	EN	Device Enable Pin, Active-High: When EN = 0, all the TX_{CH} outputs are high-Z.
N3	BEN	LVDS Output Buffer Enable Pin: BEN = 1 to enable the LVDS output buffers, BEN = 0 to disable when BSEL = 0. The BFEN bit overrides the BEN pin function, BEN pin has no effect on buffer enable if the I^2C bit, BSEL = 1; vice versa if BSEL = 0. The buffer enable is controlled by the BEN pin only.
F2	SLEEP	Chip Sleep Mode Enable Input: If SLEEP = 1, the device is in Power-Saving and Sleep mode, all register data will be preserved and all clocks freeze, except for the I^2C interface. When SLEEP = 0, device wakes up, the I^2C is ready to transmit in about 3 µs.
G3	PEN	PLL Enable Input: PEN = 1 to enable the internal PLL; PEN = 0 to disable the PLL circuit, including locked circuits. The PEN pin function can be overridden by the I^2C register, PENOVR bit = 1. If need be, PEN = 1, must pull the PEN pin high prior to EN = 1.

TABLE 3-1: PIN FUNCTION (CONTINUED)

HV7358	Symbol	Description
N1 N2	TCKP TCKN	LVDS/LVCMOS Differential Inputs for Transmit Clock: Can be driven by LVDS-2.5V or BLVDS-2.5V via DC coupled. The inputs can also be driven by LVDS-1.8V/2.5V via AC coupled. In the differential input cases, a 100Ω LVDS termination resistor must connect to the input pin pair differentially. A single TCKP or TCKN can also be driven by LVCOM-2.5 single-ended output, with biasing the other input to 1.25 VDC, and a bypass capacitor to GND.
A16, B16, C16, D16, E16, F16, G16, H16, J16, K16, L16, M16, N16, P16, R16, T16	TX[15:0]	High-Voltage Pulser B mode and CW Output of the Ch[15:0].
A10, B10, C10, D10, E10, F10, G10, H10, J10, K10, L10, M10, N10, P10, R10, T10	RX[15:0]	T/R Switch Output of the Ch[15:0].
R11	RDCP	V_{PP} Bypass Caps Discharge Resistor Pin: Connect a power resistor from RDCP to GND.
T11	RDCN	V_{NN} Bypass Caps Discharge Resistor Pin: Connect a power resistor from RDCN to GND.
K2	DISC	Fast Discharging Enable Input: DISC = 1, activate V_{PP} and V_{NN} bypass caps discharging.
A1 B1	CLKP CLKN	SPI Clock Inputs: Can be driven by LVDS-2.5V or BLVDS-2.5V via DC coupled. The inputs can also be driven by LVDS-1.8V/2.5V via AC coupled. In the differential input cases, a 100Ω LVDS termination resistor must connect to the input pin pair differentially. A single CLKP or CLKN can also be driven by LVCOM-2.5 single-ended output, with biasing the other input to 1.25 VDC, and a bypass capacitor to GND.
A2 B2	SDIP SDIN	SPI Data Inputs: Can be driven by LVDS-2.5V or BLVDS-2.5V via DC coupled. The inputs can also be driven by LVDS-1.8V/2.5V via AC coupled. In the differential input cases, a 100Ω LVDS termination resistor must connect to the input pin pair differentially. A single SDIP or SDIN can also be driven by LVCOM-2.5 single-ended output, with biasing the other input to 1.25 VDC, and a bypass capacitor to GND.
A3 B3	CSP CSN	SPI Chip Select Inputs: CSN is active-low. The inputs can be driven by LVDS-2.5V or BLVDS-2.5V via DC coupled They can also be driven by LVDS-1.8V/2.5V via AC coupled. In the differential input cases, a 100Ω LVDS termination resistor must connect to the input pin pair differentially. A single CSP or CSN can also be driven by LVCOM-2.5 single-ended output, with biasing the other input to 1.25 VDC, and a bypass capacitor to GND.
R3	CSOP	SPI Chip Select Output, LVDS Positive.
T3	CSON	SPI Chip Select Output, LVDS Negative.
R2	SDOP	SPI Data Output, LVDS Positive.
T2	SDON	SPI Data Output, LVDS Negative.
R1	CKOP	SPI Clock Output, LVDS Positive.
T1	CKON	SPI Clock Output, LVDS Negative.
E2	SPIB	SPI Fast Programming Interface SPIB Pin: SPIB = 1 to enable the SPI Broadcasting mode. SPIB = 0 to enable the Daisy-Chained mode.
A4, B4	W0, W1	Waveform Pattern Select Input: W[1:0] Select one waveform pattern to transmit or write/read.

TABLE 3-1: PIN FUNCTION (CONTINUED)

HV7358	Symbol	Description
M1 M2	TRIGP TRIGN	TX Trigger Inputs: TRIGP is active-high. The inputs can be driven by LVDS-2.5V or BLVDS-2.5V via DC coupled. They can also be driven by LVDS-1.8V/2.5V via AC coupled. In the differential input cases, a 100Ω LVDS termination resistor must connect to the input pin pair differentially. A single TRIGP or TRIGN can also be driven by LVCOM-2.5 single-ended output, with biasing the other input to 1.25 VDC, and a bypass capacitor to GND.
E1	TXRW	If TXRW = 0, the Chip is in SPI or I^2C Read/Write mode; if TXRW = 1, it is in TX_{CH} or RX_{CH} mode: TXRW rise edge will set all the launch counters, and reset the TX_{CH} and RX_{CH} state machine for ready to launch.
J2	CW	CW Enable Logic Input: CW = 1 for CW mode, CW = 0 for B mode.
J1	INV	Pulse Inversion Logic Input Selects the Polarity of the First Transmit Pulse: If INV = 1, the first transmit pulse is a negative pulse. If INV = 0, the first transmit pulse is a positive pulse. INV also selects the state of the transmitter output pins when the device is disabled. When EN = 0 and INV = 1, all the transmitter output pins are high-Z. If EN = 0 and INV = 0, all the transmitter output pins are grounded.
G1	SCL	I^2C Clock Input: Must pull up to 3.3V with a 2.2 kΩ resistor.
G2	SDA	I^2C Data Input: Must pull up to 3.3V with a 2.2 kΩ resistor.
D1, D2, D3	A0, A1, A2	I^2C Device's Address Inputs: For selecting up to eight different I^2C interfaces on the same bus.
K1	SDLY	If SDLY = 0, the SPI Writes to the Registers of DLYch[11:0], TLPch[6:0] and TLNch[6:0]: The SPI performs a 26-bit long word data transfer per channel. When SDLY = 1, the SPI writes the Delay registers, DLYch[11:0] only. The SPI performs a 12-bit word data transfer per channel.
F1	LPWM	SPI Register Block Select Pin: If LPWM = 0, the SPI write or TX_{CH} launch selects the global register block, which consists of four wave pattern parameters of pulse width, global PWM time-off and launch pulse number in a TX_{CH} burst. If LPWM = 1, select the local per channel different PWM Time-Off and Beamforming Delay registers for the SPI write or TX_{CH} launch.
P3	LCKD	PLL Locked Indicator Open-Drain Output: The LOCK output is active-high when the PLL is locked. Alternatively, the PLL locking status can be read from the I^2C Status register. Leave this pin open (NC) when not used.
A6, A11, B6, B11	V_{SUB}	The substrate of the die must be grounded for good RF and DC (0V) point of view.
C3	OTPN	Overtemperature or Undervoltage Flag: This pin is an open-drain output. OTPN = 0 when an overtemperature or undervoltage event happens. The error information will be logged in the I^2C Flag register at ADDR = 01h. The open-drain output of the OTPN pin requires an external pull-up resistor. Leave this pin open (NC) when it is not used.
R5	ETO	End-of-Transmit Open-Drain Output: ETO = 1 when all the TX_{CH} have finished the TX_{CH} launch and are ready for the next launch. The next TRIG rise edge resets ETO = 0. The initial power-on ETO status is high. The open-drain output of the ETO pin requires a pull-up resistor to V_{LL}. Leave this pin open (NC) when it is not used.
R4	ETI	End-of-Transmit Input: Pull ETI = 1 when all the TX_{CH} on board have finished the TX_{CH} launch and are ready for the next trigger. The ETI pin can be directly connected to the ETO pin with a pull-up resistor to V_{LL}. Connect the ETI pin to GND when it is not used.
B5	RSTN	Chip Hard Reset Pin, Active-Low: When V_{LL} and V_{DD} are powered on, EN = 1 and RSTN = 0. All registers will be reset into the default values; all TX_{CH} outputs will be high-Z.
R6, C7, C8, D8, E8, F8, L8, M8, N8, P8, C6	DNC1-11	Do Not Connect: These pins are internally connected for I^2C manufacture use only.

4.0 FUNCTIONAL DESCRIPTION

4.1 Overview

The HV7358 is a 16-channel, 3-level ±80V ultrasound transmitter with built-in T/R switches, gate driver and floating voltage supply regulators, PLL clock multiplier, active bleeder circuit and configuration transmit beamformer. The high integration and rich features of the HV7358 make this device suitable for portable ultrasound systems. The T/R switch and RX_{CH} damp switch are integrated into each channel, while the auto-bleeding switches for true zero voltage reduce received noise to minimum.

The HV7358 also features a built-in gate driver, and floating voltage regulators to allow V_{PP} and V_{NN} high-voltage rails to move the voltage from ±3V to ±80V, both interdependently and freely. The input 2.5V or 3.3V logic control voltages are designed to work with FPGA or LVCMOS logic family devices. It also provides the special CW mode, designed to minimize the jitter and phase noise for CW waveforms output from the reduced current HV MOSFET pairs. You can set the CW beamforming delay per channel, with a range of 0 µs to 3 µs in 12.5 ns increments, when CLK is at 80 MHz with low phase noise.

When the built-in PLL circuit is enabled (PEN = 1), the internal VCO maximum frequency is 250 MHz. It provides low jitter in B mode and PW mode. The TRIG pin provides synchronization alignment for the TX_{CH} launching time of channels and on-board chips.

4.2 Programmable PLL Clock

The HV7358 has an internal PLL circuit for clock frequency, multiplying and dividing operations. The PLL and clock management block has a very low timing jitter. The same pair of TCKP/N clock signals allows phase synchronization across multiple chips.

The TCKP and TCKN pins are the system clock differential inputs. They can take a 30 MHz to 200 MHz frequency as the input reference frequency. The PFD is designed to work at the best low jitter of a selected 30 MHz to 80 MHz frequency range for the best output jitter a process can provide. The PLL loop gain and loop filter bandwidth are also designed to best preserve the input crystal-based system clock low-jitter feature, and filter out most of the power supply ripple and noise of the ultrasound system.

The PLL output frequency divider is programmed through a 3-bit register which is accessible through I^2C.

The VCO of the PLL circuit is designed to generate up to a 250 MHz maximum frequency, with a loop filter BW selected for best rejecting power supply ripple and noise. The user's low-jitter LVDS clock source should be provided via chip LVDS distribution buffer(s) to the CLKP and CLKN inputs, with an external 100Ω termination resistor nearby. The lock-in time of the PLL has a range of 500 µs to 1 ms.

To allow the PLL to lock, set the PEN high first, then set the EN high. If enabling the PLL through I^2C, set the PLLEN bit first, then set the EN high.

4.3 LVDS Connections

Figure 4-1 shows a typical point-to-point LVDS connection. The LVDS driver, on the left, drives the two 50Ω transmission lines into the LVDS receiver on the right. The Q and $\overline{Q}$ outputs of the LVDS driver pass to the corresponding inputs of the LVDS receiver. The two 50Ω single-ended transmission lines can be microstrip, stripline, a 100Ω differential twisted pair or similar balanced differential transmission line. A 100Ω resistor needs to be connected to the LVDS receiver near the input pin pair.

LVDS uses a Current-mode driver, behaving like two equal and opposite current sources with a high output impedance. LVDS outputs typically drive ±3.5 mA to flow through the 100Ω resistor, R_T, generating a ±350 mV voltage swing differentially. The terms, "Common-mode voltage" and "offset voltage", refer to the average of the CKOP/CKON pins; for example, $(V_{CKOP} + V_{CKON})/2$. LVDS has a typical output Common-mode voltage of about 1.25V, determined by the LVDS driver.

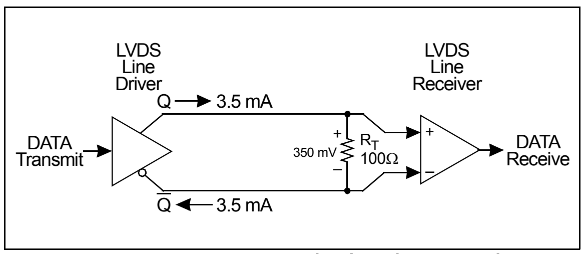


FIGURE 4-1: *A Typical Point-to-Point LVDS Connection.*

The implementation of the 50Ω lines using microstrip techniques on a PC board is recommended.

Due to differences in PCB stack-ups, you must use the 50Ω to GND LVDS trace width and spacing according to the PCB manufacture suggestion. The 100Ω termination resistor, R_T, terminates the CLKP and CLKN pins close to the device. The HV7358 LVDS receiver, as shown on the right in Figure 4-1, adheres to all the standard LVDS DC input levels specified in Table 1-12.

4.4 LVDS SPI Operation

The HV7358 features the fast programming LVDS interface for programming the transmit patterns, the channel delay counters and the local t_{OFF} counters. The fast programming LVDS interface, in all the following cases, can operate up to 200 MHz (see Figure 4-2).

When LPWM = 1, the SPI write and TX_{CH} launching process are switched to the local Beamform registers block, which contains per-channel delay and the local PWM Time-Off registers. The TX_{CH} launch waveform pattern parameters, the pulse width and repeat pulses number are always taken from the Global Waveform Pattern registers, written by the fast SPI operation, when the pin, LPWM = 0. The waveform selection is done by the W0 and W1 pins directly. You can change their selection before TXRW is pulled high. During the waveform patterns, the SPI writing the W0 and W1 pins also serves as a pointer to select one of the four Waveform Pattern registers to write.

When SDLY = 1 and LPWM = 1, only the per-channel delay counters are selected to program. The local PWM time-off counters are bypassed. The fast SPI writing operation will perform a short word (12-bit/word) data transfer. When SDLY = 0 and LPWM = 1, all the channel delay counters and local PWM Time-Off registers are selected to program. The fast SPI writing operation performs a long word (26-bit/word) data transfer. During either long or short data transfers, the chip will be able to perform the SP Broadcasting mode if SPIB = 1. That means the SPI inputs, clock, data and chip select will be copied and buffered out to SPI interface outputs.

The HV7358 also features the built-in fast programming LVDS output buffers to allow a daisy-chain operation when multiple HV7358 devices are used in the system. The retiming of the CSOP/N and SDOP/N signals ensures sufficient setup time for the next device in the chain. The LVDS output buffers eliminate the need for external LVDS buffers/drivers for each HV7358 when multiple devices are used in the system. The pins' layout is optimized for the daisy-chain operation to allow a clean PCB layout. If the built-in LVDS output buffers are not used, they can be disabled to save power by driving BEN = 0 if BSEL = 0. Alternatively, the built-in LVDS output buffers can be enabled or disabled by writing '1' or '0' to the BFEN bit in the I^2C register, if BSEL = 1. The fast programming interface can also operate in two modes: Broadcasting or Daisy-Chain. The Pin mode selects the operating mode. When SPIB = 1, the fast programming interface operates in SPI Broadcasting mode. When SPIB = 0, the fast programming interface operates in Daisy-Chain mode. Alternatively, the operating mode can be selected via the F/D bit in the I^2C register if the override bit, EN_OVR = 1.

All LVDS interface input pin pairs must have external 100Ω termination resistors between the CLKP and CLKN, SDIP and SDIN, CSP and CSN pins.

4.4.1 BROADCASTING vs. DAISY-CHAIN MODE

The fast programming interface can also operate in two modes: Broadcasting mode or Daisy-Chain mode. The pin, SPIB, selects the operating mode. When the SPIB pin is high, the SPI interface operates in Broadcasting mode. When SPIB = 0, it operates in Daisy-Chain mode. Alternatively, the operating mode can be selected via the SPIBC bit in the I^2C register, to control the SPI mode, if the override bit, SPISEL = 1.

In Daisy-Chain mode, the LVDS output SDO is the Shift register output. SDO is the fast SPI Shift register output, which is either the 12-bit Delay register DLY[11:0] or 26-bit DLY[11:0], TLP[6:0] and TLN[6:0], depending on the SDLY selection. Data is clocked out of the Transmit Pattern Shift register onto SDO on the rising edge of the CKOP.

In Broadcasting mode (pin SPIB = 1), the LVDS outputs, CSOP/CSON and SDOP/SDON, are matched in delay with the CKOP/CLON in timing, as shown in Figure 4-16.

The Broadcasting mode should be used when all devices need to be programmed with the same data. In the medical ultrasound application, all the transmit channels have the same transmit patterns. In that scenario, the Broadcasting mode should be used to reduce the programming time. The Daisy-Chain mode should be used when the programming data is different across devices. In most medical ultrasound applications, the transmit delay is different from channel to channel. In that scenario, the Daisy-Chain mode should be used when programming the channel delay counters.

Note that the programming clocks, CLKP/N, are only used for programming the transmit patterns and the channel delay counters. The CLKP/N do not need to be active all the time and they can be turned off after SPI writing.

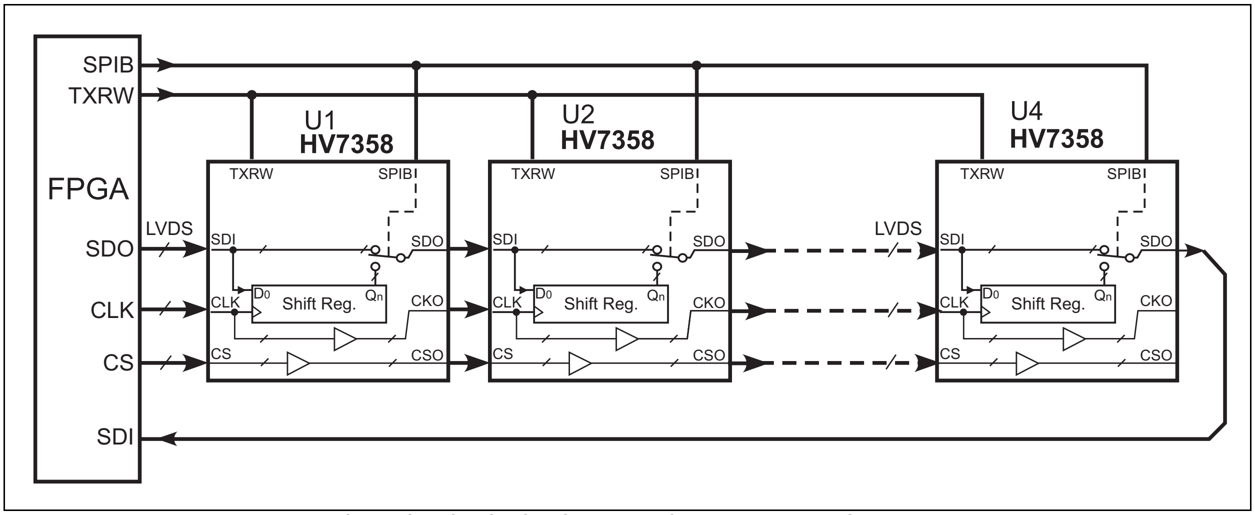


FIGURE 4-2: Connection Circuit Block Diagram of Fast SPI Interface.

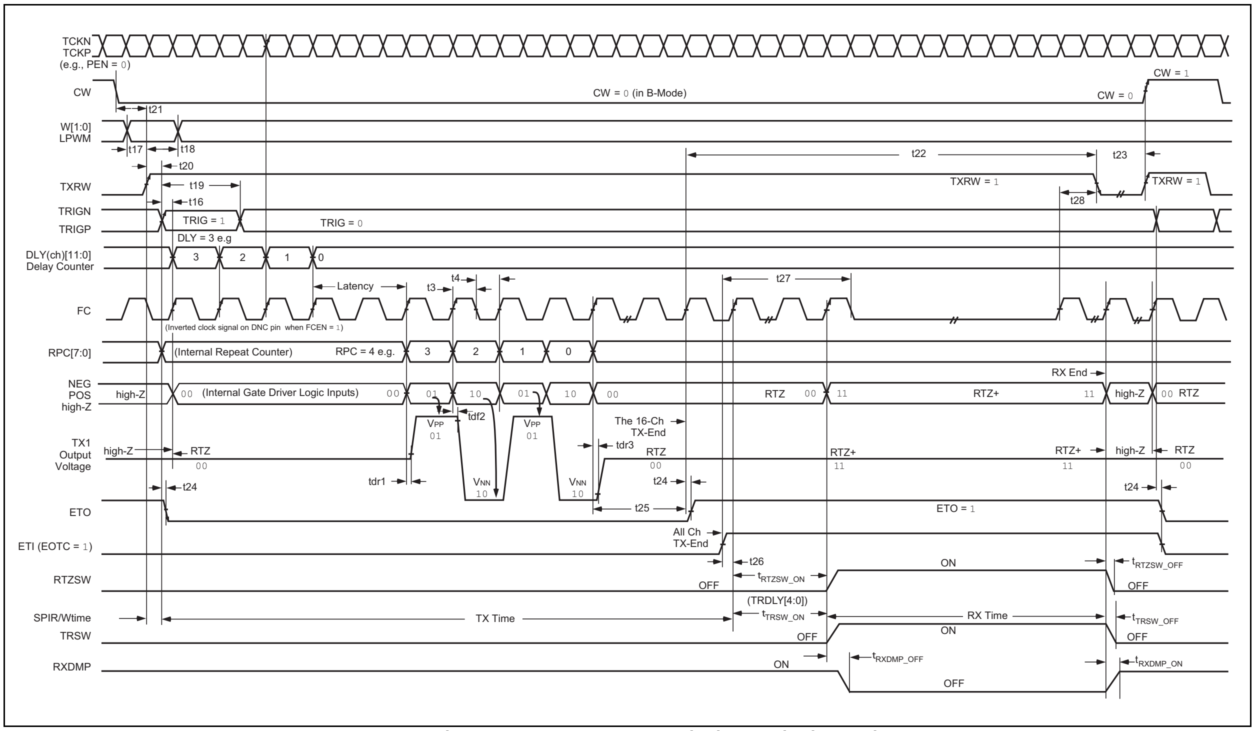


FIGURE 4-3: *TX_{CH} Output and RTZSW, TRSW Switches Timing Diagram.*

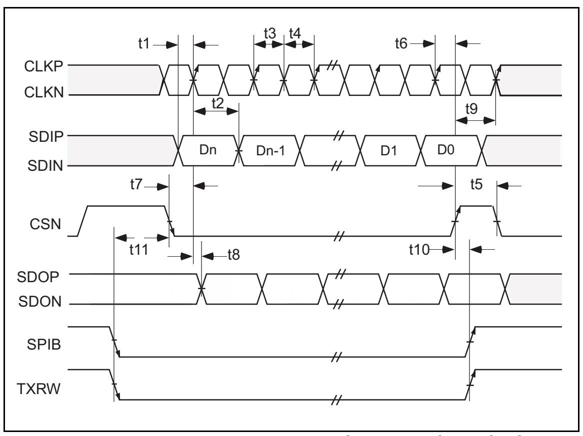


FIGURE 4-4: *SPI Register Write Timing with SPIB = `0`, TXRW = `0`.*

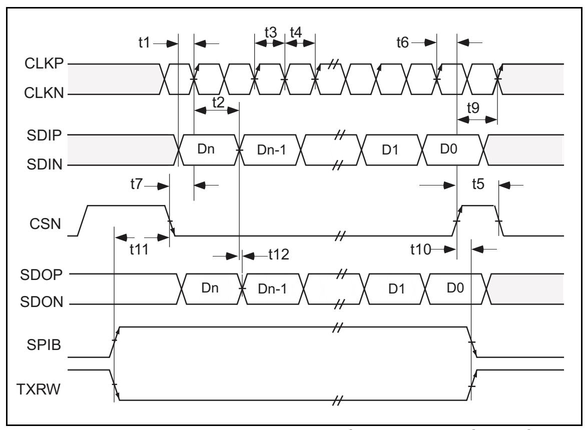


FIGURE 4-5: *SPI Register Broadcasting Write Timing with SPIB = `1`, TXRW = `0`.*

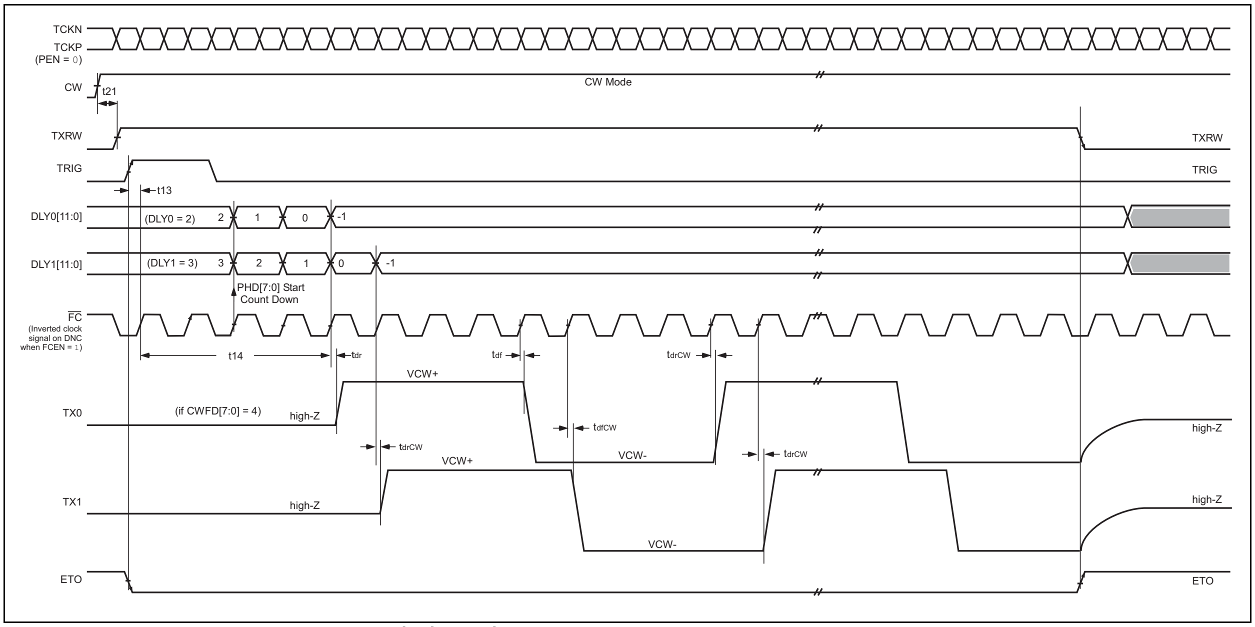


FIGURE 4-6: CW Output Timing Diagram.

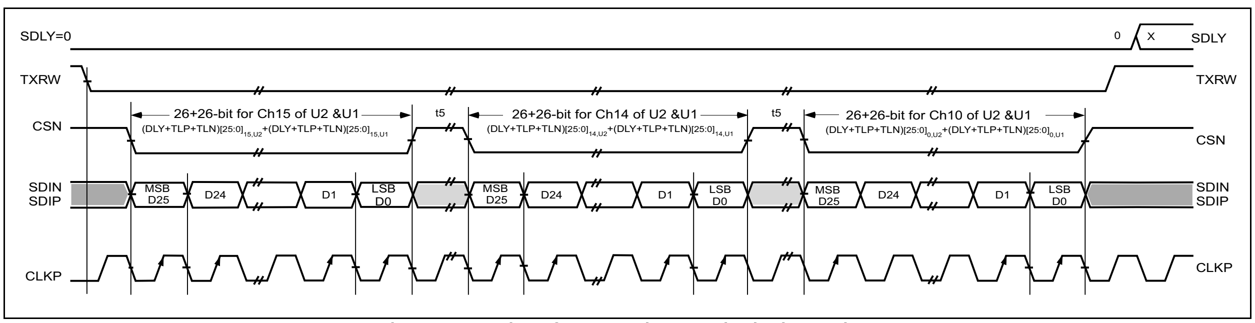


FIGURE 4-7: SPI Fast Write Example of a 26-Bit Word Timing Diagram.

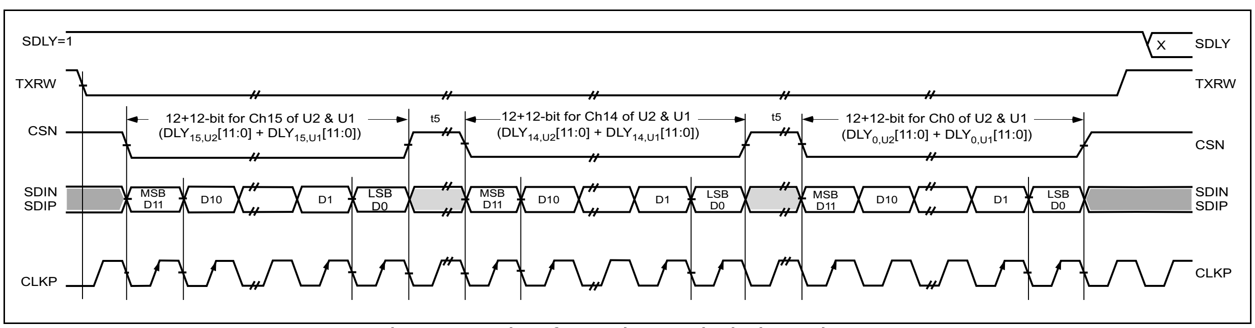


FIGURE 4-8: SPI Fast Write Example of 12-Bit Word Timing Diagram.

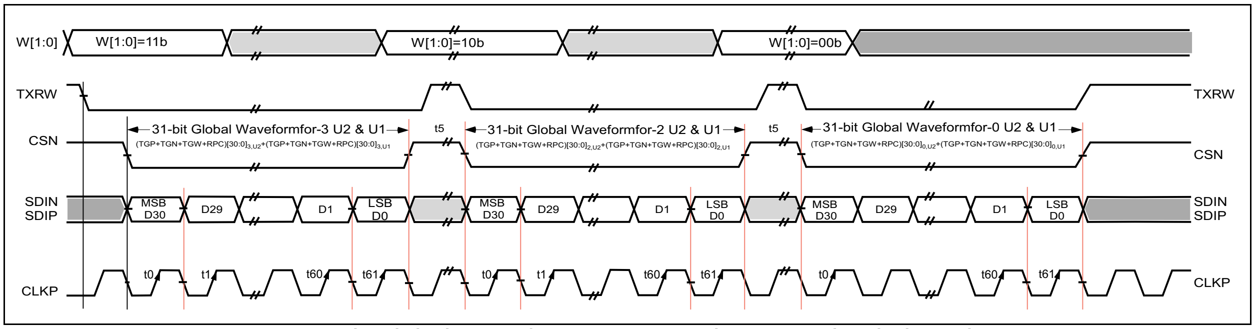


FIGURE 4-9: *SPI 31-Bit Global Waveform Pattern Write Example Timing Diagram.*

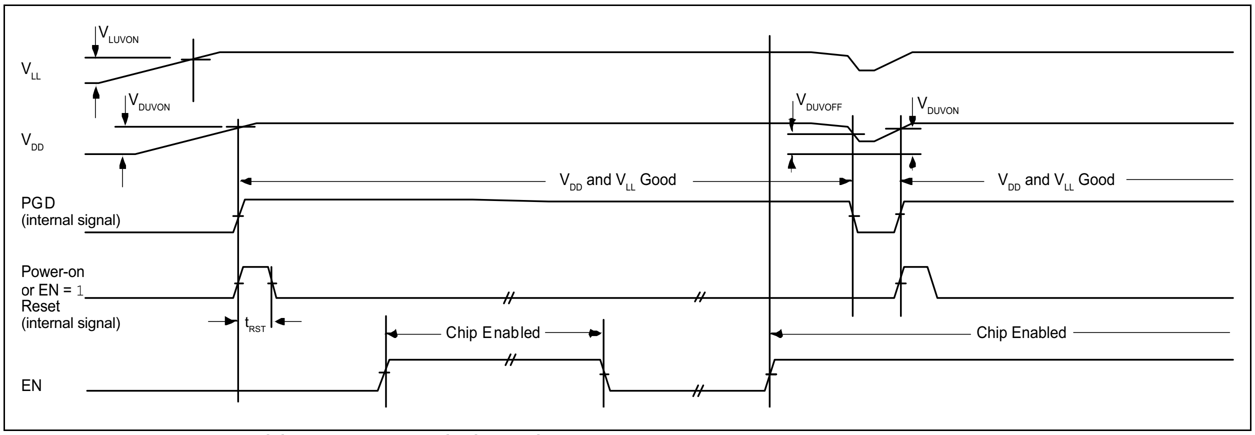


FIGURE 4-10: *Chip Power-up Timing Diagram.*

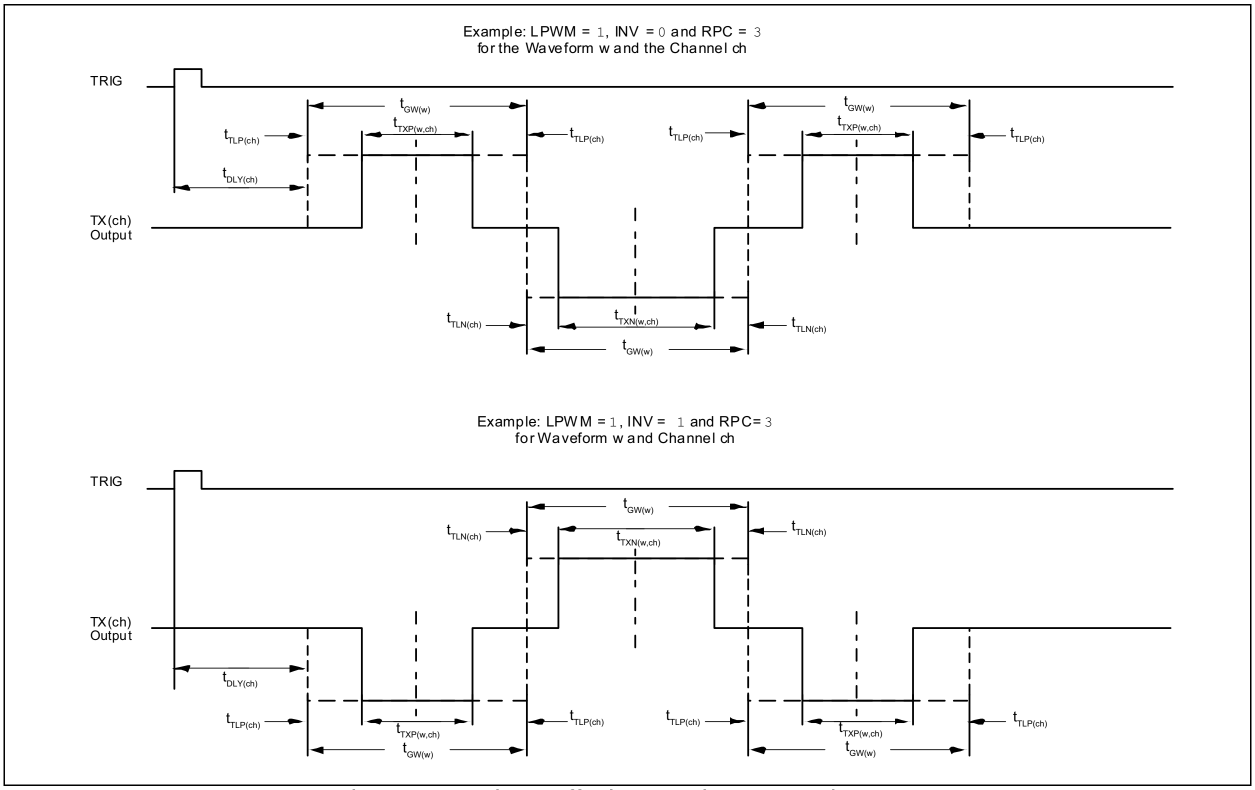


FIGURE 4-11: *TX_{CH} Pulses PWM Time-Off Diagram (LPWM = 1).*

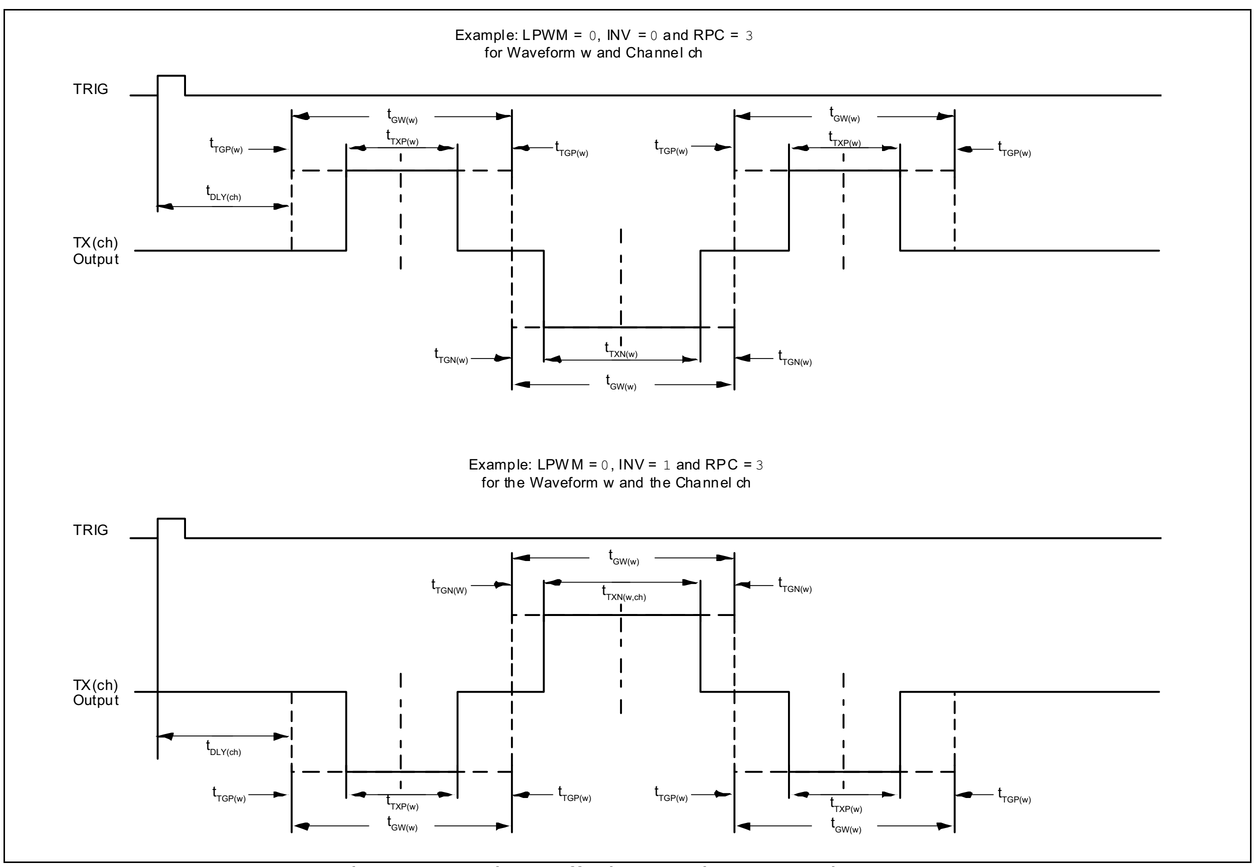


FIGURE 4-12: *TX_{CH} Pulses PWM Time-Off Diagram (LPWM = 0).*

4.5 I²C Interface Operation

1. The master (Processor/FPGA) initiates a Start condition. A Start condition is defined as a change in the state of the SDA line, from high-to-low, while the SCL line is high.
2. The master sends the 7-bit slave address, with the Most Significant bit (MSb) first, followed by the R/$\overline{W}$ bit. The R/$\overline{W}$ bit in this case is low.
3. The master waits for the Acknowledgment from the addressed slave device (HV7358). The Acknowledgment is defined as the addressed slave device when it pulls down the SDA line during the ninth clock of the SCL.
4. After the Acknowledgment is received, the master sends the APR byte with the Register Address Pointer.
5. The master waits for the Acknowledgment.
6. The master initiates a Repeated Start condition.
7. The master sends the 7-bit slave address, with the Most Significant bit first, followed by the R/$\overline{W}$ bit. The R/$\overline{W}$ bit in this case is high for the read operation.
8. The master waits for the Acknowledgment.
9. The addressed slave device sends the byte stored in the register that is addressed by the APR, the Address Pointer.
10. The master sends the Acknowledgment.
11. The master issues the Stop condition.
12. If repeated reads from the same register are desired, repeat Steps 6-11.

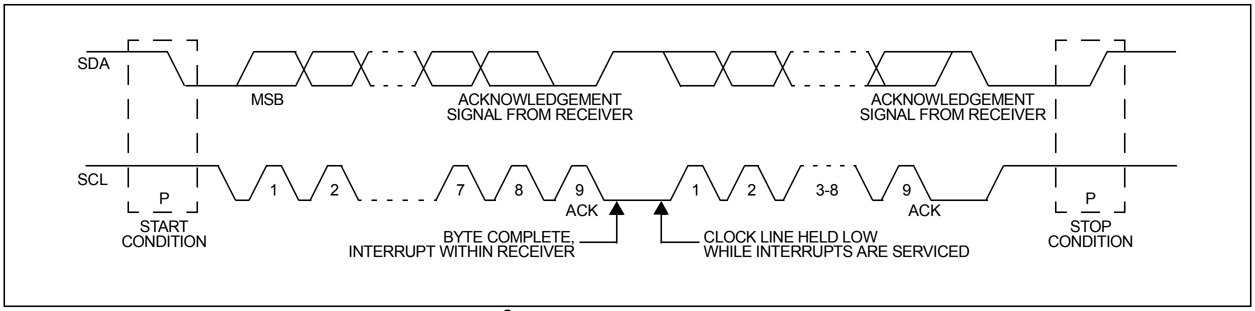


FIGURE 4-13: *Data Transfer on the I²C Bus.*

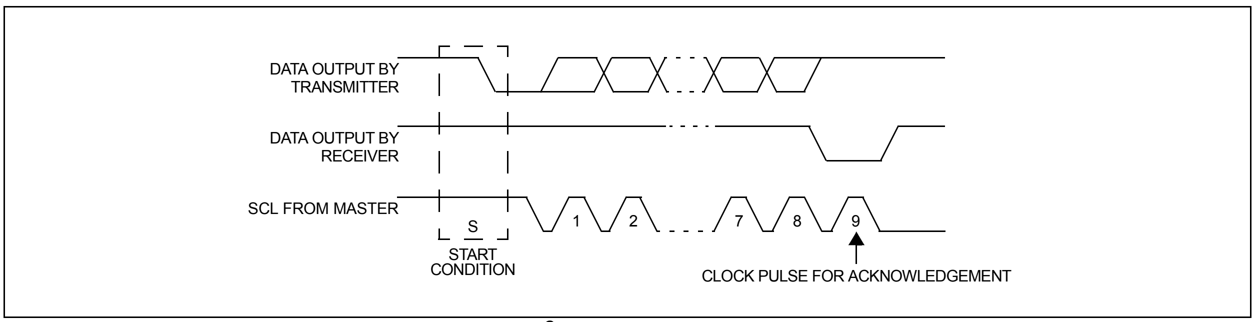


FIGURE 4-14: *Acknowledgment on the I²C Bus.*

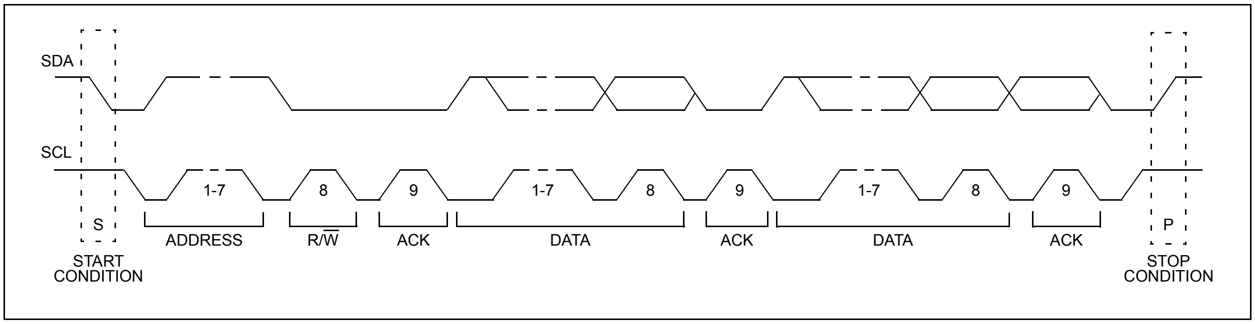


FIGURE 4-15: *Complete Data R/$\overline{W}$ on the I^2C Bus.*

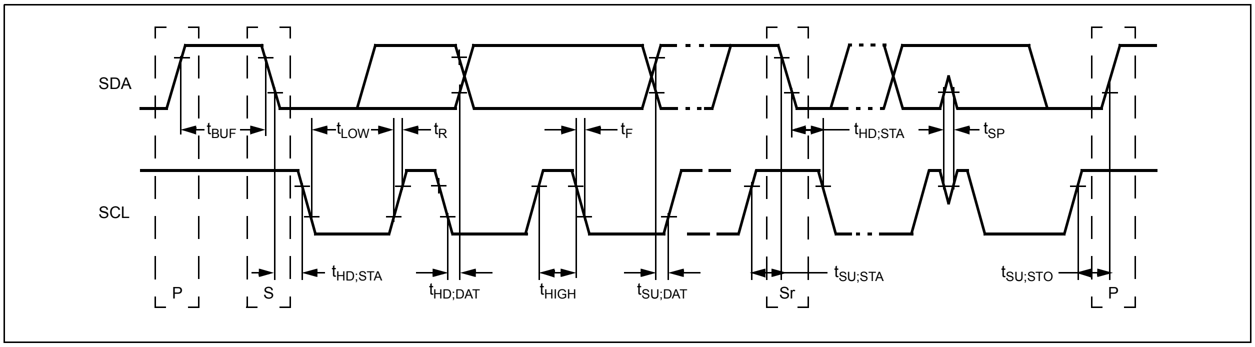


FIGURE 4-16: *I^2C Bus Timing Diagram.*

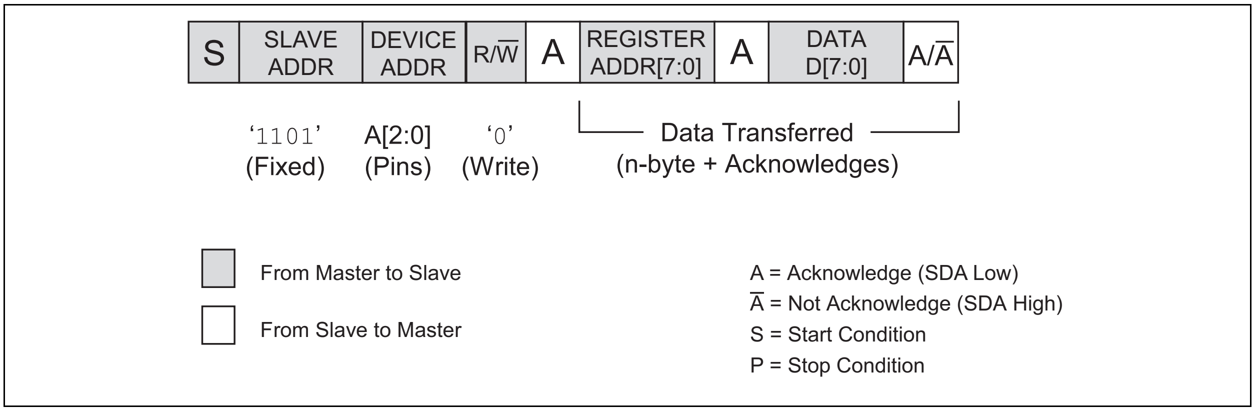


FIGURE 4-17: *I^2C Write Operation Diagram.*

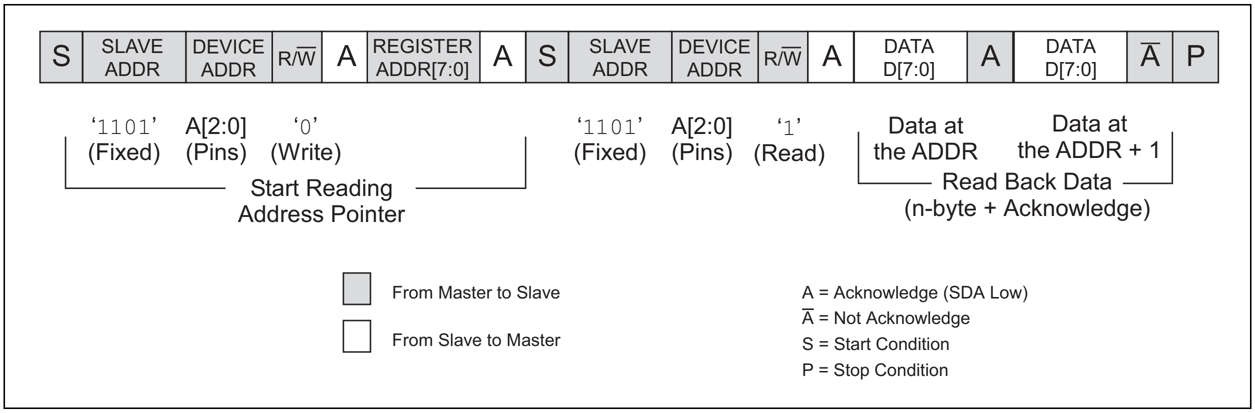


FIGURE 4-18: *I^2C Read Operation Diagram.*

4.6 SPI and I^2C Registers Description

TABLE 4-1: SPI BEAMFORM DATA PARAMETERS

Data	Description
$TGP_{(w)}[6:0]$(1)	Global PWM Time-Off register for the positive pulses if INV = 0. The time-off will be at both sides of the TGW pulse width to reduce the pulse width. The time period is $t_{OFF\_P} = TGP_{(w)}[6:0]/f_C$.
$TGN_{(w)}[6:0]$(1)	Global PWM Time-Off register for the negative pulses if INV = 0. The time-off will be at both sides of the TGW pulse width to reduce the pulse width. The time period is $t_{OFF\_N} = TGN_{(w)}[6:0]/f_C$.
$TGW_{(w)}[8:0]$(1)	Global Pulse-Width 9-Bit register for each waveform pattern.
$RPC_{(w)}[7:0]$(1)	Global Repeating Pulse Counter register for each waveform pattern.
$DLY_{(ch)}[11:0]$(2)	Beamform Delay 12-Bit registers in the local fast SPI register bank. Each channel delay time will be, $t_{DELAY\_7(ch)} = DLY_{(ch)}[11:0]/f_C$, before the next TX_{CH} launch, if 000h < DLY < FFFh after the TRIG is issued. When DLY = 000h, the channel is high-Z (the channel is not used for the next launch). When DLY = FFFh, the channel is directly going to RTZ+ mode as a receive only channel.
$TLP_{(ch)}[6:0]$(2)	Local per Channel PWM Time-Off register for the positive pulses if INV = 0. The time-off will be at both sides of the TGW pulse width to reduce the pulse width per channel. The time period is $t_{OFF\_P} = TLP_{(ch)}[6:0]/f_C$.
$TLN_{(ch)}[6:0]$(2)	Local per Channel PWM Time-Off register for the negative pulses if INV = 0. The time-off will be at both sides of the pulse-width TPW to reduce the pulse width. The time period is $t_{OFF\_N} = TLN_{(ch)}[6:0]/f_C$.

Note 1: "w" denotes the Waveform Pattern Number 0, 1, 2 or 3. It is pointed to by the pin, W[1:0].

2: "ch" denotes the local channel number, from 0 to 15. The local registers are always written or read sequentially, starting from Channel #15.

TABLE 4-2: I^2C CONTROL DATA PARAMETERS[(1)]

Data	Description
BSEL	SPI output buffers enabling the control bit in the I^2C register. If BSEL = 0, all buffers are enabled by the BEN pin; if BSEL = 1, all buffers are enabled by the BFEN bit.
BFEN	The BFEN bit overrides the BEN pin function. The BEN pin has no effect on buffer enable when BSEL = 1. The buffer enable is controlled only by the BFEN bit; vice versa if BSEL = 0.
PLLEN	PLL function enable bit in the I^2C register when PSEL = 1.
PSEL	PLL enable control selecting bit in the I^2C register. If PSEL = 0, it is controlled by the PEN pin; if PSEL = 1, it is controlled by the PLLEN bit in the I^2C register.
SPIBC	SPI Broadcasting mode enable bit in the I^2C register. If SPISEL = 1, the Broadcasting mode is controlled by this bit.
SPISEL	SPI Broadcasting mode control selecting bit in the I^2C register. If SPISEL = 0, it is controlled by the SPIB pin; if SPISEL = 1, it is controlled by the SPIBC bit in the I^2C register.
N[2:0]	PLL frequency multiplier, divider and prescaler for the integer numbers in the I^2C register. If PEN = LCKD = 1, the internal TX_{CH} frequency is $f_C = f_{TCK}$ * (N); here, $f_{TCK} = f_{REF}$ of the PFD. If PEN = LCKD = 0, the internal TX_{CH} frequency is $f_C = f_{TCK}$.
CWFD[7:0]	The CW Frequency Divisor I^2C register. CW frequency is set by: $f_{CW} = f_C/2$ * CWFD. When CWFD = 0, the TX_{CH} output is in high-Z. The CWFD initial default value is '0'. The CWFD values will be loaded into the channel's CWFD counter prior to a TXRW rise edge when the CW pin is high. The per channel CWFD counters start counting down after the beamform delay.
CWOC	I^2C control bits for the CW output R_{ON} selection. If CWOC = 0, R_{ONCW} = 30Ω; if CWOC = 1, R_{ONCW} = 45Ω. This bit is for all channels.
BOC[1:0]	I^2C control bits for the B mode output peak current. BOC = 00b, BOC = 01b for ±0.9A, BOC = 10b for ±600 mA and BOC = 11b for ±300 mA. These bits are for all channels.
OTP	Overtemperature flag bit. If OTP = 1, the chip is overtemperature; if OTP = 0, the temperature is in the specified working range. The flag will be reset after the read of the ADDR = 01h register. If the overtemperature event continues, the OTPN = 0 will be retriggered at the next EN rise edge. You must perform a read operation to clear the register after the initial power-on, OTPN = 1 and EN = 1.
V(x)UV	Undervoltage flag bit. When the one voltage rail is undervoltage, V(x)UV = 1, the flag bit(s) will be cleared by the I^2C reading of the ADDR = 01h register. If any undervoltage continues, the OTPN = 0 will be retrigged at the next EN rise edge. You must perform a read operation to clear the register after the initial power-on, OTPN = 1 and EN = 1.
TRDLY[4:0]	TRSW On-Time Delay Selection Control register. TRDLY = (8 to 288)/f_C.
RESET	If RESET = 1, reset all SPI and I^2C registers. The RESET will be zero after the Reset is done. This bit functions the same as the RSTN hardware Reset pin.
EOTC	If EOTC = 0, the RTZ+ and TRSW delay period starts immediately after all channels are finished. If EOTC = 1, the period starts at the first f_C clock rise edge after ETI becomes high and after all channels finish the TX_{CH} period.
EOT	Read-only bit for the End-of-TX_{CH} flag for all 16 channels in the chip. If EOT = 0, the TX_{CH} period is not finished. When EOT = 1, all 16 channels in this IC TX_{CH} period are finished.
LOCKD	Read-only bit for the PLL locked flag. If LOCKD = 0, the PLL is not locked; if LOCKD = 1, the PLL is locked.
URSV[1:0]	Reserved for D% control bits.

Note 1: For all register bits, the Power-on Reset is **Default Zero.**

TABLE 4-3: B MODE GLOBAL TX_{CH} PULSE-WIDTH TGW(w)[8:0], R/$\overline{W}$ VIA I^2C/SPI

W[1:0] Pins		SPI Data Write TGW(w)[8:0]									I^2C Read-Back Address of TGW(w)[8:0][2]
		D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	TX_{CH} Pulse-Width GPW0[8:0] for Wave #0									TX_{CH} Pulse Width (Half Cycle Time) for Waveform #0[1]
0	1	TX_{CH} Pulse-Width GPW1[8:0] for Wave #1									TX_{CH} Pulse Width (Half Cycle Time) for Waveform #1[1]
1	0	TX_{CH} Pulse-Width GPW2[8:0] for Wave #2									TX_{CH} Pulse Width (Half Cycle Time) for Waveform #2[1]
1	1	TX_{CH} Pulse-Width GPW3[8:0] for Wave #3									TX_{CH} Pulse Width (Half Cycle Time) for Waveform #3[1]

Note 1: The half-cycle period TX_{CH} pulse width, t_{Pulse_Width} = TGW(w)[8:0]/f_C, where 2 ≤ TGW(w) ≤ 511. When TGW(w) = 0 or 1, the channel TX_{CH} output will be RTZ, where the "w" denotes the Global Waveform Patterns #0~3.

2: The 9-bit data read-back from two I^2C addresses.

TABLE 4-4: TRSW ON-TIME DELAY TRDLY[4:0], R/$\overline{W}$ VIA I^2C

TRDLY[4:0][1]					k Value (Dec)	TRSW Switch-On Delay After ETI = 1: t_{TRSW_ON} = k/f_C (in ns)			
D4	D3	D2	D1	D0		f_C = 80 MHz	f_C = 120 MHz	f_C = 160 MHz	f_C = 200 MHz
0	0	0	0	0	1	12.5	8.4	6.3	5.0
0	0	0	0	1	8	100	67	50	40
0	0	0	1	0	12	150	100	75	60
0	0	0	1	1	16	200	133	100	80
0	0	1	0	0	20	250	166	125	100
0	0	1	0	1	24	300	200	150	120
0	0	1	1	0	36	450	300	225	180
0	0	1	1	1	40	500	333	250	200
0	1	0	0	0	48	600	400	300	240
0	1	0	0	1	60	750	500	375	300
0	1	0	1	0	64	800	533	400	320
0	1	0	1	1	72	900	600	450	360
0	1	1	0	0	80	1000	667	500	400
0	1	1	0	1	96	1200	800	600	480
0	1	1	1	0	100	1250	833	625	500
0	1	1	1	1	120	1500	1000	750	600
1	0	0	0	0	128	1600	1067	800	640
1	0	0	0	1	144	1800	1200	900	720
1	0	0	1	0	160	2000	1333	1000	800
1	0	0	1	1	192	2400	1600	1200	960
1	0	1	0	0	200	2500	1667	1250	1000
1	0	1	0	1	240	3000	2000	1500	1200
1	0	1	1	0	288	3600	2400	1800	1440

Note 1: When TRDLY[4:0] > 10110b, the TRSW switch-on delay is the same as k = 288.

TABLE 4-5: B MODE GLOBAL TX_{CH} PWM TIME-OFF, R/$\overline{W}$ VIA I^2C/SPI

W[1:0] Pin		TGP(w)[6:0][3,4]			Description
		D6	D5...D1	D0	
Tx_{CH} P-FETs Time-Off at INV = 0 or N-FETs Time-Off at INV = 1[2]					
0	0	TGP0[6:0]			Global TX_{CH} PWM Time-Off for P Side of Waveform #0
0	1	TGP1[6:0]			Global TX_{CH} PWM Time-Off for P Side of Waveform #1
1	0	TGP2[6:0]			Global TX_{CH} PWM Time-Off for P Side of Waveform #2
1	1	TGP3[6:0]			Global TX_{CH} PWM Time-Off for P Side of Waveform #3
W[1:0] pin		**TGN(w)[6:0][3,4]**			**Description**
		D6	**D5...D1**	**D0**	
Tx_{CH} N-FETs Time-Off at INV = 0 or P-FETs Time-Off at INV = 0[1]					
0	0	TGN0[6:0]			Global TX_{CH} PWM Time-Off for N Side of Waveform #0
0	1	TGN1[6:0]			Global TX_{CH} PWM Time-Off for N Side of Waveform #1
1	0	TGN2[6:0]			Global TX_{CH} PWM Time-Off for N Side of Waveform #2
1	1	TGN3[6:0]			Global TX_{CH} PWM Time-Off for N Side of Waveform #3

Note 1: PWM time-off, t_{OFF_P} = TGP(w)[6:0]/f_C.

2: PWM time-off, t_{OFF_N} = TGN(w)[6:0]/f_C.

3: TGP(w) + TGN(w) ≠ 1; otherwise, the channel TX_{CH} output will be RTZ.

4: If TGP(w) + TGN(w) ≥ 2, then TGW – 2 * TGN(w) ≥ 2 and TGW – 2 * TGP(w) ≥ 2. If TGP(w) = TGN9(w) = 0, then TGW ≥ 2; otherwise, the TX_{CH} output will be RTZ.

TABLE 4-6: TX_{CH} PULSER AND RX_{CH} SWITCH OUTPUT STATUS AT POWERED ON

Control Pins				Logic to Gate Drive		CW Mode	TX0~15 Outputs and RX_{CH} Switches Status				
EN	TXRW	CW	INV	POS	NEG	CW Logic	ETO/ ETI(5)	TX0~15 Output	RTZSW/ TRSW	RXDMP	Notes
1	1	0	0	0	0	Disable	0	RTZ	Off	On	TX_{CH} B mode noninverting(1)
1	1	0	0	1	0	Disable	0	V_{PP}	Off	On	
1	1	0	0	0	1	Disable	0	V_{NN}	Off	On	
1	1	0	0	1	1	Disable	1	RTZ+(3)	On	Off	RX_{CH} mode
1	1	0	1	0	0	Disable	0	RTZ	Off	On	TX_{CH} B mode inverting(1)
1	1	0	1	0	1	Disable	0	V_{NN}(6)	Off	On	
1	1	0	1	1	0	Disable	0	V_{PP}(6)	Off	On	
1	1	0	1	1	1	Disable	1	RTZ+(3)	On	Off	RX_{CH} mode(3)
1	1	1	0	0	0	Enable	0	high-Z(4)	Off	On	CW mode noninverting(2)
1	1	1	0	1	0	Enable	0	VCW+	Off	On	
1	1	1	0	0	1	Enable	0	VCW-	Off	On	
1	1	1	0	1	1	Enable	0	RTZ+(3)	ON	Off	
1	1	1	1	0	0	Enable	0	high-Z(4)	Off	On	CW mode inverting(2)
1	1	1	1	0	1	Enable	0	VCW-	Off	On	
1	1	1	1	1	0	Enable	0	VCW+	Off	On	
1	1	1	1	1	1	Enable	0	RTZ+(3)	ON	Off	
1	0	x	x	0	0	Disable	0	high-Z(4)	Off	On	SPI/I^2C RW
0	x	x	x	x	x	Disable	0	high-Z(4)	Off	ON	IC disabled

Note 1: In B mode, you must use a low duty cycle (D% ≤ 10%) due to the IC power dissipation limit.

2: In CW mode (D% = 100%), the V_{PP}/V_{NN} output voltage must be reduced due to the IC power dissipation limit.

3: When the TX_{CH} output is in RTZ+ state, the channel is in Receiving mode (RTZ+).

4: When the TX_{CH} output is in high-Z state, all output MOFETs are off.

5: When ETI = 1 (TRSW), all channels are in Receiving mode after the delay.

6: When INV = 1, Tx0~15 are inverting the output waveforms.

TABLE 4-7: CHIP ENABLE, SLEEP AND OTP STATUS

EN	OTP, VLLUV, VDDUV	SLEEP	PEN	BEN	I^2C	SPI	PLL	V_{PLL}	V_{NEG}, V_{PF}, V_{NF}, LRs	SDO, CSO, CKO	TX_{CH} Output
1	0	0	x	1	On	On	X	On	On	Enable	Normal (V_{PP}, V_{NN}, RTZ, high-Z, RTZ+ or CW)
1	0	0	1	1	On	On	On	On	On	Enable	
1	0	0	0	1	On	On	Off	On	On	Enable	
1	0	0	x	0	On	On	X	On	On	Disable	
1	0	1	x	x	On	Off	Off	Off	On	X	high-Z
1	1	x	x	x	On	Off	Off	Off	Off	Disable	high-Z
0	x	x	x	x	On	Off	Off	Off	Off	Disable	high-Z

TABLE 4-8: I²C CONTROL PARAMETERS ADDRESS

I²C ADDR (Hex)	I²C Control Register Data for Write or Read							
	D7	D6	D5	D4	D3	D2	D1	D0
00h	0	0	0	0	0	0	EOT	LOCKD
01h	0	VNFUV	VPFUV	VPLLUV	VNEGUV	VDDUV	VLLUV	OTP
02h	—	EOTC	BSEL	BFEN	SPISEL	SPIBC	PSEL	PLLEN
03h	URSV1	URSV0	BOC[1:0]		CWOC	N[2:0]		
04h	CWFD[7:0]							
05h	—	—	—	TRDLY[4:0]				
06h	RESET	—	—	—	—	—	—	—
10h	TGW0[7:0] Read-Back for Waveform Pattern #0							
11h	TGW1[7:0] Read-Back for Waveform Pattern #1							
12h	TGW2[7:0] Read-Back for Waveform Pattern #2							
13h	TGW3[7:0] Read-Back for Waveform Pattern #3							
14h	TGW0[8]	TGP0[6:0] Read-Back for Waveform Pattern #0						
15h	TGW1[8]	TGP1[6:0] Read-Back for Waveform Pattern #1						
16h	TGW2[8]	TGP2[6:0] Read-Back for Waveform Pattern #2						
17h	TGW3[8]	TGP3[6:0] Read-Back for Waveform Pattern #3						
18h	0	TGN0[6:0] Read-Back for Waveform Pattern #0						
19h	0	TGN1[6:0] Read-Back for Waveform Pattern #1						
1Ah	0	TGN2[6:0] Read-Back for Waveform Pattern #2						
1Bh	0	TGN3[6:0] Read-Back for Waveform Pattern #3						
1Ch	RPC0[7:0] Read-Back for Waveform Pattern #0							
1Dh	RPC1[7:0] Read-Back for Waveform Pattern #1							
1Eh	RPC2[7:0] Read-Back for Waveform Pattern #2							
1Fh	RPC3[7:0] Read-Back for Waveform Pattern #3							
20h	0	0	0	0	DLY0[11:8] Read-Back for Ch #0 High Nibble			
21h	DLY0[7:0] Read-Back for Ch #0 Lo Byte							
22h	0	0	0	0	DLY1[11:8] Read-Back for Ch #1 High Nibble			
23h	DLY1[7:0] Read-Back for Ch #1 Low Byte							
......	......	......	......	......	......			
......	......							
3Eh	0	0	0	0	DLY15[11:8] Read-Back Ch #15 High Nibble			
3Fh	DLY15[7:0] Read-Back Ch #15 Low Byte							
40h	0	TLP0[6:0] for Ch #0						
41h	0	TLP1[6:0] for Ch #1						
......	0	......						
4Fh	0	TLP15[6:0] for Ch #15						
50h	0	TLN0[6:0] for Ch #0						
51h	0	TLN1[6:0] for Ch #1						
......	0	......						
5Fh	0	TLN15[6:0] for Ch #15						

TABLE 4-9: BEAMFORM PER CHANNEL DELAY TIME, R/$\overline{W}$ VIA I^2C/SPI

DLY(ch)[11:0](1)			Delay Time per Channel B Mode and CW Mode	Description
D11	D10...D1	D0		
0000, 0000, 0000			The channel(ch) is in high-Z	Channel off TX_{CH} high-Z
0000, 0000, 0001			$t_{DLY(ch)} = 1/f_C$	The per channel (ch) B-pulses/CW waveform (w) launch after the delay time, $t_{DLY(ch)}$
....			....	
1111, 1111, 1110			$t_{DLY(ch)} = 4094/f_C$	
1111, 1111, 1111			The channel is in RX_{CH} only	No TRIG TRSW and RTZSW on in RX_{CH} mode only

Note 1: The 12-bit data of DLY (ch) read back from two I^2C ADDRs.

TABLE 4-10: TX_{CH} OUTPUT PEAK CURRENT SELECTION R/$\overline{W}$ VIA I^2C

BOC[1:0]		TX_{CH} Output Peak Current	Description
D1	D0		
0	0	±1.6A	1.6A and 1.0A are for B mode only. For CW mode, you must select the 0.5A or 0.3A dependent CW lasting time due to the package power dissipation limit.
0	1	±1.0A	
1	0	±0.5A	
1	1	±0.3A	

TABLE 4-11: SPI DATA SELECT PIN LPWM FUNCTION

LPWM(1)	SPI Write to the Registers of TXRW = 0(2)	TX_{CH} B Mode Use (TXRW = 1)
0	Global TGP_w[6:0], TGN_w[6:0],TGW_w[8:0] and RPC_w[7:0] (31-bit/word)	Global registers parameters
1	Local DLY_{ch}[11:0], TLP_{ch}[6:0] and TLN_{ch}[6:0] (26-bit/word) when SDLY = 0; or DLY_{ch}[11:0] (12-bit/word) only when SDLY = 1	Local registers parameters

Note 1: Write one word per $\overline{CS}$ operation. When LPWM = 1, the Writing Channel Pointer starts at ch = 15, advanced automatically per $\overline{CS}$ rise. The pointer will be reset at the falling edge of TXRW.

2: All register data writing must be MSB first.

TABLE 4-12: SPI WORD LENGTH CONTROL PIN SDLY FUNCTION

SDLY(1)	SPI Write to the Registers of TXRW = 0(2)	Word Length
0	All-Fast-Reg: DLY_{ch}[11:0], TLP_{ch}[6:0] and TLN_{ch}[6:0] (26-bit/word)	26-bit (long word)
1	Select the Beamform Delay registers only: DLY_{ch}[11:0] (12-bit/word)	12-bit (short word)

Note 1: Write one word per $\overline{CS}$ operation. When LPWM = 1, the Writing Channel Pointer starts at ch = 15, advanced automatically per $\overline{CS}$ rise. The pointer will be reset at the falling edge of TXRW.

2: All register data writing must be MSB first.

TABLE 4-13: B MODE PWM TIME-OFF PER CHANNEL R/$\overline{W}$ VIA I^2C

TLP(ch)[6:0][3,4]			PWM Time-Off for P (per channel)	Description
D6	D5...D1	D0		
TX_{CH} P-FETs Time-Off at INV = 0 or N-FETs Time-Off at INV = 1[1]				
0000000			$t_{OFF\_P} = 0/f_C$	The per channel (ch) B-pulses PWM off-time on both sides of the P-pulse if INV = 0
0000001			$t_{OFF\_P} = 1/f_C$	
......			......	
1111110			$t_{OFF\_P} = 126/f_C$	
1111111			$t_{OFF\_P} = 127/f_C$	
TLN(ch)[6:0][3,4]			**PWM Time-Off for N (per channel)**	**Description**
D6	**D5...D1**	**D0**		
TX_{CH} N-FETs Time-Off at INV = 0 or P-FETs Time-Off at INV = 1[2]				
0000000			$t_{OFF\_N} = 0/f_C$	The per channel (ch) B-pulses PWM off-time on both sides of the N-pulse if INV = 0
0000001			$t_{OFF\_N} = 1/f_C$	
......			......	
1111110			$t_{OFF\_N} = 126/f_C$	
1111111			$t_{OFF\_N} = 127/f_C$	

Note 1: The same time-off on both sides of the P-pulse.
2: The same time-off on both sides of the N-pulse.
3: TLP(w) + TLN(w) ≠ 1; otherwise, the TX_{CH} output will be RTZ.
4: If TLP(w) + TLN(w) ≥ 2, then TGW – 2 * TLN(w) ≥ 2 and TGW – 2 * TLP(w) ≥ 2. If TLP(w) = TLN9(w) = 0, then TGW ≥ 2; otherwise, the TX_{CH} output will be RTZ.

TABLE 4-14: CW FREQUENCY DIVIDER NUMBER R/$\overline{W}$ VIA I^2C[1]

CWFD[7:0]			CW Transmit Clock Frequency f_{CW}	Description
D7	D6 ... D1	D0		
0000, 0000b			All TX0 to 15 in high-Z (default)	The per channel (ch) CW frequency divide down counter if CW = 1
0000, 0001b			$f_{CW} = f_{TCK}/2 \times 1$	
0000, 0010b			$f_{CW} = f_{TCK}/2 \times 2$	
0000, 0011b			$f_{CW} = f_{TCK}/2 \times 3$	
0000, 0100b			$f_{CW} = f_{TCK}/2 \times 4$	
......			......	
1111, 1111b			$f_{CW} = f_{TCK}/2 \times 255$	

Note 1: $f_{CW} = f_{TCK}/2 \times CWFD[7:0]$, where 1 ≤ CWFD ≤ 255.

TABLE 4-15: PLL LOOP FREQUENCY DIVIDER NUMBER, R/$\overline{W}$ VIA I^2C

N[2:0]			PLL Output Frequency f_C[(1)]	Description
D2	D1	D0		
0	0	0	$f_C = 1 \times f_{TCK}$ (default)	N is an integer number from 1 to 8
0	0	1	$f_C = 1 \times f_{TCK}$	
0	1	0	$f_C = 2 \times f_{TCK}$	
0	1	1	$f_C = 3 \times f_{TCK}$	
1	0	0	$f_C = 4 \times f_{TCK}$	
1	0	1	$f_C = 5 \times f_{TCK}$	
1	1	0	$f_C = 6 \times f_{TCK}$	
1	1	1	$f_C = 8 \times f_{TCK}$	

Note 1: $f_{VCO} = f_C$.

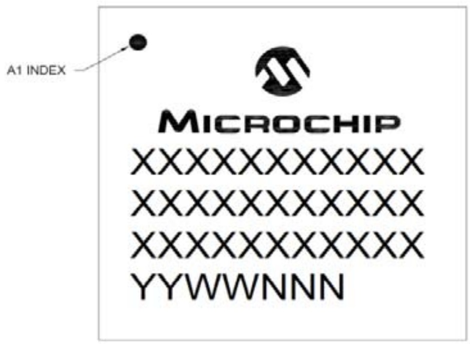
TABLE 4-16: I^2C DEVICE ADDRESS

I^2C Address Pin			Device Address	Device on the Bus
A2	A1	A0		
0	0	0	0000, 0000b	Broadcast Address
0	0	0	1101, 0000b	U0
0	0	1	1101, 0001b	U1
0	1	0	1101, 0010b	U2
0	1	1	1101, 0011b	U3
1	0	0	1101, 0100b	U4
1	0	1	1101, 0101b	U5
1	1	0	1101, 0110b	U6
1	1	1	1101, 0111b	U7

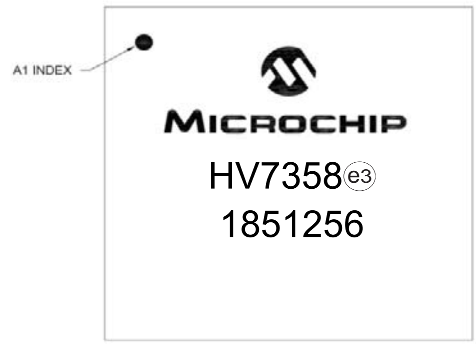
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

168-Lead TFBGA 13 mm x 13 mm



Example

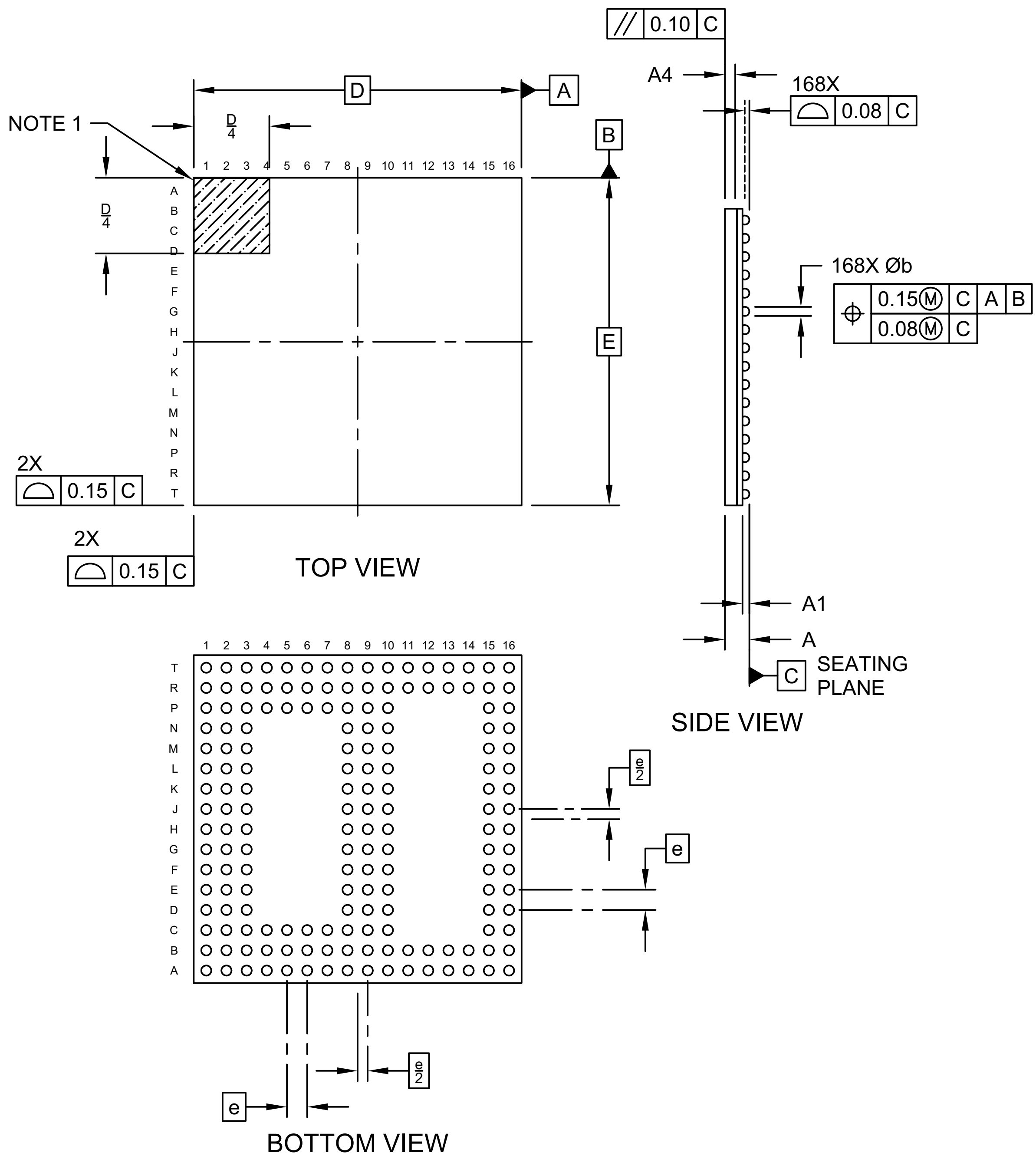


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

168-Ball Thin Fine-Pitch Ball Grid Array (AFA) - 13x13x1.2 mm Body [TFBGA]

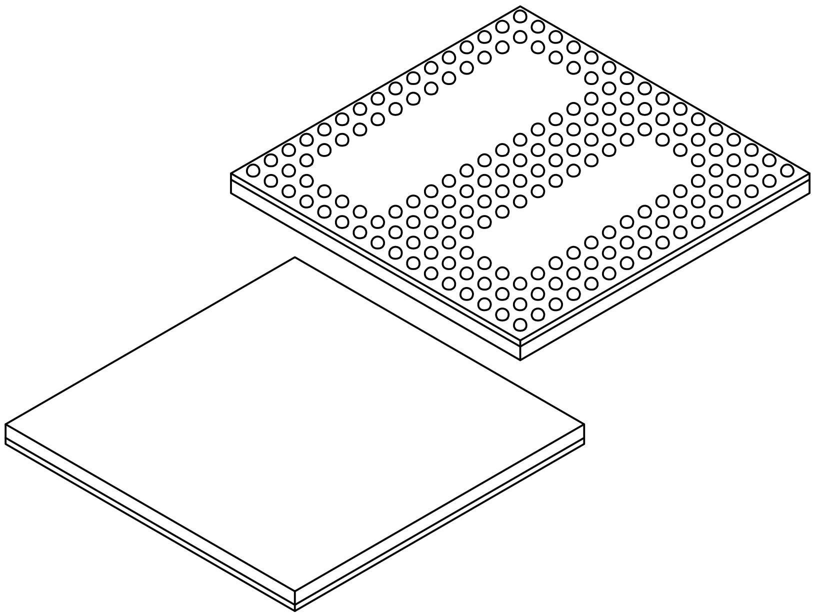
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1191B Sheet 1 of 2

168-Ball Thin Fine-Pitch Ball Grid Array (AFA) - 13x13x1.2 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		168	
Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.23	0.33	-
Mold Cap Height	A4		0.53 REF	
Overall Length	D		13.00 BSC	
Overall Width	E		13.00 BSC	
Ball Diameter	b	0.35	0.40	0.45

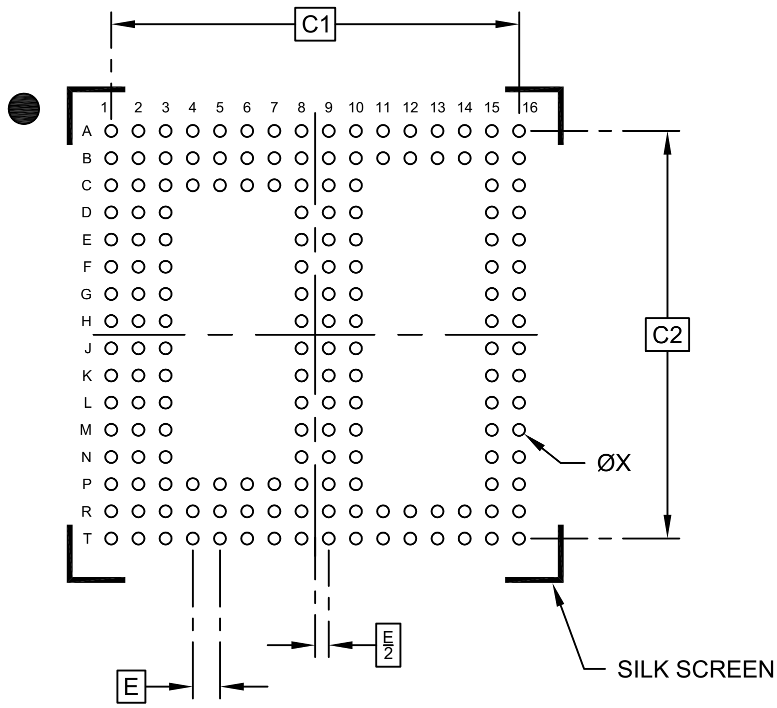
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1191B Sheet 2 of 2

168-Ball Thin Fine-Pitch Ball Grid Array (AFA) - 13x13x1.2 mm Body [TFBGA]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Overall Contact Pad Spacing	C1		12.00 BSC	
Overall Contact Pad Spacing	C2		12.00 BSC	
Pad Diameter (X168)	ØX			0.35

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3191B

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (June 2018)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	—	X	/XX
Device		Temperature Range	Package

Device:	HV7358:	16-Channel, 3-Level HV Ultrasound Transmitter with Built-in Transmit Beamformer
Temperature Range:	V =	0°C to +85°C
Package:	AFA =	168-Lead TFBGA 13 mm x 13 mm

Examples:

a) HV7358-V/AFA: HV7358, Industrial Temperature, 168-Lead TFBGA Package.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV

═ ISO/TS 16949 ═

Trademarks

ISBN: 978-1-5224-3281-4

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra’anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820