HMC984LP4E

v02.0112

DIGITAL PHASE-FREQUENCY DETECTOR

Typical Applications

The HMC984LP4E is suitable for:

- Test Equipment
- Portable Instruments
- High Performance Fractional-N Frequency Synthesizers with Ultra Low Spurious Emissions
- Military

Features

Ultra-Low Noise:

-231 dBc/Hz FOM Integer Mode

-227 dBc/Hz FOM Fractional Mode

Ultra Low Spurious Emissions:
- Less Than 60 dBc Fractional Spurious

Differential Phase Detector Input

14-bit Reference Frequency Divider

Lock Indicator Output

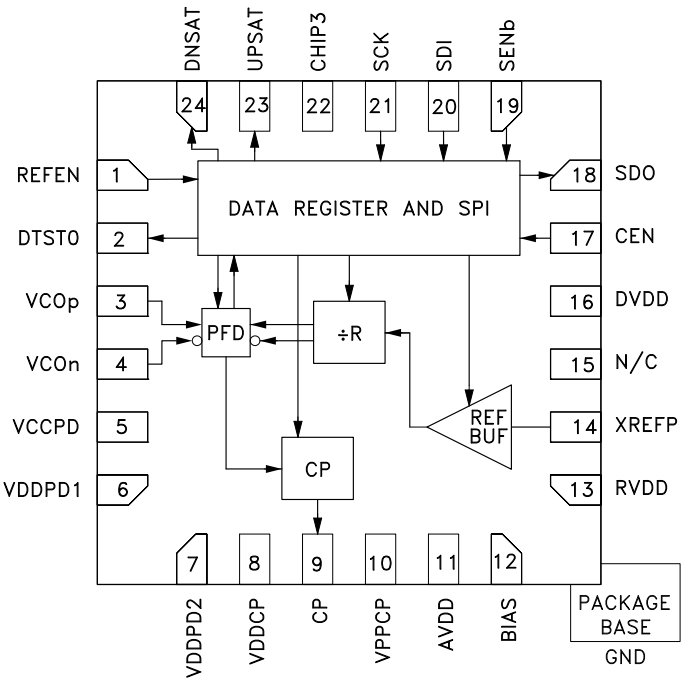
Phase Measurement Capability

GPIO (General Purpose Input/Output) Test Pin

Cycle Slip Prevention Support with HMC984LP4E

24 pin, 4 x 4 mm, LP4E Package

Functional Diagram



General Description

HMC984LP4E is a high-performance, ultra-low phase noise, SiGe BiCMOS Phase-Frequency Detector and Charge Pump targeted to be used together with the HMC983LP5E (Fractional Frequency Divider) to together form a high performance, low noise, ultra low spurious emission fractional-N frequency synthesizer.

Although best performance and maximum features are achieved when used together with the HMC983LP5E, the HMC984LP4E can also be used as a stand-alone, low phase noise phase frequency detector.

The HMC984LP4E can receive differential VCO input, and a reference frequency as high as 150 MHz. It features a 14-bit reference frequency R-Divider, and automatic and/or configurable Lock Detect Indicator, as well as integrated CSP (Cycle Slip Prevention) capability, when used together with the HMC983LP5E, that significantly improves frequency lock time.

Integrated Charge Pump phase swap option enables seamless interfaced to VCOs and active loop filters with inverted polarity.

Additional features include adjustable Charge Pump gain and offset current that improve linearity and performance, and a Soft Reset feature that resets all register to default values without having to perform a power-cycle.

The HMC984LP4E is housed in a compact 24 pin 4x4 mm LP4 package.

Product covered by US and Foreign Patents including US Pat. No. 8,531,217.

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Table 1. Electrical Specifications

TA = +25 °C, AVDD, RVDD, VDDPD1, VDDPD2, DVDD = 3 V; VCCPD, VPPCP, VDDCP = 5 V; GND = 0 V

Parameter	Conditions	Min.	Typ.	Max.	Units
Ref. Input Characteristics					
Frequency Range		DC	50	350	MHz
Ref. Input Power Range	50 Ω Source		6	12	dBm
Ref. Input Impedance			100||3		Ω||pF
Ref/-Divider Range (14-bit)		1		16383	
Phase Detector (PD)					
PD Input Internal Pull-Up Resistance	VCOp, VCOn, Each Side		50		Ω
PD Input Current	VCOp, VCOn, 2.5 mA Steps	12.5	15	17.5	mA
PD Input Voltage Swing	Single-Ended Peak-to-Peak	625	750	875	mV
Fractional Mode					
Phase Detector Frequency	12 dBm Sine-Wave Input, Mode A & B	DC	50	125	MHz
	2 dBm Square-Wave Input, Mode A & B	DC	50	90	MHz
Integer Mode					
Phase Detector Frequency	12 dBm Sine-Wave Input	DC	50	175	MHz
	2 dBm Square-Wave Input	DC	50	150	MHz
Charge Pump (CP)					
CP Output Current	7-bit Programmable, 20 uA/Step, Charge Pump Gain = CP Current/2π Amps/rad	0.02		2.5	mA
CP HiK	See "Charge Pump High Gain (HiK) Mode" section		3.5	6	mA
Offset Current	7-bit Programmable,5 uA/Step	5		635	µA
Phase noise [1]					
Floor Figure of Merit (FOM)	Integer Mode		-230		dBc/Hz
	Fractional Modes A & B		-227		dBc/Hz
	HiK Integer Mode		-232		dBc/Hz
	HiK Fractional Mode A		-230		dBc/Hz
	HiK Fractional Mode B		-229		dBc/Hz
Flicker Figure of Merit (FOM)	Integer Mode		-269		dBc/Hz
	Fractional Modes A & B		-267		dBc/Hz
	HiK Integer Mode		-268		dBc/Hz
	HiK Fractional Mode A		-266		dBc/Hz
	HiK Fractional Mode B		-266		dBc/Hz
Spurious [1]					
Integer Boundary Spurs @ 2.1 GHz	Frequency offsets less than loop bandwidth F_{PD}=50 MHz, Mode A		-60	-55	dBc
Integer Boundary Spurs @ 2.1 GHz	Frequency offsets less than loop bandwidth F_{PD}=50 MHz, Mode B		-70	-65	dBc
1/2 Integer Boundary Spurs	F_{PD}=50 MHz		-75	-70	dBc
1/3 Integer Boundary Spurs	F_{PD}=50 MHz		-85	-80	dBc

[1] Measured with HMC983LP5E/HMC984LP4E as fractional-N synthesizer chip set.

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Table 1. Electrical Specifications *Continued...*

TA = +25 °C, AVDD, RVDD, VDDPD1, VDDPD2, DVDD = 3 V; VCCPD, VPPCP, VDDCP = 5 V; GND = 0 V

Parameter	Conditions	Min.	Typ.	Max.	Units
1/5 Integer Boundary Spurs	Fpd=50 MHz		-85		dBc
Logic Inputs					
VIH Input High Voltage				DVDD - 0.4	V
VIL Input Low Voltage		0.4			V
Logic Outputs					
VOH Output High Voltage				DVDD- 0.4	V
VOL Output Low Voltage		0.4			V
DC Load			1.5		mA
Serial Port					
Serial Port Clock Frequency				30	MHz
Power Supplies					
AVDD, RVDD	Analog Supplies, AVDD should equal DVDD	2.8	3	3.3	V
VCCPD	5 V Analog Supply for PD	4.5	5	5.5	V
VPPCP	CP Analog Supply	4.5	5	5.5	V
VDDCP	CP Digital Supply	4.5	5	5.5	V
DVDD, VDDPD1, VDDPD2	Digital Supplies	2.8	3	3.3	V
Current Consumption					
IDD- Total Current Consumption			123.6		mA
I-AVDD (3 V)	AVDD Current		4.8		mA
I-RVDD (3 V)	Reference Path Current		22		mA
I-VCCPD (5 V)	PD Current		83.5		mA
I-VDDPD1 (3 V)	PD Digital Supply Current		2.7		mA
I-VDDPD2 (3 V)	PD Digital Supply Current		2.7		mA
I-VPPCP (5 V)	CP Analog Supply Current		3		mA
I-VDDCP (5 V)	CP Digital Supply Current		2.9		mA
I-DVDD (3 V)	Total DVDD Current		2		mA
Bias Reference Voltage[2]	Measured with 10 GΩ Volt Meter	1.58	1.72	1.86	V

[2] Bias voltage cannot drive external load. It must be measured with a 10 GΩ voltmeter such as Agilent 34410A. A typical 10 MΩ Digital Volt Meter will read erroneously.

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TYPICAL PERFORMANCE CHARACTERISTICS

Figure 1. HMC984LP4E & HMC983LP5E PLL Flicker FOM vs Temperature [1]

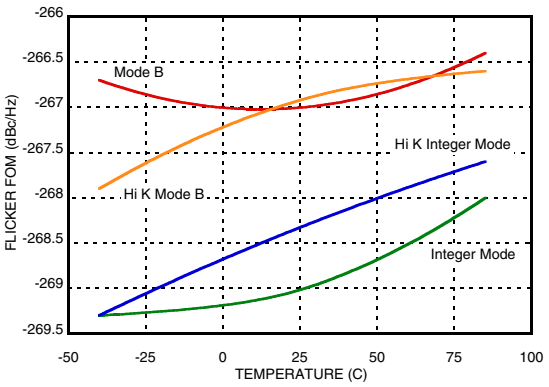


Figure 2. HMC984LP4E & HMC983LP5E PLL Floor FOM vs Temperature [1]

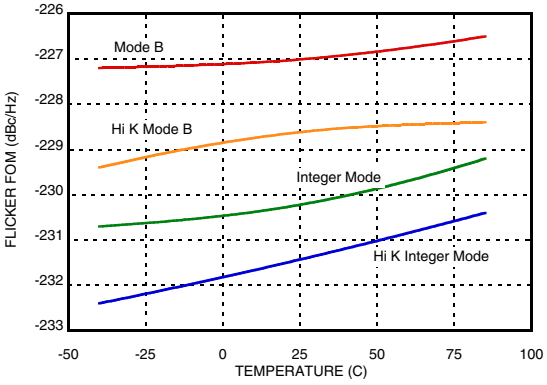


Figure 3. HMC984LP4E & HMC983LP5E PLL Flicker FOM vs Frequency [1]

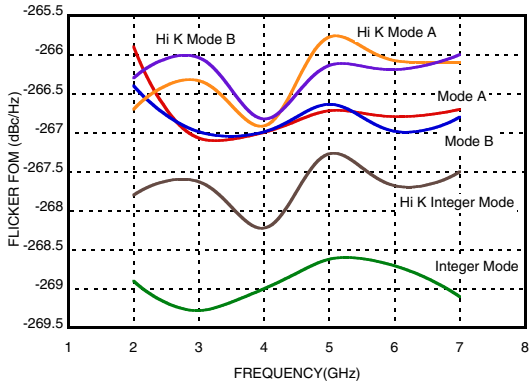


Figure 4. HMC984LP4E & HMC983LP5E PLL Floor FOM vs Frequency [1]

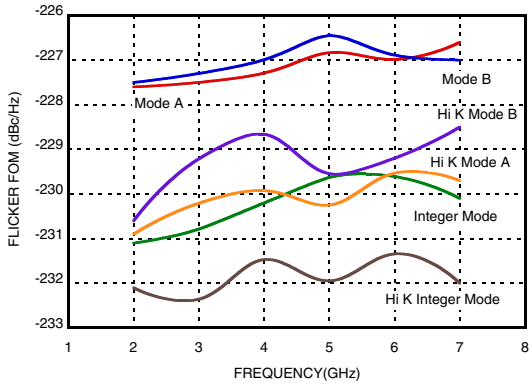


Figure 5. HMC984LP4E & HMC983LP5E PLL Flicker FOM vs Reference Power [1]

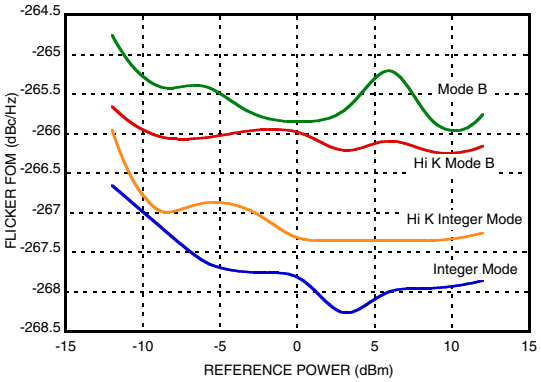
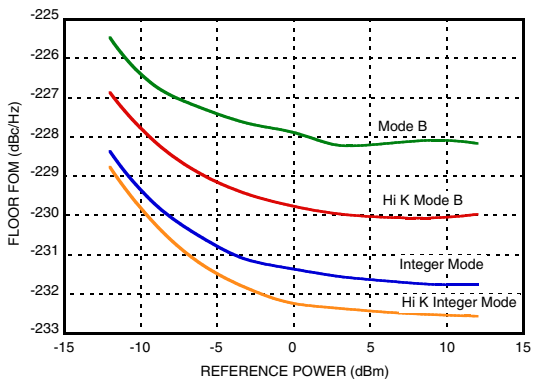


Figure 6. HMC984LP4E & HMC983LP5E PLL Floor FOM vs Reference Power [1]



[1] Crystal frequency = 100 MHz, PFD frequency = 50 MHz, Active Loop Filter with 220 KHz Bandwidth. Measured at 4101 MHz in fractional mode and 4100 MHz in integer mode.

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Figure 7. HMC984LP4E & HMC983LP5E PLL Flicker FOM vs CP Current [2]

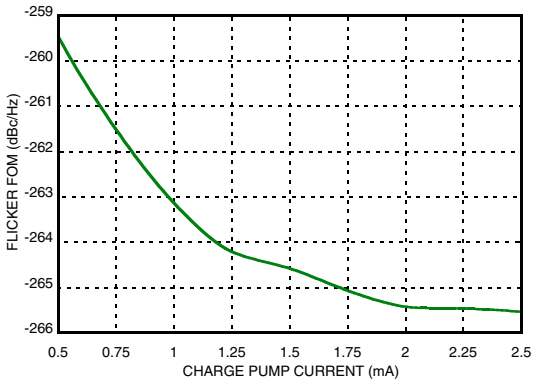


Figure 8. HMC984LP4E & HMC983LP5E PLL Floor FOM vs CP Current [2]

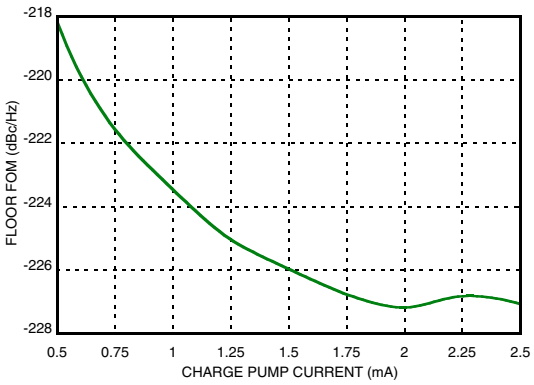


Figure 9. HMC984LP4E & HMC983LP5E PLL Flicker FOM vs CP Voltage [3]

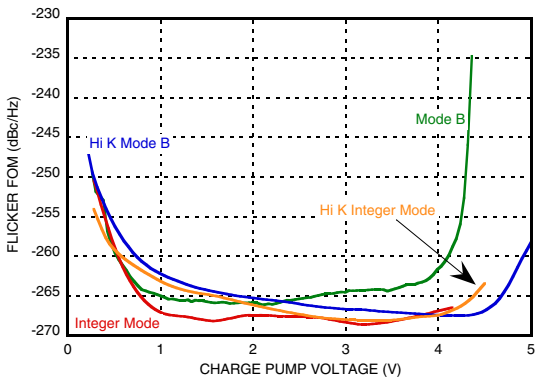


Figure 10. HMC984LP4E & HMC983LP5E PLL Floor FOM vs CP Voltage [3]

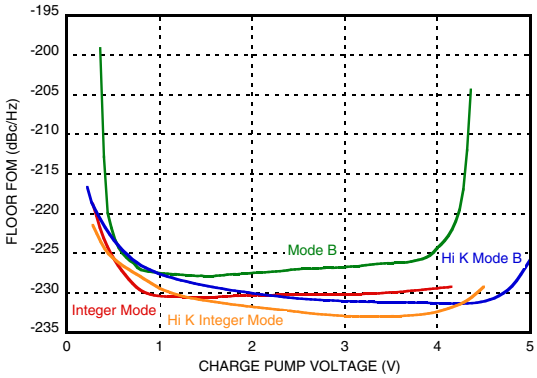


Figure 11. HMC984LP4E & HMC983LP5E PLL Performance at 7000.01 MHz [4]

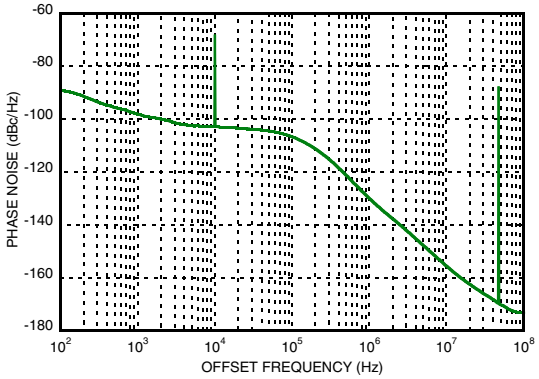
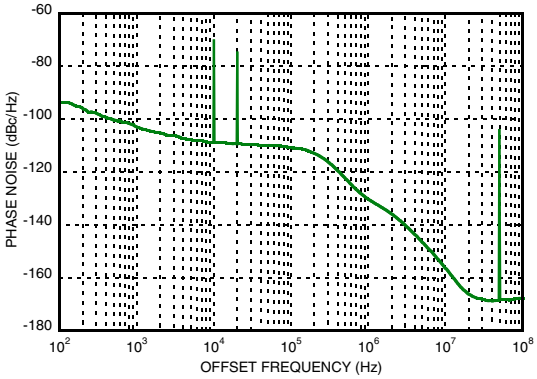


Figure 12. HMC984LP4E & HMC983LP5E PLL Performance at 4100.01 MHz [5]



[2] PLL operated in Mode B, CP Votage = 2.5 V, Active Loop Filter with 220 kHz bandwidth used
[3] Charge Pump Current = 2.5 mA
[4] Crystal frequency=100MHz, PD frequency=50MHz, CP current=2.5mA, CP offset current=255 µA, Loop bandwidth = 87 kHz, PLL in Mode B.
[5] Reference frequency=100 MHz, PD frequency=50 MHz, CP current=2.5 mA, CP offset current=280 µA, Loop bandwidth = 87 kHz, PLL in Mode B.

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Figure 13. HMC984LP4E & HMC983LP5E PLL Performance at 2100.01 MHz [6]

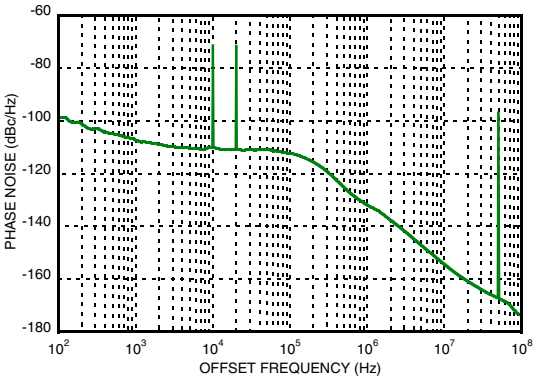


Figure 14. HMC984LP4E & HMC983LP5E [6]

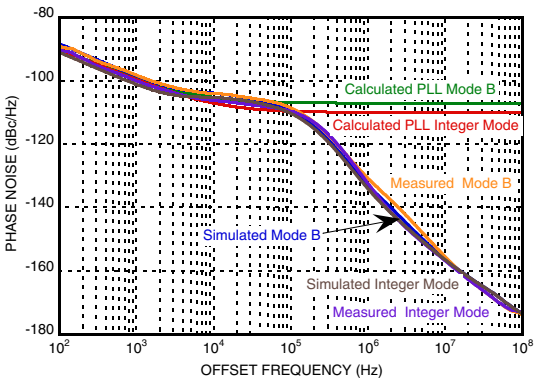


Figure 15. HMC984LP4E & HMC983LP5E PLL In Band Fractional Spurs vs. Offset Current [8]

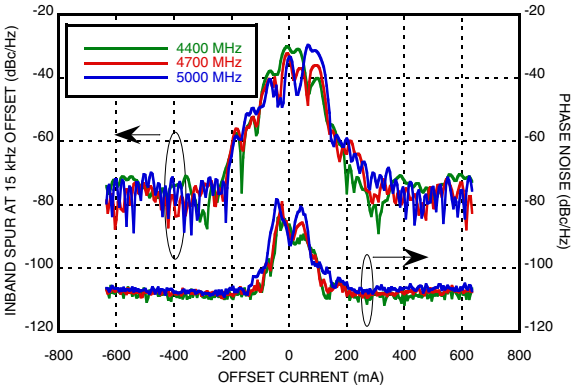


Figure 16. HMC984LP4E & HMC983LP5E PLL Floor FOM vs. RF Input Power

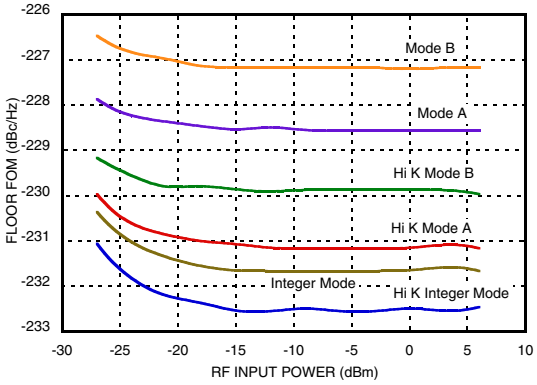


Figure 17. HMC984LP4E & HMC983LP5E PLL Flicker FOM vs. RF Input Power

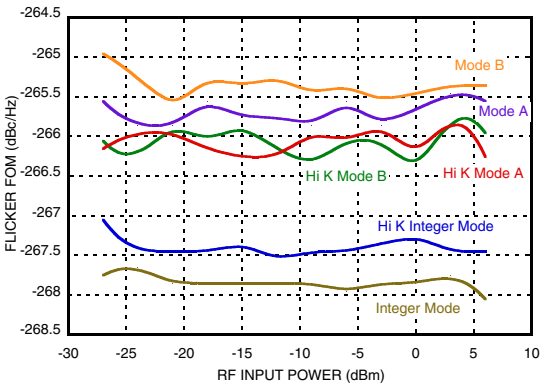
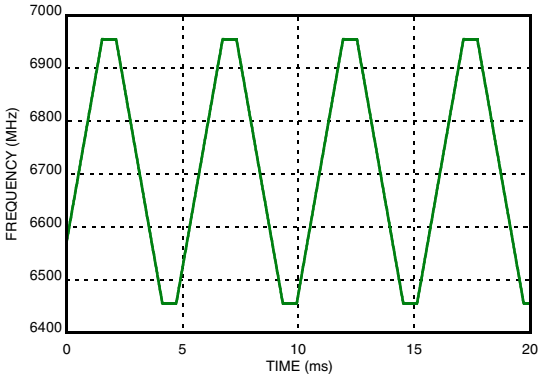


Figure 18. HMC984LP4E & HMC983LP5E PLL Two-Way Auto Frequency Sweep [9]



[6] Crystal frequency=100 MHz, PFD frequency=50 MHz, CP current=2.5 mA, CP offset current=280 µA, Loop bandwidth = 87 kHz, PLL Mode

[7] Measured at 7 GHz in Integer Mode and 7.001 GHz in Fractional mode B. PD Frequency = 50 MHz, and loop filter BW = 87 kHz. Simulated results were obtained using Hittite PLL Design software.

[8] Active Loop filter bandwidth 150 kHz, measured at 10 kHz offset, PFD Frequency=50 MHz. Offset polarity should be positive for inverting configurations and negative otherwise.

[9] 50 MHz PFD

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Figure 19. HMC984LP4E & HMC983LP5E PLL One-Way Triggered Frequency Sweep [10]

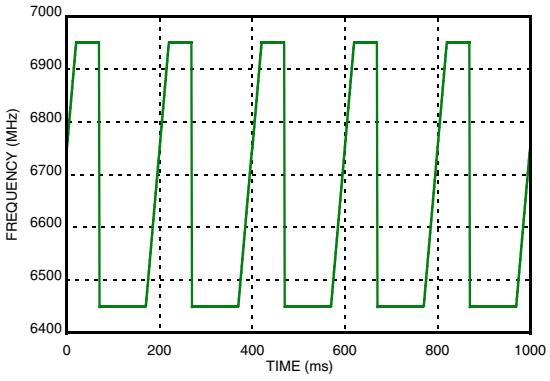


Figure 20. HMC984LP4E & HMC983LP5E PLL Floor FOM Vs. Sine-Wave Ref Input Level [11]

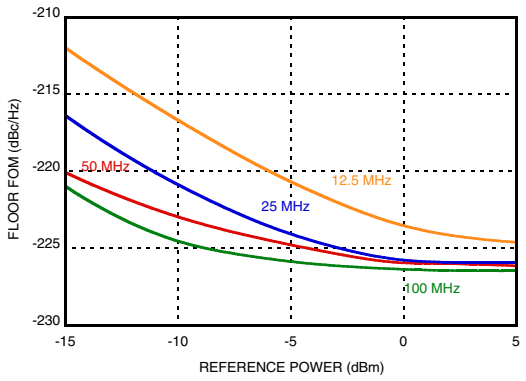


Figure 21. HMC984LP4E & HMC983LP5E PLL Floor FOM Vs Square-Wave Ref Input Level [11]

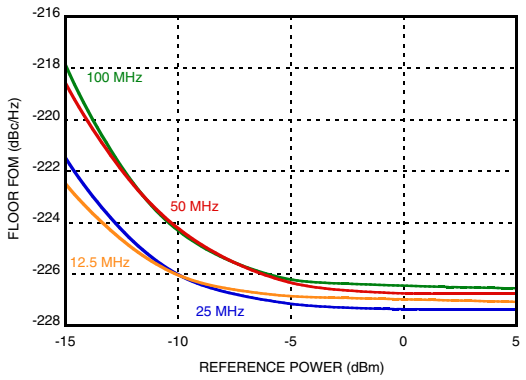


Figure 22. HMC984LP4E & HMC983LP5E PLL Reference Input Return Loss [12]

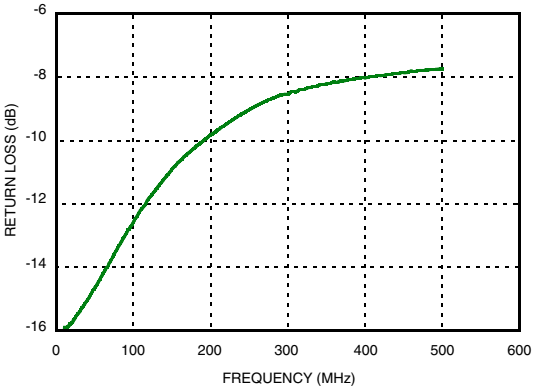


Figure 23. HMC984LP4E & HMC983LP5E PLL Cycle Slip Prevention at 100 MHz PD [13]

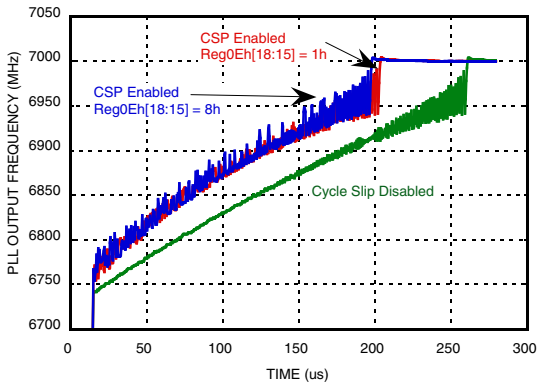
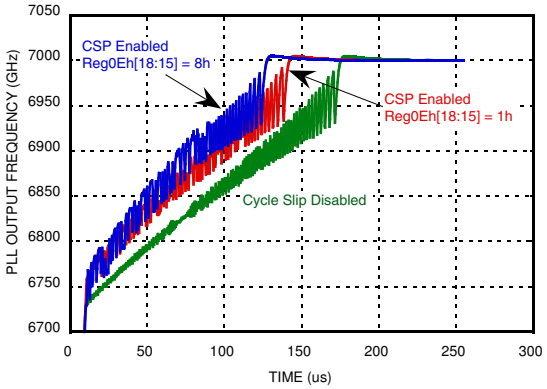


Figure 24. HMC984LP4E & HMC983LP5E PLL Cycle Slip Prevention at 50 MHz PD [13]



[10] Using 10 Hz external trigger. PFD frequency = 10 MHz. Measured with HMC983LP5E/HMC984LP4E fractional-N synthesizer chip set.

[11] Measured with a 100 Ω external resistor termination, resulting in 50 Ω effective input impedance of Reference. Full FOM performance up to maximum 3.3 Vpp input voltage.

[12] Measured with 100 Ω external termination AC coupled on HMC984LP4E & HMC983LP5E evaluation board.

[13]Measured with HMC983LP5E/HMC984LP4E chip set as fractional-N synthesizer. Crystal input frequency = 100 MHz, CP current = 2.5 mA, CP offset current = 245 uA, Loop filter bandwidth = 87 KHz, DSM Mode B selected. Cycle Slip Prevention (CSP) is disabled in HMC984LP4E by setting Reg 01h [4] = 0. Setting Reg 01h [4] = 1 enables CSP in the two chip PLL.

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Table 2. Pin Descriptions

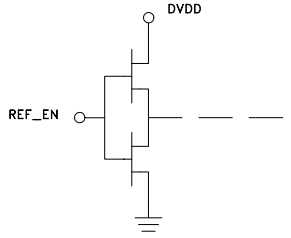
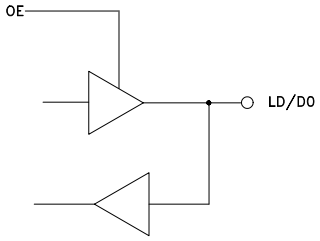
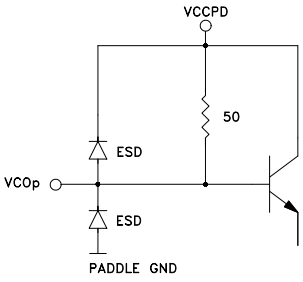
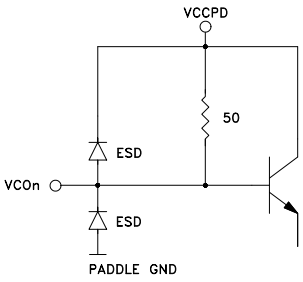
Pin Number	Function	Description	Interface Schematic
1	REF_EN	Gate control output for TCXO clock export	
2	DTSTO	Lock Detect/GPIO bit 0	
3	VCOp	Positive Input Pin for PFD	
4	VCOn	Negative Input Pin for PFD	
5	VCCPD	5 V Analog Supply for Differential PFD	
6,7	VDDPD1, VDDPD2	3 V Phase Detector Supply 1, 3 V Phase Detector Supply 2	
8	VDDCP	5 V Charge Pump Supply	

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Table 2. Pin Descriptions *Continued...*

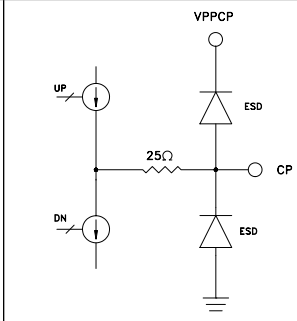
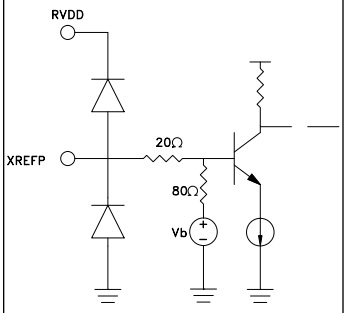
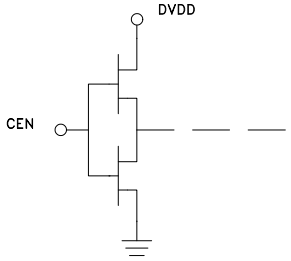
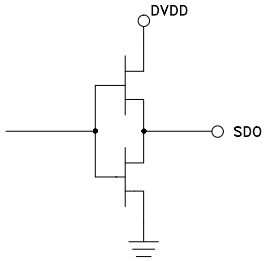
Pin Number	Function	Description	Interface Schematic
9	CP	Charge Pump Output Pin	
10	VPPCP	5 V Analog Power Supply Pin Charge Pump	
11	AVDD	3 V Analog Supply	
12	BIAS	External Decoupling for Analog Bias Circuits	
13	RVDD	3 V Supply Pin for Reference Circuits	
14	XREFP	Reference/TCXO Input Pin	
15	NC	No Connect Pin	
16	DVDD	3 V Digital Supply Pin	
17	CEN	Chip Enable Pin	
18	SDO	Serial Data Output Pin	

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Table 2. Pin Descriptions *Continued...*

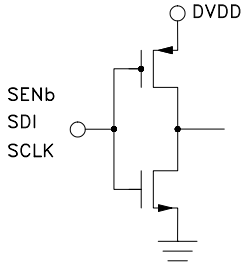
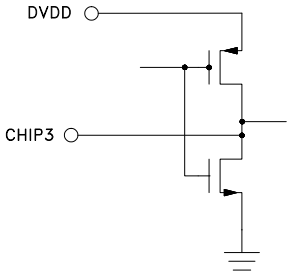
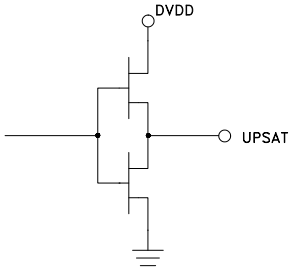
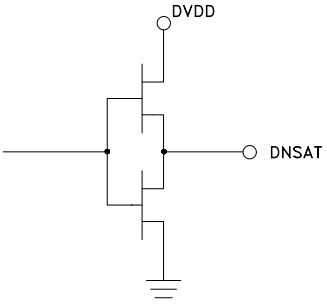
Pin Number	Function	Description	Interface Schematic
19, 20, 21	SENb, SDI, SCLK	Serial Port Enable Input Pin, Active Low, Serial Port Data Input Pin, Serial Data Clock Input Pin	
22	CHIP3	Chip Address Bit 3	
23	UPSAT	Reference Saturation Output	
24	DNSAT	VCO Saturation Output Flag Also Multiplexed with Crystal Oscillator Clock	

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Table 19. Absolute Maximum Ratings

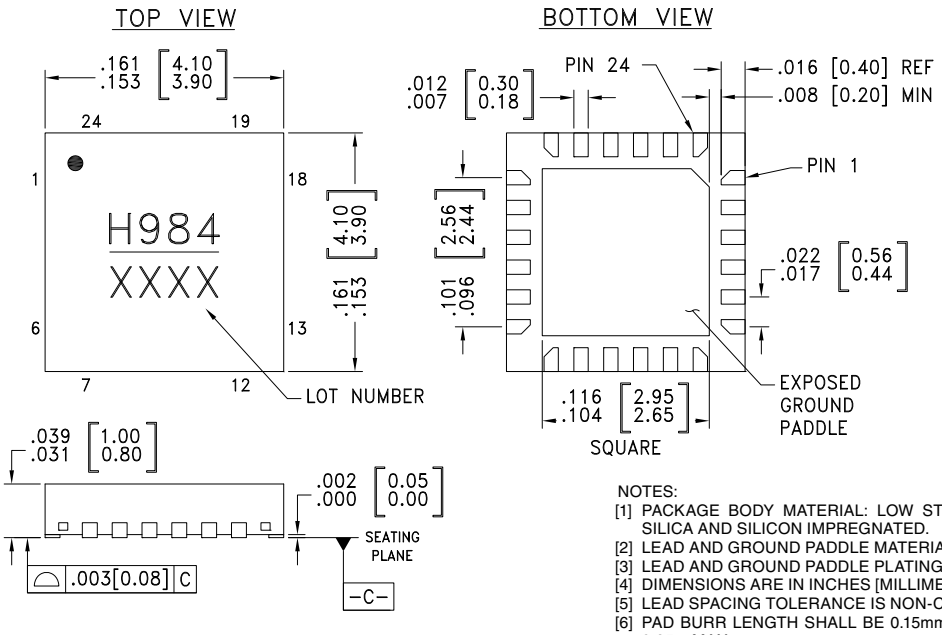
Max VDC to Paddle on Supply Pins 6, 7, 11, 13, 16	-0.3 to 3.6 V
VCCPD, VPPCP, VDDCP	-0.3 to +5.5 V
VCOp, VCOn Common Mode Voltage	VCCPD - 1.4 V
XREFP 50 Ω Source	+ 12 dBm
Digital Input Voltage Range	0.25 to DVDD + 0.5 V
Digital Load	1 kΩ Minimum
Operating Temperature Range	-40 to +85 °C
Operating Temperature Range	-65 to +125 °C
Maximum Junction Temperature	125 °C
Storage Temperature	-65 to +125 °C
Thermal Resistance (Rth) (junction to ground paddle)	12 °C/W

Reflow Soldering Peak Temperature Time at Peak Temperature	 260 °C 40 s
ESD Sensitivity (HBM)	Class 1 B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
[1] PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
[2] LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
[3] LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
[4] DIMENSIONS ARE IN INCHES [MILLIMETERS].
[5] LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
[6] PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25m MAX.
[7] PACKAGE WARP SHALL NOT EXCEED 0.05mm
[8] ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
[9] REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating [2]	Package Marking [1]
HMC984LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H984 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

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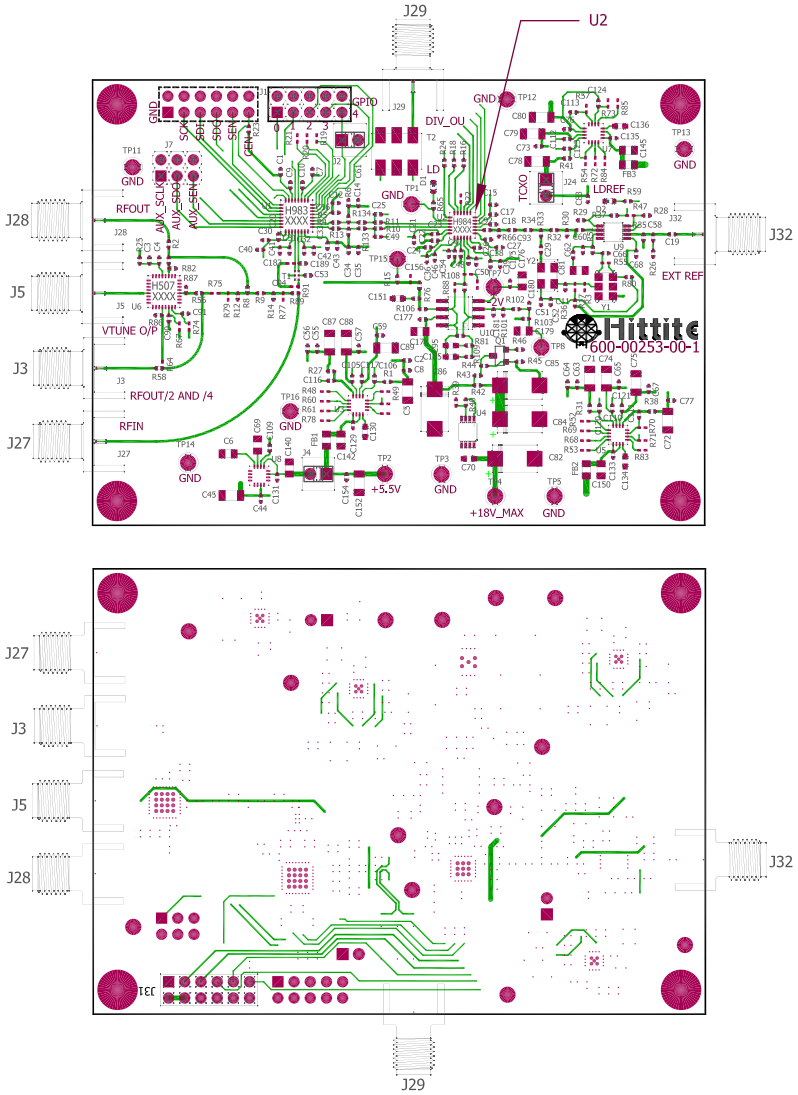
Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohms impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown unless mentioned otherwise. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Table 20. Evaluation Order Information

Item	Contents	Part Number
Evaluation Kit	HMC984LP4E and HMC983LP5E PLL Chipset Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software)	EKIT01-HMC983LP5E

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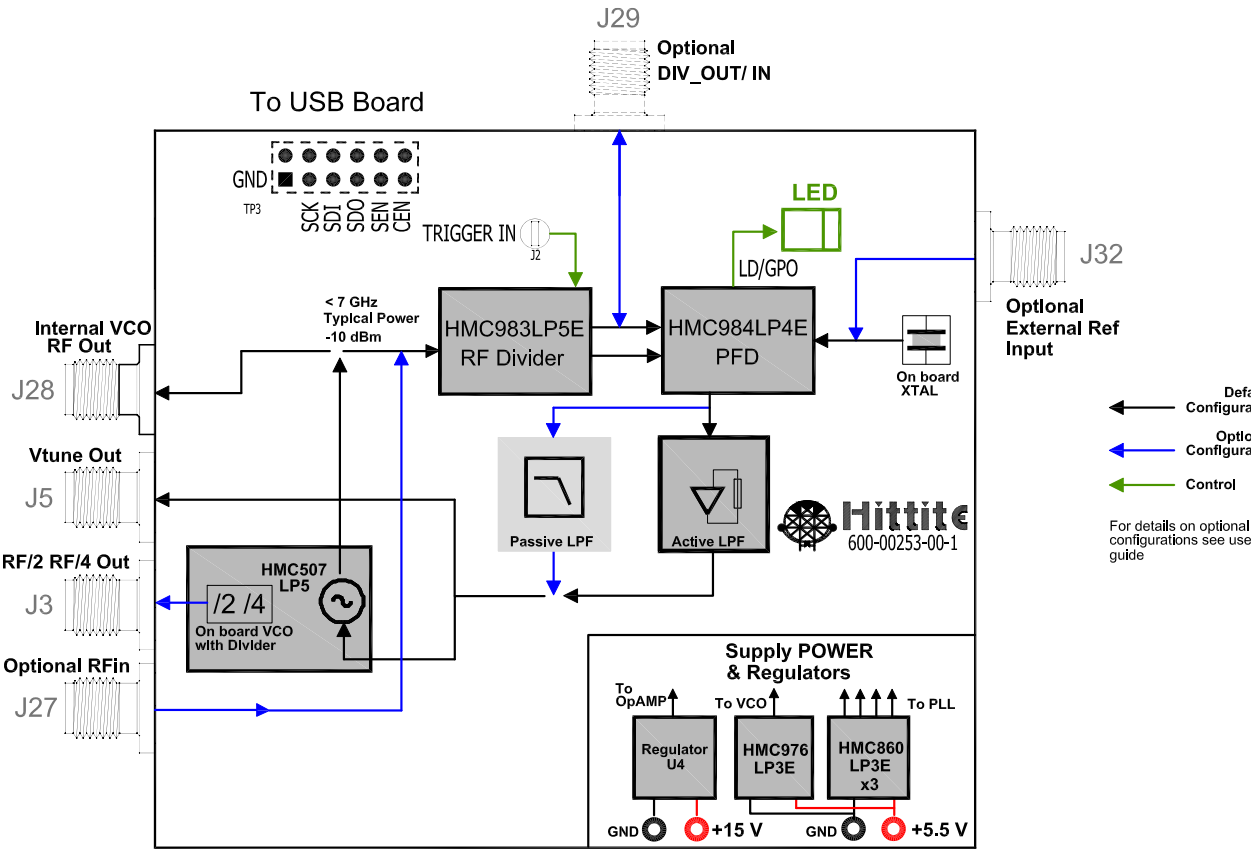
RoHS✓ EARTH FRIENDLY

Evaluation PCB Block Diagram



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Typical Performance Characteristics

Theory of Operation

Primary target application of the HMC984LP4E is to be used with the HMC983LP5E as shown in Figure 25. Together these two components form a high performance, low noise, ultra low spurious emissions fractional-N frequency synthesizer. The two components are separated in order to maximize isolation between them, and minimize common distortion and modulation by-products that exist in all PLLs. Careful IC design and increased isolation between the two components result in high performance , high spectral efficiency PLL, with extremely low spurious emissions.

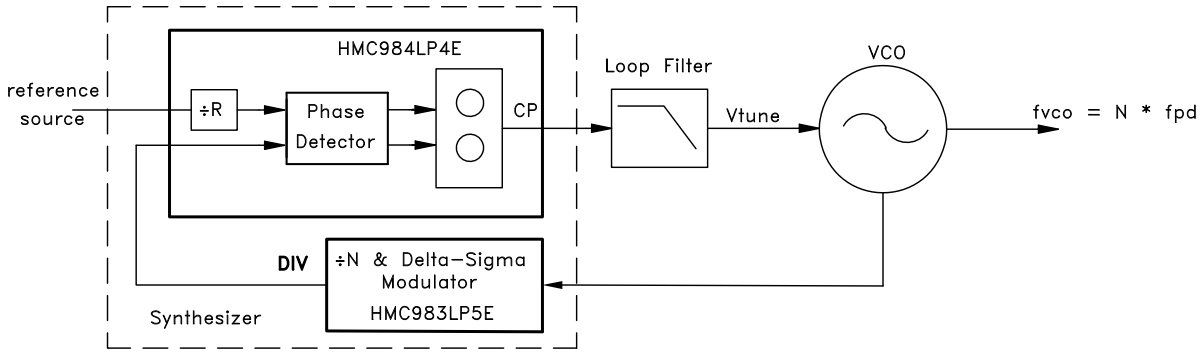

Figure 25. Typical Application of HMC984LP4E with HMC983LP5E to Form a Frequency Synthesizer

HMC984LP4E is a high performance low noise phase detector and charge pump. It consists of the following main functional blocks;

1. Reference/Crystal Buffer
2. Reference Path 'R' Divider
3. Differential Phase/Frequency Detector
4. 5 V Charge Pump
5. Two Lock Detect Circuits
6. Serial Port Interface

PLL Performance Metrics (Figure of Merit, Noise Floor, and Flicker Noise Models)

The phase noise of an ideal phase locked oscillator is dependent upon a number of factors:

- **a.** Frequency of the VCO, and the Phase detector
- **b.** VCO Sensitivity, kvco, and VCO and Reference Oscillator phase noise profiles
- **c.** Charge Pump current, Loop Filter and Loop Bandwidth
- **d.** Mode of Operation: Integer, Fractional modulator style

The contributions of the PLL to the output phase noise can be characterized in terms of a Figure of Merit (FOM) for both the PLL noise floor and the PLL flicker (1/f) noise regions, as follows:

PLL PHASE NOISE

$$\Phi_p^2\left(f_0, f_m, f_{pd}\right) = \frac{F_{p1} f_0^2}{f_m} + \frac{F_{p0} f_0^2}{f_{pd}} \qquad \text{(Eq 1)}$$

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where:

Φ_p^2	Phase Noise Contribution of the PLL (rads²/Hz)
f_o	Frequency of the VCO (Hz)
f_{pd}	Frequency of the Phase Detector (Hz)
f_m	Frequency offset from the carrier (Hz)
F_{po}	Figure of Merit (FOM) for the phase noise floor
F_{p1}	Figure of Merit (FOM) for the flicker noise region

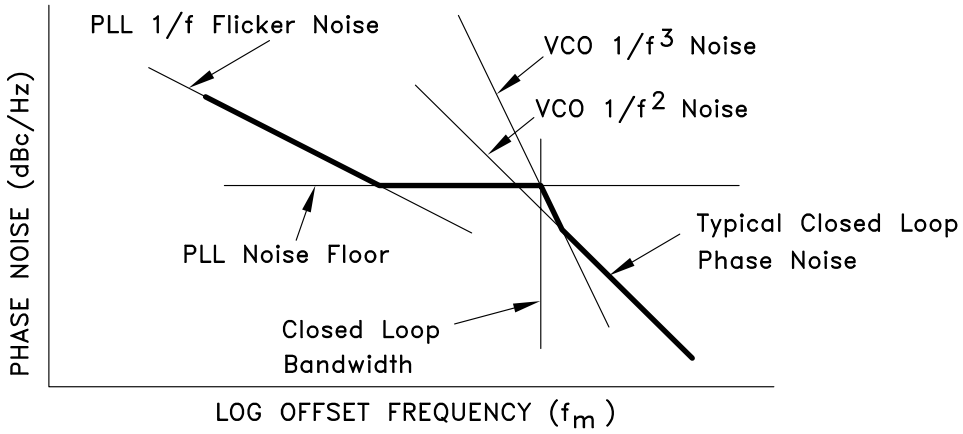

Figure 26. Figure of Merit Noise Models for the PLL

If the free running phase noise of the VCO is known, it may also be represented by a figure of merit for both $1/f^2$, F_{v2}, and the $1/f^3$, F_{v3}, regions.

VCO PHASE NOISE

$$\Phi_v^2(f_0, f_m) = \frac{F_{v2} f_0^2}{f_m^2} + \frac{F_{v3} f_0^2}{f_m^3} \quad \text{(Eq 2)}$$

The Figures of Merit are essentially normalized noise parameters for both the PLL and VCO that can allow quick estimates of the performance levels of the PLL at the required VCO, offset and phase detector frequency. Normally, the PLL IC noise dominates inside the closed loop bandwidth of the synthesizer, and the VCO dominates outside the loop bandwidth at offsets far from the carrier. Hence a quick estimate of the closed loop performance of the PLL can be made by setting the loop bandwidth equal to the frequency where the PLL and free running phase noise are equal.

The Figure of Merit is also useful in estimating the noise parameters to be entered into a closed loop design tool such as Hittite PLL Design, which can give a more accurate estimate of the closed loop phase noise and PLL loop filter component values.

Given an optimum loop design, the approximate closed loop performance is simply given by the minimum of the PLL and VCO noise contributions.

$$\Phi^2 = \min\left(\Phi_p^2, \Phi_v^2\right) \quad \text{(Eq 3)}$$

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An example of the use of the FOM values to make a quick estimate of PLL performance: Estimate the phase noise of an 7 GHz closed loop PLL with a 100 MHz reference operating in Fractional Mode B with the VCO operating at 7 GHz. Assume an HMC505LP4E VCO has free running phase noise in the $1/f^2$ region at 1 MHz offset of -130 dBc/Hz and phase noise in the $1/f^3$ region at 1 kHz offset of -48 dBc/Hz.

F_{v1_dB} =	-130	Free Running VCO PN at 1 MHz offset
	+20*log10(1e6)	PNoise normalized to 1 Hz offset
	-20*log10(7e9)	PNoise normalized to 1 Hz carrier
	= -206.9 dBc/Hz at 1 Hz	VCO FOM
F_{v3_dB} =	-48	Free Running VCO PN at 1 kHz offset
	+30*log10(1e3)	PNoise normalized to 1 Hz offset
	-20*log10(7e9)	Pnoise normalized to 1 Hz carrier
	= -154.9 dBc/Hz at 1 Hz	VCO Flicker FOM

We can see from Figure 3 and Figure 4 respectively that the PLL FOM floor and FOM flicker parameters in fractional Mode A are approximately:

Fpo_dB = -227 dBc/Hz at 1 Hz
Fp1_dB = -267 dBc/Hz at 1 Hz

Each of the Figure of Merit equations result in straight lines on a log-frequency plot. We can see in the example below the resulting

PLL floor at 7 GHz = F_{po_dB} + 20log10(fvco) - 10log10(fpd) = -227+ 196.9 -80 = -110.1 dBc/Hz
PLL Flicker at 1 kHz = F_{p1_dB} + 20log10(fvco) - 10log10(fm) = -267 + 196.9-30 = -100.1 dBc/Hz

VCO at 1 MHz = F_{v1_dB} + 20log10(fvco) - 20log10(fm) = -206.9 +196.9-120 = -130 dBc/Hz
VCO flicker at 1 kHz = F_{v3_dB}+20log10(fvco)-30log10(fm)= -154.9 +196.9-90 = -48 dBc/Hz

These four values help to visualize the main contributors to phase noise in the closed loop PLL. Each falls on a linear line on the log-frequency phase noise plot shown in Figure 25.

Spurious Performance

Integer Operation

The VCO always operates at an integer multiple of the PD frequency in an integer PLL. In general, spurious signals originating from an integer PLL can only occur at multiples of the PD frequency. These unwanted outputs are often simply referred to as reference sidebands.

Spurs unrelated to the reference frequency must originate from outside sources. External spurious sources can modulate the VCO indirectly through power supplies, ground, or output ports, or bypass the loop filter due to poor isolation of the filter. It can also simply add to the output of the PLL.

The HMC984LP4E together with the HMC983LP5E have been designed and tested for ultra-low spurious performance. Reference spurious levels can be typically below -100 dBc with a well designed board layout. A regulator with low noise and high power supply rejection, such as the HMC860LP3E, is recommended to minimize external spurious sources.

Reference spurious levels of below -100 dBc require superb board isolation of power supplies, isolation of the VCO from the digital switching of the synthesizer and isolation of the VCO load from the PLL. Typical board layout, regulator design, demo boards and application information are available for very low spurious operation. Operation with lower levels of isolation in the application circuit board, from those recommended by Hittite, can result in higher spurious levels.

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Of course, if the application environment contains other interfering frequencies unrelated to the PD frequency, and if the application isolation from the board layout and regulation are insufficient, then the unwanted interfering frequencies will mix with the desired PLL output and cause additional spurs. The level of these spurs is dependant upon isolation and supply regulation or rejection (PSRR).

Fractional Operation

Unlike an integer PLL, spurious signals in a fractional PLL can occur due to the fact that the VCO operates at frequencies unrelated to the PD frequency. Hence intermodulation of the VCO and the PD harmonics can cause spurious sidebands. Spurious emissions are largest when the VCO operates very close to an integer multiple of the PD. When the VCO operates exactly at a harmonic of the PD then, no in-close mixing products are present.

Interference is always present at multiples of the PD frequency, f_{pd}, and the VCO frequency, f_{vco}. If the fractional mode of operation is used, the difference, Δ, between the VCO frequency and the nearest harmonic of the reference, will create what are referred to as integer boundary spurs. Depending upon the mode of operation of the PLL, higher order, lower power spurs may also occur at multiples of integer fractions (sub-harmonics) of the PD frequency. That is, fractional VCO frequencies which are near $n \cdot f_{pd} + f_{pd} \cdot d/m$, where n, d and m are all integers and $d \leq m$ (mathematicians refer to d/m as a rational number). We will refer to $f_{pd}d/m$ as an integer fraction. The denominator, m, is the order of the spurious product. Higher values of m produce smaller amplitude spurious at offsets of mΔ and usually when $m > 4$ spurs are small or unmeasurable.

The worst case, in fractional mode, is when $d=1$, and the VCO frequency is offset from $n \cdot f_{pd}$ by less than the loop bandwidth. This is the “in-band fractional boundary” case.

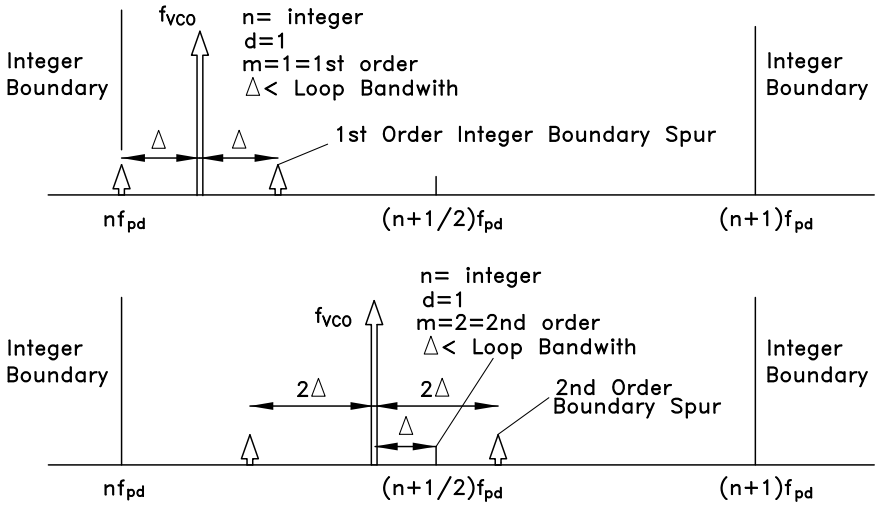

Figure 27. Fractional Spurious Example

Characterization of the levels and orders of these products is not unlike a mixer spur chart. Exact levels of the products are dependent upon isolation of the various synthesizer parts. Hittite can offer guidance about expected levels of spurious with our PLL and VCO application boards. Regulators with high power supply rejection ratios (PSRR) are recommended, especially in noisy applications.

When operating in fractional mode, charge pump and phase detector linearity is of paramount importance. Any non-linearity degrades phase noise and spurious performance. Phase detector linearity degrades when the phase error is very small and is operating back and forth between reference lead and VCO lead. To mitigate these non-linearities in fractional mode it is critical to operate the phase detector with some finite phase offset such that either the reference or VCO always leads. To provide a finite phase error, extra current sources can be enabled which provide a constant

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DC current path to VDD (VCO leads always) or ground (reference leads always). These current sources are called charge pump offset and they are controlled via Reg 04h[20:14]. The time offset at the phase detector should be ~2.5 ns + 4 T_{ps}, where T_{ps} is the RF period at the fractional prescaler input in nanoseconds. The specific level of charge pump offset current is determined by this time offset, the comparison frequency and the charge pump current and can be calculated from:

$$\text{Required CP Offset} = (2.5 \cdot 10^{-9} + 4T_{PS}) \cdot (F_{comparison}) \cdot I_{CP} \text{ where:} \quad \text{(Eq 4)}$$

T_{PS}: is the RF period at the fractional prescaler input (sec)

I_{CP}: is the full scale current setting of the switching charge pump (A)

Fcomparison: is the comparison frequency (Hz)

Note that this calculation can be performed for the center frequency of the VCO, and does not need refinement for small differences (<25%) in center frequencies. Also, operation with unreasonably large charge pump offset may cause Lock Detect to incorrectly indicate an unlocked condition. To correct, reduce the offset to recommended levels.

Reference/Crystal Input Buffer

The ultra-low noise phase-detector requires the best possible reference signal. The low phase noise reference input buffer is optimized for this purpose. The input pin XREFP is DC coupled internally and there is 800 mV DC bias on the pin. The reference source should be AC coupled to the pin. The maximum input power can be up to 12 dBm from a 50 Ω source. In order to achieve best phase noise performance, the reference source should have a phase noise floor of -160 dBc/Hz or better.

Reference Path 'R' Divider

HMC984LP4E has 14-bit frequency divider that divides the incoming reference frequency by any number from 1 to 2^{14}-1 = 16,383 inclusive. The maximum frequency at which the phase detector can work depends on the mode of operation when working as a PLL with its companion chip HMC983LP5E. In integer mode, the reference buffer and divider can work up to 175 MHz, and in fractional mode the maximum frequency is typically 125 MHz. Hence higher crystal frequencies need to be divided down by the R divider in order to generate phase comparison frequency that meets the limits of the phase detector. The minimum reference frequency can be as low as 100 kHz provided that sharp rise and fall times (less than 500 ps) are guaranteed. Internally, the reference signal is used by other circuitry, besides the phase detector. For best performance, it is recommended to use a higher reference frequency that is divided by the internal R-Divider to generate the required phase comparison frequency.

Table 3. Reference Sensitivity Table

	Square Input			Sinusoidal Input		
Frequency (MHz)	Slew > 0.5V/ns	Recommended Swing (Vpp)			Recommended Power Range (dBm)	
	Recommended	Min	Max	Recommended	Min	Max
< 10	YES	0.6	2.5	x	x	x
10	YES	0.6	2.5	x	x	x
25	YES	0.6	2.5	ok	8	15
50	YES	0.6	2.5	YES	6	15
100	YES	0.6	2.5	YES	5	15
150	ok	0.9	2.5	YES	4	12
200	ok	1.2	2.5	YES	3	8
200 to 350	x	x	x	YES[1]	5	10
Note: For greater than 200 MHz operation, use buffer in High Frequency Mode. Reg 08h[11] = 1						

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Differential Phase-Frequency Detector

As shown in Figure 25, the HMC984LP4E features an ultra-low noise digital differential Phase Detector (PD) with two differential inputs. One input comes from the reference path divider and the other from VCO path divider. The reference input is internal to HMC984LP4E whereas the divided VCO input is external. The output from the PD is fed to the charge pump in HMC984LP4E which converts the PD digital output to a current with programmable gain. The output of the CP is directly proportional to the phase difference between the divided reference and the VCO path signals.

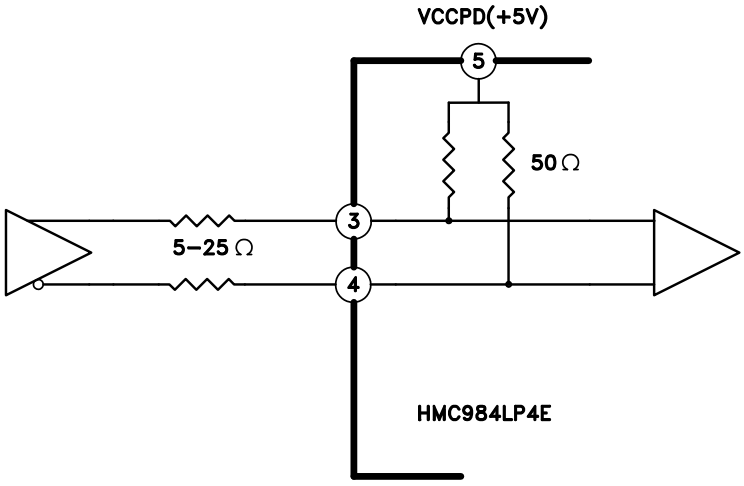

Figure 28. HMC984LP4E Input Interface

The input of PD is a differential current-input. The input interface configurations are shown in Figure 25 and Figure 25. The HMC984LP4E is designed to work with its companion divider part, the HMC983LP5E, that provides an open collector output. The inputs are internally pulled up to VCCPD with on-chip 50 Ω resistors. Thus, any open collector buffer can drive the PD inputs. A minimum of 750 mVpp single-ended level is needed to drive the PD inputs.

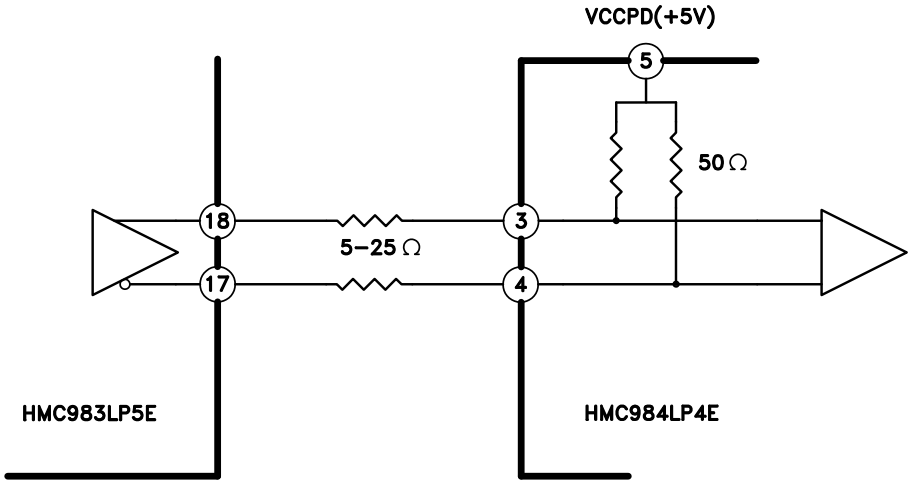

Figure 29. HMC984LP4E Input Interface with Companion Part HMC983LP5E

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The PD has several features and controls including:

- Phase Swap
- UP/DN Enable
- Forced Outputs

Phase swap

The input phase signals to the PD can be swapped internally by writing Reg 03h[4] = 1. When swapped, the PD gain will be reversed. This feature enables the HMC984LP4E to be interfaced with reverse polarity VCOs (VCOs that have negative gain curve), as well as systems that use an active loop filter where the operational amplifier introduces a reverse phase polarity.

Forced Outputs

The UP or DN outputs from the PD can be forced with SPI control to keep constantly active in order to achieve faster lock (to force UP write Reg 04h[26] = 1, to force DN write Reg 04h[27] = 1). This capability is used in CSP (Cycle Slip Prevention) feature when large phase errors are detected. In such a case the CP is continuously turned on the appropriate direction (UP or DN) by the internal state machine to force faster phase convergence, and thus achieve faster lock. Forced otput capability is also useful for testing purposes. It can be used to bring the VCO tune control voltage to supply or ground, and observe the limits of the VCO.

Cycle Slip Prevention

When the frequency of the synthesizer is changed and the current VCO frequency is far from the desired locked frequency, the phase difference at the PD varies rapidly over a range larger than ±2π radians. Since the gain of the PD varies linearly with phase only up to ±2π, the gain of conventional PDs will cycle from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly more than 2π radians. This phenomena is known as cycle slipping. Cycle slipping causes the pull-in rate during the phase acquisition to vary cyclically as shown in the red curve in Figure 25. Cycle slipping can dramatically increase the time to lock to a value far greater than that predicted by normal small signal Laplace analysis.

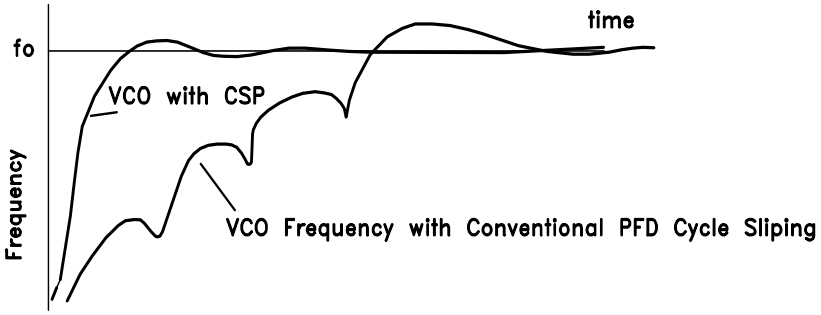

Figure 30. Cycle Slipping

The HMC984LP4E PD features Cycle Slip Prevention (CSP) only when working in conjunction with the companion part, the HMC983LP5E. When enabled, the CSP feature holds the PD gain in the appropriate polarity until such time as the frequency difference is near zero. This enables significantly faster lock times as shown in Figure 25. The use of CSP feature is enabled with CSP Enable (Reg 01h[4] = 1) and CSP Output Enable (Reg 01h[13] = 1). The CSP feature may be optimized for a given set of PLL dynamics by adjusting the PD sensitivity to cycle slipping. This is achieved by adjusting CSP Reset Delay (Reg 03h[2:0]).

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The HMC984LP4E has two outputs, UPSAT and DNSAT, which indicate to the HMC983LP5E whether the Reference or the VCO is leading in phase. These outputs are CMOS signal with DVDD levels. When HMC983LP5E detects saturation (large phase error), it configures itself, and the HMC984LP4E in order to eliminate or reduce cycle clipping. There are additional controls for adjusting the CSP operation in HMC983LP5E. The controls for CSP feature are;

1. Register 0Eh bits [18:15] control the step size, where step is a VCO cycle.
2. Register 0Eh bit [29] increases the step size by a factor of 16 for operations with low reference frequencies.

The actual operation of CSP will depend on the Reference and VCO frequencies and will need to be tailored for each application.

Charge Pump

The charge pump in HMC984LP4E converts the phase detector digital outputs to appropriate current level that is proportional to phase difference between the reference and the VCO. A simplified block diagram of the charge pump is shown in Figure 25. The HMC984LP4E CP has programmable current gain and offset current.

Charge Pump Gain Current

CP gain current defines the gain of Phase Detector vs. Phase Difference in Amps/radians. The UP and DOWN gain currents are configured in Reg 04h[6:0] and Reg 04h[13:7] respectively. Both UP and DOWN currents can be programmed to provide up to 2.5 mA independently in 127 steps (20 µA/step). Resulting phase detector gain is the total current from one side divided by 2π. For example, if both UP and DOWN currents are set 2 mA each, the gain would be 2 mA/2π = 318.31 µA/radian. Typically both of the gain currents are set to the same value.

Charge Pump Phase Offset

Either of the UP or DOWN charge pumps may have a DC offset current added to it. Offset current allows the phase detector to operate with a phase offset between the reference and the divided VCO inputs. The phase offset is proportional to the ratio of the offset current to the main current times the period of the phase comparison clock.

$$\text{PD Phase offset} = \frac{\text{Offset Current}}{\text{CP Current}} \times \frac{1}{f_{PD}} \qquad \text{(Eq 5)}$$

It is recommended to operate the HMC984LP4E with a phase offset when using fractional mode to reduce non-linear effects from any UP and DN pump mismatches that may exist. Phase noise in fractional mode is strongly affected by charge pump offset.

The magnitude of offset current is set in Reg 04h[20:14], and can be added to the UP (Reg 04h[21] = 1) or DOWN (Reg 04h[22] = 1) pumps.

As an example, if the main pump gain was set at 2 mA, an offset of 160 µA (Reg 04h[20:14] = 20h) and 50 MHz PFD rate would represent a phase offset of about (160/2000)*360 = 28.8 degrees or (163.5 µA/2000 µA)*20 ns = 1.6 ns phase offset at the PD input.

Charge Pump High Gain (HiK) Mode

Operating the CP of the HMC984LP4E in High Gain mode (Reg 04h[23] = 1) can improve PLL phase noise performance by up to 3 dB. In High Gain mode the charge pump can deliver current of 3.5 mA + normal programmed CP current. High gain mode can be used without the normal charge pump current in which case the loop filter should be designed with a current of 3.5 mA. In the case where high gain mode is used with the normal CP current, the loop filter should be designed with a charge pump current of 3.5 mA + programmed CP current. The high gain mode current is depended on the loop filter voltage, therefore the high gain mode should be used with active loop filters to keep a constant voltage a the charge pump output.

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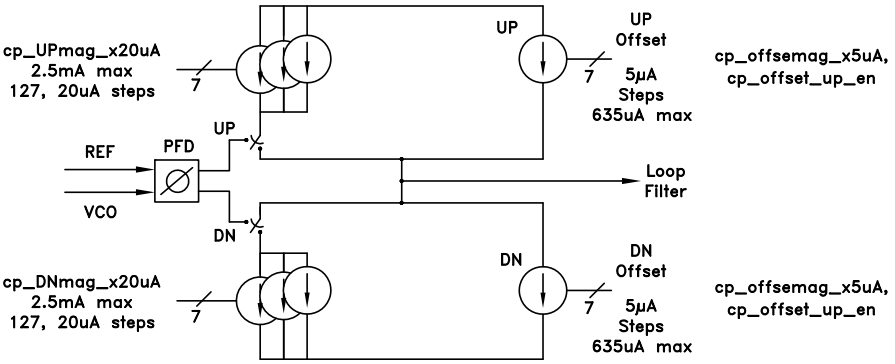

Figure 31. Charge Pump Block Diagram

PFD Jitter and Lock Detect Background

In normal phase locked operation the divided VCO signal arrives at the phase detector in phase with the divided crystal signal, known as the reference signal. Despite the fact that the device is in lock, the phase of the VCO signal and the reference signal vary in time due to the phase noise of the crystal and VCO oscillators, the loop bandwidth used and the presence of fractional modulation or not. The total integrated noise on the VCO path normally dominates the variations in the two arrival times at the phase detector if fractional modulation is turned off.

To determine weather the VCO is in lock or not, it is necessary to distinguish between normal phase jitter when in lock and phase jitter when not in lock.

First, the meaning of jitter of the synthesizer that is observed at the phase detector in integer or fractional modes needs to be understood.

The standard deviation of the arrival time of the VCO signal, or the jitter, in integer mode may be estimated with a simple approximation if it is assumed that the locked VCO has a constant phase noise, Φ2 (*f*0), at offsets less than the loop 3 dB bandwidth and a 20 dB per decade roll off at greater offsets. The simple locked VCO phase noise approximation is shown on the left of Figure 25.

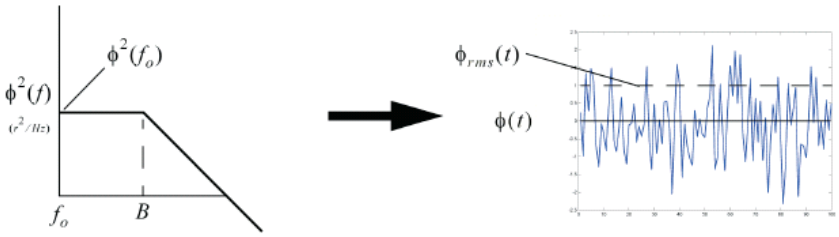

Figure 32. Synthesizer Phase Noise & Jitter

With this simplification the single sideband integrated VCO phase noise, Φ2 , in rads² at the phase detector is given by

$$\Phi SSB^2 = \left(\Phi^2(fo)B\frac{\pi}{2}\right) / N^2 \qquad \text{(Eq 6)}$$

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where

$\Phi^2_{SSB}(f0)$ is the single sideband phase noise in rads²/Hz inside the loop bandwidth, B is the 3 dB corner frequency of the closed loop PLL and N is the division ratio of the prescaler.

The rms phase jitter of the VCO in rads, Φ , results from the power sum of the two sidebands:

$$\Phi = \sqrt{2\Phi^2_{SSB}} \quad \text{(Eq 7)}$$

Since the simple integral of (EQ 6) is just a product of constants, the integral in the log domain can easily be done . For example if the VCO phase noise inside the loop is -100 dBc/Hz at 10 kHz offset and the loop bandwidth is 100 kHz, and the division ratio N=100, then the integrated single sideband phase noise at the phase detector in dB is given by Φ^2 dB = 10log ($\Phi^2(f_0)B\pi / N^2$) = -100 + 50 + 5 - 40 = -85 dBrads, or equivalently $\Phi = 10^{-85/20}$ = 56 urads rms or 3.2 milli-degrees rms.

While the phase noise reduces by a factor of 20Log10(N) after division to the reference, the jitter is a constant.

The rms jitter from the phase noise is then given by T_{jnp} = Tref Φ / 2π

In this example if the reference was 50 MHz, T_{ref} = 20 nsec, and hence T_{jpn} = 178 femto-sec.

A normal 3 sigma peak-to-peak variation in the arrival time therefore would be

$$\pm 3 \cdot \sqrt{2} \cdot T_{jpn} = 0.756\ ps$$

If the synthesizer was in fractional mode, the fractional modulation of the VCO divider will dominate the jitter. The exact standard deviation of the divided VCO signal will vary based upon the modulator chosen, however a typical modulator will vary by about ±3 VCO periods, ±4 VCO periods, worst case.

If, for example, a nominal VCO at 5 GHz is divided by 100 to equal the reference at 50 MHz, then the worst case division ratios will vary by 100±4. Hence the peak variation in the arrival times caused by ΔΣ modulation of the fractional synthesizer at the reference will be

$$T_{j\Delta\Sigma pk} = \pm T_{vco} * (N_{max} - N_{min}) / 2 \quad \text{(Eq 8)}$$

In this example, $T_{j\Delta\Sigma pk}$ = ±200 ps (104-96)/2 = ±800 psec. If it is assumed that the distribution of the delta sigma modulation is approximately Gaussian, $T_{j\Delta\Sigma pk}$ could be approximated as a 3 sigma jitter, and hence the rms jitter of the ΔΣ modulator could be estimated as ~ 1/3 of $T_{j\Delta\Sigma pk}$ or ~ 267 psec in this example.

Hence the total rms jitter T_j, expected from the delta sigma modulation plus the phase noise of the VCO would be given by the rms sum , where

$$T_j = \sqrt{T^2_{jpn} + \left(\frac{T_{j\Delta\Sigma pk}}{3}\right)^2} \quad \text{(Eq 9)}$$

It is apparent that the jitter from (EQ. 9) at the phase detector is dominated by the fractional modulation. In general, ~t ±0.8 nsec of normal variation in the phase detector arrival times has to be expected when in fractional mode. In addition, lower VCO frequencies with high reference frequencies will have much larger variations. For example, a 1 GHz VCO operating at near the minimum nominal divider ratio of 36, would, according to (EQ 8), exhibit about ±4 nsec of peak variation at the phase detector, under normal operation. The lock detect circuit must not confuse this modulation as being out of lock.

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HMC984LP4E Lock Detect Circuits

HMC984LP4E includes two lock detect circuits.

- Legacy Lock Detect Function
- Phase Measurement Based Lock Detect Function

Reg 01h[6:8] enables the lock detect functions of the HMC984LP4E. The LD output is available either from the GPO pin D0 or through SPI register Reg 12h.

Legacy Lock Detect Function

The Lock Detect circuit in the HMC984LP4E places a one shot window around the reference. The one shot window may be generated by either an analog one shot circuit or a digital one shot based upon an internal ring oscillator timer. Clearing LKDOS One Shot Select (Reg 07h[22]=0) will result in a nominal ±10 nsec 'analog' window of fixed length, as shown in Figure 9. Setting this bit to 1 will result in a variable length 'digital' widow. The digital one shot window is controlled by LKDOS Ring Oscillator Speed (Reg 07h[20:19]). The resulting lock detect window period is then generated by the number of ring oscillator periods defined in LKDOS One Shot Pulse Width (Reg 07h[18:16]). The lock detect ring oscillator may be observed on the GPO port by setting Reg 07h[21] =1 and configuring the Reg 08h[7:0] = C1h in (GPO). Lock detect does not function when this test mode is enabled.

LKDOS OK Count (Reg 07h[15:0]) defines the number of consecutive counts of the VCO that must land inside the lock detect window to declare lock. If for example LKDOS OK Count = 1000 , then the VCO arrival would have to occur inside the selected lock window 1000 times in a row to be declared locked. When locked the Lock Detect flag (Reg 12h[2]=1) is set, Reg 12h is a read only register. A single occurrence outside of the window will result in clearing the Lock Detect flag.

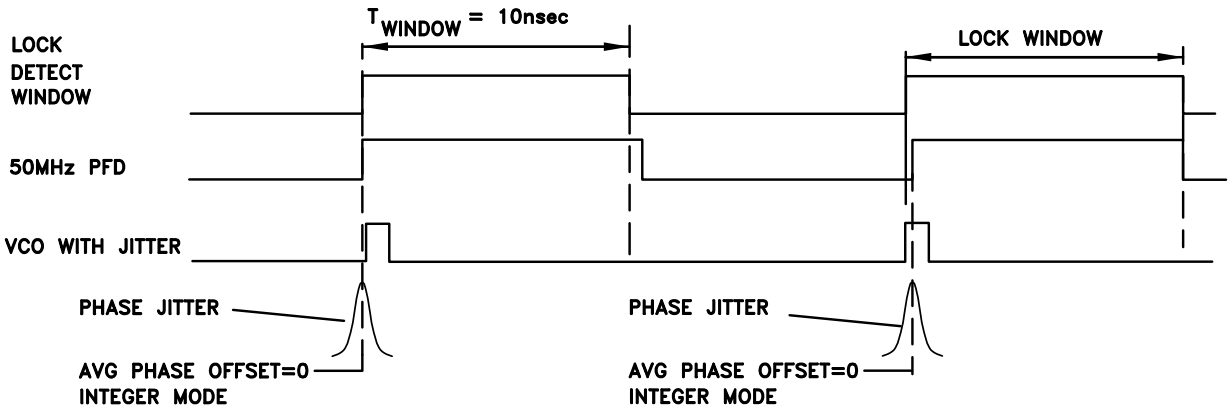

Figure 33. Normal Lock Detect Window - Integer Mode, Zero Offset

Lock Detect with Phase Offset

When operating in fractional mode the linearity of the phase detector and charge pump is more critical than in integer mode. The phase detector linearity deteriorates when operating with zero phase offset. Hence in fractional mode it is necessary to offset the phase of the reference and the VCO at the phase detector. In such a case, for example with an offset delay, the mean phase of the VCO will always occur after the reference, as shown in Figure 10. The lock detect circuit window can be made more selective with a fixed offset delay by setting Reg 05h [0]=1 and Reg 05h[1]=1. The offset can be assigned in advance of the reference by setting Reg 05h[1]=0 and Reg 05h [0]=1.

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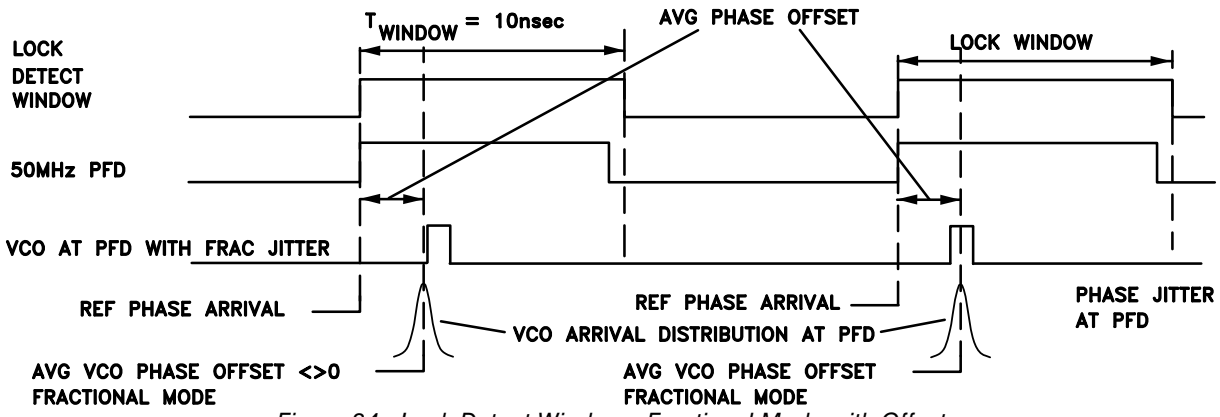

Figure 34. Lock Detect Window - Fractional Mode with Offset

Lock Detect with Phase Measurement

Lock Detect with Phase Measurement is based on phase error measurement at the PFD output. The phase error measurement is done in terms of the reference period at the PFD input. The period of the reference is first measured with a delay line and this count is available in read-only register Reg 10h. The phase error at the output of the PFD is then measured with the same delay line and this count is available in the read-only register Reg 11h. When the PLL is not locked, the measured phase error count will vary every time the Reg 11h is read and will become a stable value once PLL is locked. The phase error count will then be proportional to the static phase error at the PFD output. For example, assuming that PLL is locked, if the reference duration count is 150 in Reg 10h and Reg 11h reads 35 then the approximate static phase error at the PFD output is 20*(35/150) = 4.7 ns assuming a 20 ns reference period or Fpfd of 50 MHz. Reg 06h [13:0] defines the low and high thresholds for current phase error count. Reg 06h[23:14] defines the number of reference cycles that the phase error has to be within the thresholds before the lock is declared. For example, if the low threshold is set to Reg 06h [6:0] = 20d and high threshold is set to Reg 06h [13:7] = 50d and the LD OK Count is set to Reg 06h[23:14] = 512d, then the phase error count has to be between 20 and 50 for 512 consecutive reference cycles before that lock is declared. The thresholds make it easier to define lock condition in case of fractional operation where the static phase error is expected to be larger due to charge pump offset currents.

Chip Address Pins

HMC984LP4E has three programmable chip address bits, which enable the HMC984LP4E to be used in an SPI bus configuration. Two LSB chip address bits are internal and bond wire programmable at the time of packaging. The MSB bit is available externally as pin CHIP3. The chip address pins are read at power-up and every time the chip is reset. By default, all CHIP3 is internally pulled to DVDD thus there is no need to connect the pin to DVDD if the address bit is to be set as logic high. To assign a 0 to address bit, pin should be connected to ground. The internal CHIP1 and CHIP2 bits are internally tied to ground.

The chip address for the companion chip HMC983LP5E is stored in Reg 09h[2:0] of HMC984LP4E. In cases when an SPI command is common to both devices, it is not necessary to send separate commands to each part. Both parts are always listening to the SPI bus and when a common command is issued, they will take the command and update the corresponding registers. Writing its own chip address to the companion chip address register Reg 09h[2:0] will disable this feature.

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General Purpose Input Output Pin D0

HMC984LP4E has one GPIO pin D0. This pin normally functions as the output for the lock detect. It can be programmed to test and probe several internal signals. Following signals are available (Reg 08h[3:0]).

1. gpo_test_out.
2. Lock Detect or Lock Indicator output
3. PFD UP output going to Lock Detect
4. PFD DN output going to Lock Detect
5. R-Divider output to digital
6. R-Divider output
7. Saturation reset Signal
8. PFD saturation DN (VCO) output
9. PFD saturation UP (REF) output
10. Ring oscillator test output
11. One-shot pulse output
12. One-shot trigger output
13. Pull UP hard
14. Pull down hard
15. VCO divider output to digital
16. Crystal oscillator buffer output

See the serial port section for programming configuration, Reg 08h.

Serial Port Interface

The HMC984LP4E features a four wire serial port for simple communication with the host controller. Typical serial port operation can be run with SCK at speeds up to 30 MHz.

The details of SPI access for the HMC984LP4E are provided in the following sections. Note that the READ operation below is always preceded by a WRITE operation to Register 0 to define the register to be queried. Also note that every READ cycle is also a WRITE cycle in that data sent to the SPI while reading the data will also be stored by the HMC984LP4E when SEN goes high. If this is not desired then it is suggested to write to Reg 00h during the READ operation so that the status of the device will be unaffected.

Power on Reset and Soft Reset

The HMC984LP4E has a built in Power On Reset (POR) and a serial port accessible Soft Reset (SR). POR is accomplished when power is cycled for the HMC984LP4E while SR is accomplished via the SPI by writing Reg 00h = 80h, followed by writing Reg 00h = 00h. All chip registers will be reset to default states approximately 250 us after power up.

Serial Port WRITE Operation

The host changes the data on the falling edge of SCK and the HMC984LP4E reads the data on the rising edge.

A typical WRITE cycle is shown in Figure 1. It is 40 clock cycles long.

1. The host both asserts SEN (active low Serial Port Enable) and places the MSB of the data on SDI followed by a rising edge on SCK.
2. HMC984LP4E reads data on SDI (the MSB) on the 1st rising edge of SCK after SEN.

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3. HMC984LP4E registers the data bits, D29:D0, in the next 29 rising edges of SCK (total of 30 data bits).
4. Host places the 7 register address bits, A6:A0, on the next 7 falling edges of SCK (MSB to LSB) while the HMC984LP4E reads the address bits on the corresponding rising edge of SCK.
5. Host places the 3 chip address bits, CA2:CA0=[110], on the next 3 falling edges of SCK (MSB to LSB). Note the HMC984LP4E chip address is fixed as "4d" or "100b".
6. SEN goes from low to high after the 40th rising edge of SCK. This completes the WRITE cycle.
7. HMC984LP4E also exports data back on the SDO line. For details see the section on READ operation.

Serial Port READ Operation

The SPI can read from the internal registers in the chip. The data is available on SDO pin. This pin itself is tri-stated when the device is not being addressed. However, when the device is active and has been addressed by the SPI master, the HMC984LP4E controls the SDO pin and exports data on this pin during the next SPI cycle.

HMC984LP4E changes the data to the host on the rising edge of SCK and the host reads the data from HMC984LP4E on the falling edge.

A typical READ cycle is shown in Figure 1. Read cycle is 40 clock cycles long. To specifically read a register, **the address of that register must be written to dedicated** Reg 00h. This requires two full cycles, one to write the required address, and a 2nd to retrieve the data. A read cycle can then be initiated as follows;

1. The host asserts SEN (active low Serial Port Enable) followed by a rising edge SCK.
2. HMC984LP4E reads SDI (the MSB) on the 1st rising edge of SCK after SEN.
3. HMC984LP4E registers the data bits in the next 29 rising edges of SCK (total of 30 data bits). **The LSBs of the data bits represent the address of the register that is intended to be read.**
4. Host places the 7 register address bits on the next 7 falling edges of SCK (MSB to LSB) while the HMC984LP4E reads the address bits on the corresponding rising edge of SCK. **For a read operation this is "0000000".**
5. Host places the 3 chip address bits [100] on the next 3 falling edges of SCK (MSB to LSB). Note the HMC984LP4E chip address is fixed as "4d" or "100b".
6. SEN goes from low to high after the 40th rising edge of SCK. This completes the first portion of the READ cycle.
7. The host asserts SEN (active low Serial Port Enable) followed by a rising edge SCK.
8. HMC984LP4E places the 30 data bits, 7 address bits, and 3 chip id bits, on the SDO, on each rising edge of the SCK, commencing with the first rising edge beginning with MSB.
9. The host de-asserts SEN (i.e. sets SEN high) after reading the 40 bits from the SDO output. The 40 bits consists of 30 data bits, 7 address bits, and the 3 chip id bits. This completes the read cycle.

   Note that the data sent to the SPI by the host during this portion of the READ operation is stored in the SPI when SEN is de-asserted. This can potentially change the state of the HMC984LP4E. If this is undesired it is recommended that during the second phase of the READ operation that Reg 00h is addressed with either the same address or the address of another register to be read during the next cycle.

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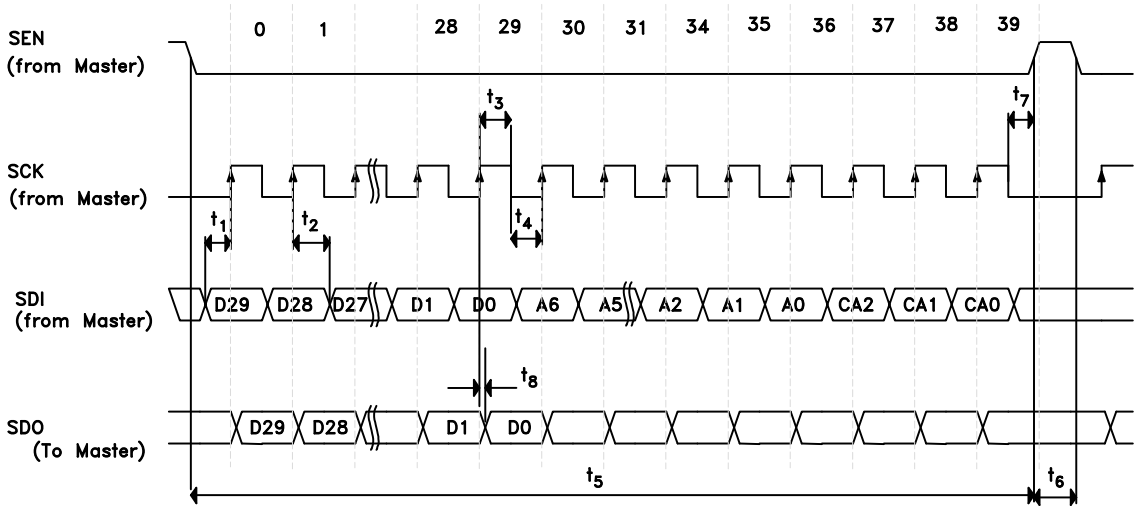

Figure 35. SPI Timing Diagram

DVDD = 5 V ±10%, GND = 0 V

Table 4. Main SPI Timing Characteristics

Parameter	Conditions	Min	Typ	Max	Units
t_1	SDI to SCK Setup Time	8			nsec
t_2	SDI to SCK Hold Time	8			nsec
t_3	SCK High Duration [1]	10			nsec
t_4	SCK Low Duration	10			nsec
t_5	SEN Low Duration	20			nsec
t_6	SEN High Duration	20			nsec
t_7	SCK to SEN [2]	8			nsec
t_8	SCK to SDO out [3]			8	nsec

[1] The SPI is relatively insensitive to the duty cycle of SCK.
[2] SEN must rise after the 32nd falling edge of SCK but before the next rising SCK edge. If SCK is shared amongst several devices this timing must be respected.
[3] Typical load to SDO is 10 pF, maximum 20 pF

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Register Map

Table 5. Reg 00h Chip ID, Soft Reset, Read Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[6:0]	R/W	Read Address Register	7	0	Address of the register to be read in the next cycle.
[7]	R/W	Soft Reset	1	0	Soft Reset. Writing 1 generates soft reset. Resets all the digital and registers to default states. Writing 0 resumes normal chip operation.
[31:8]	R/W	Chid ID	24	97331h	Part Number, Description. Read reg00h returns chip ID.

Table 6. Reg 01h Enable Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[0]	R/W	Use SPI Chip Enable	1	0	0 = Use CEN pin for chip enable. 1 = Ignore CEN pin and use SPI chip_en bit.
[1]	R/W	SPI CE	1	1	Chip enable from SPI = 1 allows chip control through SPI software.
[2]	R/W	R Divider Enable	1	1	Enable Reference Divider enabled
[3]	R/W	PFD Enable	1	1	1 = PFD enabled 0 = PFD disabled
[4]	R/W	CSP Enable	1	1	Enable cycle-slip prevention.
[5]	R/W	Charge Pump Enable	1	1	Enable Charge Pump.
[6]	R/W	Lock Detect Enable	1	1	Main Lock Detect enable
[7]	R/W	Lock Detect Watch Dog Enable	1	1	Lock Detected Watch Dog. Declares unlock if no UP/DN pulses are received from PFD.
[8]	R/W	One Shot Lock Detect Enable	1	1	Legacy Lock Detect enable.
[9]	R/W	GPO Enable	1	1	1 = GPIO output enable, D0 pin is output. 0 = D0 pin configured as input.
[10]	R/W	Reference Buffer Enable	1	1	Enable Reference Buffer.
[11]	R/W	Test Clocks Enable	1	1	Enable test clocks to digital (Xtal, Rdiv, Vdiv).
[12]	R/W	Bias Enable	1	1	Enables the bias currents to the analog blocks.
[13]	R/W	CSP Output Enable	1	1	Enables the output pad for
[14]	R/W	CP OP-AMP Enable	1	1	Enables the charge pump operational amplifier.
[17:15]	R/W	Unused bits	3	111b	
[18]	R/W	VCO Input Test Clock Enable	1	0	Enable for VCO/Divider input test clock.
[19]	R/W	Unused bit	4	0	

Table 7. Reg 02h REFDIV Reference Divider Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[13:0]	R/W	R-Divider Ratio	14	1	Reference Divider Division Ratio R. Minimum = 1, Maximum = 16383d.

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Table 8. Reg 03h PFD Settings Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[2:0]	R/W	CSP Reset Delay	3	100b	The number of reference clock cycles after which the saturation detection is reset.
[3]	R/W	CSP Auto Disable	1	1	When 1, PD saturation is disabled when Lock Detect becomes 1.
[4]	R/W	PD Phase Swap	1	0	Swap PD inputs when 1.
[5]	R/W	PD Short Mode Enable	1	0	1 = Apply reference to both PFD inputs when pfd_swap_phase Reg08h[4]= 0 or applies Divider output to both PFD inputs when pfd_swap_phase Reg08h[4] = 1.
[6]	R/W	PD Up Enable	1	1	1 = Enable UP output from PD. 0 = Disable UP output from PD.
[7]	R/W	PD Down Enable	1	1	1 = Enable DN output from PD. 0 = Disable DN output from PD.
[8]	R/W	PD Force Up	1	0	1 = Forces UP output from the PD to stay continuously on. 0 = Normal UP operation.
[9]	R/W	PD Force Down	1	0	1 = Forces DN output from the PD to stay continuously on. 0 = Normal DN operation.
[10]	R/W	PD Outputs to LD Enable	1	1	1 Enables PD outputs to Lock Detect in the Digital.
[11]	R/W	Reset PD when Xtal Gate	1	1	1 resets the PD when crystal is exported to the companion Prescaler/Sigma Delta chip HMC983LP5E

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Table 9. Reg 04h Charge Pump Settings Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[6:0]	R/W	Up Current	7	0x7h	Charge Pump DOWN MAIN current, 20 µA step, 127 steps 0000000 = Tristate if PFD also disabled. 0000001 = 20 µA 0000010 = 40 µA ... 1111111 = 2.54 mA
[13:7]	R/W	Down Current	7	0x7h	Charge Pump UP MAIN current, 20 µA step, 127 steps 000 = Tristate if PFD also disabled. 0000001 = 20 µA 0000010 = 40 µA ... 1111111 = 2.54 mA
[20:14]	R/W	Offset Current	7	0x7h	Charge Pump offset current magnitude, 5 µA step, 127 steps 0000000 = Tristate if PFD also disabled. 0000001 = 5 µA 0000010 = 10 µA ... 1111111 = 635 µA
[21]	R/W	Up Offset Current Enable	1	0	Enable for Charge pump offset current in up direction. Reference signal is lagging when phase swap is 0.
[22]	R/W	Down Offset Current Enable	1	0	Enable for Charge pump offset current in down direction, VCO/Divider is lagging when phase swap is 0.
[23]	R/W	High Gain Mode Enable	1	0	Enables high gain mode for the charge pump with uncontrolled 1 mA - 3.5 mA of additional charge pump current.
[25:24]	R/W	OP-Amp Bias	2	11b	Charge Pump Op-Amp bias select. 00 = 540 µA 01 = 689 µA 10 = 943 µA 11 = 1503 µA
[26]	R/W	CP Force Up Enable	1	0	Force Up current from the charge pump output.
[27]	R/W	CP Force Down Enable	1	0	Force Down current from the charge pump output.
[28]	R/W	CP Force Mid Rail Enable	1	0	Force the charge pump output to mid rail voltage. cp_force_up (Reg09h[26]) or cp_force_dn (Reg09h[27]) have precedence over this bit.
[29]	R/W	Ring Oscillator Output to CP Enable	1	0	Exports ring oscillator to pulluphard/pulldnhard for test purpose.

Table 10. Reg 05h LKD_FLXCPGAIN (Lock Detect) Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[0]	R/W	LD Asymmetric Window Enable	1	0	Enable asymmetric window for Lock Detect.
[1]	R/W	LD Asymmetric Direction Select	1	0	0 = Reference is expected first. 1 = VCO/Divider is expected first.
[2]	R/W	Reference Edge for LD Select	1	0	0 = Use falling edge. 1 = Use rising edge.
[4:3]	R/W	Flex CP Mode Select	2	00b	Forces UP or DN if phase error exceeds the register value. 00 = Disabled 01 = Force when phase error > 1 ns. 10 = Force when phase error > 3 ns. 11 = Force when phase error > 5 ns.

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Table 11. Reg 06h LKDOS (Lock Detect) Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[6:0]	R/W	LD High Threshold Duration	7	7Fh	High threshold for measuring PFD pulse width.
[13:7]	R/W	LD Low Threshold Duration	7	0x00	Low threshold for measuring PFD pulse width.
[23:14]	R/W	LD OK Count Threshold	10	200h	Number of consecutive counts within the time window to declare lock. "Theory of Operation" on page 14

Table 12. Reg 07h LKDOS (Legacy Lock Detect) Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[15:0]	R/W	LKDOS OK Count	16	0x1000 4096d	Number of consecutive counts within the time window to declare lock. "Legacy Lock Detect Function" on page 24
[18:16]	R/W	LKD One Shot Pulse Width	3	100b	
[20:19]	R/W	LKDOS Ring Oscillator Speed	2	00b	Set ring oscillator speed or frequency. 00 = fastest. 11 = slowest.
[21]	R/W	LKDOS Ring Oscillator Mode	1	0	1 = Force ring oscillator for test. 0 = Normal operation.
[22]	R/W	LKDOS One Shot Select	1	1	1 = Select digital one-shot. 0 = Select analog one-shot.

Table 13. Reg 08h GPIO Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[3:0]	R/W	GPO Output Signal Select	4	0000b	Select signal to be probed on the GPIO output pin. 0000 = gpo_test. 0001 = Locked. 0010 = PFD UP output to LKD. 0011 = PFD dn output to LKD. 0100 = R-Divider output to digital. 0101 = R-Divider output. 0110 = PFD saturation reset. 0111 = PFD saturation DN (VCO) output. 1000 = PFD saturation UP (REF) output. 1001 = Ring oscillator test output. 1010 = One-shot pulse output. 1011 = One-shot trigger output. 1100 = Pull up hard. 1101 = Pull down hard. 1110 = VCO divider output to digital. 1111 = Crystal oscillator buffer output.
[5:4]	R/W	GPO Static Test Value	2	00b	Static test values for GPIO.
[7:6]	R/W	GPO Output Enable	2	11b	Only LSB is used. 1 = Enable GPIO output. 0 = Configure GPIO as input.

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Table 14. Reg 09h REFDIVSET (Reference Divider Settings) Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[2:0]	R/W	HMC983LP5E Chip Address	3	001	Chip address of the Prescaler/Divider HMC983LP5E. When a new REFDIV value is selected through the SPI, either of the two chips will take the same command. This makes it unnecessary to issue two separate WRITE cycles to change the REFDIV value. To disable this feature, write the chip address of the HMC984LP4E itself so that it will not listen to the command issued to the other chip. See "Chip Address Pins" on page 25 for more information.
[3]	R/W	Force R-Divider to Bypass	1	0	1 = Force REFDIV bypass when RDIV is not equal to 1.

Table 15. Reg 0Ah Spare Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[9:0]	R/W	Not used	10	3FFh	
[10]	R/W	XtalDisSat	1	0	Disables saturation protection on reference (Xtal) buffer.
[11]	R/W	XtalHighFreq	1	0	Extends bandwidth of the reference buffer.

Table 16. Reg 10h MEAS_REF Read Only Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[19:0]	R	Measured Reference Duration	20	0	Measured duration of the reference period for Lock Detect calibration.
[20]	R	Reference Measure Overflow Flag	1	0	REF measurement overflow flag.

Table 17. Reg 11h MEAS_PFD Read Only Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[19:0]	R	Measured Phase Error	20	0	Measured duration of the PFD. Sign is available in Reg 12h, bit 0.
[20]	R	Phase Error Overflow Flag	1	0	PFD pulse measurement overflow flag.

Table 18. Reg 12h STATUS Read Only Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[0]	R	Phase Error Sign	1	0	Sign of PFD duration
[1]	R	LD Output from Phase Error Measurement	1	0	Lock Detect result from pulse duration based Lock Detect circuit.
[2]	R	LD Output from Legacy Lock Detect	1	0	Lock Detect result from legacy one-shot Lock Detect circuit.

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