

# HI-8200, HI-8201, HI-8202 Quad 10 Ohm +/-12V outside-the-rails

November 2017

Analog Switch with Open Circuit when Power Off

# **GENERAL DESCRIPTION**

The HI-8200 is a quad analog CMOS switch fabricated with Silicon-on-Insulator (SOI) technology for latch-up free operation and maximum switch isolation. High voltage gate drive is entirely created on-chip enabling +/-12V switching range from a single 3.3V or 5V supply. These switches are ideally suited for applications demanding low switch leakage when the power pins are 0V.

At 25°C and with VDD from 3.0V to 5.5V, the switch resistance (RON) is typically  $8\Omega$ . RON is independent of VDD. In a switching range of -5V to +5V, the maximum deviation of RON from flat is less than 5%.

These switches conduct equally well in either direction. Power down and Off state leakages are less than 10nA maximum. Charge injection is less than 10pC. Switching times are typically 180ns to the On state and 60ns to the Off state. The onboard charge pump allows an On/Off cycle time of 5KHz for all four switches simultaneously before the switching range becomes restricted.

The HI-8200 provides four each normally open switches when the switch control inputs are low. The HI-8201 provides four each normally closed switches when the switch control inputs are low. The HI-8202 provides a combination of two normally closed and two normally open switches.

Industry-standard plastic package options include 20-pin TSSOP, 16-pin DIP and 16-pin QFN. Ceramic packaging is available on request. All three products are offered in both industrial (-40°C to +85°C) and extended (-55°C to +125°C) temperature range options.

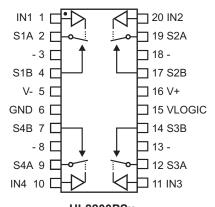
## **APPLICATIONS**

- Avionics
- Data bus isolation
- Sample-and-Hold circuits
- Test Equipment
- Communications Systems

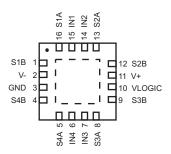
## **FEATURES**

- CMOS analog switches with up to +/-12V switching range from a single 3.3V or 5V supply
- Low RON: 10Ω max at 25°C
- Robust CMOS Silicon-on-Insulator (SOI) technology
- · Switch nodes are open-circuit when chip is powered down
- SOI switch isolation with 1nA typical Off leakage
- ESD protection > 4KV HBM
- · Fast switching time with break-before-make
- Low power
- Extended Temperature Range (-55°C to +125°C)

## PIN CONFIGURATIONS (Top Views)



HI-8200PSx 20-Pin TSSOP package



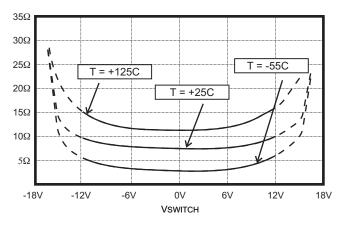
HI-8200PCx 16-pin 5mm x 5mm Chip-scale package (see page 6 for additional package configurations)

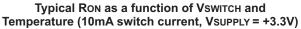
PRODUCT OPTIONS								
PART TYPE	IN1	Switch 1	IN2	Switch 2	IN3	Switch 3	IN4	Switch 4
HI-8200	0	Open	0	Open	0	Open	0	Open
	1	Closed	1	Closed	1	Closed	1	Closed
HI-8201	0	Closed	0	Closed	0	Closed	0	Closed
	1	Open	1	Open	1	Open	1	Open
HI-8202	0	Open	0	Closed	0	Closed	0	Open
	1	Closed	1	Open	1	Open	1	Closed

SIGNAL	FUNCTION	DESCRIPTION			
IN1	Logic Input	HI-8200 and HI-8202 are normally Open when input Low			
S1A	Switch Node	Switch 1 Node			
S1B	Switch Node	Switch 1 Node			
V-	CAP -	Bulk storage capacitor. Add 0.1uF ceramic capacitor to GND. (20V or higher).			
GND	Supply	Reference Ground			
S4B	Switch Node	Switch 4 Node			
S4A	Switch Node	Switch 4 Node			
IN4	Logic Input	HI-8200 and HI-8202 are normally Open when input Low			
IN3	Logic Input	HI-8201 and HI-8202 are normally Closed when input Low			
S3A	Switch Node	Switch 3 Node			
S3B	Switch Node	Switch 3 Node			
VLOGIC	Supply	3.3V or 5.0V Logic supply			
V+	CAP +	Bulk storage capacitor. Add 0.1uF ceramic capacitor to GND. (20V or higher).			
S2B	Switch Node	Switch 2 Node			
S2A	Switch Node	Switch 2 Node			
IN2	Logic input	HI-8201 and HI-8202 are normally Closed when input Low			

## **PIN DESCRIPTIONS**

**NOTE:** V+ and V- pins are **only** to be used for connection of bulk storage capacitors and **MUST NOT** be loaded.





## **ABSOLUTE MAXIMUM RATINGS**

(Voltages referenced to GND = 0V)

Supply Voltage, VLOGIC     7.0V       Switch Current (either direction, DC):     20mA       Peak Switch Current (1 ms pulse, 10% duty cycle max.)     100mA       Digital Input Voltage (IN1-4):     -0.3V to VLOGIC + 0.3V	SO Package (derate 6.7mW/°C above 70°C)696mW Plastic DIP (derate 10.53 mw/°C above 70°C)842mW
Operating Temperature Range: (Industrial)40°C to +85°C	Storage Temperature Range:65°C to +150°C
(Hi-Temp)55°C to +125°C Maximum Junction Temperature	Soldering Temperature: (Ceramic)60 sec. at +300°C (Plastic - leads)10 sec. at +280°C

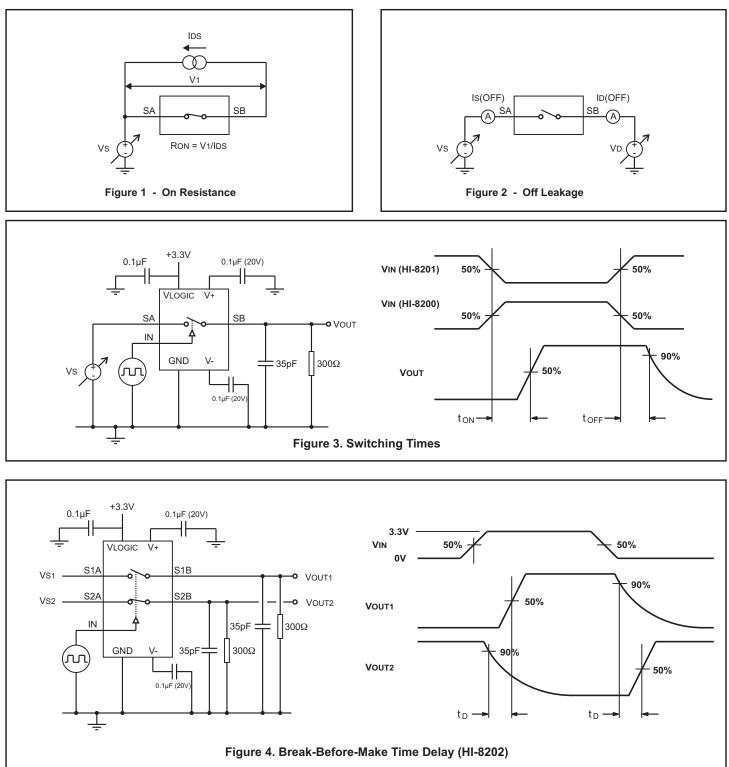
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## **ELECTRICAL CHARACTERISTICS**

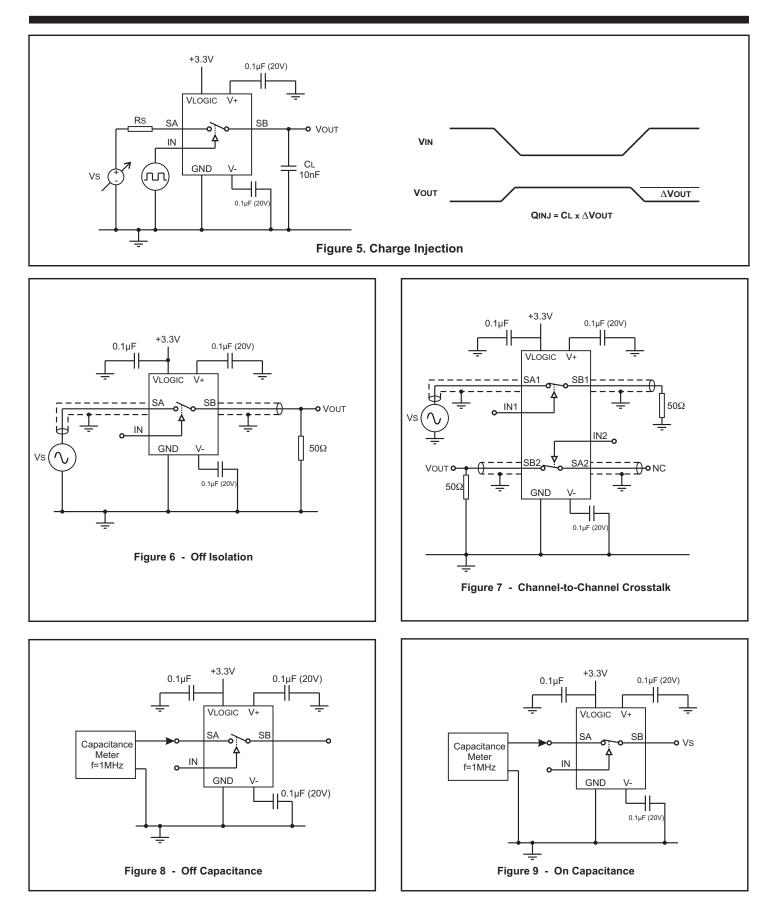
VLOGIC = 3.3V or 5.0V, GND = 0V. Operating temperature range (unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS	FIGURE	MIN	ТҮР	MAX	UNIT
SWITCH PARAMETERS							
Switch Resistance, 25°C, 10mA	Ron	12V > Vs > -12V	1	6	8	10	Ω
Leakage - (open circuit and power down)	ISWLEAK	12V > Vs > -12V	2		1	10	nA
Leakage - (open circuit and power on)	ISWLEAKp	12V > Vs > -12V	2		1	100	nA
LOGIC INPUTS							-
Input High Voltage	Vih			75%			V
Input Low Voltage	VIL					25%	V
Input Current	Ін	80K Ohm pulldown VLogic = 3.3V Vlogic = 5.0V			45 65	0.5	μΑ μΑ μΑ
SUPPLY	lı∟					0.5	μΑ
					1		
VLogic Operating Range	VDD			3.0		5.5	V
VLogic Operating Current	IDD	inputs static VLogic = 3.3V Vlogic = 5.0V				1.0 2.5	mA mA
DYNAMIC PARAMETERS							
Max Vin On/Off cycling	fcycle	any load				5	Khz
Turn On Time	Тол		3		180	250	ns
Turn Off time	Toff		3		80	150	ns
Break-Before-Make Time	TD		4	40	80		ns
Charge Injection	Q	Vs=0V, Rs=0Ω, 25°C	5		-20		рС
Off Isolation	RR	f = 1 MHz, 25°C	6		65		dB
Crosstalk	CR	f = 1 MHz, 25°C	7		90		dB
Capacitance	Coff Con	Switch Off, 25°C Switch On, 25°C	8 9		15 60		pF pF
Charge Pump Power On	Tvon	V+ and V- = +/-14.5V VLogic = 5.0V	10	10			ms
					1		

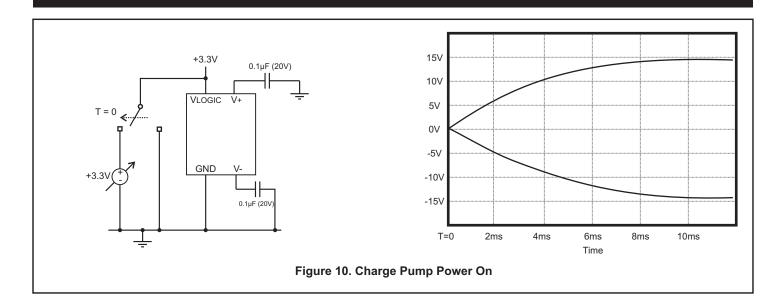
## **TEST CIRCUITS**



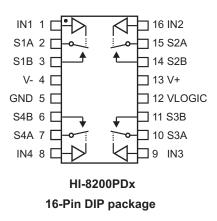
#### HI-8200, HI-8201, HI-8202



HOLT INTEGRATED CIRCUITS



## Additional package configurations



## **FREQUENCY RESPONSE**

Figure 11 shows a typical frequency response.

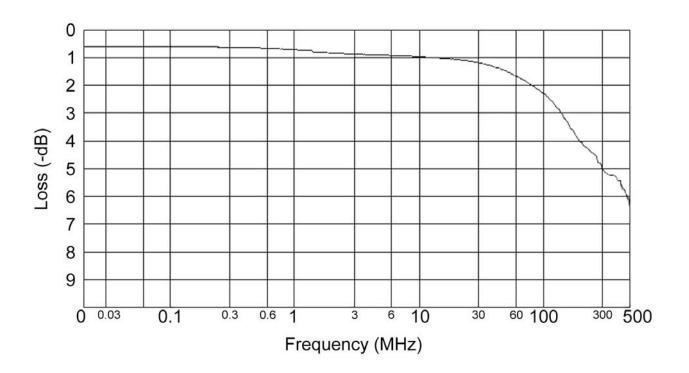


Figure 11. Frequency Response.

# **ORDERING INFORMATION**

# HI - <u>820x xx x x</u>

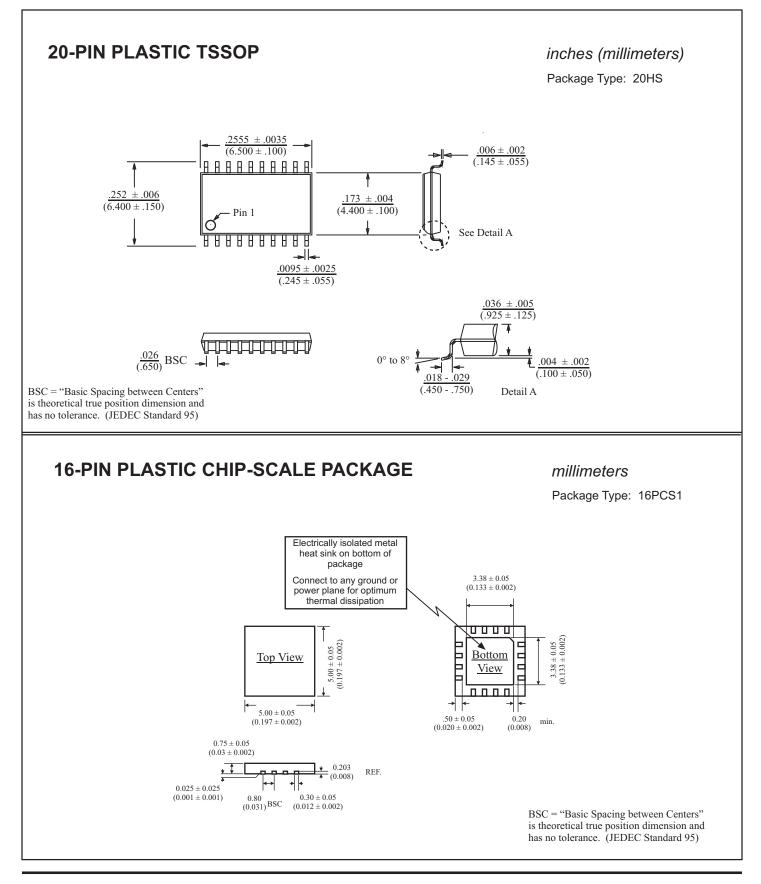
		PART NUMBER	LEAD FINISH						
Blank			Tin / Lead (Sn / Pb) Solder						
		F							
		PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	]			
		1	-40°C TO +85°C	1	NO	•			
		Т	-55°C TO +125°C	Т	NO				
		М	-55°C TO +125°C	М	YES				
1 1			PACKAGE DESCRIPTION						
		PART NUMBER							
			DESCRIPTION	5 mm CHI	P SCALE (1	6PCS1) (No M-flow, Pb-free only)			
		NUMBER	DESCRIPTION			6PCS1) (No M-flow, Pb-free only)			
		NUMBER   PC	DESCRIPTION         16 PIN PLASTIC 5 x 5	OP (20H		6PCS1) (No M-flow, Pb-free only)			
		NUMBER     PC     PS	DESCRIPTION     16 PIN PLASTIC 5 x 5     20 PIN PLASTIC TSS	OP (20H		6PCS1) (No M-flow, Pb-free only)			
		NUMBER     PC     PS     PD	DESCRIPTION       16 PIN PLASTIC 5 x 5       20 PIN PLASTIC TSS       16 PIN PLASTIC DIP	OP (20HS (16P)	5)	6PCS1) (No M-flow, Pb-free only)			
		NUMBER     PC     PS     PD	DESCRIPTION       16 PIN PLASTIC 5 x 5       20 PIN PLASTIC TSS       16 PIN PLASTIC DIP       FUNCTION	OP (20HS (16P) RMALLY C	S) DPEN	6PCS1) (No M-flow, Pb-free only)			

# **REVISION HISTORY**

Rev	Date	Description of Change
New	10/18/12	Initial Release
А	10/22/12	Remove 1MOhm resistor to GND from test circuits. Correct typo in Pin Descriptions
В	12/18/12	Clarify that V+/V- pins must not be loaded. Used only for connection of bulk storage caps.
С	04/18/16	Add leakage spec for power on condition.
D	11/07/17	Add frequency response curve.
	New A B C	New10/18/12A10/22/12B12/18/12C04/18/16



# **HI-8200 PACKAGE DIMENSIONS**





# **HI-8200 PACKAGE DIMENSIONS**

