ATCA-F125ATCA-F125 (6873M Artwork)

Installation and Use

P/N: 6806800J94K

August 2014

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EMBEDDED TECHNOLOGIES

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Contact Address

Artesyn Embedded Technologies
Marketing Communications
2900 S. Diablo Way, Suite 190
Tempe, Arizona 85282

Artesyn Embedded Technologies
Lilienthalstr. 17-19
85579 Neubiberg/Munich
Germany

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About this Manual

Overview of Contents

This manual is divided into the following chapters and appendices.

- *Introduction* gives an overview of the features of the product, standard compliances, mechanical data, and ordering information.
- *Hardware Preparation and Installation* outlines the installation requirements, hardware accessories, and installation procedures.
- *Controls, LEDs, and Connectors* describes external interfaces of the board. This include connectors, LEDs, and mechanical switches.
- *Functional Description* includes a block diagram and functional description of major components of the product.
- *U-Boot* describes the boot firmware.
- *Battery Exchange* contains the procedures for replacing the battery.
- *Related Documentation* provides a listing of related product documentation, manufacturer's documents, and industry standard specifications.
- *Safety Notes* summarizes the safety instructions in the manual.
- *Sicherheitshinweise* is a German translation of the Safety Notes chapter.

Abbreviations

This document uses the following abbreviations:

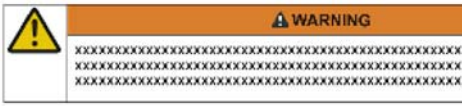
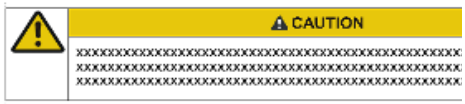
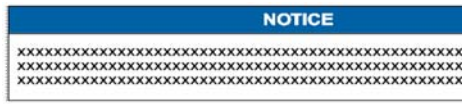
Abbreviation	Definition
ATCA	Advanced Telecom Computing Architecture
AMC	Advanced Mezzanine Card
IPMI	Intelligent Platform Management Interface
IPMC	Intelligent Platform Management Controller
JTAG	Joint Test Action Group

Abbreviation	Definition
PICMG	PCI Industrial Computer Manufacturers Group
POST	Power-on Self Test
PrAMC	Processor Advanced Mezzanine Card
RTM	Rear Transition Module

Conventions

The following table describes the conventions used throughout this manual.

Notation	Description
0x00000000	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
0b0000	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands in body text
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)

Notation	Description
|	Logical OR
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury
	Indicates a property damage message
	No danger encountered. Pay attention to important information

Summary of Changes

This manual has been revised and replaces all prior editions.

Part Number	Publication Date	Description
6806800J94A	December, 2009	First edition
6806800J94A	January, 2011	GA Release.
6806800J94A	June, 2011	Added Figure "Declaration of Conformity" on page 18. Edited Table "Faceplate LEDs" on page 43.
6806800J94B	March, 2012	Updated Chapter 4, *Functional Description, on page 61*, Chapter P, *EMC, on page 118*, and Chapter P, *Installation, on page 119*.

Part Number	Publication Date	Description
6806800J94C	August, 2012	Updated *Ordering Information* on page 18, Figure "Serial Number Locator" on page 20, Figure "Module Connectors Location" on page 54, and *Functional Description* on page 61
6806800J94D	December 2012	Updated *Standard Compliances* on page 16.
6806800J94E	October, 2013	Updated Table 2-2 on page 28.
6806800J94F	November, 2013	Updated title as ATCA-F125 (6873M Artwork) Table 1-3 on page 19, Table 2-1 on page 26.
6806800J94G	December, 2013	Replaced “Product Name Short” with ATCA-F125.
6806800J94H	January, 2014	Updated Table 3-3 on page 49.
6806800J94J	April, 2014	Re- branded to Artesyn template.
6806800J94K	August 2014	Removed instances of Stratum 3E and updated Declaration of Conformity.

1.1 Features

The ATCA-F125 is a hub board as defined *in PICMG 3.0 Revision 3.0 Advanced TCA Base Specification* and *PICMG 3.1 Revision 1.0 Specification Ethernet/Fiber Channel for AdvancedTCA Systems*. It supports several Base and Fabric Channel Ethernet interfaces to the Zone 2 backplane. It also supports 1 Gb and 10 Gb Ethernet uplinks to the front panel and to a Rear Transition Module (RTM) through the Zone 3 connector.

Broadcom Ethernet switches and PHYs are used for the base and fabric channels. The entire board is managed by a Freescale P2020 QorIQ Integrated Processor.

The ATCA-F125 has several optional features including a processor AMC, local storage and Telecom clocking.

See the list below for some of the key features of the ATCA-F125:

- Single slot ATCA form factor (280 mm x 322 mm)
- Freescale P2020 QorIQ Integrated Processor for the on board service processor functions
- Two DDR3 memory DIMM slots each of which can support up to 2 GB of DDR3 SDRAM with ECC
- 2 GB default configuration
- 2 GB embedded USB Flash module for User Flash memory
- Onboard SATA connector for an optional drive with selectable interface to either the service processor or the processor AMC
- Real time clock
- RJ-45 UART Console interface to service processor on front panel
- RJ-45 10/100/1000 BaseTx Ethernet Management port on the front panel for P2020 QorIQ Integrated Processor
- Single USB port on front panel for P2020 processor
- Broadcom BCM56334 managed switch device for the Base Channel to provide 24 ports of Gigabit Ethernet and four 10G XAUI ports with two 10G uplink channels on the front panel
- Broadcom BCM56820 managed switch device for the Fabric Channel to provide 24 10G XAUI ports and four 1G SGMII ports with two 10G uplink channels on the front panel

- Multiple 1 GbE SGMII and 10 GbE XAUI ports routed to Zone 3 connectors for base and fabric uplink channels on RTM
- Stratum 3 Telecom clock options with master/slave sync and five inter-shelf sync connectors on front panel along with 2 BITS/SSU front panel connectors
- Synchronous Ethernet support
- One AMC bay for application processor support
- IPMC functionality for the board management by the Shelf Management Controller

1.2 Standard Compliances

This blade, when installed in a compliant shelf, meets the following standards.:

Table 1-1 Standard Compliances

Standard	Description
UL/CSA No. 60950-1 EN 60950-1 IEC 60950-1 CB Scheme UL/CSA No. 60950-1	Legal safety requirements
ANSI T1.319-2002 NEBS GR-63-CORE	ANSI Fire Spread Criteria
AT&T Document ATT-TP-76200	Network Equipment Power, Grounding, Environmental, and Physical Design Requirements
ETSI Acoustic Noise ETS 300 753 Class 3.1	ETSI acoustic noise requirements
ETSI Stationary Use: EN 300 019-2-3 Class 3.1	ETSI stationary use requirements (temperature-controlled locations
ETSI Storage EN 300 019-2-1 Class 1.2	ETSI storage requirements in system level (not temperature- controlled storage locations)
ETSI Transportation: EN 300 019-2-2 Class 2.3	ETSI public transportation requirement on system level
Telcordia GR-1089	Ports and litra-building lightning for telecommunication port

Table 1-1 Standard Compliances (continued)

Standard	Description
Telcordia GR-1089-CORE	Electromagnetic Compatibility and Electrical Safety - Generic Criteria for Network Telecommunications Equipment
Telcordia GR-63-CORE	NEBS Requirements: Physical Protection
Telcordia SR-3580	NEBSCriteria Level 3
EN55022 Class A (EU) EN 55024 (EU) FCC 47 CFR Part 15 Subpart B (US), Class A AS/NZS CISPR 22 Class A (Australia/New Zealand) VCCI Class A (Japan)	EMC requirements (legal) on system level (predefined Artesyn Embedded Technologies system)
Verizon Document VZ.NEBS.TE.NPI.2004.015: NEBS Checklist	Telecommunications Carrier Group NEBS Checklist

To fulfill the requirements of Telcordia GR-1089,R4-14, use Shielded Twisted Pair (STP) cables grounded at both ends to connect to the Ethernet ports.

The product has been designed to meet the directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS) Directive 2011/65/EU.

Figure 1-1 Declaration of Conformity

EC Declaration of Conformity

According to EN 17050-1:2004

Manufacturer's Name:	Artesyn Embedded Technologies Embedded Computing
Manufacturer's Address:	Zhongshan General Carton Box Factory Co. Ltd. No 62, Qi Guan Road West, Shiqi District, 528400 Zhongshan City Guangdong, PRC

Declares that the following product, in accordance with the requirements of 2004/108/EC, 2006/95/EC, 2011/65/EU and their amending directives,

Product:	ATCA-F125 Series Switch Blade & RTM-ATCA-F125 Series
Model Name/Number:	ATCA-F125, ATCA-F125-14S, ATCA-F125-14S-C10, ATCA-F125-STD-01-L2, ATCA-F125-STD-02-L2, ATCA-F125-TCLK3, ATCA-F125-TCLK3-C01, RTM-ATCA-F125, RTM-ATCA-F125-C01, RTM-ATCA-F125-C10, RTM-ATCA-F125-STD-01

has been designed and manufactured to the following specifications:

EN55022:2006 (A1: 2007) Class A

EN55024: 1998 (A1: 2001 + A2: 2003)

ETSI EN 300 386 V1.5.1 (2010-10)

IEC 60950-1:2005 (2nd Edition), EN60950-1:2006+A11:2009

2011/65/EU RoHS Directive

As manufacturer we hereby declare that the product named above has been designed to comply with the relevant sections of the above referenced specifications. This product complies with the essential health and safety requirements of the above specified directives. We have an internal production control system that ensures compliance between the manufactured products and the technical documentation.

Tom Tuttle, Manager, Product Testing Services

08/28/2014
Date (MM/DD/YYYY)

CE

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1.3 Mechanical Data

The following table provides details about the blade's mechanical data, such as dimensions and weight.

Table 1-2 Mechanical Data

Data	Value
Dimensions	30 mm x 351 mm x 312 mm (8U form factor)
Weight	2.3 kg

1.4 Ordering Information

The following table lists the blade variants that were available as of the time of writing this manual. Consult your local Artesyn Embedded Technologies sales representative for the availability of further variants.

Table 1-3 Blade Variants - Ordering Information

Product Name	Description	PWB Artwork/Assembly No. (See NOTE)
ATCA-F125-14S	10G ATCA switch blade with (1) AMC site and optional SATA storage, ETH between CPU/Base interface	6873M / 0106873Mxxx
ATCA-F125	10G ATCA switch blade with one (1) AMC site and optional SATA storage	6859G / 0106859Gxxx
ATCA-F125-TCLK3	10G ATCA switch blade with one (1) AMC site, optional storage and telecom CLK Stratum 3	6873M / 0106873Mxxx

NOTE: This manual covers the ATCA-F125-14S product. It also covers ATCA-F125-TCLK3 product manufactured with 6873M PWB artwork.
For 6859G PWB artwork documentation, refer to *ATCA-F125 Installation & Use manual 6806800J94B*. The PWB artwork may be identified by the assembly number, which is marked near the serial number as shown in Figure 1-2 on page 21.

1.4.1 Blade Accessories

The following table lists the blade accessories that were available as of the time of writing this manual. Consult your local sales representative for the availability of further accessories.

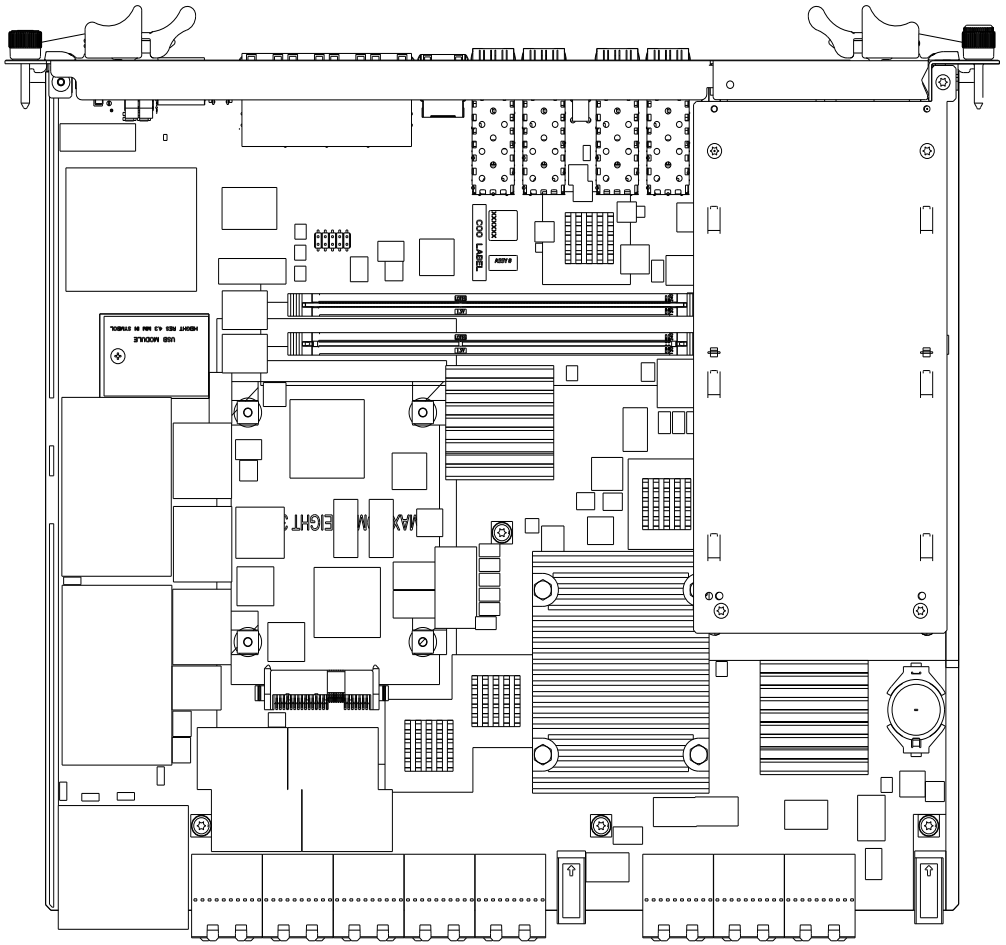
Table 1-4 Blade Accessories - Ordering Information

Accessory	Description
RTM-ATCA-F125	RTM for the ATCA-F125 with SFP and SFPP receptacles
SFP-MM-SX-LC	1G Single Form Factor (SFP) module - 850NM, SX, LC connector
SFP-CO-RJ-45	1G copper Single Form Factor (SFP) module - RJ-45 connector
SFPP-MM-SR-LC	10 G Single Form Factor Plus (SFPP) module - 850NM, SR, LC connector
SFPP-SM-LR-LC	10G Single Form Factor Plus (SFPP) module -1310NM, LR, LC connector
SFPP-CO-RJ-45-3M	10G copper Single Form Factor Plus (SFPP) modules with molded cable - 3M
CABLE-OPT-F102-5M	Optical cable for multi-mode, SFP and SFPP connections (5M)
PRAMC-7211	AMC CPU blade with Intel© Core2Duo 64B @ 1.5GHZ, 2G DDR2 & mid-size
SA-BBS-721X	PRAMC-721X, BBS only, BINARY RPMS, PNE 2.X, CD
SA-BBS-WR2X-721X	PrAMC-721x, BBS binary RPMs, Eval kernel+runtime, PNE LE 2.x, CD

1.5 Product Identification

The following graphic shows the location of the serial number label.

Figure 1-2 Serial Number Locater



2.1 Overview

This chapter provides the information that you need to install the ATCA-F125 and its accessories into your AdvancedTCA system. Removal procedures are also included.

To install the blade, follow these steps:

1. Unpack and inspect the blade.
2. Make sure that environmental, thermal, and power requirements are met.
3. If applicable, install the Rear Transition Module.
4. Configure the ATCA-F125.
5. Install the ATCA-F125.
6. If applicable, install the AMC module.
7. Configure the software.

2.2 Unpacking and Inspecting the Blade

NOTICE

Damage of Circuits

- Electrostatic discharge and incorrect installation and removal of the blade can damage circuits or shorten its life.
- Before touching the product make sure that you are working in an ESD-safe environment or wearing an ESD wrist strap or ESD shoes. Hold the product by its edges and do not touch any components or circuits.

Damage to blade/Backplane or System Components

- Bent pins or loose components can cause damage to the blade, the backplane, or other system components. Therefore, carefully inspect the blade and the backplane for both pin and component integrity before installation.

Shipment Inspection

1. Verify that you have received all items of your shipment:
   - Safety Notes Summary
   - ATCA-F125 blade
   - Any optional items ordered
2. Check for damage and report any damage or differences to customer service.

The blade is thoroughly inspected before shipment. If any damage occurs during transportation or any items are missing, please contact customer service immediately.

3. Remove the desiccant bag shipped together with the blade.

NOTICE

Environmental Damage

- Improper disposal of used products may harm the environment.
- Always dispose of used products according to your country's legislation and manufacturer's instructions.

2.3 Requirements

This section shows the environmental and power requirements of the ATCA-F125 (6873M Artwork).

2.3.1 Environmental Requirements

When operated in your particular system configuration, make sure that the blade meets the environmental requirements specified in this section.

Operating temperatures refer to the temperature of the air circulating around the blade, and not to component temperatures.

If you integrate the blade in your own non-Artesyn Embedded Technologies system, please contact your local sales representative for further safety information.

NOTICE

Blade Damage

- High humidity and condensation on the blade surface may cause it to short circuit.
- Do not operate the blade outside the specified environmental limits. Make sure the blade is completely dry and there is no moisture on any surface before applying power.
- Do not operate the blade below -5°C.

Table 2-1 Environmental Requirements

Requirement	Operating	Non-Operating
Temperature	Normal Operation: +5 °C (41 °F) to +40 °C (104 °F) according to Telcordia GR-63-CORE (NEBS) and ETSI EN 300 019-1-3, Class 3.1 Exceptional Operation: -5 °C (23 °F) to +55 °C (131 °F) according to Telcordia GR-63-CORE (NEBS) Note: this exceeds ETSI EN 300 019-1-3, Class 3.1E requirements (-5°C to +45°C)	-40 °C (-40 °F) to +70 °C (158 °F) according Telcordia GR-63-CORE (NEBS) and ETSI EN 300 019-1-2, Class 2.3 Note: This exceeds ETSI EN 300 019-1-1, Class 1.2 requirements (storage from -25°C to +55°C Note: This may be further limited by installed accessories
Temp. Change	+/- 0.25 °C/min according to Telcordia GR-63-CORE	+/- 0.25 °C/min
Relative Humidity	Normal Operation: 5%rH to 85%rh non-condensing Exceptional Operation: 5%rH to 90%rh non-condensing According to Telcordia GR-63-CORE (NEBS) and EN 300 019-1-3, Classes 3.1 and 3.1E	5%rH to 95%rH non-condensing According to Telcordia GR-63-CORE (NEBS) and EN 300 019-1-1, Classes 1.2 and 2.3
Vibration	1g from 5 to 200Hz and back to 5Hz at a rate of 0.25 octave/minute (according to Telcordia GR-63-core)	5-20 Hz at 0.01 g^2/Hz (according to Telcordia GR-63-core and ETSI EN 300 019-2-2) 20-200 Hz at -3 dB/octave Hz (according to Telcordia GR-63-core and ETSI EN 300 019-2-2) Random 5-20Hz at 1 m^2/s^3 Random 20-200Hz at 3 m^2/s^3
Shock	Half-sine, 11 ms at 30 m/s^2	Blade level packaging Half-sine, 6 ms at 180 m/s^2
Free Fall	-	1.2 m/ packaged (according to ETSI 300 019-2-2) 100 mm unpackaged (according to Telcordia GR-63-core)

2.3.2 Thermal Requirements

In order for the ATCA-F125 to cool properly when the operating temperature is at the maximum (55C), the chassis must meet or exceed CP-TA B.3 ATCA Chassis Specification. CP-TA B.4 compliance is preferred.

Contact your Artesyn Embedded Technologies sales representative for current information on the detailed thermal information including airflow and resistance of the blade.

NOTICE

System Overheating

- Cooling Vents
  - Improper cooling can lead to system damage and can void the manufacturer's warranty.
  - To ensure proper cooling and undisturbed airflow through the system, do not obstruct the ventilation openings of the system. Make sure that the fresh air supply is not mixed with hot exhaust from other devices.

⚠ CAUTION

Personal Injury

- During operation, hot surfaces may be present on the heat sinks and the components of the product.
- To prevent injury from hot surface, do not touch any of the exposed components or heatsinks on the product when handing. Use the handle and face plate, where applicable, or the board edge when removing the product from the enclosure.

2.3.3 Power Requirements

The blade's power requirements depend on the installed hardware accessories. To install the accessories on the blade, the load of the respective accessory has to be added to that of the blade. The following table show typical examples of the power requirements, with and without accessories installed. For information on the accessories' power requirements, refer to the documentation delivered together with the respective accessory or consult your local Artesyn Embedded Technologies representative for further details.

The blade must be connected to a TNV-2 or a safety-extra-low-voltage (SELV) circuit. A TNV-2 circuit is a circuit whose normal operating voltages exceed the limits for a SELV circuit under normal operating conditions, and which is not subject to overvoltages from telecommunication networks.

Table 2-2 Power Requirements

Characteristic	Value
Rated Voltage Exception in the US and Canada	-48 VDC to -60 VDC, US and -48 VDC, Canada
Operating Voltage Exception in the US and Canada	-39 VDC to -72 VDC, US and -39 VDC to -60 VDC, Canada
Max. power consumption of ATCA-F125 with SATA drive and RTM-ATCA-F125	125 W (98 W typical)
Max. power consumption of ATCA-F125 with SATA drive (without RTM-ATCA-F125)	105 W (80 W typical)

2.4 Rear Transition Modules

If applicable, install a rear transition module. For more information, refer the RTM-ATCA-F125 documents listed in Appendix B, *Related Documentation*.

The RTMs are not hot-swappable. Before installation, make sure that no front blade is installed in its respective slot, or that the front blade is powered-down. For further details about the RTM installation, refer to the installation and use guide of the respective RTM.

NOTICE

Damage of the Product and Additional Devices and Modules

- Incorrect installation or removal of additional devices or modules damages the product or the additional devices or modules.
- Before installing or removing additional devices or modules, read the respective documentation and use appropriate tools.

2.5 Blade Configuration

There are no configuration switch settings for normal operational mode. Switch changes are for activating various debug modes. Setting any switched to the ON state may cause unpredictable operation.

NOTICE

Product Malfunction

- Switches marked as “reserved” may carry production-related functions and can cause the product to malfunction if the setting is changed.
- Do not change settings of switches marked as “reserved”.

Product Damage

- Setting/resetting the switches during operation can cause damage to the product.
- Check and change switch settings before installing the product.

Product Damage

- Too much force may damage the reset switch.
- Use minimal force when pressing the reset switch.

2.5.1 SATA Drive Installation

An optional SATA drive may be installed on the ATCA-F125. An 80GB drive designed for extreme temperature and vibration environments has been test and approved for use on the ATCA-F125. Contact your Artesyn Embedded Technologies sales representative and order the HDD-80G-SATA kit which includes the hard drive, all the required mounting hardware, and the installation instructions.

2.6 Blade Installation and Removal

The blade is fully compatible to the AdvancedTCA standard and is designed to be used in AdvancedTCA shelves.

The blade must only be installed into the proper slot type of shelf, hub blades in hub slots, payload blades in blade slots. The proper slots may vary by system type. Refer to the system's documentation for information which slots these are in your particular configuration.

NOTICE

Damage of Circuits

- Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten its life.
- Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Damage of the blade

- Incorrect installation of the blade can cause damage to the blade.
- Only use handles when installing/removing the blade to avoid damage/deformation to the face plate and/or PCB.

2.6.1 Installing Blade

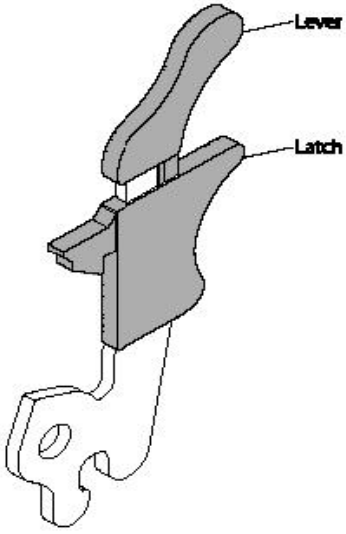
To install the blade into an AdvancedTCA Shelf, proceed as follows.

Installing the Blade

The following procedure describes the installation of the blade in a hub slot that does not have an RTM. It assumes that your system is powered. If your system is powered down, you can disregard the blue LED and thus skip its respective step. In this case it is a purely mechanical installation.

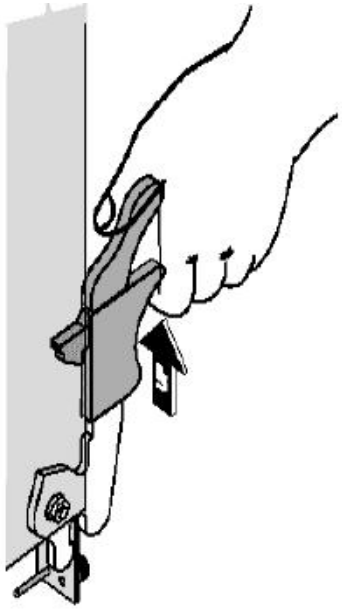
If there is a Rear Transition Module (RTM) to install, install and secure the RTM first as described in the RTM-ATCA-F125 Installation and Use Guide, then install the front blade. If an RTM is already installed, make sure that the RTM faceplate screws are fully tightened to secure the RTM to the shelf.

1. Visually inspect the blade and backplane connectors for damage or bent pins before attempting to insert a board. If any connector damage or pin damage in observed, stop before inserting the blade and send the damaged item through proper repair channels.
2. Ensure that the top and bottom ejector handles are in the outward position by squeezing the lever and the latch together.



3. Insert blade into the shelf by placing the top and bottom edges of the blade in the card guides of the shelf. Make sure that the guiding module of shelf and blade are aligned properly.
4. Apply equal and steady pressure to the blade to carefully slide the blade into the shelf until you feel resistance. Continue to gently push the blade until the blade connectors engage.
5. Squeeze the lever and the latch together and hook the lower and the upper handle into the shelf rail recesses.

6. Fully insert the blade and lock it to the shelf by squeezing the lever and the latch together and turning the handles towards the face plate.



If you feel that you need an abnormal amount of force during blade insertion to insert the blade into the slot, please extract the blade, then carefully inspect the blade and slot for problems to prevent damage.

If your shelf is powered, as soon as the blade is connected to the backplane power pins, the blue LED is illuminated.
When the blade is completely installed, the blue LED starts to blink. This indicates that the blade announces its presence to the shelf management controller.

If an RTM is connected to the front blade, make sure that the handles of both the RTM and the front blade are closed in order to power up the blade's payload.

7. Wait until the blue LED is switched off, then tighten the face plate screws which secure the blade to the shelf. When the blue LED is switched OFF and the green LED "OK" is switched ON, this indicates that the payload has been powered up and that the blade is active.
8. Connect cables to the face plate, if applicable.

2.6.2 Removing blade

This section describes how to remove the blade from an AdvancedTCA system.

NOTICE

Damage of circuits

- Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten its life.
- Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Damage of the blade

- Incorrect installation of the blade can cause damage of the blade.
- Only use handles when installing/removing the blade to avoid damage/deformation to the face plate and/or PCB.

Removing the Blade

The following procedure describes how to remove the blade from a system. It assumes that the system is powered. If the system is powered down, you can disregard the blue LED and skip the respective step. In that case it is a purely mechanical procedure.

1. Unlatch the lower handle from the face plate by squeezing the lever and the latch together and turning the handle outward. Do not rotate the handle fully outward. The blue LED blinks indicating that the blade power-down process is ongoing.

NOTICE

Data Loss

- Removing the blade with the blue LED still blinking causes data loss.
- Wait until the blue LED is steadily lit before removing the blade.

2. Wait until the blue LED is illuminated permanently. Unfasten the screw of the faceplate, then unlatch the upper handle and rotate both handles fully outward until the blade is detached from the shelf.

If the LED continues to blink, it is possible that the upper layer software rejects the blade extraction request.

3. Remove the face plate cables, if applicable.
4. Remove the blade from the shelf.

2.7 AMC Module Installation and Removal

The blade comes with an AMC Bay. For more information, see *AMC Bay, on page 84*.

NOTICE

Damage of Circuits

- Electrostatic discharge and incorrect installation and removal of the blade can damage circuits or shorten its life.
- Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

AMC Module Damage

- The AMC bay supports only AMC modules that are officially supported by Artesyn Embedded Technologies. Installing and operating other AMC modules may damage the AMC bay and the blade.

Limitation of Operating Temperature Range

- Installing AMC modules with small operating temperature ranges into the ATCA-F125 may further restrict the operating temperature range of the ATCA-F125.
- Make sure that the operating temperature of any installed AMC modules and the ATCA-F125 as a bundle are within allowed limits.

Poor Shelf Cooling and EMC Compliance Violation

- An empty AMC bay may result in poor shelf cooling and strong EMC radiation and lead to EMC compliance violation.
- Always cover empty or unused AMC bays with a filler panel.

Installation Procedure

This procedure assumes that the AdvancedATCA system is powered. If your system is powered down, you can disregard the instructions regarding the blue LED.

1. If the AMC bay is occupied by an AMC filler panel, remove the filler panel.
2. Make sure that the AMC module handle is in the extracted position: pulled outward, away from the face plate.
3. Using your thumb, apply equal and steady pressure on the face plate as necessary to carefully slide the AMC module into the guide rails.
4. Continue pushing the module gently along the guide rails until the module is fully engaged with the connector. Avoid using excessive force.
5. Wait for the blue LED to glow. The blue LED glows when the AMC module is completely engaged with the connector.
6. Press module handle inwards towards the face plate to lock the AMC module on the AMC bay.
7. Wait for the blue LED to perform a series of long blinks. The blue LED blinks when the handle is locked in position indicating module detection and activation by the carrier board.
8. Observe blue LED status/activity. The module is fully installed when the blue LED stops blinking and stays OFF.

Removal Procedure

This procedure assumes that the AdvancedATCA system is powered. If your system is powered down, you can disregard the instructions regarding the blue LED.

1. Remove any cables that are connected to the AMC module face plate connectors.
2. Gently pull the module latch outwards, approximately 3 mm away from its locked position.

3. Wait for the blue LED to perform short blinks, and then glow steadily.

NOTICE

Data Loss

- Removing the blade with the blue LED still blinking causes data loss.
- Wait until the blue LED is steadily lit, before removing the blade.

4. Once the blue LED glows steadily, gently pull the AMC module handles outwards to disconnect the module from the AMC connectors. Continue to gently slide the module outwards along the guide rails.
5. Install the filler panel.

2.8 Installing and Removing SFP Modules

This section describes how to install and remove SFP modules.

⚠ CAUTION

Eye Damage

- Optical SFP modules may emit laser radiation when no cable is connected.
- Avoid staring into open apertures to avoid damage to your eyes.

Personal Injury and Damage of the RTM and SFP Modules

- Installing and using SFP modules which are not fully certified and which do not meet all relevant safety standards may damage the RTM and the SFP modules and may lead to personal injury.
- Only use and install SFP modules which are fully certified and which meet all relevant safety standards.

Personal Injury

- Optical SFP modules may be classified as laser products. When installing and using any of these SFP modules, the regulations which correspond to the respective laser class apply to the whole RTM. Not complying to these regulations, may lead to personal injury.
- When installing and using optical SFP modules which are classified as laser products, make sure to comply to the respective regulations.

SFP modules can be installed/removed while the RTM is both powered and or powered off. The presence and also the type of SFP modules is automatically detected.

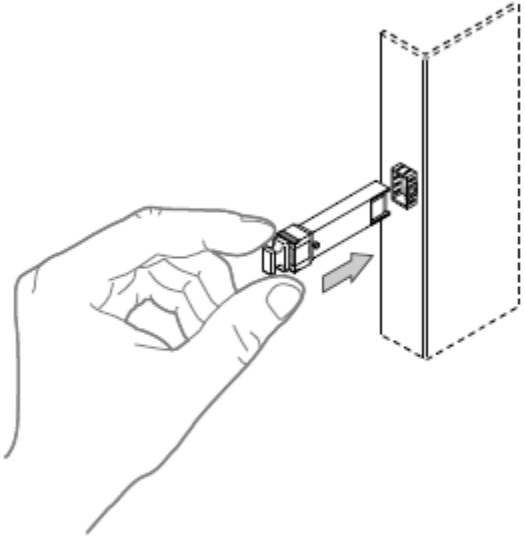
The maximum power consumption of all installed SFP modules must not exceed 12 W.

2.8.1 Installing an SFP Module

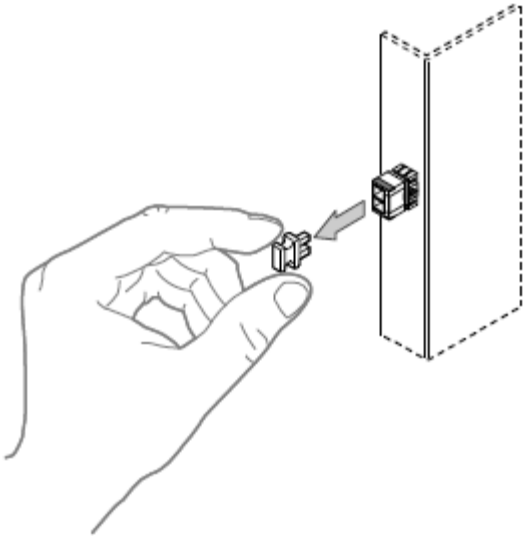
Procedure

In order to install an SFP module, proceed as follows:

1. Slide the SFP module into the slot until it locks into position.



2. Remove the optical port plug.

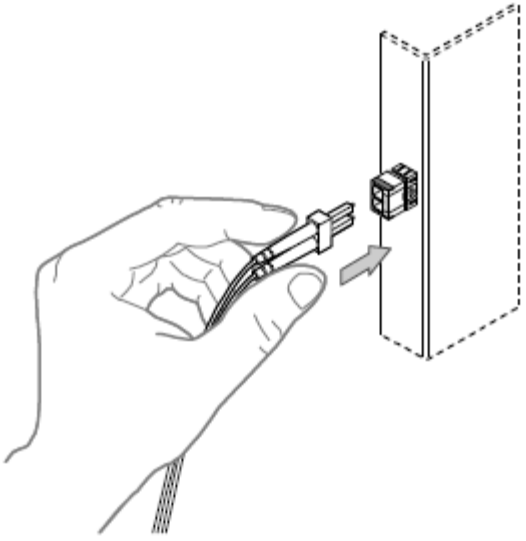


NOTICE

SFP Module Damage

- The optical port plug protects the sensitive optical fibres against dirt and damage. Dirt and damage can render the SFP module inoperable.
- Only remove the optical plug when you are ready to connect a cable to the SFP module. When no cable is connected, cover the port with an optical port plug.

3. Connect the network cable to the SFP module

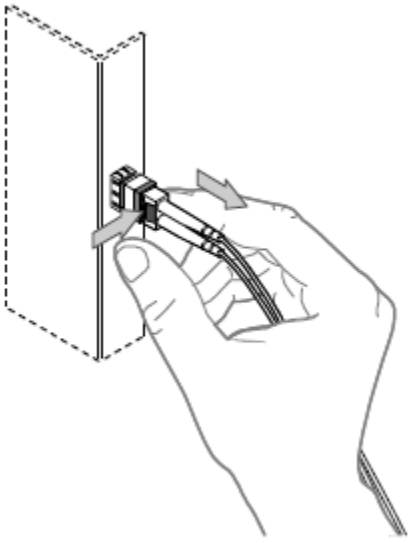


2.8.2 Removing an SFP Module

Procedure

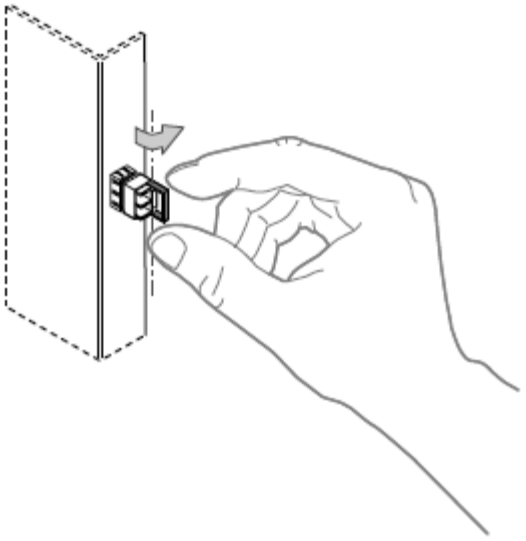
In order to remove an SFP module, proceed as follows.

1. Remove any connected cable from the SFP module.

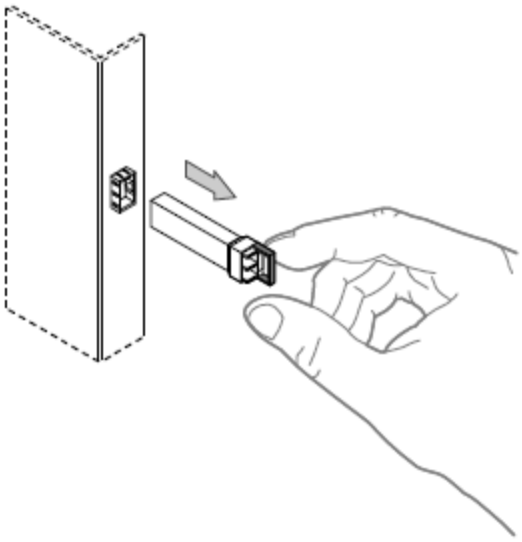


2. Open the SFP latch. Note that the latch mechanism of your SFP module may be

slightly different compared to the latch shown in the following figure.



3. Grasp the SFP module and carefully slide it out of the slot.



4. Cover the optical port with the optical port plug.

NOTICE

SFP Module Damage

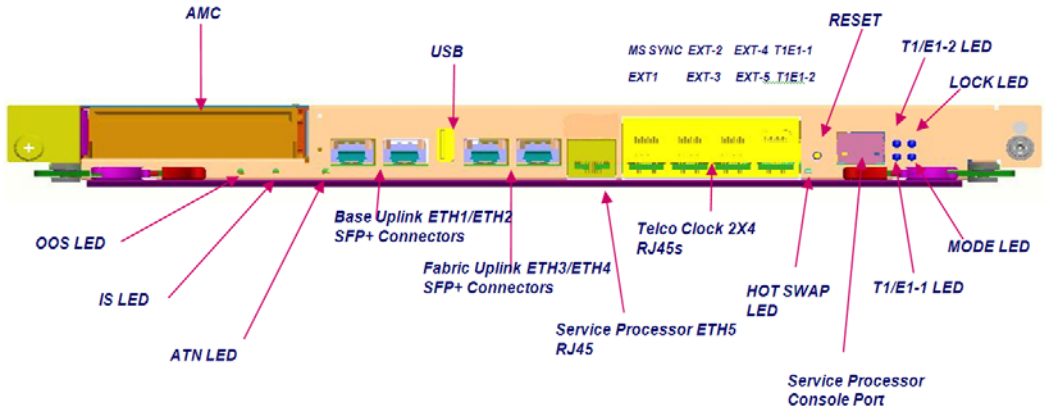
- The optical port plug protects the sensitive optical fibres against dirt and damage. Dirt and damage can render the SFP module inoperable.
- Only remove the optical plug when you are ready to connect a cable to the SFP module. When no cable is connected, cover the port with an optical port plug.

3.1 Overview

3.2 Blade Layout

The following figure shows the front panel face plate design.

Figure 3-1 ATCA-F125 Face Plate



3.3 Faceplate LEDs

This section describes the details of the ATCA-F125 faceplate LEDs.

Table 3-1 Faceplate LEDs

Label	LED	Color	Function
OOS	Out of Service	Red	This LED is enabled by the IPMC upon initially entering the M4 state. Once the HPM Agent starts up, this LED is disabled.
IS	In Service	Green	This LED is enabled by HPM Agent upon initialization. This indicates that the payload software is up and running.

Table 3-1 Faceplate LEDs (continued)

Label	LED	Color	Function
ATN	Attention	Yellow	Blade attention required. This LED is controlled by higher layer software, such as middleware or applications
H/S	Hot Swap	Blue	FRU State Machine ● During blade installation: – Permanently blue: On-board IPMC powered up – Blinking blue: Blade communicating with shelf manager – OFF: Blade is active ● During blade removal: – Blinking blue: Blade notifies shelf manager of its desire to deactivate – Permanently blue: Blade is ready to be extracted
	ETH5 Activity	Green	Blinking - Service Processor Ethernet port activity
	ETH5 Link	Yellow	10/100/1000 Ethernet link on service processor ethernet port
T1/E1-1	Telco Clock LED 2	Yellow	Loss of Signal
		Green	Status OK
		Red	Blinking - Initializing
T1/E1-2	Telco Clock LED 4	Yellow	Loss of Signal
		Green	Status OK
		Red	Blinking - Initializing
MODE	Telco Clock LED 1	Yellow	Slave Clock Generator
		Green	On - Master Clock Generator Blinking - Stand alone Master
		Red	Blinking - Initializing
LOCK	Telco Clock LED 3	Yellow	On -Hold over Blinking - Free Run
		Green	Locked

Table 3-1 Faceplate LEDs (continued)

Label	LED	Color	Function
		Red	Blinking - Initializing

3.4 Reset Switch

The front panel has a recessed reset switch. A small pointed object must be inserted through the hole in the front panel to activate the reset switch. Activating this switch will reset the service processor and all of the ethernet switches. It will not reset the IPMC or the AMC.

3.5 Faceplate Connectors

The following tables provide the pinout for the face plate connectors.

Table 3-2 Service Processor Ethernet RJ45 Connector Pin Assignment (J9)

RJ45 Pin	10Base-T or 100Base-TX	1000Base-T
1	ETH_TX+	ETH_DA+
2	ETH_TX-	ETH_DA-
3	ETH_RX+	ETH_DB+
4		ETH_DC+
5		ETH_DC-
6	ETH_RX-	ETH_DB-
7		ETH_DD+
8		ETH_DD-

Table 3-3 Service Processor Serial RS232 RJ45 Connector (J1)

RJ45 Pin	Function (RS232)
1	RTS
2	Not used
3	TX

Table 3-3 Service Processor Serial RS232 RJ45 Connector (J1) (continued)

RJ45 Pin	Function (RS232)
4	GND
5	GND
6	RX
7	Not used
8	CTS

Table 3-4 Service Processor USB Connector (J10)

USB Pin	Function
1	+0.5 V
2	DATA_N
3	DATA_P
4	GND

Table 3-5 SFP+ Connectors Pin Assignment (J4-J7)

Contact Number	Function	Contact Number	Function
1	GND	11	GND
2	TX_FAULT	12	RX-
3	TX_DISABLE	13	RX+
4	I2C_SDA	14	GND
5	12C_SCL	15	VCCr (+3.3 V)
6	MOD_ABS	16	VCCr (+3.3 V)
7	RATE_SEL[1]	17	GND
8	LOS	18	TX+
9	GND	19	TX-
10	GND	20	GND

1. Configured with a pull-up to allow high speed connection

Table 3-6 Master/Slave Sync Connector (J12-U1)

RJ45 Pin	Function
1	Transmit +
2	Transmit -
3	Receive +
4	
5	
6	Receive -
7	
8	

Table 3-7 Inter-Shelf Connectors (J12-L1, L2, L3, U2, U3)

RJ45 Pin	Function
1	Port 1 +
2	Port 1 -
3	Port 2 +
4	Port 3 +
5	Port 3 -
6	Port 2 -
7	Port 4 +
8	Port 4 -

Table 3-8 T1/E1 Port Connectors (J12-L4 and J12-U4)

RJ45 Pin	Function
1	RX Ring
2	RX Tip
3	
4	TX Ring
5	TX Tip

Table 3-8 T1/E1 Port Connectors (J12-L4 and J12-U4) (continued)

RJ45 Pin	Function
6	Port 2 -
7	Shield
8	Shield

3.6 Backplane Connectors

3.6.1 Zone 1

The following table shows the pinout assignment for the Zone 1 ATCA power connector.

Table 3-9 Zone 1 Connector P1 Pin Assignment

Contact Number	Destination	Description
1 - 4	Reserved	Reserved
5	IPMC Port 2 bit 0	Hardware Address Bit 0
6	IPMC Port 2 bit 1	Hardware Address Bit 1
7	IPMC Port 2 bit 2	Hardware Address Bit 2
8	IPMC Port 2 bit 3	Hardware Address Bit 3
9	IPMC Port 2 bit 4	Hardware Address Bit 4
10	IPMC Port 2 bit 5	Hardware Address Bit 5
11	IPMC Port 2 bit 6	Hardware Address Bit 6
12	IPMC Port 2 bit 7	Hardware Address Bit 7
13	IPMC Port C bit 0	IPMB Clock Port A
14	IPMC Port C bit 1	IPMB Data Port A
15	IPMC Port C bit 2	IPMB Clock Port B
16	IPMC Port C bit 3	IPMB Data Port A
17 - 24	Not used	Not used
25	Shelf Ground	Shelf Ground

Table 3-9 Zone 1 Connector P1 Pin Assignment (continued)

Contact Number	Destination	Description
26	Logic Ground	Logic Ground
27	IPM300 ENABLE B	Enable B
28	IPM300 48VRTN_A	Voltage Return A
29	IPM300 48VRTN_B	Voltage Return B
30	IPM300 -48V_A	Early -48V A
31	IPM300 -48V_A	Early -48V B
32	IPM300 ENABLE A	Enable A
33	IPM300 -48V_A	-48V A
34	IPM300 -48V_A	-48V A

3.6.2 Zone 2

The following table shows the pinout assignment for the Zone 2 ATCA connectors.

Table 3-10 Connector P20 Pin Assignment

P20								
Row	Column AB		Column CD		Column EF		Column GH	
1	CLK1A+	CLK1A-	CLK1B+	CLK1B-	CLK2A+	CLK2A-	CLK2B+	CLK2B-
2	UC_P4_TX+	UC_P4_TX-	UC_P4_RX+	UC_P4_RX-	CLK3A+	CLK3A-	CLK3B+	CLK3B-
3	UC_P2_TX+	UC_P2_TX-	UC_P2_RX+	UC_P2_RX-	UC_P3_TX+	UC_P3_TX-	UC_P3_RX+	UC_P3_RX-
4	UC_P0_TX+	UC_P0_TX-	UC_P0_RX+	UC_P0_RX-	UC_P1_TX+	UC_P1_TX-	UC_P1_RX+	UC_P1_RX-
5	FIX_P15_TX2+	FIX_P15_TX2-	FIX_P15_RX2+	FIX_P15_RX2-	FIX_P15_TX3+	FIX_P15_TX3-	FIX_P15_RX3+	FIX_P15_RX3-
6	FIX_P15_TX0+	FIX_P15_TX0-	FIX_P15_RX0+	FIX_P15_RX0-	FIX_P15_TX1+	FIX_P15_TX1-	FIX_P15_RX1+	FIX_P15_RX1-
7	FIX_P14_TX2+	FIX_P14_TX2-	FIX_P14_RX2+	FIX_P14_RX2-	FIX_P14_TX3+	FIX_P14_TX3-	FIX_P14_RX3+	FIX_P14_RX3-
8	FIX_P14_TX0+	FIX_P14_TX0-	FIX_P14_RX0+	FIX_P14_RX0-	FIX_P14_TX1+	FIX_P14_TX1-	FIX_P14_RX1+	FIX_P14_RX1-
9	FIX_P13_TX2+	FIX_P13_TX2-	FIX_P13_RX2+	FIX_P13_RX2-	FIX_P13_TX3+	FIX_P13_TX3-	FIX_P13_RX3+	FIX_P13_RX3-
10	FIX_P13_TX0+	FIX_P13_TX0-	FIX_P13_RX0+	FIX_P13_RX0-	FIX_P13_TX1+	FIX_P13_TX1-	FIX_P13_RX1+	FIX_P13_RX1-

Table 3-11 Connector P21 Pin Assignment

P21								
Row	Column AB		Column CD		Column EF		Column GH	
1	FIX_P12_TX2+	FIX_P12_TX2-	FIX_P12_RX2+	FIX_P12_RX2-	FIX_P12_TX3+	FIX_P12_TX3-	FIX_P12_RX3+	FIX_P12_RX3-
2	FIX_P12_TX0+	FIX_P12_TX0-	FIX_P12_RX0+	FIX_P12_RX0-	FIX_P12_TX1+	FIX_P12_TX1-	FIX_P12_RX1+	FIX_P12_RX1-
3	FIX_P11_TX2+	FIX_P11_TX2-	FIX_P11_RX2+	FIX_P11_RX2-	FIX_P11_TX3+	FIX_P11_TX3-	FIX_P11_RX3+	FIX_P11_RX3-
4	FIX_P11_TX0+	FIX_P11_TX0-	FIX_P11_RX0+	FIX_P11_RX0-	FIX_P11_TX1+	FIX_P11_TX1-	FIX_P11_RX1+	FIX_P11_RX1-
5	FIX_P10_TX2+	FIX_P10_TX2-	FIX_P10_RX2+	FIX_P10_RX2-	FIX_P10_TX3+	FIX_P10_TX3-	FIX_P10_RX3+	FIX_P10_RX3-
6	FIX_P10_TX0+	FIX_P10_TX0-	FIX_P10_RX0+	FIX_P10_RX0-	FIX_P10_TX1+	FIX_P10_TX1-	FIX_P10_RX1+	FIX_P10_RX1-
7	FIX_P9_TX2+	FIX_P9_TX2-	FIX_P9_RX2+	FIX_P9_RX2-	FIX_P9_TX3+	FIX_P9_TX3-	FIX_P9_RX3+	FIX_P9_RX3-
8	FIX_P9_TX0+	FIX_P9_TX0-	FIX_P9_RX0+	FIX_P9_RX0-	FIX_P9_TX1+	FIX_P9_TX1-	FIX_P9_RX1+	FIX_P9_RX1-
9	FIX_P8_TX2+	FIX_P8_TX2-	FIX_P8_RX2+	FIX_P8_RX2-	FIX_P8_TX3+	FIX_P8_TX3-	FIX_P8_RX3+	FIX_P8_RX3-
10	FIX_P8_TX0+	FIX_P8_TX0-	FIX_P8_RX0+	FIX_P8_RX0-	FIX_P8_TX1+	FIX_P8_TX1-	FIX_P8_RX1+	FIX_P8_RX1-

Table 3-12 Connector P22 Pin Assignment

P22								
Row	Column AB		Column CD		Column EF		Column GH	
1	FIX_P7_TX2+	FIX_P7_TX2-	FIX_P7_RX2+	FIX_P7_RX2-	FIX_P7_TX3+	FIX_P7_TX3-	FIX_P7_RX3+	FIX_P7_RX3-
2	FIX_P7_TX0+	FIX_P7_TX0-	FIX_P7_RX0+	FIX_P7_RX0-	FIX_P7_TX1+	FIX_P7_TX1-	FIX_P7_RX1+	FIX_P7_RX1-
3	FIX_P6_TX2+	FIX_P6_TX2-	FIX_P6_RX2+	FIX_P6_RX2-	FIX_P6_TX3+	FIX_P6_TX3-	FIX_P6_RX3+	FIX_P6_RX3-
4	FIX_P6_TX0+	FIX_P6_TX0-	FIX_P6_RX0+	FIX_P6_RX0-	FIX_P6_TX1+	FIX_P6_TX1-	FIX_P6_RX1+	FIX_P6_RX1-
5	FIX_P5_TX2+	FIX_P5_TX2-	FIX_P5_RX2+	FIX_P5_RX2-	FIX_P5_TX3+	FIX_P5_TX3-	FIX_P5_RX3+	FIX_P5_RX3-
6	FIX_P5_TX0+	FIX_P5_TX0-	FIX_P5_RX0+	FIX_P5_RX0-	FIX_P5_TX1+	FIX_P5_TX1-	FIX_P5_RX1+	FIX_P5_RX1-
7	FIX_P4_TX2+	FIX_P4_TX2-	FIX_P4_RX2+	FIX_P4_RX2-	FIX_P4_TX3+	FIX_P4_TX3-	FIX_P4_RX3+	FIX_P4_RX3-
8	FIX_P4_TX0+	FIX_P4_TX0-	FIX_P4_RX0+	FIX_P4_RX0-	FIX_P4_TX1+	FIX_P4_TX1-	FIX_P4_RX1+	FIX_P4_RX1-
9	FIX_P3_TX2+	FIX_P3_TX2-	FIX_P3_RX2+	FIX_P3_RX2-	FIX_P3_TX3+	FIX_P3_TX3-	FIX_P3_RX3+	FIX_P3_RX3-
10	FIX_P3_TX0+	FIX_P3_TX0-	FIX_P3_RX0+	FIX_P3_RX0-	FIX_P3_TX1+	FIX_P3_TX1-	FIX_P3_RX1+	FIX_P3_RX1-

Table 3-13 Connector P23 Pin Assignment

P23								
Row	Column AB		Column CD		Column EF		Column GH	
1	FIX_P2_TX2+	FIX_P2_TX2-	FIX_P2_RX2+	FIX_P2_RX2-	FIX_P2_TX3+	FIX_P2_TX3-	FIX_P2_RX3+	FIX_P2_RX3-
2	FIX_P2_TX0+	FIX_P2_TX0-	FIX_P2_RX0+	FIX_P2_RX0-	FIX_P2_TX1+	FIX_P2_TX1-	FIX_P2_RX1+	FIX_P2_RX1-
3	FIX_P1_TX2+	FIX_P1_TX2-	FIX_P1_RX2+	FIX_P1_RX2-	FIX_P1_TX3+	FIX_P1_TX3-	FIX_P1_RX3+	FIX_P1_RX3-
4	FIX_P1_TX0+	FIX_P1_TX0-	FIX_P1_RX0+	FIX_P1_RX0-	FIX_P1_TX1+	FIX_P1_TX1-	FIX_P1_RX1+	FIX_P1_RX1-
5	BIX_P1A_TX+	BIX_P1A_TX-	BIX_P1A_RX+	BIX_P1A_RX-	BIX_P1B_TX+	BIX_P1B_TX-	BIX_P1B_RX+	BIX_P1B_RX-
6	BIX_P2_DA+	BIX_P2_DA-	BIX_P2_DB+	BIX_P2_DB-	BIX_P2_DC+	BIX_P2_DC-	BIX_P2_DD+	BIX_P2_DD-
7	BIX_P3_DA+	BIX_P3_DA-	BIX_P3_DB+	BIX_P3_DB-	BIX_P3_DC+	BIX_P3_DC-	BIX_P3_DD+	BIX_P3_DD-
8	BIX_P4_DA+	BIX_P4_DA-	BIX_P4_DB+	BIX_P4_DB-	BIX_P4_DC+	BIX_P4_DC-	BIX_P4_DD+	BIX_P4_DD-
9	BIX_P5_DA+	BIX_P5_DA-	BIX_P5_DB+	BIX_P5_DB-	BIX_P5_DC+	BIX_P5_DC-	BIX_P5_DD+	BIX_P5_DD-
10	BIX_P6_DA+	BIX_P6_DA-	BIX_P6_DB+	BIX_P6_DB-	BIX_P6_DC+	BIX_P6_DC-	BIX_P6_DD+	BIX_P6_DD-

Table 3-14 Connector P24 Pin Assignment

P24								
Row	Column AB		Column CD		Column EF		Column GH	
1	BIX_P7_DA+	BIX_P7_DA-	BIX_P7_DB+	BIX_P7_DB-	BIX_P7_DC+	BIX_P7_DC-	BIX_P7_DD+	BIX_P7_DD-
2	BIX_P8_DA+	BIX_P8_DA-	BIX_P8_DB+	BIX_P8_DB-	BIX_P8_DC+	BIX_P8_DC-	BIX_P8_DD+	BIX_P8_DD-
3	BIX_P9_DA+	BIX_P9_DA-	BIX_P9_DB+	BIX_P9_DB-	BIX_P9_DC+	BIX_P9_DC-	BIX_P9_DD+	BIX_P9_DD-
4	BIX_P10_DA+	BIX_P10_DA-	BIX_P10_DB+	BIX_P10_DB-	BIX_P10_DC+	BIX_P10_DC-	BIX_P10_DD+	BIX_P10_DD-
5	BIX_P11_DA+	BIX_P11_DA-	BIX_P11_DB+	BIX_P11_DB-	BIX_P11_DC+	BIX_P11_DC-	BIX_P11_DD+	BIX_P11_DD-
6	BIX_P12_DA+	BIX_P12_DA-	BIX_P12_DB+	BIX_P12_DB-	BIX_P12_DC+	BIX_P12_DC-	BIX_P12_DD+	BIX_P12_DD-
7	BIX_P13_DA+	BIX_P13_DA-	BIX_P13_DB+	BIX_P13_DB-	BIX_P13_DC+	BIX_P13_DC-	BIX_P13_DD+	BIX_P13_DD-
8	BIX_P14_DA+	BIX_P14_DA-	BIX_P14_DB+	BIX_P14_DB-	BIX_P14_DC+	BIX_P14_DC-	BIX_P14_DD+	BIX_P14_DD-
9	BIX_P15_DA+	BIX_P15_DA-	BIX_P15_DB+	BIX_P15_DB-	BIX_P15_DC+	BIX_P15_DC-	BIX_P15_DD+	BIX_P15_DD-
10	BIX_P16_DA+	BIX_P16_DA-	BIX_P16_DB+	BIX_P16_DB-	BIX_P16_DC+	BIX_P16_DC-	BIX_P16_DD+	BIX_P16_DD-

Table 3-15 Connector P32 Pin Assignment

P32								
Row	Column AB		Column CD		Column EF		Column GH	
1	FIX_P21_TX2+	FIX_P21_TX2-	FIX_P21_RX2+	FIX_P21_RX2-	FIX_P21_TX3+	FIX_P21_TX3-	FIX_P21_RX3+	FIX_P21_RX3-
2	FIX_P21_TX0+	FIX_P21_TX0-	FIX_P21_RX0+	FIX_P21_RX0-	FIX_P21_TX1+	FIX_P21_TX1-	FIX_P21_RX1+	FIX_P21_RX1-
3	FIX_P22_TX2+	FIX_P22_TX2+	FIX_P22_TX2+	FIX_P22_TX2+	FIX_P22_TX2+	FIX_P22_TX2+	FIX_P22_TX2+	FIX_P22_TX2+
4	FIX_P22_TX0+	FIX_P22_TX0+	FIX_P22_TX0+	FIX_P22_TX0+	FIX_P22_TX0+	FIX_P22_TX0+	FIX_P22_TX0+	FIX_P22_TX0+
5	RFX_P14_TX2+	RFX_P14_TX2-	RFX_P14_RX2+	RFX_P14_RX2-	RFX_P14_TX3+	RFX_P14_TX3-	RFX_P14_RX3+	RFX_P14_RX3-
6	RFX_P14_TX0+	RFX_P14_TX0-	RFX_P14_RX0+	RFX_P14_RX0-	RFX_P14_TX1+	RFX_P14_TX1-	RFX_P14_RX1+	RFX_P14_RX1-
7	RFX_P15_TX2+	RFX_P15_TX2-	RFX_P15_RX2+	RFX_P15_RX2-	RFX_P15_TX3+	RFX_P15_TX3-	RFX_P15_RX3+	RFX_P15_RX3-
8	RFX_P15_TX0+	RFX_P15_TX0-	RFX_P15_RX0+	RFX_P15_RX0-	RFX_P15_TX1+	RFX_P15_TX1-	RFX_P15_RX1+	RFX_P15_RX1-
9	SCL	SDA	SPI-SS#	RTM_RST#	RTM_HANDLE#	RTM_PWR_GOOD	RBX_P19/RFX_GE0_TX+	RBX_P19/RFX_GE0_TX-
10	VP12_RTM	VP12_RTM	SPI-MISO	SPI-MOSI	SPI-SCK	RTM_PS0#	RBX_P19/RFX_GE0_RX+	RBX_P19/RFX_GE0_RX-

3.6.3 Zone 3

All of the Zone 3 connectors are of the same type as the Zone 2 connectors. The position of the Zone 3 connectors is specified in the ATCA Rear Transition Module I/O Specification JETIS L1.3-601. The following tables show the pinout assignment for the connectors.

Table 3-16 Connector P30 Pin Assignment

P30								
Row	Column AB		Column CD		Column EF		Column GH	
1	VP12_RTM	RTM_INT#	SynchE_CLK_O+	SynchE_CLK_O-	RTM_REF_CLK	RTM_PS1#	RBX_P20/RFX_GE1_TX+	RBX_P20/RFX_GE1_TX-
2	BIX_MDC	BIX_MDIO	BIX_XG_MDC	BIX_XG_MDIO	FIX_XG_MDC	FIX_XG_MDIO	RBX_P20/RFX_GE1_RX+	RBX_P20/RFX_GE1_RX-
3	FIX_P17_TX2+	FIX_P17_TX2-	FIX_P17_RX2+	FIX_P17_RX2-	FIX_P17_TX3+	FIX_P17_TX3-	FIX_P17_RX3+	FIX_P17_RX3-

Table 3-16 Connector P30 Pin Assignment (continued)

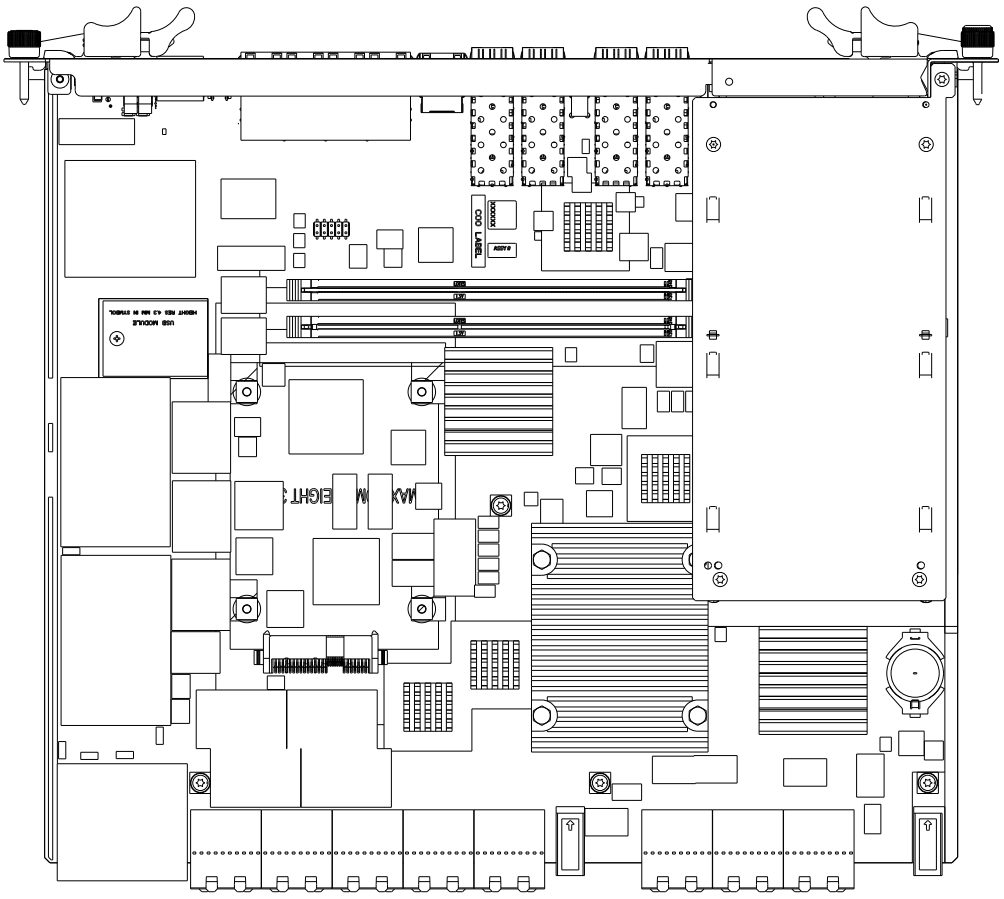
P30								
Row	Column AB		Column CD		Column EF		Column GH	
4	FIX_P17_TX0+	FIX_P17_TX0-	FIX_P17_RX0+	FIX_P17_RX0-	FIX_P17_TX1+	FIX_P17_TX1-	FIX_P17_RX1+	FIX_P17_RX1-
5	FIX_P18_TX2+	FIX_P18_TX2-	FIX_P18_RX2+	FIX_P18_RX2-	FIX_P18_TX3+	FIX_P18_TX3-	FIX_P18_TX3+	FIX_P18_TX3-
6	FIX_P18_TX0+	FIX_P18_TX0-	FIX_P18_RX0+	FIX_P18_RX0-	FIX_P18_TX1+	FIX_P18_TX1-	FIX_P18_TX1+	FIX_P18_TX1-
7	FIX_P19_TX2+	FIX_P19_TX2-	FIX_P19_RX2+	FIX_P19_RX2-	FIX_P19_TX3+	FIX_P19_TX3-	FIX_P19_RX3+	FIX_P19_RX3-
8	FIX_P19_TX0+	FIX_P19_TX0-	FIX_P19_RX0+	FIX_P19_RX0-	FIX_P19_TX1+	FIX_P19_TX1-	FIX_P19_RX1+	FIX_P19_RX1-
9	FIX_P20_TX2+	FIX_P20_TX2-	FIX_P20_RX2+	FIX_P20_RX2-	FIX_P20_TX3+	FIX_P20_TX3-	FIX_P20_RX3+	FIX_P20_RX3-
10	FIX_P20_TX0+	FIX_P20_TX0-	FIX_P20_RX0+	FIX_P20_RX0-	FIX_P20_TX1+	FIX_P20_TX1-	FIX_P20_RX1+	FIX_P20_RX1-

Table 3-17 Connector P31 Pin Assignment

P31								
Row	Column AB		Column CD		Column EF		Column GH	
1	BIX_XG0_TX2+	BIX_XG0_TX2-	BIX_XG0_RX2+	BIX_XG0_RX2-	BIX_XG0_TX3+	BIX_XG0_TX3-	BIX_XG0_RX3+	BIX_XG0_RX3-
2	BIX_XG0_TX0+	BIX_XG0_TX0-	BIX_XG0_RX0+	BIX_XG0_RX0-	BIX_XG0_TX1+	BIX_XG0_TX1-	BIX_XG0_RX1+	BIX_XG0_RX1-
3	BIX_XG1_TX2+	BIX_XG1_TX2-	BIX_XG1_RX2+	BIX_XG1_RX2-	BIX_XG1_TX3+	BIX_XG1_TX3-	BIX_XG1_RX3+	BIX_XG1_RX3-
4	BIX_XG1_TX0+	BIX_XG1_TX0-	BIX_XG1_RX0+	BIX_XG1_RX0-	BIX_XG1_TX1+	BIX_XG1_TX1-	BIX_XG1_RX1+	BIX_XG1_RX1-
5	AMC_TX4+	AMC_TX4-	AMC_RX4+	AMC_RX4-	RBX_P21_TX+	RBX_P21_TX-	RBX_P21_RX+	RBX_P21_RX-
6	AMC_TX5+	AMC_TX5-	AMC_RX5+	AMC_RX5-	RBX_P22_TX+	RBX_P22_TX-	RBX_P22_RX+	RBX_P22_RX-
7	AMC_TX6+	AMC_TX6-	AMC_RX6+	AMC_RX6-	RBX_P23_TX+	RBX_P23_TX-	RBX_P23_RX+	RBX_P23_RX-
8	AMC_TX7+	AMC_TX7-	AMC_RX7+	AMC_RX7-	RBX_P24_TX+	RBX_P24_TX-	RBX_P24_RX+	RBX_P24_RX-
9	RBX_P13_TX+	RBX_P13_TX-	RBX_P13_RX+	RBX_P13_RX-	RBX_P14_TX+	RBX_P14_TX-	RBX_P14_RX+	RBX_P14_RX-
10	VP12_RTM	VP3P3_MP_RTM	PCIE_REFCLK+	PCIE_REFCLK-	SynchE_RC2	GPS_1PPS	SynchE_RC1	RTM_EN# / TYPE#

3.7 Module Connectors

Figure 3-2 Module Connectors Location



3.7.1 AMC Connector

The following table shows the AMC connector pinout assignment.

Table 3-18 J8 AMC Bay Connector Pin Assignment

AMC Bay									
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	35	Unused	69	AMC_RX7-	103	AMC_ P10_MUX_RX+	137	GND
2	+12V	36	Unused	70	GND	104	GND	138	TCLKD-
3	PS1#	37	GND	71	IPMBL_SDA	105	AMC_ P11_MUX_TX-	139	TCLKD+
4	+3.3V IPMI	38	Unused	72	+12V	106	AMC_ P11_MUX_TX+	140	GND
5	GA0	39	Unused	73	GND	107	GND	141	Unused
6	Reserved	40	GND	74	TCLKA+	108	AMC_ P11_MUX_RX-	142	Unused
7	GND	41	ENABLE#	75	TCLKA-	109	AMC_ P11_MUX_RX+	143	GND
8	Reserved	42	+12V	76	GND	110	GND	144	Unused
9	+12V	43	GND	77	TCLKB+	111	Unused	145	Unused
10	GND	44	AMC_TX4+	78	TCLKB-	112	Unused	146	GND
11	BIX_P18_RX+	45	AMC_TX4-	79	GND	113	GND	147	Unused
12	BIX_P18_RX-	46	GND	80	PCIe_CLK+	114	Unused	148	Unused
13	GND	47	AMC_RX4+	81	PCIe_CLK-	115	Unused	149	GND
14	BIX_P18_TX+	48	AMC_RX4-	82	GND	116	GND	150	Unused
15	BIX_P18_TX-	49	GND	83	PS0#	117	Unused	151	Unused
16	GND	50	AMC_TX5+	84	+12V	118	Unused	152	GND
17	GA1	51	AMC_TX5-	85	GND	119	GND	153	Unused
18	+12V	52	GND	86	GND	120	Unused	154	Unused
19	GND	53	AMC_RX5+	87	AMC_ P8_MUX_TX-	121	Unused	155	GND

Table 3-18 J8 AMC Bay Connector Pin Assignment (continued)

AMC Bay									
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
20	FIX_GE0_AMC P1_RX+	54	AMC_RX5-	88	AMC_ AMC_P8_TX+	122	GND	156	Unused
21	FIX_GE0_AMC P1_RX-	55	GND	89	GND	123	Unused	157	Unused
22	GND	56	IPMBL_SCL	90	AMC_ P8_MUX_RX-	124	Unused	158	GND
23	FIX_GE0_AMC P1_TX+	57	+12V	91	AMC_ P8_MUX_RX+	125	GND	159	Unused
24	FIX_GE0_AMC P1_TX-	58	GND	92	GND	126	Unused	160	Unused
25	GND	59	AMC_TX6+	93	AMC_ P9_MUX_TX-	127	Unused	161	GND
26	GA2	60	AMC_TX6-	94	AMC_ P9_MUX_TX+	128	GND	162	Unused
27	+12V	61	GND	95	GND	129	Unused	163	Unused
28	GND	62	AMC_RX6+	96	AMC_ P9_MUX_RX-	130	Unused	164	GND
29	SATA_AMC_RX +	63	AMC_RX6-	97	AMC_ P9_MUX_RX+	131	GND	165	TCK
30	SATA_AMC_RX -	64	GND	98	GND	132	Unused	166	TMS
31	GND	65	AMC_TX7+	99	AMC_ P10_MUX_TX-	133	Unused	167	TRST#
32	SATA_AMC_TX +	66	AMC_TX7-	100	AMC_ P10_MUX_TX+	134	GND	168	TDO
33	SATA_AMC_TX -	67	GND	101	GND	135	TCLKC-	169	TDI
34	GND	68	AMC_RX7+	102	AMC_ P10_MUX_RX-	136	TCLKC+	170	GND

3.7.2 SAS/SATA Connector

The following table shows the pinout assignment for the SAS/SATA connector. The board only supports SATA drives.

Table 3-19 J11 SAS/SATA Connector Pin Assignment

Contact Number	Description	Contact Number	Description
P1	NC	S1	GND
GE21	NC	S2	DRIVE_RX+ (input)
P3	NC	S3	DRIVE_RX- (input)
P4	GND	S4	GND
P5	GND	S5	DRIVE_TX- (output)
P6	GND	S6	DRIVE_TX+ (output)
P7	+5V	S7	GND
P8	+5V	S8	NC
P9	+5V	S9	NC
P10	GND	S10	NC
P11	NC	S11	NC
P12	GND	S12	NC
P13	NC	S13	NC
P14	NC	S14	NC
P15	NC		

3.7.3 Embedded USB Connector

The ATCA-F125 contains a 10-pin 2mm header for an embedded USB module. The following table shows the pinout assignment for the eUSB header.

Table 3-20 P8 eUSB Header Pin Assignment

Contact Number	Description	Contact Number	Description
1	+5V	2	No Connect

Table 3-20 P8 eUSB Header Pin Assignment (continued)

Contact Number	Description	Contact Number	Description
3	Data-	4	No Connect
5	Data+	6	No Connect
7	GND	8	No Connect
9	No Pin Key	10	No Connect

3.7.4 Processor COP Header

The ATCA-F125 contains a 16-pin 0.1" header for the P2020 JTAG COP header. The following table shows the pinout assignment for the processor COP header.

Table 3-21 P50 COP Header Pin Assignment

Contact Number	Description	Contact Number	Description
1	COP_TDO	2	+3.3V pull-up
3	COP_TDI	4	COP_TRST_L
5	+3.3V pull-up	6	COP_VDD_SENSE
7	COP_TCK	8	COP_CHKSTP_IN_L
9	COP_TMS	10	No Connect
11	COP_SRESET_L	12	COP_PRESENT_L
13	COP_HRESET_L	14	No Pin Key
15	COP_CHKSTP_OUT_L	16	GND

3.7.5 H8S Console and Programming Header

The ATCA-F125 contains an 8-pin 0.1" header to provide access to the H8S serial console and to enable the H8S boot loader for initial programming. The H8S boot loader is enabled when shunts are installed shorting pins 2 to pin 4 and pin 6 to pin 8. The following table shows the pinout assignment for this header.

Table 3-22 P9 H8S Console Header Pin Assignment

Contact Number	Description	Dir	Contact Number	Description	Dir
1	H8S_TXD	Out	2	H8S_MD1	In
3	GND	N/A	4	Pull down	Out
5	H8S_RXD	IN	6	H8S_MD2#	In
7	GND	NA	8	Pull down	Out

3.8 Switches

Mechanical switches are provided for debug configuration options. All switch settings are OFF by default. Setting any switches to the ON state may conflict with normal operating modes.

Table 3-23 Switch Settings

Switch	Options	Default
SW1.1	Manual power enable of 12V OFF: 12 V power is controlled by IPMI ON: Enable 12V	OFF
SW1.2	Manual power enable of POL OFF: POL power is controlled by IPMI ON: Enable POL supplies by initiating power up sequence	OFF
SW1.3	Manual power enable of AMC and RTM OFF: AMC and RTM power is controlled by IPMI ON: Enable AMC and RTM power	OFF

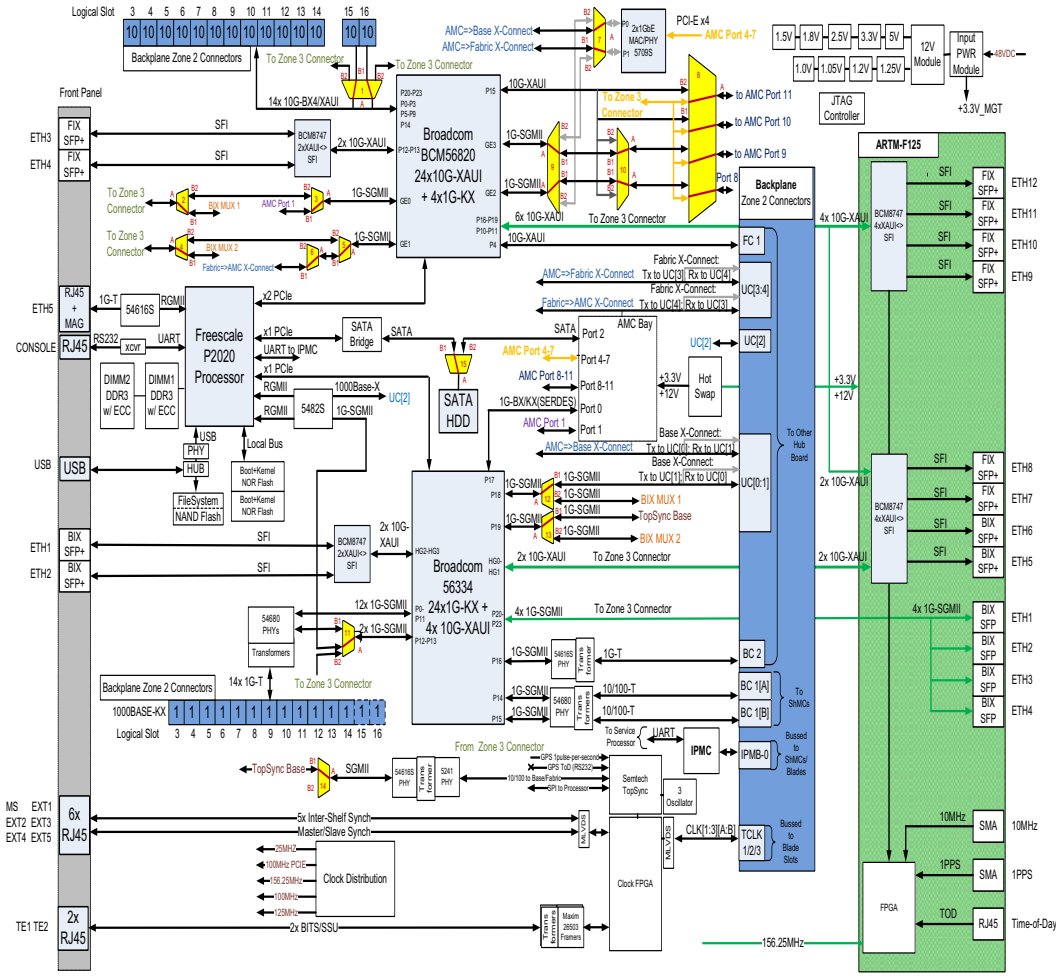
Table 3-23 Switch Settings (continued)

Switch	Options	Default
SW1.4	Disable IPMC Watchdog Timer OFF: Watchdog timer is enabled ON: Disable IPMC Watchdog Timer	OFF

4.1 Block Diagram

The following block diagram provides a high level functional view of the ATCA-F125 board and its interfaces to the front panel, backplane, and RTM.

Figure 4-1 Block Diagram



4.2 Processor

A Freescale P2020 QorIQ Integrated Processor is present on the ATCA-F125 as the onboard service processor. The processor is manufactured in 45nm process technology and contains two e500 Book E-compatible cores with system logic to support a variety of applications. The default speed grade used on ATCA-F125 is 1000 MHz.

The P2020 QorIQ Integrated Processor provides the following features:

- Dual e500 cores
- On-die 32 KB L1 cache for each core
- On-die common 512 KB L2 cache with ECC
- DDR3 memory controller and interface
- Local bus controller and interface
- DUART
- Programmable interrupt controller
- Three PCI Express interfaces
- 4-channel DMA controller
- Three 10/100/1000 Gigabit Ethernet MACs
- One high speed USB interface
- Enhanced secure digital (SD) host controller
- SPI interface
- Two I2C controllers
- Security engine with XOR acceleration
- JTAG interface

The package type is a 31 mm × 31 mm, 689 plastic ball grid array. Maximum package height is 2.46 mm.

4.3 Memory

The P2020 QorIQ Integrated Processor provides an on-chip DDR3 compliant memory controller with the following features:

- Programmable timing supporting DDR3 SDRAM
- 64-bit data interface
- Full ECC support
- Sleep mode support for self-refresh SDRAM
- On-die termination support when using DDR3
- Supports auto refreshing
- Registered DIMM support
- +1.5V DDR3 compatible interface

4.3.1 Memory Interface

The memory bus is 64-bit wide with ECC protection. It connects the P2020 QorIQ Integrated Processor directly to the DIMM memory sockets. The memory data bus runs at a maximum frequency of 400 MHz providing a total bandwidth of 6.4 Gbyte/s.

4.3.2 Memory Sockets

Two 240-pin DDR3 DIMM sockets are provided on the ATCA-F125 to host up to 2 Gbyte of memory on each DIMM socket using single or dual rank DDR3 registered DIMM memory modules.

4.3.3 Memory Modules

The ATCA-F125 requires very low profile VLP DDR3 DIMM modules in order to fit within the maximum component height profile of an ATCA blade. The ATCA-F125 board has been tested and qualified to operate with a 2GB DDR3 VLP RDIMM from Smart Modular. The operating system is currently limited to 2GB of DDR3 memory

The SPD-SROM (Serial Presents Detect) on each DIMM module provides all necessary information (speed, size, type and the like) to the boot firmware. The SPD-SROM is read through I2C Bus connected to the P2020 QorIQ Integrated Processor.

4.3.4 Persistent Memory

On the ATCA-F125, the persistent memory is part of the DDR memory subsystem. A dedicated register is available in the FPGA to enable or disable persistent memory by software. If persistent memory is enabled, the memory contents of the main memory stays unchanged after any applied reset, except power-up reset. After power-up reset the persistent memory feature is disabled.

A special procedure needs to be followed to use the persistent memory feature. This procedure is automatically executed by the U-Boot during initialization.

1. Set DDR_SDRAM_CFG_2[SR_IE] bit inside the memory controller of the P2020 QorIQ Integrated Processor.
2. Set these fields in the PIC of P2020 QorIQ Integrated Processor:
   - EIVPRn[PRIORITY] to 0xF (highest priority)
   - EIDRn[EP]
3. Enable persistent memory feature by setting persistent memory bit inside the FPGA.
4. Any reset may occur except power-up reset.
5. The FPGA generates an interrupt (IRQ_N[11]) to the P2020 QorIQ Integrated Processor.
6. This external interrupt is steered through the PIC of P2020 QorIQ Integrated Processor to the IRQ_OUT signal.
7. The IRQ_OUT signal from the interrupt controller is then automatically detected by the DDR controller, which immediately causes main memory to enter self-refresh mode.
8. 1ms after the interrupt signal (IRQ_N[11]) the FPGA asserts the reset signal for at least 50ms.
9. Read persistent memory bit in FPGA.
10. Initialize main memory but do not clear persistent memory area.

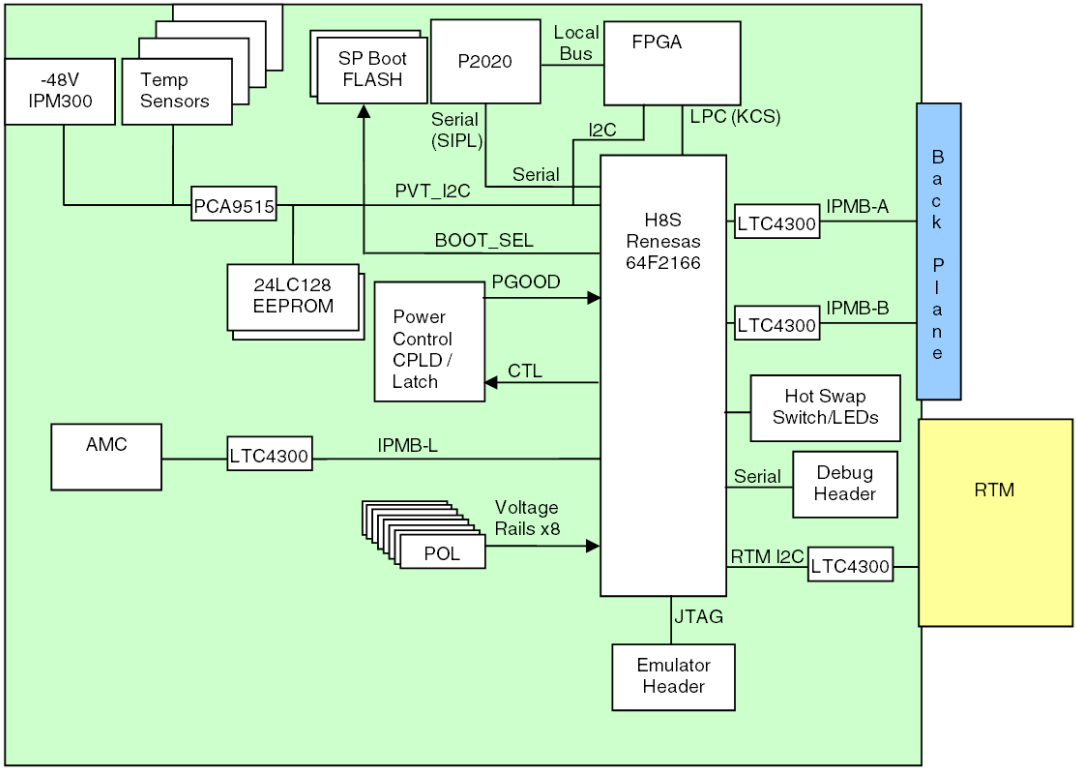
4.4 IPMI

The IPMI function on ATCA-F125 is implemented using the Artesyn Embedded Technologies common ATCA base IPMI design. This building block is based on the Pigeon Point Systems IMPI implementation using the Renesas HD64F2166 microcontroller which is part of the H8S controller family. The IPMI building block implementation provides the following features:

- Two IPMB interfaces to the back-plane
- One local IPMB interface for onboard IPMI
- One I2C/IPMB interface for intelligent or non-intelligent RTMs
- One private I2C interface for non-intelligent I2C devices
- Serial UART (SIPL) and KCS/LPC interfaces to the P2020 service processor
- Analog voltage sensor inputs
- Service processor boot flash fail over selection
- Watch-dog timer

- Hot swap control
- Temperature Sensors

Figure 4-2 IPMI Block Diagram



The ATCA-F125 board design supports a KCS LPC-based interface between the H8S controller and the P2020 service processor. The H8S contains a native Low Pin Count (LPC) interface. The P2020 does not have a LPC interface so a P2020 Local Bus to LPC bus interface is implemented inside the FPGA.

Serial Port 2 of the H8S controller is routed to the on-board H8S debug header through an RS232 buffer to support device programming and the IPMC console interface. Refer to Table 58 for the header pinout. This serial port will operate at 9600 baud rate.

The IPMC building block is designed to keep the payload running even during firmware upgrade. When the payload is powered off, hot plug compatible buffers are used on signals which bridge the management power domain and the payload power domain to prevent leakage currents to the payload power domain. In case of an IPMC firmware upgrade, the output signals to the payload remain unchanged. After IPMC firmware update is finished, the IPMC reads status of the signals before driving them again.

4.4.1 Temperature Sensors

The on board temperature sensors are implemented using National LM75 digital temperature sensors. The following table provides the location, the upper non critical, critical and non recoverable temperature thresholds for each of the onboard temperature sensors. These thresholds will be determined by correlating the sensor temperature to the critical component temperature during thermal testing.

Table 4-1 Temperature Sensors

Device	Temperature Thresholds					
	Lower Non Critical	Lower Critical	Lower Non Recoverable	Upper Non Critical	Upper Critical	Upper Non Recoverable
Air Inlet Component Side 1	0 C	-5 C	-10 C	54 C	61 C	72 C
BIX (BCM56334)	0 C	-5 C	-10 C	50 C	100 C	115 C
FIX (BCM56820)	0 C	-5 C	-10 C	55 C	100 C	115 C
SP (P2020)	0 C	-5 C	-10 C	50 C	100 C	115 C

4.5 FPGA

A Xilinx XC3S700A Spartan 3A family FPGA is used on the board to provide a combination of glue logic functions and telecom clock support functions. The FPGA functions include the following:

- Local Bus Interface
- Local Bus Address Latch and Decoder
- Low Pin Count Interface between Host and IPMC

- Interrupt Routing Unit
- Reset Controller
- Local Bus to SPI Interface
- Telecom Clocking Support
- Service Processor Watchdog Timer

4.5.1 Serial Configuration PROM

The FPGA is configured at power up by loading the contents of an Atmel AT45DB041 SPI PROM device. This configuration uses standard SPI Flashes for the FPGA configuration. For fault recovery during the remote upgrade of the FPGA PROM, the ATCF125 board will provide a backup SPI device. Both PROMs will be programmed with identical images during the production process. The IPMI infrastructure can be used to select the secondary boot device. The primary PROM device is selected by default.

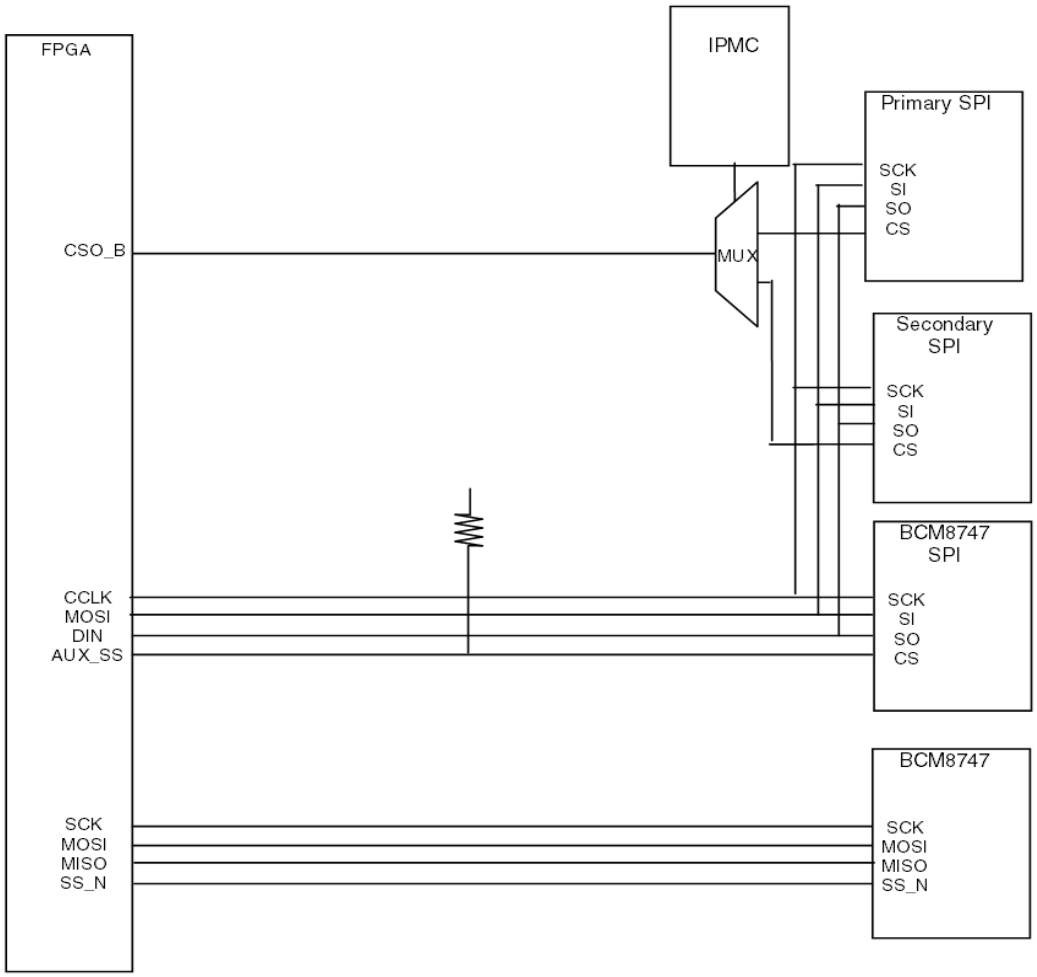
The SPI device chain will also include the SPI device for the BCM8747 microcode so that it can be upgraded by the service processor.

There are four different modes of operation for the FPGA and the SPI flash devices:

- FPGA Configuration - The FPGA automatically controls the CSO_B, CCLK and MOSI pins and reads the configuration data over DIN. Whether the configuration data is supplied by SPI Flash 1 or 2 is determined by the routing of the CSO_B signal which is controlled by the IPMC. AUX_SS is deasserted by virtue of the fact the FPGA is not configured.
- Configuration Flash programming - A SPI controller in the FPGA (driven by the service processor over the local bus) controls CSO_B, CCLK and MOSI, and monitors DIN. The IPMC has to select the chip select routing for the primary SPI device. The secondary SPI device, which is for fail-safe backup purposes only, is write protected and cannot be programmed in the field through the FPGA SPI interface. AUX_SS is deasserted by the SPI controller.

- BCM8747 microcode Flash programming - The same SPI controller in the FPGA is used as with configuration Flash programming, but now AUX_SS is driven instead of CSO_B (which is deasserted), allowing SPI Flash 3 to be programmed.
- BCM8747 microcode loading - The SPI port from the BCM8747 is routed to AUX_CS, CCLK, MOSI and DIN pins in the FPGA to allow the microcode to be read from SPI Flash 3.

Figure 4-3 FPGA SPI ROM Configuration



4.6 Boot and User Flashes

Two 256 Mbit NOR Flash devices are used as boot devices for the service processor. The flash devices used will be Numonyx PC28F256P33BF or equivalent devices. The data bus width to the flash devices is 16 bit, supporting word accesses only.

4.6.1 Boot Flash Backup Recovery

By default, the payload processor boots from the Boot Flash device #1. An IPMI OEM command can be used to send a message to the IPMC to change the boot device. The IPMC provides an IPMI sensor to control the signal BOOT_SELECT. If the BOOT_SELECT signal is set high, the payload processor will boot from Boot Flash device #2 after reset. The boot device from which the service processor has booted (active bank) is write protected and cannot be reprogrammed, whereas the redundant boot device can be erased and reprogrammed.

Figure 4-4 Boot PROM Backup Recovery

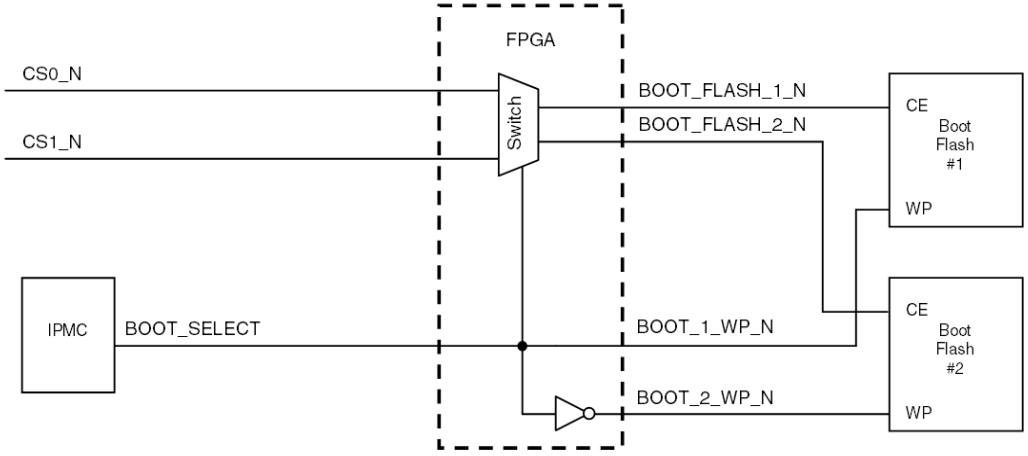


Table 4-2 Boot PROM Backup Recovery Operation

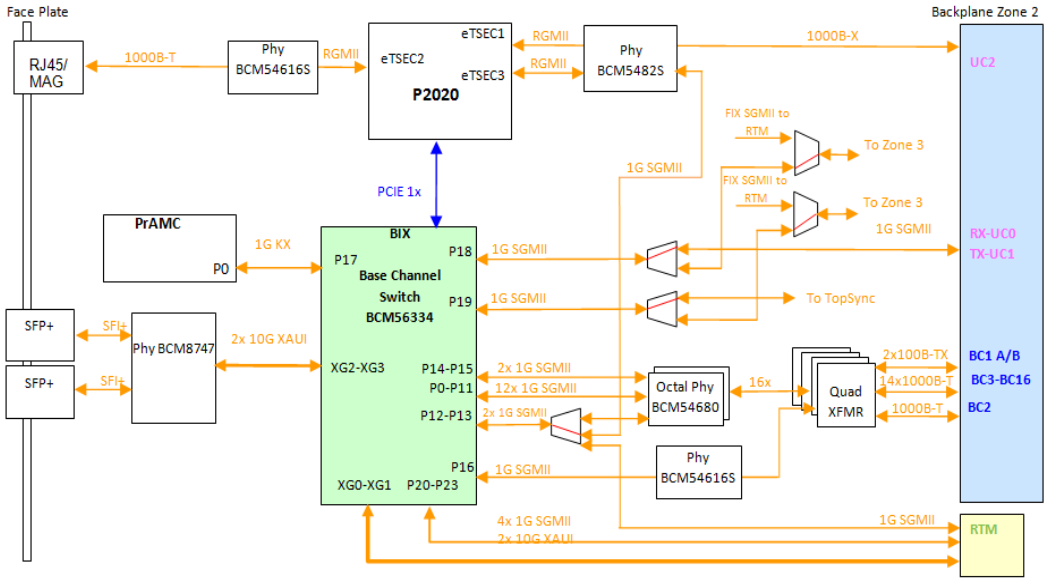
BOOT SELECT	Chip Select Mapping	Boot Device	Erase Protection
Low	BOOT_FLASH_1_N = CS0_N BOOT_FLASH_2_N = CS1_N	Boot Flash #1	Flash #1 = Yes Flash #2 = No. Upgrade enabled
High	BOOT_FLASH_1_N = CS1_N BOOT_FLASH_2_N = CS0_N	Boot Flash #2	Boot Flash #1 = No. Upgrade Enabled Flash #2 = Yes

4.7 Base Channel Interface

The Broadcom BCM56334 switch device provides 24 10/100/1000 Mbps ports and four 10G stacking ports. The BCM56334 supports advanced Layer2 switching, L3 routing, ACL and key carrier protocols. The PCI Express 1x interface of the Broadcom BCM56334 is attached to one of the PCI Express ports of the P2020 QorIQ Integrated Processor to provide the service processor configuration and management capability to the switch as well as to provide full

access to the BCM56334 switch traffic. A block diagram of the base channel interconnect is shown in Figure 4-5.

Figure 4-5 Base Channel Block Diagram



Some of the 1GbE SGMII ports from the BCM56334 have the option of being routed through muxes to different destinations as seen in the block diagram above (for example, to ToPSync or RTM). The select pins for these mux/demux switches are located in the FGPA to route the SGMII ports to the desired destination. FPGA registers can be accessed through two different methods:

1. Through the P2020 local bus interface, the service processor can program registers in the FPGA
2. Through the IPMI controller private I2C bus, the IPMC controller can set the various mux select before enabling reset on the remainder to the payload.

The table below lists each BCM56334 port by number, the device to which it is connected, and the connection type utilized.

Table 4-3 BCM56344 Base Channel Switch Connections

Port	Base Channel	Management Interface	PHY ADDR/ Front Board	CONNECTED TO PHY	CONNECTION BETWEEN	LINK TYPE
0	3	BIX_MDIO/BIX_MDC	1	BCM54680-1	BIX - Backplane Channel 3	1000B-T
1	4	BIX_MDIO/BIX_MDC	2	BCM54680-1	BIX - Backplane Channel 4	1000B-T
2	5	BIX_MDIO/BIX_MDC	3	BCM54680-1	BIX - Backplane Channel 5	1000B-T
3	6	BIX_MDIO/BIX_MDC	4	BCM54680-1	BIX - Backplane Channel 6	1000B-T
4	7	BIX_MDIO/BIX_MDC	5	BCM54680-1	BIX - Backplane Channel 7	1000B-T
5	8	BIX_MDIO/BIX_MDC	6	BCM54680-1	BIX - Backplane Channel 8	1000B-T
6	9	BIX_MDIO/BIX_MDC	7	BCM54680-1	BIX - Backplane Channel 9	1000B-T
7	10	BIX_MDIO/BIX_MDC	8	BCM54680-1	BIX - Backplane Channel 10	1000B-T
8	11	BIX_MDIO/BIX_MDC	9	BCM54680-2	BIX - Backplane Channel 11	1000B-T
9	12	BIX_MDIO/BIX_MDC	10	BCM54680-2	BIX - Backplane Channel 12	1000B-T
10	13	BIX_MDIO/BIX_MDC	11	BCM54680-2	BIX - Backplane Channel 13	1000B-T
11	14	BIX_MDIO/BIX_MDC	12	BCM54680-2	BIX - Backplane Channel 14	1000B-T
12	15	BIX_MDIO/BIX_MDC	13	BCM54680-2	BIX - Backplane Channel 15 or RTM	1000B-T
13	16	BIX_MDIO/BIX_MDC	14	BCM54680-2	BIX - Backplane Channel 16 or Service Proc eTSEC3	1000B-T
14	1A	BIX_MDIO/BIX_MDC	15	BCM54680-2	BIX - BC 1A	10/100B-T
15	1B	BIX_MDIO/BIX_MDC	16	BCM54680-2	BIX - BC 1B	10/100B-T
16	2	BIX_MDIO/BIX_MDC	0	BCM54616S-1	BIX-BC 2	1000B-T
17				-	BIX-PrAMC/P0	SERDES
18				-	BIX X-connect or RTM	SGMII
19			17	BCM54616S to TopSync	Clock TopSync or RTM	SGMII
20				-	BIX-RTM ETH1	SGMII
21				-	BIX-RTM ETH2	SGMII

Table 4-3 BCM56344 Base Channel Switch Connections (continued)

Port	Base Channel	Management Interface	PHY ADDR/ Front Board	CONNECTED TO PHY	CONNECTION BETWEEN	LINK TYPE
22				-	BIX-RTM ETH3	SGMII
23				-	BIX-RTM ETH4	SGMII
HG-0		BIX_XGMDIO/BIX_XGMDC	22	BCM8747-2 on RTM	BIX- RTM ETH6	XAUI
HG-1		BIX_XGMDIO/BIX_XGMDC	23	BCM8747-2 on RTM	BIX-RTM ETH5	XAUI
HG-2		BIX_XGMDIO/BIX_XGMDC	24	BCM8747	BIX- Front ETH1	XAUI
HG-3		BIX_XGMDIO/BIX_XGMDC	25	BCM8747	BIX-Front ETH2	XAUI

Port 0-16 of the base channel switch are configured as SGMII interfaces, so they can support auto-negotiation. Ports 17-23 can be either configured as SGMII or SERDES channels. Port configuration is done by software.

4.7.1 Base Channel PHYs

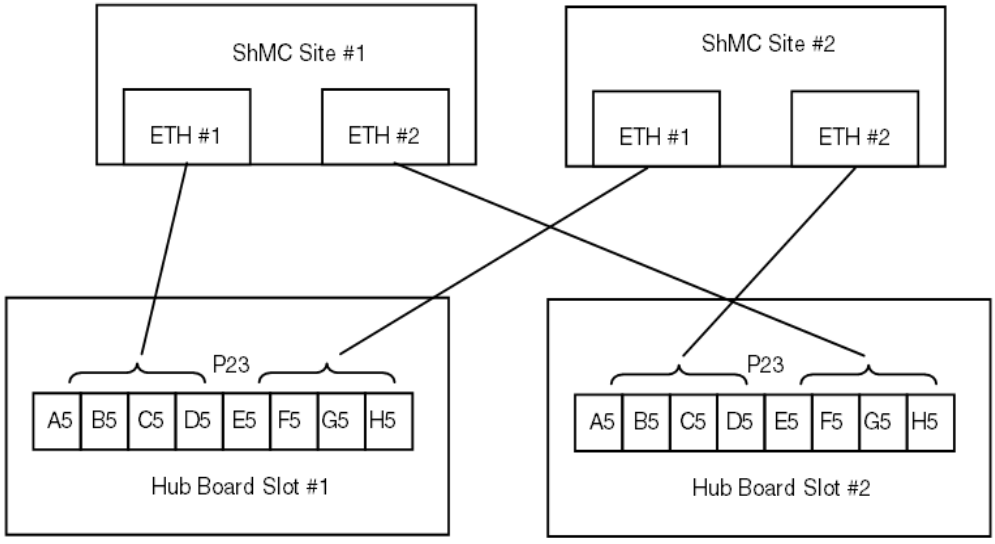
The ATCA-F125 uses two Broadcom BCM54680 octal PHYs, a BCM54616S PHY, and a BCM8747 PHY for the base channel. Each BCM54680 supports eight SGMII channels to the BCM56334 and provides the physical layer functions for the 10/100/1000Base-T connections or 10/100-T connections to the backplane. The BCM54616S PHY is a single PHY that supports an SGMII channel to the BCM56334 and provides the physical layer functions for a 10/100/1000 Base-T connection to the backplane.

The BCM8747 PHY is a four port XAUI to 10 Gb SFI PHY that provides the interface between two of the Base Switch 10 GbE stacking ports and the front panel SFP+ modules. The other two ports of the BCM8747 PHY provide the interface between two of the Fabric Switch 10 GbE stacking ports and the front panel SFP+ modules. The BCM8747 requires an external SPI flash device to load microcode into the device. An AT25256B or equivalent SPI flash device is used for this purpose.

4.7.2 ShMC Cross-Connect

Two 100 Base-Tx ports of the base channel switch are connected to the split Base Interface ShMC port (BC1) connector at the backplane. This connection is compliant to the "cross-connect" ECN 3.0-2.0-001 to PICMG3.0 R3.0 as shown in the following figure.

Figure 4-6 Standard ShMC Cross-Connect



4.8 Fabric Channel Interface

The Broadcom BCM56820 switch device provides 24 10Gbps XAUI ports and four 1Gbps SGMII ports. Fourteen of the 10Gbps ports are routed to the backplane for the switch fabric. Two of these 14 port may be routed to the RTM under control of high speed muxes. One XAUI port is provided to connect the switch to the secondary hub board. Six 10-Gbps uplink interfaces from the switch are routed to the Zone 3 connectors for use by an RTM. Two other XAUI uplink ports are routed to the BCM8747 XAUI-SFI PHY to provide two SFP+ uplinks on the front panel. One XAUI port is connected to a mux which can route the XAUI interface to AMC ports 8-11. The four 1 Gbps SGMII ports of the BCM56820 can be routed to different destinations across the board using a series of 2 channel 2:1 muxes. The select pins for these mux/demux switches are controlled by the FGPA.

The P2020 service processor or the H8S IPMC can program registers in the FPGA to route the SGMII ports to the desired destination. The P2020 service processor communicates with the BCM56820 through the PCI Express interface to initialize and manage the switch as well as to provide full access to the BCM56820 switch traffic.

Figure 4-7 Fabric Channel Block Diagram

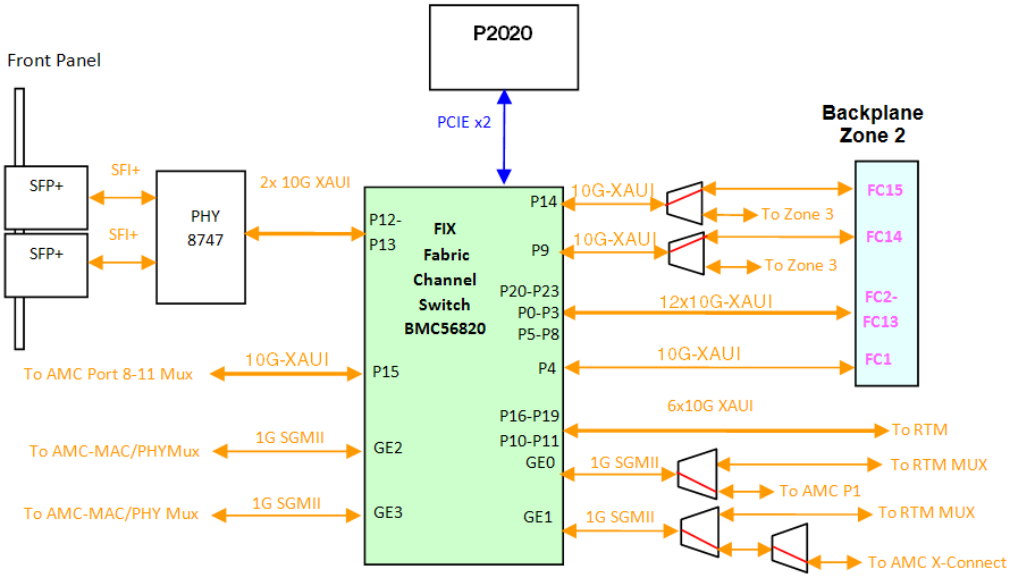


Table 4-4 Fabric Channel Switch Connections

BCM56820 Port	Fabric Channel Port	Management Interface	PHY ADDR/ Front Board	Connect to PHY	Connection Between	Link Type
4	1				FIX- Backplane FC1	10GBase-BX4
20	2				FIX - Backplane FC2	10GBase-BX4
21					FIX - Backplane FC3	10GBase-BX4

Table 4-4 Fabric Channel Switch Connections (continued)

BCM56820 Port	Fabric Channel Port	Management Interface	PHY ADDR/ Front Board	Connect to PHY	Connection Between	Link Type
22	4				FIX - Backplane FC4	10GBase-BX4
23	5				FIX - Backplane FC5	10GBase-BX4
0	6				FIX - Backplane FC6	10GBase-BX4
1	7				FIX - Backplane FC7	10GBase-BX4
2	8				FIX - Backplane FC8	10GBase-BX4
3	9				FIX - Backplane FC9	10GBase-BX4
5	10				FIX - Backplane FC10	10GBase-BX4
6	11				FIX - Backplane FC11	10GBase-BX4
7	12				FIX - Backplane FC12	10GBase-BX4
8	13				FIX - Backplane FC13	10GBase-BX4
9	14				FIX - Backplane FC14 or RTM	10GBase-BX4
14	15				FIX - Backplane FC15 or RTM	10GBase-BX4
15					FIX-AMC Port 8-11	XAUI
16		FIX_MDIO/FIX_MDC(2)	16	BCM8747-1-RTM	FIX-RTM ETH12	XAUI
17		FIX_MDIO/FIX_MDC(2)	17	BCM8747-1-RTM	FIX-RTM ETH11	XAUI
18		FIX_MDIO/FIX_MDC(2)	18	BCM8747-1-RTM	FIX-RTM ETH10	XAUI
19		FIX_MDIO/FIX_MDC(2)	19	BCM874-1-RTM	FIX-RTM ETH9	XAUI

Table 4-4 Fabric Channel Switch Connections (continued)

BCM56820 Port	Fabric Channel Port	Management Interface	PHY ADDR/ Front Board	Connect to PHY	Connection Between	Link Type
10		FIX_MDIO/FIX_MDC(2)	20	BCM8747-2-RTM	FIX-RTM ETH8	XAUI
11		FIX_MDIO/FIX_MDC(2)	21	BCM8747-2-RTM	FIX-RTM ETH7	XAUI
12		FIX_MDIO/FIX_MDC(2)	26	BCM8747	FIX- Front ETH3	XAUI
13		FIX_MDIO/FIX_MDC(2)	27	BCM8747	FIX- Front ETH4	XAUI
1G-0					FIX-RTM or AMC Port 1	SGMII
1G-1		FIX_MDIO/FIX_MDC(0)			FIX-RTM or AMC X-Connect	SGMII
1G-2					FIX-AMC Port 8 or MAC/PHY Port 0	SGMII
1G-3					FIX-AMC Port 9 or MAC/PHY Port 1	SGMII

4.9 SFP+ Modules

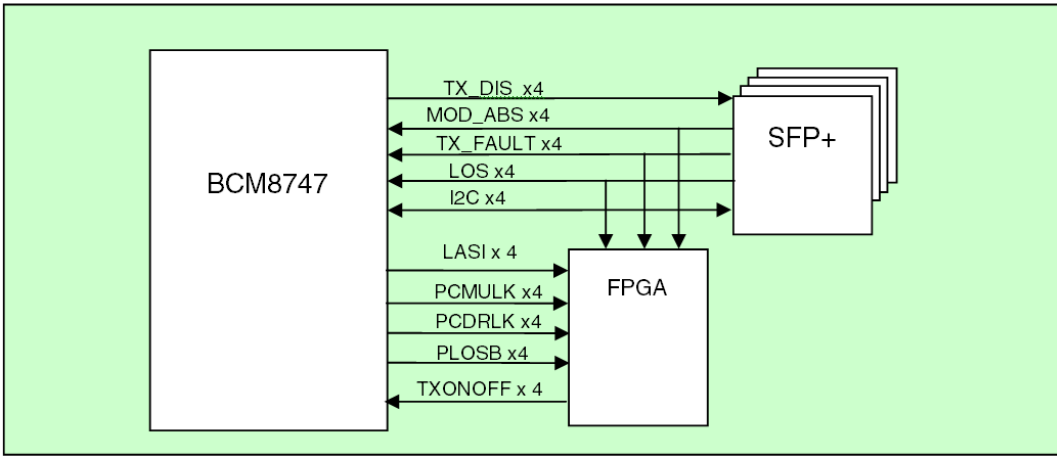
The ATCA-F125 provides four SFP+ module receptacles on the front panel, two for base uplinks and two for fabric uplinks. The SFP+ signals LOS, TX_FAULT and MOD_ABS are monitored for status by the BCM8747 PHY. Status changes will result in a service processor interrupt.

Each SFP+ module's I2C signals are routed to the BCM8747 PHY which provides four separate SFP+ I2C interfaces. The service processor uses these I2C interfaces, accessed through the PHY management port, to read the module's on-board EEPROM information to determine type and vendor specific information.

The individual TXONOFF signals on the BCM8747 are connected to the FPGA which allows them to be driven under software control. This enables software to individually enable and disable the SFP+ optical outputs.

The PCMULK, PCDRLK, PLOSB and LASI signals from each BCM8747 port are connected to the FPGA to allow them to be monitored by software. The PLOSB and LASI signals can also generate an interrupt to the service processor.

Figure 4-8 SFP+ Module Status and Control Interface



The SFP+ module receptacles are designed to support standard SFP modules, SFP+ modules as well as direct attach copper SFP+ cables. The following table lists the SFP+ module types that have been tested and verified for use on the ATCA-F125.

Table 4-5 Tested SFP+ Modules

Artesyn Embedded Technologies Part Number	Vendor Part Number	Vendor	Description
SFPP-MM-SR-LC	FTLX8571D3BCL	Finisar	10Gb/s 850nm multimode SFP+ transceiver
SFPP-SM-LR-LC	FTLX1471D3BCL	Finisar	SFP+ 10GB LR Optical Module
SFP-CO-RJ-45	DM7-41-R-L	Methode	COPPER SFP (MODULE, SFP, RJ45 CONNECTOR
SFP-MM-SX-LC	AFBR-57L5AZP	Avago	SFP optical module

Table 4-5 Tested SFP+ Modules (continued)

Artesyn Embedded Technologies Part Number	Vendor Part Number	Vendor	Description
SFPP-CO-RJ-45-3M	74752-1301	Molex	3 m direct attach copper SFP+ cable

4.10 AMC Bay

The ATCA-F125 provides one AMC bay to support a processor AMC as an application processor. The slot is connected by an AMC type B+ connector and supports a midsize single width PrAMC module with access to an on board SATA drive and to a dual gigabit Ethernet controller through the AMC.

Some PrAMC modules support 10Gb XAUI or 1Gb SGMII channels on ports 8-11 while other PrAMCs will have PCI Express channels on ports 8-11. The ATCA-F125 has high speed signal multiplexers to support routing of the AMC port 8-11 signals depending on the PrAMC installed.

The ATCA-F125 also routes AMC ports 4-7 as a x4 PCIE port directly to a BCM5709s dual MAC/PHY controller.

The ATCA-F125 provides current limiting power control to the AMC. A hot swap control device is used to control the 12 V payload power and 3.3 V management power to the AMC as well as providing current limiting.

The IPMC sets a control output pin to control the direction of a SATA mux. This determines whether the service processor or the PrAMC has access to the SATA hard disk drive. The SATA mux control from the IPMC is routed through the FPGA so that the SATA mux control can be controlled by the service processor through the FPGA.

Figure 4-9 AMC Bay Connection Diagram

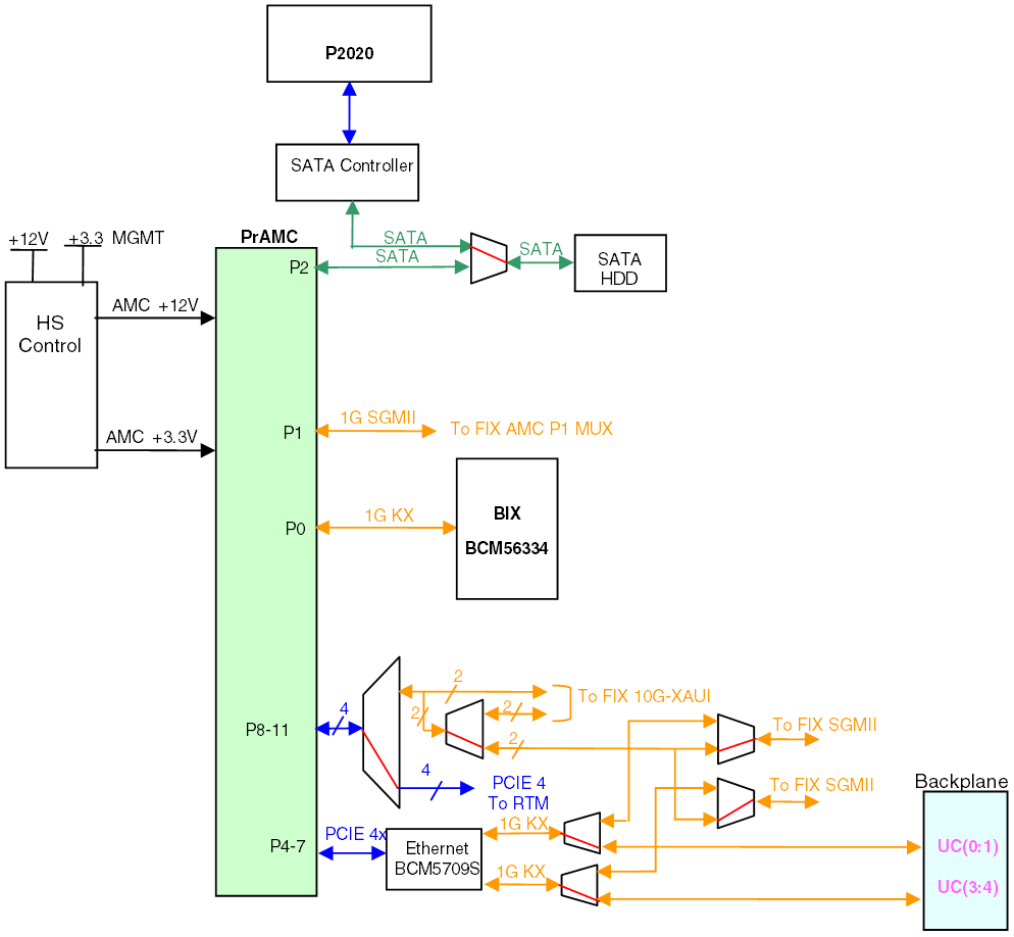


Table 4-6 AMC Bay Port Assignments

Connector Region	Port No.	PrAMC Usage	ATCA-F125 Source/Target
Clocking	1	TCLKA	From FPGA Telecom Clock logic
	2	TCLKB	From FPGA Telecom Clock logic
	3	TCLKC	From FPGA Telecom Clock logic
	4	TCLKD	From FPGA Telecom Clock logic
	5	FCLKA	From PCIE 100 MHz differential clock distribution
Common Options	0	Gigabit Ethernet Link 0	To BCM56334
	1	Gigabit Ethernet Link 1	To BCM56820 using mux
	2	SATA Link 0	To SATA HDD Mux
	3	SATA Link 1	Unused
Fat Pipes	4	PCI-Express Lane 0	To BCM5709S x4 PCIE
	5	PCI-Express Lane 1	
	6	PCI-Express Lane 2	
	7	PCI-Express Lane 3	
	8	PCIE/XAUI/SGMII	To RTM or FIX XAUI or FIX SGMII
	9	PCIE/XAUI/SGMII	
	10	PCIE/XAUI/SGMII	To RTM or FIX XAUI
	11	PCIE/XAUI/SGMII	
Extended Options	12	Unused	Unused
	13-20	Unused	Unused

4.10.1 BCM5709S Dual Gigabit Ethernet MAC/PHY

The Broadcom BCM5709S is a PCI Express based single-chip dual Gigabit Ethernet MAC controller with integrated PHY and SerDes cores. This device supports a 4x PCI Express v1.1/v2.0 compliant interface to the host processor in the AMC bay. The dual MAC/PHY supports either 1Gb SERDES or triple speed copper interfaces. This device will be configured to use the SERDES interfaces. Controller 0 is routed to the AMC-Base cross connect mux. Controller 1 is routed to the AMC-Fabric cross connect mux.

The BCM5709S uses an external SPI flash device to store microcontroller boot code, configuration data, MAC addresses, etc. A 1 Mbit Atmel AT45DB011 device will be used for this purpose.

4.10.2 Channel Cross-Connect for BCM5709S

The channel cross connect scheme for the BCM5709S is shown below in the following two figures.

Figure 4-10 Base Channel Cross Connect

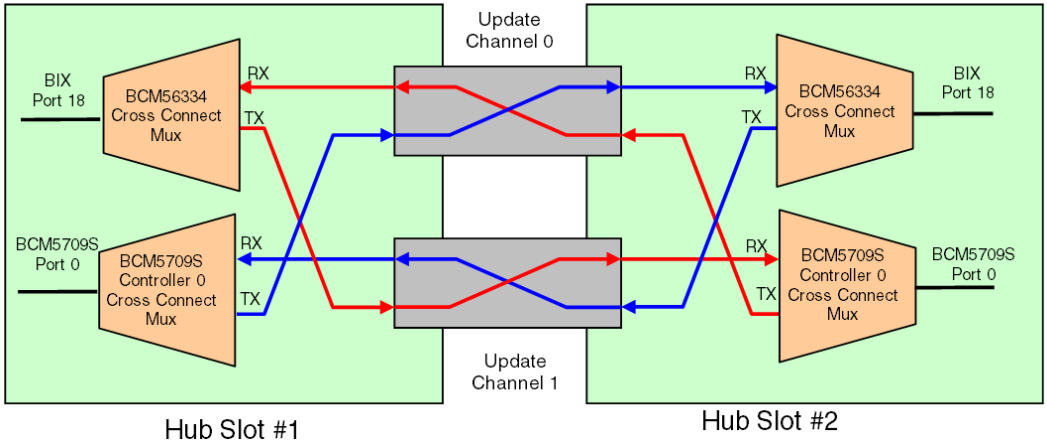
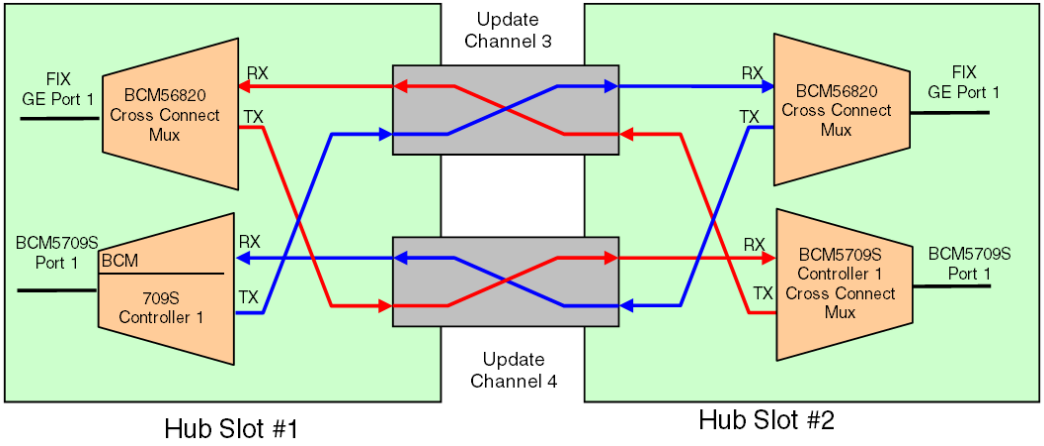


Figure 4-11 Fabric Channel Cross Connect



4.10.3 Storage Hard Disk Drive

The ATCA-F125 provides a SATA connector and mounting features to install a 2.5" SATA hard disk drive on the board. This HDD can be used to store system management data, configuration data, and boot images for the service processor or the PrAMC. An 80Gbyte extreme duty drive or equivalent may be installed to support "enterprise class" features, like permanent operation (24/7) and extended temperature range. The HDD can be accessed by either the service processor or the PrAMC processor, depending on the state of the onboard SATA mux. The mux may be controlled the service processor or the IPMC through registers in the FPGA. By default, the mux will be configured to connect the SATA drive to the service processor.

4.11 Telecom Clocking

The ATCA-F125 supports an optional telecom clocking subsystem that is responsible for the generation and distribution of traceable telecom clocks per use throughout the local shelf and up to five connected extension shelves. Specifically, the following key features are provided:

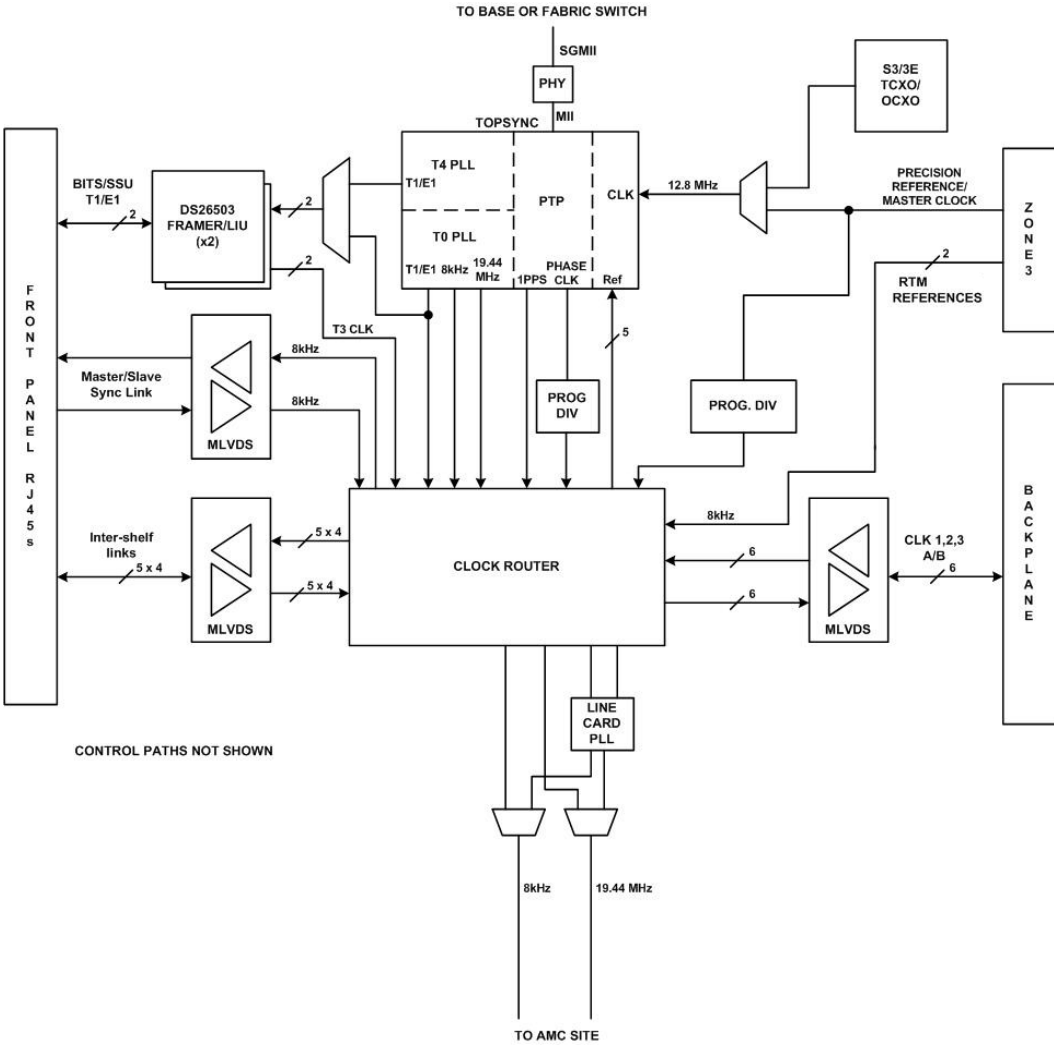
- T0 and T4 PLLs for the generation of T[0] system clocks and a T[4] SSU clock
- Dual T1/E1 ports to allow reception of redundant T[3] BITS/SSU clocks
- Stratum 3 oscillator

- Generation of a traceable clock
- Routing of telecom clocks to AMC site

4.11.1 Telecom Clocking Subsystem

This section shows an overall block diagram of the telecom clocking subsystem. Later sections elaborate on the functionality of each block.

Figure 4-12 Telecom Clocking Subsystem



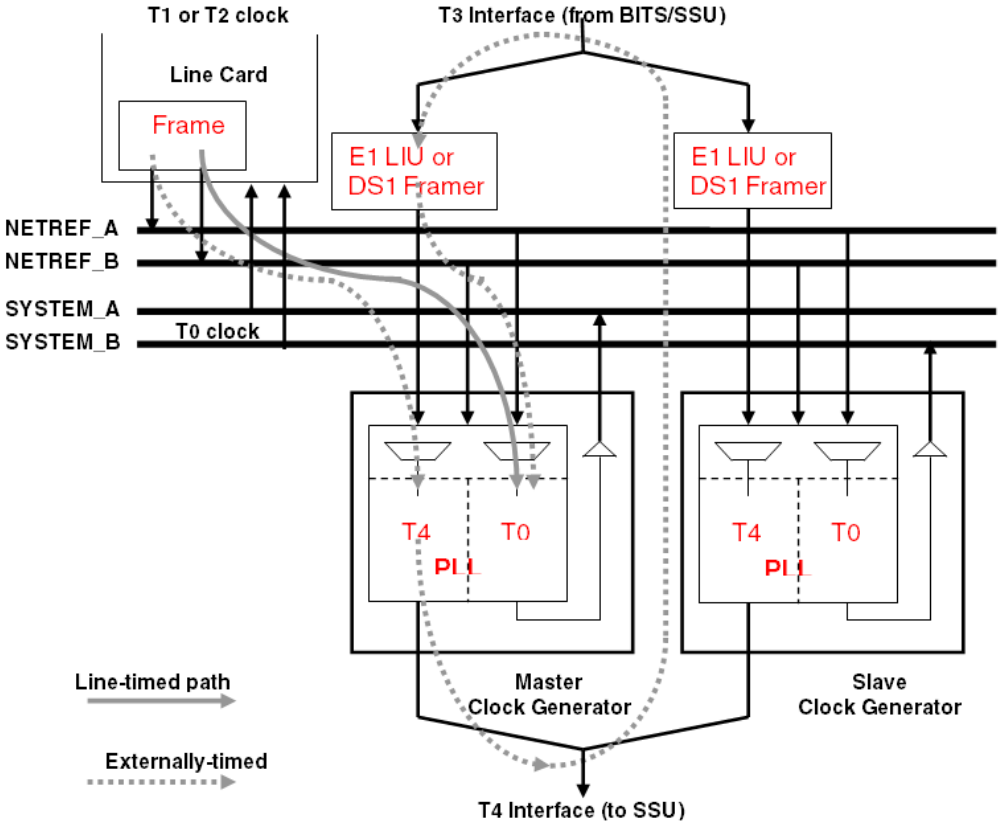
4.11.2 BITS/SSU Support

Many facilities where the ATCA-F125 is likely to be deployed, such as central offices, will include a central Building Integrated Timing Supply (BITS) or Source Synchronization Unit (SSU).

A BITS is typically an output-only device that provides a precision timing reference, known as the T[3] clock, to shelf-level products that use this for synchronizing the local telecom clocks. An SSU is similar to a BITS but can in turn synchronize itself to a linecard derived reference known as a T[4] clock.

The ATCA-F125 provides dual T1/E1 interfaces to support both BITS and SSU operation.

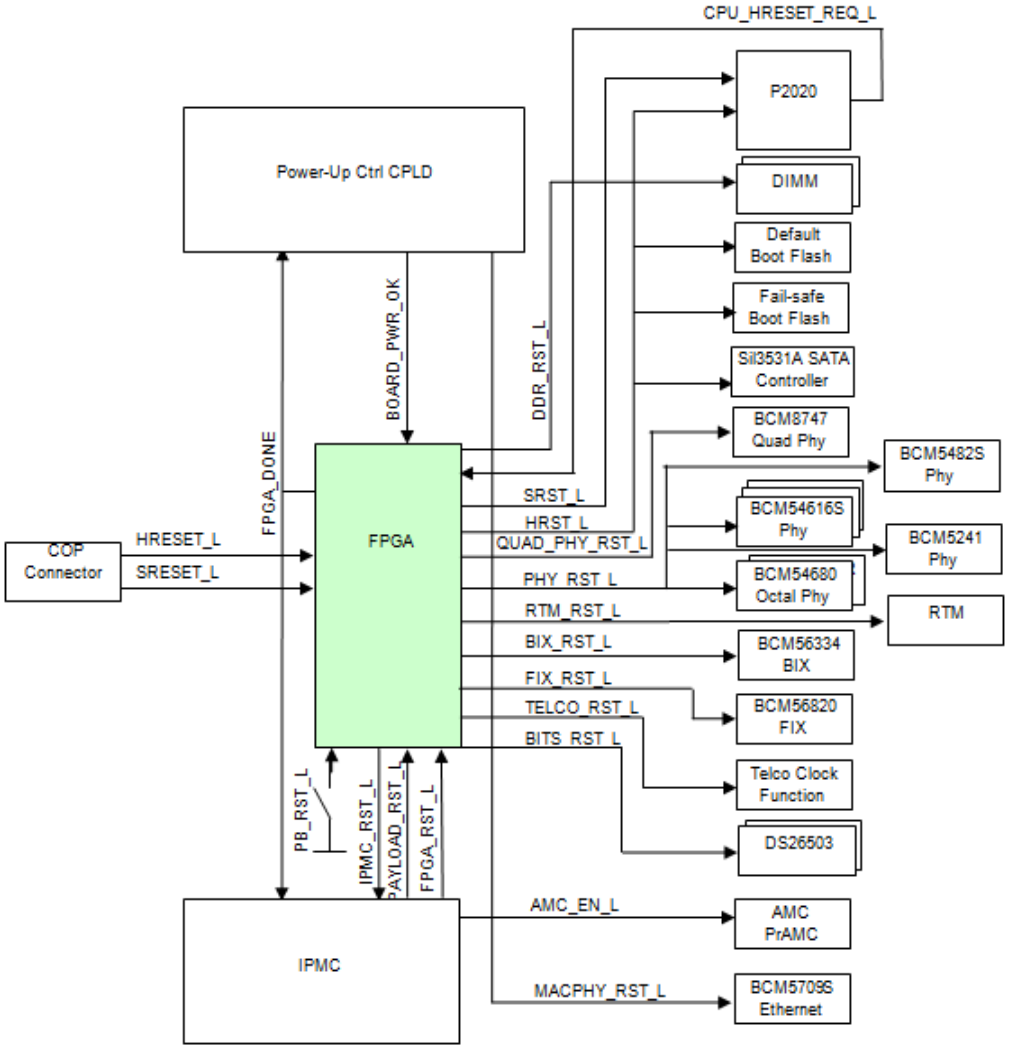
Figure 4-13 BITS/SSU Clock Flow



4.12 Reset Structure

The reset structure for the ATCA-F125 is controlled by the FPGA. The block diagram below shows the reset structure of the ATCA-F125.

Figure 4-14 Reset Structure Block Diagram



A software controlled reset register within the FPGA will provide software controlled resets to the FIX, BIX and PHY functions. The FPGA will also implement a last reset register to capture the source of the last reset generated on the board.

Table 4-7 Reset Signals

Reset Source	HRST_L	SRST_L	FIX_RST_L	BIX_RST_L	PHY_RST_L	QUAD_PHY_RST_L	TELCO_RST_L	BITS_RST_L	MACPHY_RST_L	RTM_RST_L	DDR_RST_L
BOARD_PWR_OK	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
PAYLOAD_RST_L	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No
FRONT_PANEL_RST_L	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No
HRST_REQ_L	Yes	No	No	No	No	No	No	No	No	No	No
COP_HRESET_L	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No
COP_SRESET_L	No	Yes	No	No	No	No	No	No	No	No	No
AMC_EN	No	No	No	No	No	No	No	No	Yes	No	No
AMC_PWR_GOOD	No	No	No	No	No	No	No	No	Yes	No	No
Software Control in FPGA	No	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No

4.12.1 Service Processor Core Reset Domain

The service processor core includes the P2020 QorIQ Integrated Processor, its memory and the onboard resources attached to the local bus.

4.12.1.1 Service Processor

The hard reset signal HRST_L causes the P2020 QorIQ Integrated Processor to abort all current internal and external transactions and set all registers to their default values. HRST_L may be asserted at any time completely asynchronously. HRST_L needs to be asserted during power-on reset. During HRST_L assertion, the configuration input signals are sampled into registers inside the P2020 QorIQ Integrated Processor.

The request output signal HRESET_REQ_L of the P2020 QorIQ Integrated Processor indicates to the board that a condition requiring the assertion of HRST_L has been detected. HRESET_REQ_L may be activated by a watchdog timer inside the P2020 QorIQ Integrated Processor, or by software. HRESET_REQ_L may occur at any time synchronous to the core complex bus clock and stays active until HRST_L is asserted.

The soft reset input signal SRST_L causes a machine check interrupt to both e500 cores of the P2020 QorIQ Integrated Processor. SRST_L need not to be asserted during a hard reset. SRST_L may be asserted at any time completely asynchronously.

4.12.1.2 Memory

The registers of a registered DIMM are reset by the DDR_RST_L signal.

4.12.1.3 Onboard Flash

All onboard boot flash devices which are attached to the local bus are reset in parallel when the HRST_L signal gets asserted.

4.12.1.4 Persistent Memory

The persistent memory is only reset after power-on reset. In all other onboard reset events, the persistent memory is not reset if the persistent memory feature is enabled.

4.12.2 Ethernet Switch Resets

4.12.2.1 Broadcom BCM56334

A power-on or hard reset is initiated by an active low pulse on the BIX_RST_L signal of the Broadcom BCM56334 Base Channel Switch. The initialization process loads all the pin configure modes, clears all switching tables and places the switch in a disabled and idle state.

4.12.2.2 Broadcom BCM56820

A power-on or hard reset is initiated by an active low pulse on the FIX_RST_L signal of the Broadcom BCM56820 Fabric Channel Switch. The initialization process loads all the pin configured modes, clears all switching tables and places the switch in a disabled and idle state.

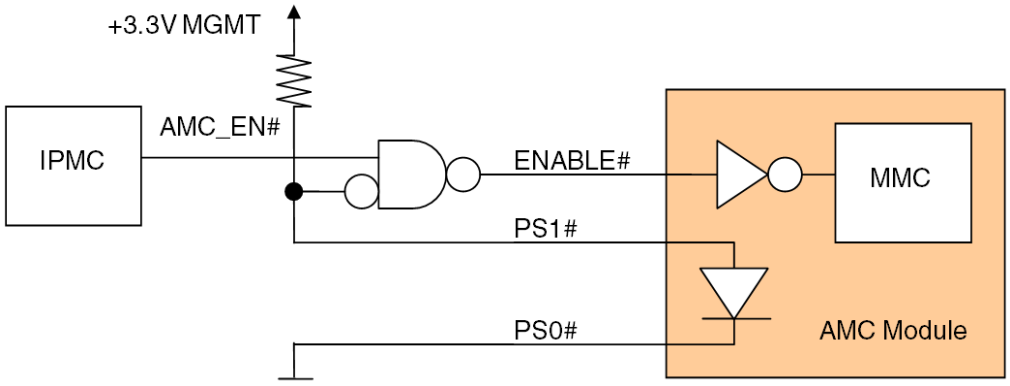
4.12.3 Physical Interconnect Devices

Broadcom PHYs uses a hardware reset pin PHY_RST_L, which resets all internal nodes to a known state. Mode pins are latched during hardware reset being deasserted. All PHYs are reset by the PHY_RST_L signal except for the BCM8747 which is reset by QUAD_PHY_RST_L.

4.12.4 AMC Bay

The IPMC on the ATCA-F125 is responsible for resetting the AMC bay. It initiates a reset cycle after an AMC module is plugged in or if the payload power of the carrier board is in a power cycle. The IPMC drives the ENABLE# signal active low as an input to the AMC module.

Figure 4-15 AMC Enable Logic



Broadcom BCM5709S Ethernet controller is reset in parallel to AMC by using the MACPHY_RST_L signal generated from the power control CPLD.

4.12.5 Rear Transition Module

The ARTM-F125 does not have an MMC. During normal operation the ARTM-F125 and the ATCA-F125 front board are treated as one reset domain using the RTM_RST_L signal from the FPGA.

4.13 Interrupt Structure

All external interrupts belonging to the service processor interrupt structure are routed to the P2020 QorIQ Integrated Processor. The PIC inside the P2020 QorIQ Integrated Processor is compliant with the OpenPIC architecture.

The interrupt controller provides interrupt management, and is responsible for receiving hardware-generated interrupts from different sources (both internal and external), prioritizing them, and delivering them to the CPU for servicing. The PIC is set to the mixed mode on ATCA-F125 so that both internal and external interrupts are delivered using normal priority and delivery mechanisms.

Some interrupt sources are collected by the onboard FPGA. This FPGA includes an interrupt source register, which reflects the actual interrupt status. The interrupt inputs of the FPGA are mapped to the IRQ[11:0] signals, which are connected to the P2020 QorIQ Integrated Processor.

Table 4-8 Interrupt Mapping

Interrupt Source		Port	Signal	Source	Type		P2020 IRQ
BCM56334	INTA		P2020 PCIE 1 INTA	Internal			0
BITS Framer 1 DS26503	INT_L		BITS1_INT_L	Direct	Active Low	OD	1
BITS Framer 2 DS26503	INT_L		BITS2_INT_L	Direct	Active Low	OD	2
DIMMs	EVENT_L		DIMM_EVENT_L	Direct	Active Low	OD	3
88SE6121 SATA	INTA		P2020 PCI2 INTA	Internal			4
RTM FPGA	INT_L		RTM_INT_L	Direct	Active Low	LVTTL	5
FPGA UART	UART_INT		SP_IRQ_6	FPGA (ORed)	Active Low	LVTTL	6
IPMC LPC	SERIRQ_INTOUT						
Watchdog Timer	1st stage WDT						

Table 4-8 Interrupt Mapping (continued)

Interrupt Source		Port	Signal	Source	Type		P2020 IRQ
BIX Octal PHY 1 BCM54680-1	IRQ_L	1-8	SP_IRQ7	FPGA (ORed)	Active Low	LVTTL	7
BIX Octal PHY 2 BCM54680-2	IRQ_L	1-8					
BIX PHY 3 BCM54616S-1	IRQ_L	1					
TopSync PHY BCM54616S-2	IRQ_L	1					
Front Panel PHY BCM54616S-3	IRQ_L	1					
UC2 PHY BCM5482S	IRQ_L	1					
SP-to-BIX PHY BCM5482S	IRQ_L	2					
BCM56820	INTA		P2020 PCIE 3 INTA	internal			8

Table 4-8 Interrupt Mapping (continued)

Interrupt Source		Port	Signal	Source	Type		P2020 IRQ
Quad Optical PHY BCM8747	LASI1_L PCMULK1 PCDRLK1 PLOSB1	1	SP_IRQ9	FPGA (ORed)	Active Low	LVTTL	9 (GPIO2)
	LASI2_L PCMULK2 PCDRLK2 PLOSB2	2					
	LASI_3 PCMULK3 PCDRLK3 PLOSB3	3					
	LASI4_LPC MULK4 PCDRLK4 PLOSB4	4					
BIX SFP+ 1	ABS_INT						
	FLT_INT						
	LOS_INT						
BIX SFP+ 2	ABS_INT						
	FLT_INT						
	LOS_INT						
FIX SFP+ 1	ABS_INT						
	FLT_INT						
	LOS_INT						
FIX SFP+ 2	ABS_INT						
	FLT_INT						
	LOS_INT						

Table 4-8 Interrupt Mapping (continued)

Interrupt Source		Port	Signal	Source	Type		P2020 IRQ
FPGA Clock Monitor	Clock Monitor Done INT		SP_IRQ10	FPGA	Active Low	LVTTL	10 (GPIO3)
FPGA Clock Monitor	Clock Monitor Range INT						
ACS9510	TOPSYNC_INT_S						
PERSISTENT MEMORY	FPGA		SP_IRQ11	FPGA	Active Low	LVTTL	11 (GPIO4)

5.1 Overview

This product uses Das U-Boot, a boot loader software based on the GNU Public License. It boots the blade and is the first software to be executed on after it is powered on.

Its main functions are:

- Initialize the hardware
- Pass boot parameters to the Linux kernel
- Starting the Linux kernel
- Update Linux kernel and U-boot images

This section describes U-Boot features and procedures that are specific to the ATCA-F125. For general information on U-Boot, see http://www.denx.de/wiki/U-Boot/WebHome.

5.2 Accessing U-Boot

The U-boot can be accessed using the serial interface connector at the face plate of the ATCA-F125. To connect, you need a computer with a serial interface connector and a terminal emulation software such as HyperTerm running on it.

1. Connect the console interface connector of the ATCA-F125 to the serial interface connector of the computer.
2. Configure the terminal software to use the access parameters that are specified in U-Boot. By default, the access parameters are as follows:
   - Baud rate: 9600
   - Flow control: XON/XOFF
   - PC ANSI
   - 8 data bits
   - No parity

- 1 stop bit

These serial access parameters are the default values. These can be changed from within U-Boot. For details refer to the U-boot documentation.

3. Boot the ATCA-F125 by resetting it or powering it up.
4. Press CTRL+C when you see a prompt onscreen.
   U-Boot aborts the boot sequence and enters into a command line interface mode.

If you want to disable the auto-boot feature of U-boot and make sure that U-Boot directly enters into the command line interface mode after the next reboot/power up, enter the following command: **`setenv bootdelay -1 saveenv`**

5.3 Configuring Boot Options

5.3.1 Configuring U-Boot for Network Boot

In this mode, U-Boot downloads and boots the Linux kernel from an external TFTP server and mounts a root file system located on a network server.

This procedure assumes that the ATCA-F125 is connected to a TFTP server and that the U-Boot command nfsboot has been defined. The external TFTP server must be connected using the ATCA-F125 face plate connector "ETH5", which is the Ethernet management interface. Any other interfaces, such as the base or fabric interfaces, are not yet functional at this stage of the boot phase, as the corresponding drivers are not initialized yet.

For more information, see the U-Boot documentation.

1. Execute the following commands to specify the IP addresses of the ATCA-F125 and the TFTP server by entering the following commands:
   ```
   setenv ipaddr <IP address of ATCA-F125>
   setenv serverip <IP address of TFTP server>
   ```

2. Specify the names of the Linux kernel image and the NFS root directory.
```
setenv bootfile <Linux kernel image file name>
setenv rootpath <NFS root directory>
setenv blobfile <dtb file name>
```

3. Configure U-Boot to use NFS boot.
```
setenv bootcmd $nfsboot
```

4. Depending on your network configuration, you may have to specify a gateway IP address and a netmask. Use the following commands:
```
setenv gatewayip <gateway IP>
setenv netmask <netmask>
```

5. Enter `saveenv`, and then enter `boot`.

5.3.2 Configuring U-Boot to Boot from RAM Disk

If the Linux kernel and root file system are available as RAM disk image, you may want to boot from that RAM disk.

This procedure assumes that the U-Boot command `ramboot` has been defined and that the RAM disk image is stored on an external TFTP server that is connected to the ATCA-F125. During each boot process, the image is downloaded from the TFTP server into the main memory of the blade. The external TFTP server must be connected using the ATCA-F125 face plate connector "BBP ETH", which is the Ethernet management interface. Any other interfaces, such as the base or fabric interfaces, are not yet functional at this stage of the boot phase, as the corresponding drivers are not initialized yet.

1. Specify the IP address of the ATCA-F125 and the TFTP server that contains the RAM disk:
```
setenv ipaddr <IP address of ATCA-F125>
setenv serverip <IP address of TFTP server>
```

2. Depending on your network configuration, you may have to specify a gateway IP address and a netmask. Use the following commands:
```
setenv gatewayip <gateway IP>
setenv netmask <netmask>
```

3. Specify the name of the RAM disk image file:
```
setenv ramdiskfile <filename>
setenv blobfile <dtb file name>
```

4. Configure U-Boot to boot from RAM disk:

```
setenv bootcmd $ramboot
```

5. Specify the name of the kernel image file:
   ```
   setenv bootfile <filename>
   ```
6. Enter `saveenv`, and then enter `boot` .

5.3.3 Configuring U-Boot to Boot from Flash

The blade provides two redundant boot flashes which contain the U-boot images and also Linux kernel images. It also contains two redundant root file systems.

This section describes how to configure U-boot to boot a Linux kernel stored in the boot flash and to mount the root file system in the user flash. The procedure uses the U-Boot script flashboot, which has been predefined by Artesyn Embedded Technologies.

1. Configure U-boot to boot from flash:
   ```
   setenv bootcmd $flashboot
   ```
2. Depending on your system configuration, you may want to specify network parameters as follows:
   ```
   setenv ipaddr <IP address>
   setenv serverip <IP address>
   setenv netmask <netmask>
   setenv gatewayip <IP address>
   ```
3. Enter `saveenv`, and then enter `boot`.

5.4 Selecting the Boot Flashes

This configuration determines which flash the blade is to boot from on the next restart. You can either boot through IPMI or through a U-Boot command.

- Using IPMI - This option uses the System Boot Options feature. For more information, see the ATCAF125: Control using IPMI Programmer's Reference.
- Using U-Boot command - Use `bootsel 0|1|switch`, where 0 selects boot flash 0, 1 selects boot flash 1 and switch selects the currently stand-by boot flash.

Generally, there is a fixed link between the U-Boot firmware and the kernel image in the respective boot flash. This means that when the U-Boot in a particular flash is executed, it subsequently boots the kernel image in the same flash.

If necessary, however, you can select the kernel to boot manually using the following commands:

- `setenv kerneladdr e0000000` (for the kernel in the currently active boot flash)
- `setenv kerneladdr e2000000` (for the kernel in the currently stand-by boot flash).

Use these commands with care.

Each of the two U-Boot firmware images in the two flashes holds a separate set of U-Boot environmental variables/boot parameters. Therefore, after switching to another boot flash, you may need to reconfigure the boot parameters/environmental variables of the new U-Boot image according to your needs.

5.5 Using the Persistent Memory Feature

Persistent memory means that the memory RAM is not deleted during a reset. Memory content can be deleted by performing a power cycle or by temporarily removing the power and then powering up the blade again. This feature is enabled by default on the ATCA-F125.

This feature can be useful in many situations, including:

- Analyzing kernel logs after a Linux kernel panic
- Defining a particular memory region for the persistent storage of application specific data

Analyzing Kernel Log Files after a Kernel Panic

If the Linux OS running on the ATCA-F125 indicates a kernel panic and you wish to analyze the cause, then you can issue a reset (using the face plate button for example) and subsequently analyze kernel log files. Because of the persistent memory feature, these log files are still available in the memory.

To analyze the kernel log files:

1. Issue a reset.
2. Connect to U-Boot. For more information, see *Accessing U-Boot* on page 101.
3. Using the kernel memory map, find the memory addresses of the kernel logs.
4. To display the kernel logfile at any of these memory addresses, enter the following command: `.printf (<memory address>)`

The persistent memory feature can also be useful in the storage of application-specific data. Use the standard U-Boot variable `pram` to reserve a memory region (at the end of the physical memory). This allows the reserved region to not be overwritten by U-Boot. U-Boot reports less memory to the Linux kernel (through the `mem` parameter) so that Linux will not use it either.

5.6 Memory Map

The following table shows the physical address map of the ATCA-F125.

Table 5-1 Physical Address Map

Device	Start Address	Size
DDR3-RAM	0x00000000	Max. 2 GByte
P2020 CPU	0xFFE00000	32 Kbytes
FPGA	0xFFDF0000	32 Kbytes
BITS1	0xFFA00000	32 Kbytes
BITS2	0xFFA100000	32 Kbytes
Stand-by boot flash	0xE2000000	32 Mbytes
Active boot flash	0xE0000000	32 Mbytes

Regardless which of the two boot flashes is selected as the currently active boot device (using IPMI), the start address is always mapped to 0xE0000000.

5.7 Linux Devices

The following table lists all predefined Linux character devices and the respective memory blocks which they are assigned to.

Table 5-2 Linux Devices

Linux Device Name	Content	Memory Area	Hardware Device
/dev/mtd0	Kernel image	0xE0000000 - 0xE05FFFFF	Active boot flash
/dev/mtd1	Empty	0xE0600000 - 0xE1EFFFFF	Active boot flash
/dev/mtd2	Kernel DTB	0xE1F00000 - 0xE1F1FFFF	Active boot flash
/dev/mtd3	U-boot parameters	0xE1F00000 - 0xE1F1FFFF	Active boot flash
/dev/mtd4	U-Boot image	0xE2000000 - 0xE25FFFFF	Active boot flash
/dev/mtd5	Kernel image	0xE2000000 - 0xE25FFFFF	Stand-by boot flash
/dev/mtd6	Empty	0xE2600000 - 0xE3EFFFFF	Stand-by boot flash
/dev/mtd7	Kernel DTB	0xE3F00000 - 0xE3F1FFFF	Stand-by boot flash
/dev/mtd8	U-Boot boot parameters	0xE3F40000 - 0xE3F5FFFF	Stand-by boot flash
/dev/mtd9	U-Boot image	0xE3F80000 - 0xE3FFFFFF	Stand-by boot flash
/dev/mtd10	FPGA	-	-

5.8 Power-On Self Test

When the ATCA-F125 is booted, U-boot executes a series of Power-On Self test (POST) routines. These routines check the functionality of different controllers and other on-board resources. The result is stored in memory and has the following format.

Table 5-3 POST Result Format

Offset	Description
0x0	Magic word: 0xAA55FCE0
0x4	CRC32 checksum over the POST result string
0x8	POST result string. This is a zero-terminated string based on the following XML-like syntax:[<T=tag>[<E>Error_description</E>]*</T>]* `tag` identifies the device that was tested. If no POST error was detected, then the closing tag `</T>` follows immediately after the opening tag. `Error_Description` contains an error description of the corresponding <T> tag. Note that the <T> tags can be nested, if for example several subtests are performed in one device. See the following example. <T=FPGA></T> <T=DRAM><E>Address line</E></T> <T=PCI><T=BIX></T><T=FIX2></T><T=FIX1></T></T> <T=SPI><T=BEXT></T></T> <T=I2C><T=CTRL1></T><T=CTRL2></T></T> <T=MDIO><T=PHY0></T><T=PHY1></T><T=PHY2> </T><T=PHY3></T></T>

Information about the POST status can also be obtained by reading the SYS FW PROGRESS IPMI sensor. Depending on the POST status, the sensor holds the following values.

Table 5-4 Post Results in SYS FW PROGRESS IPMI Sensor Reading Data

Value	Description
0x01	No memory detected
0x02	Memory error. The address and data line test failed.
0x0b	U-boot image CRC mismatch detected

Table 5-4 Post Results in SYS FW PROGRESS IPMI Sensor Reading Data (continued)

Value	Description
0x0D	Wrong CPU speed
0xfd	Artesyn Embedded Technologies specific POST error code. For more information, see Table "SYS FW PROGRESS IPMI Sensor - POST Error Event Codes" on page 109.
0x00	One of the remaining POST errors was detected.

Table 5-5 SYS FW PROGRESS IPMI Sensor - POST Error Event Codes

Event Data (Byte 3)	Description
0x1E	Error accessing the switch devices
0x03	Error in network loop back test
0x20	Error in network PHY test
0x1F	Error in glue logic (FPGA) test
0x0A	Error in I2C bus test
0x16	Error in RTC test
0x09	Error in flash test
0x21	Error in CPU test
0x22	Error in PCI bus test

5.8.1 POST Routines

The following table describes that POST routines are performed.

Table 5-6 POST Routines

Device	Description
CPU	Check PLL configuration (PORPLLSR register). Check device configuration (PORDEVSR register)
FPGA	Register sanity check. The version code is checked. It must not be 0x00 or 0xFF.
DRAM	Address line and data-line test.

Table 5-6 POST Routines (continued)

Device	Description
Switch devices	The PCI interface is checked as follows: ● Check for configuration space access (vendor/device ID) ● Perform walking-one test on first memory-mapped register
Base interface extender/SPI	Data test on LED register page 0, offset 0x12
I2C buses	Check whether bus addresses 0x50,0x51, 0x52 are accessible on bus 0 and 0x50, 0x6E on bus 1.
RTC	Checks whether the second counter is advancing. Compares the number of CPU ticks in one second against the expected system clock frequency (66 MHz)
MDIO/PHY	Attempts to read model and device ID from PHY address 0..3
TSEC network port	The PHY for each TSEC port is configured to loop back mode, 100 and 1000 MBPS, and 10000 loop back packets are sent and verified.
Boot flash	Flash devices are sent into CFI query mode and the query string is verified.
RTM	Check connectivity of 10G repeater devices on RTM

5.8.2 Controlling the Execution of the POST

The environment variable `post_control` allows to configure when POST is executed. Possible values of `post_control` and their meaning are described in the following table.

Table 5-7 Environment Variable post_control

Value	Description
`off`	Disables POST altogether
`always`	POST is executed after all types of blade resets

Table 5-7 Environment Variable post_control (continued)

Value	Description
`hard`	POST is executed only after hard resets. A hard reset is a reset of the entire payload and can be issued by the following reset sources: ● Watchdog inside CPU ● Boot sequence failure ● Software ● Face plate reset key A hard reset is NOT an CPU internal reset, such as a reset issued through the U-Boot command `reset` or the Linux command `reboot`.

You can start the POST execution manually by invoking the following command at the U-Boot command line interface: `.post_all()`

As you can see from the syntax, this command invokes an underlying C function which starts the POST execution. This command can be invoked at any time and it is independent of the environment variable post_enable.

5.9 ATCA-F125 Specific U-Boot Commands

Table 5-8 ATCA-F125 Specific U-Boot Commands

Command	Description
bparams_set	Allows to configure IPMI system boot options
hreset	Issues a hard reset on the ATCA-F125. A hard reset resets the entire payload.
bootsel 0 | 1 | switch	Selects the boot flash which the ATCA-F125 is to boot from after the next restart. 0 selects boot flash 0, 1 selects boot flash 1, and switch selects the currently not selected boot flash, i.e. switches between the boot flashes.

5.10 ATCA-F125-Specific U-Boot Environment Variables

Table 5-9 ATCA-F125 Specific U-Boot Environment Variables

Environment Variable	Description
`post_control`	See Table "Environment Variable post_control" on page 110
`phy_localloop`	Can be set to 10/100/1000 to configure a ETSEC port into PHY local loopback mode
`firmware_build`	Firmware-build count (read-only)
`inicmd`	Can be used to define a command sequence to be executed at the end of the boot sequence, i.e. before the shell or bootcmd are executed
`drvargs`	Contains blade-specific values for the Linux kernel command line. It should be part of the bootargs environment variable.
`reset_cause`	Indicates the reason for the last reset. Possible values are: ● `warm`: CPU reset ● `power`: Power-on ● `frpl_pb`: Face plate push button ● `rtm_pb`: RTM push button) ● `cpu_hreset`: CPU HRESET_REQ ● `cop_hreset`: COP HRESET ● `ipmc:`: IPMC reset request ● `sw_wdog`: Software watchdog reset ● `ini_wdog`: Initial watchdog reset
`post_result`	Contains the POST result string, if POST has been executed
`rom_corruption`	Set to 1 if the CRC of the u-boot image is incorrect

5.11 Updating U-Boot

This procedure describes how you can update U-Boot using the U-Boot command line interface. It is assumed that the new U-Boot image is placed in the download directory of a TFTP server which has network access to the ATCA-F125. All files names and IP addresses shown below were only chosen for illustration purposes. This procedure consists of updating the stand-by boot flash and then switching the boot flashes, so that after the next reset/boot flash the ATCA-F125 boots from the new active, previously updated boot flash.

It is recommended that you update the U-boot firmware using the BBS/Linux or the shelf manager. Refer to the respective documentation for further details.

When updating the U-Boot image, the U-Boot boot parameters are not updated. They remain as they were before the update. The boot parameters are stored separately from the U-Boot image in a memory area within each boot flash. See also Table "Linux Devices" on page 107.

Each of the two U-Boot firmware images in the two flashes holds a separate set of U-Boot environmental variables/boot parameters. Therefore, after switching to another boot flash, you may need to reconfigure the boot parameters/environmental variables of the new U-Boot image according to your needs.

1. Connect to U-boot. For more information, see *Accessing U-Boot* on page 101.
2. Specify the IP address of the ATCA-F125 and the TFTP server by entering the following commands:
   ```
   setenv ipaddr <IP address of ATCA-F125>
   setenv serverip <IP address of TFTP server>
   ```
3. Depending on your network configuration, you may have to specify a gateway IP address as well as a netmask:
   ```
   setenv gatewayip <gateway IP>
   setenv netmask <netmask>
   ```

4. Load the image to the RAM.
   `tftpboot $loadaddr <U-boot file name, for example: u-boot-1.1.6-59.bin>`

```
Speed: 1000, full duplex
Using eTSEC0 device
TFTP from server 172.16.128.254; our IP address is 172.16.13.2
Filename 'u-boot-1.1.6-59.rom'.
Load address: 0x300000
Loading:
#################################################################
#####################################
done
Bytes transferred = 524288 (80000 hex)
```

5. Unprotect the currently stand-by U-Boot bank:
   protect off 2:252-258

```
Un-Protect Flash Sectors 252-258 in Bank # 1....... done
```

protect off 2:252-258 addresses to the currently stand-by U-Boot bank, while **protect off 1:252-258** addresses the currently active U-Boot bank.

6. Erase the following flash area in the currently stand-by U-Boot bank:
   `erase e3f80000 e3ffffff`

```
........ done
Erased 4 sectors
```

The currently stand-by U-boot bank is always mapped to the start address 0xE2000000, while the currently active U-boot bank is always mapped to 0xE0000000.

If you wish to set a particular U-boot bank into the active state, then you need to set the System Boot Options Parameter #96 (bit 0) appropriately and reboot. If this bit is set to 0, then U-boot bank 1 will be active after the next reboot. If the bit is set to 1, then U-boot bank 2 will be active. Note that depending on the blade's IPMI firmware version, the switch between the U-boot banks may be effective immediately.

7. Copy the image from the RAM to the currently stand-by U-boot bank:
   `cp.b $loadaddr e3f80000 80000`

```
Copy to Flash...
done
```

8. Make stand-by U-boot active and vice versa, by entering the following command:
   `bootsel switch`
9. In order to boot the new U-Boot, reset the blade.

Battery Exchange

A.1 Replacing the Battery

The battery provides data retention of seven years summing up all periods of actual data use. Artesyn Embedded Technologies therefore assumes that there is usually no need to replace the battery except, for example, in case of long-term spare part handling.

NOTICE

Board/System Damage

- Incorrect replacement of lithium batteries can result in a hazardous explosion.
- Therefore, replace the battery as described in this chapter.

Data Loss

- If the battery voltage drops below the minimum required level, the RTC time will be lost.
- Therefore, replace the battery before seven years of actual battery use have elapsed.

Data Loss

- Replacing the battery will result in RTC data loss. The RTC will have to be re-initialized after the battery is replaced.

Data Loss

- Installing another battery type other than what is mounted at board delivery may cause limited operation. This is because other battery types may be specified for other environments or may have a shorter lifespan. Therefore, only use the same type of lithium battery as is already installed.

Replacement Procedure

To replace the battery, proceed as follows:

1. Remove the battery. See Figure 3-2 for location.

NOTICE

PCB and Battery Holder Damage

- Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent this damage, do not use a screw driver to remove the battery from its holder.

2. Install the new battery following the "positive" and "negative" signs.

B.1 Artesyn Embedded Technologies - Embedded Computing Documentation

The publications listed below are referenced in this manual. You can obtain electronic copies of Artesyn Embedded Technologies - Embedded Computing publications by contacting your local Artesyn sales office. For released products, you can also visit our Web site for the latest copies of our product documentation.

1. Go to www.artesyn.com/computing.
2. Under SUPPORT, click **TECHNICAL DOCUMENTATION**.
3. Under FILTER OPTIONS, click the Document types drop-down list box to select the type of document you are looking for.
4. In the **Search** text box, type the product name and click GO.

Table B-1 Artesyn Embedded Technologies - Embedded Computing Publications

Document Title	Publication Number
ATCA-F125 Quick Start Guide	6806800K92
ATCA-F125 Safety Notes Summary	6806800K94
RTM-ATCA-F125 Installation and Use	6806800K30
RTM-ATCA-F125Quick Start Guide	6806800M56
RTM-ATCA-F125 Safety Notes Summary	6806800M15
SRS on ATCA-F125 Document Collection	6806800L89

B.2 Related Specifications

Refer to the table below for related specifications. Note that the information in these documents are subject to change without notice.

Table B-2 Specifications

Organization	Document
PICMG	ATCA Base Specification Revision 3.0 Ethernet/Fiber Channel Specification Revision 1.0 Advanced Mezzanine Card Base Specification Revision 2.0

Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

Artesyn Embedded Technologies intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your Artesyn Embedded Technologies representative.

The product has been designed to meet the standard industrial safety requirements. It must only be used in its specific area of office telecommunication industry, industrial control, and development. It must not be used in safety critical components, life supporting devices or on aircraft.

Only personnel trained by Artesyn Embedded Technologies or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product. The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only factory authorized service personnel or other qualified service personnel is allowed to remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local Artesyn Embedded Technologies representative for service and repair to make sure that all safety features are maintained.

Artesyn Embedded Technologies and our suppliers take significant steps to make sure that there are no bent pins on the backplane or connector damage to the boards prior to leaving the factory. Bent pins caused by improper installation or by inserting boards with damaged connectors could void the Artesyn Embedded Technologies warranty for the backplane or boards.

This product operates with dangerous voltages that can cause injury or death. Use extreme caution when handling, testing, and adjusting this equipment and its components.

EMC

FCC Class A
This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules, EN55022. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, can cause harmful interference to radio communications.
Operation of this equipment in a residential area is likely to cause harmful interference in which case the user is required to correct the interference at his own expense.
To ensure EMC protection use only shielded cables when connecting peripherals to assure that appropriate radio frequency emissions compliance is maintained. Installed blades must have the face plates installed and all vacant slots in the shelf must be covered.

For applications where this product is provided without a face plate, or where the face plate has been removed, your system chassis/enclosure must provide the required electromagnetic interference (EMI) shielding to maintain EMC compliance.

Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a compliant system maintains the required performance.

As soon as you modify the product or change the default configuration you are responsible for complying with all relevant regulatory standards.

VCCI

This is a Class A product based on the standard of the Voluntary Control Council for Interference by Information Technology Interference (VCCI). If this equipment is used in a domestic environment, radio disturbance can arise. When such trouble occurs, the user is required to take corrective actions.

Installation

Damage of Circuits
Electrostatic discharge and incorrect installation and removal of the product can damage circuits or shorten its life.
Before touching the product make sure that you are working in an ESD-safe environment or wearing an ESD wrist strap or ESD shoes. Hold the product by its edges and do not touch any components or circuits.

Damage of the Product and Additional Devices and Modules
Incorrect installation or removal of additional devices or modules damages the product or the additional devices or modules.
Before installing or removing additional devices or modules, read the respective documentation and use appropriate tools.

Blade Damage
Incorrect installation of the blade can cause damage of the blade,
Only use handles when installing/removing the blade to avoid damage/deformation to the face plate and/or PCB.

Damage to blade/Backplane or System Components
Bent pins or loose components can cause damage to the blade, the backplane, or other system components. Therefore, carefully inspect the blade and the backplane for both pin and component integrity before installation.

Data loss
Removing the blade with the blue LED still blinking causes data loss. Wait until the blue LED is permanently illuminated before removing the blade.

System Damage
WARNING: The intra-building port(s) of the equipment or subassembly is suitable for connection to intra-building or unexposed wiring or cabling only. The intra-building port(s) of the equipment or subassembly MUST NOT be metallically connected to interfaces that connect to the OSP or its wiring. These interfaces are designed for use as intra-building interfaces only (Type 2 or Type 4 ports as described in GR-1089) and require isolation from the exposed OSP cabling. The addition of Primary Protectors is not sufficient protection in order to connect these interfaces metallically to OSP wiring.

Operation

Blade Damage
High humidity and condensation on the blade surface causes short circuits. Do not operate the blade outside the specified environmental limits. Make sure the blade is completely dry and there is no moisture on any surface before applying power. Do not operate the blade below -5°C.

Overheating and Blade Damage
Operating the blade without forced air cooling may lead to overheating and thus damage of the blade. When operating the blade, make sure that forced air cooling is available in the shelf.

Injuries or Short Circuits
Blade or power supply In case the ORing diodes of the blade fail, the blade may trigger a short circuit between input line A and input line B so that line A remains powered even if it is disconnected from the power supply circuit (and vice versa). To avoid damage or injuries, always check that there is no more voltage on the line that has been disconnected before continuing your work.

Configuration Switches/Jumpers

Product Malfunction
Switches marked as “Reserved” might carry production-related functions and can cause the product to malfunction if their setting is changed.
Do not change settings of switches marked as “reserved”.

Product Damage
Setting/resetting the switches during operation can cause damage to the product.
Check and change switch settings before you install the product.

Product Damage
Too much force may damage the reset switch.
Use minimal force when pressing the reset switch.

Cabling and Connectors

Blade Damage
The RJ-45 connector(s) on the face plate are twisted-pair Ethernet (TPE) or E1/T1/J1 interfaces. Connecting an E1/T1/J1 line to an Ethernet connector may damage the product.

- Make sure that TPE connectors near your working area are clearly marked as network connectors.
- Verify that the length of an electric cable connected to a TPE bushing does not exceed 100 meters.
- Make sure the TPE bushing of the system is connected only to safety extra low voltage circuits (SELV circuits).

If in doubt, ask your system administrator.

AMC Module

Limitation of Operating Temperature Range.
Installing AMC modules with small operating temperature ranges into the ATCA-F125 may further restrict the operating temperature range of the ATCA-F125. Make sure that the operating temperature of any installed AMC modules and the ATCA-F125 as a bundle are within allowed limits

Poor Shelf Cooling and EMC Compliance Violation
An empty AMC bay may result in poor shelf cooling and strong EMC radiation and thus lead to EMC compliance violation. Therefore, always cover empty or unused AMC bays with a filler panel.

Hot Swap

Data Loss
Removing the product with the blue LED still blinking causes data loss.
Wait until the blue LED is permanently illuminated before removing the product.

SFP/SFP+ Modules

Personal Injury and Damage of the RTM and SFP/SFP+ Modules
Installing and using SFP/SFP+ modules which are not fully certified and which do not meet all relevant safety standards may damage the RTM and the SFP/SFP+ modules and may lead to personal injury.
Only use and install SFP/SFP+ modules which are fully certified and which meet all relevant safety standards.

Personal Injury
Optical SFP/SFP+ modules may be classified as laser products. When installing and using any of these SFP/SFP+ modules, the regulations which correspond to the respective laser class apply to the whole RTM. Not complying to these regulations may lead to personal injury.
When installing and using optical SFP/SFP+ modules which are classified as laser products, make sure to comply to the respective regulations.

Eye Damage
Optical SFP/SFP+ modules may emit laser radiation when no cable is connected. This laser radiation is harmful to your eyes.
Do not look into the optical lens at any time.

SFP/SFP+ Module Damage
The optical port plug protects the optical fibres against dirt and damage. Dirt and damage can render the SFP/SFP+ module inoperable.
Only remove the optical plug when you are ready to connect a cable to the SFP/SFP+ module.
When no cable is connected, cover the port with an optical port plug.

Battery

Data Loss
Installing another battery type than the one that is mounted at product delivery may cause data loss since other battery types may be specified for other environments or may have a shorter lifetime.
Only use the same type of lithium battery as is already installed.

PCB and Battery Holder Damage
Removing the battery with a screw driver may damage the PCB or the battery holder.
Do not use a screw driver to remove the battery from its holder.

Environment

Environmental Damage
Improperly disposing of used products may harm the environment.
Always dispose of used products according to your country's legislation and manufacturer's instructions.

Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Systems innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am System zur Folge haben.

Artesyn Embedded Technologies ist darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem System in diesem Handbuch bereit zu stellen. Da es sich jedoch bei dem System um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von Artesyn Embedded Technologies.

Das Produkt erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschließlich für Anwendungen in der Telekommunikationsindustrie, im Zusammenhang mit Industriesteuerungen und in der Entwicklung verwendet werden. Es darf nicht in sicherheitskritischen Anwendungen, lebenserhaltenden Geräten oder in Flugzeugen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Artesyn Embedded Technologies ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

Halten Sie sich von stromführenden Leitungen innerhalb des Systems fern. Entfernen Sie auf keinen Fall die Systemabdeckung. Nur werksseitig zugelassenes Wartungspersonal oder anderweitig qualifiziertes Wartungspersonal darf die Systemabdeckung entfernen, um Systemkomponenten zu ersetzen oder andere Anpassungen vorzunehmen.

Installieren Sie keine Ersatzteile oder führen Sie keine unerlaubten Veränderungen am System durch, sonst verfällt die Garantie. Wenden Sie sich für Wartung oder Reparatur bitte an die für Sie zuständige Geschäftsstelle von Artesyn Embedded Technologies. So stellen Sie sicher, dass alle sicherheitsrelevanten Aspekte beachtet werden.

Artesyn Embedded Technologies und unsere Zulieferer unternehmen größte Anstrengungen um sicherzustellen, dass sich Pins und Stecker von Boards vor dem Verlassen der Produktionsstätte in einwandfreiem Zustand befinden. Verbogene Pins, verursacht durch fehlerhafte Installation oder durch Installation von Boards mit beschädigten Steckern kann die durch Artesyn Embedded Technologies gewährte Garantie für Boards und Backplanes erlöschen lassen.

Dieses Produkt wird mit gefährlichen Spannungen betrieben, die zu Verletzungen und Tod führen können. Seien Sie im Umgang mit dem Produkt und beim Testen und Anpassen des Produktes und seiner Komponenten äußerst vorsichtig.

EMV

FCC Class A
Das Produkt wurde getestet und erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Produkts in Geschäfts-, Gewerbe- sowie Industriebereichen gewährleisten. Das Produkt arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.
Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen; in diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen und dafür aufzukommen.
Benutzen Sie zum Anschließen von Peripheriegeräten ausschließlich abgeschirmte Kabel. So stellen Sie sicher, dass ausreichend Schutz vor Störstrahlung vorhanden ist. Die Blades müssen mit der Frontblende installiert und alle freien Steckplätze müssen mit Blindblenden abgedeckt sein.
Änderungen, die nicht ausdrücklich von Artesyn Embedded Technologies erlaubt sind, können Ihr Recht das System zu betreiben zunichte machen.

Wenn dieses Produkt ohne Frontblende ausgeliefert wird oder wenn die Frontblende entfernt wird, muss Ihr System die notwendigenSchutzmechnismen gegen elektromagnetische interferenzen bereitstellen, um die Einhaltung der eletromagnetischen Verträglichkeit des Systems zu gewährleisten.

Boardprodukte werden in einem repräsentativen System getestet, um zu zeigen, dass das Board den oben aufgeführten EMV-Richtlinien entspricht. Eine ordnungsgemäße Installation in einem System, welches die EMV-Richtlinien erfüllt, stellt sicher, dass das Produkt gemäß den EMV-Richtlinien betrieben wird.

Sobald Sie das Produkt oder seine Standardkonfiguration verändern, müssen Sie dafür sorgen, dass alle relevanten Richtlinien eingehalten werden.

VCCI

Das Produkt ist eine Einrichtung der Klasse A gemäß dem Standard des Voluntary Control Council for Interference von Information Technology Interference (VCCI). Wird das Produkt in Wohngegenden betrieben, können Störungen im Hochfrequenzbereich auftreten. In einem solchen Fall ist der Benutzer verpflichtet, entsprechende Gegenmaßnahmen zu ergreifen.

Installation

Beschädigung von Schaltkreisen
Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau des Produktes kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.
Bevor Sie das Produkt oder elektronische Komponenten berühren, vergewissern Sie sich, daß Sie in einem ESD-geschützten Bereich arbeiten.

Beschädigung des Produktes und der Zusatzmodule
Fehlerhafter Ein- oder Ausbau von Zusatzmodulen führt zu Beschädigung des Produktes oder der Zusatzmodule.
Lesen Sie deshalb vor dem Ein- oder Ausbau von Zusatzmodulen die Dokumentation und benutzen Sie angemessenes Werkzeug.

Beschädigung des Blades
Fehlerhafte Installation des Blades kann zu einer Beschädigung des Blades führen. Verwenden Sie die Handles, um das Blade zu installieren/deinstallieren. Auf diese Weise vermeiden Sie, dass das Front Panel oder die Platine deformiert oder zerstört wird.

Beschädigung des Blades, der Backplane oder von System Komponenten
Verbogene Pins oder lose Komponenten können zu einer Beschädigung des Blades, der Backplane oder von Systemkomponenten führen. Überprüfen Sie daher das Blade sowie die Backplane vor der Installation sorgältig und stellen Sie sicher, dass sich beide in einwandfreien Zustand befinden und keine Pins verbogen sind.

Datenverlust
Wenn Sie das Blade deinstallieren, obwohl die blaue Hot-Swap-LED noch blinkt, kann dies zu Datenverlust führen. Warten Sie daher, bis die blaue LED durchgehend leuchtet, bevor Sie das Blade deinstallieren

Beschädigung des Systems
Die Gebäude-internen Schnittstellen ("intra-building ports" per GR-1089-CORE) der Geräte oder Baugruppen sind nur für gebäudeinterne Verkabelung vorgesehen. Die Schnittstellen sind als Typ 2 oder Typ 4 definiert (wie in GR-1089-Core beschrieben) und erfordern eine Isolation zu Leitungen außerhalb des Gebäudes.
Die Gebäude-internen Schnittstellen dürfen keine elektrisch leitende Verbindung zu Leitungen außerhalb des Gebäudes haben. Ein "Primary Protector" (wie in GR-1089-CORE beschrieben) ist keine ausreichende Absicherung, um die Gebäude-internen Schnittstellen mit Leitungen außerhalb des Gebäudes zu verbinden.

Operation

Beschädigung des Blades
Hohe Luftfeuchtigkeit und Kondensat auf der Oberfläche des Blades können zu Kurzschlüssen führen. Betreiben Sie das Blade nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Blade kein Kondensat befindet und betreiben Sie das Blade nicht unter -5°C.

Überhitzung und Beschädigung des Blades
Betreiben Sie das Blade ohne Zwangsbelüftung, kann das Blade überhitzt und schließlich beschädigt werden. Bevor Sie das Blade betreiben, müssen Sie sicher stellen, dass das Shelf über eine Zwangskühlung verfügt.

Verletzungen oder Kurzschlüsse
Blade oder Stromversorgung Falls die ORing Dioden des Blades durchbrennen, kann das Blade einen Kurzschluss zwischen den Eingangsleitungen A und B verursachen. In diesem Fall ist Leitung A immer noch unter Spannung, auch wenn sie vom Versorgungskreislauf getrennt ist (und umgekehrt). Prüfen Sie deshalb immer, ob die Leitung spannungsfrei ist, bevor Sie Ihre Arbeit fortsetzen, um Schäden oder Verletzungen zu vermeiden.

Schaltereinstellungen

Fehlfunktion des Produktes
Schalter, die mit 'Reserved' gekennzeichnet sind, können mit produktionsrelevanten Funktionen belegt sein. Das Ändern dieser Schalter kann im normalen Betrieb Störungen auslösen.
Verstellen Sie nur solche Schalter, die nicht mit 'Reserved' gekennzeichnet sind.

Beschädigung des Produktes
Das Verstellen von Schaltern während des laufenden Betriebes kann zur Beschädigung des Produktes führen.
Prüfen und ändern Sie die Schaltereinstellungen, bevor Sie das Produkt installieren.

Beschädigung des Produktes
Zu viel Druck kann den Reset Schalter beschädigen.
Drücken Sie den Reset Schalter nur leicht.

Kabel und Stecker

Beschädigung des Blades
Die RJ-45-Stecker an der Frontblende sind für Anschlüsse vom Typ Twisted-Pair Ethernet (TPE) oder E1/T1/J1 vorgesehen. Der Anschluss eines E1/T1/J1-Interfaces an einen Ethernet-Stecker kann zur Zerstörung des Blades führen.

- Stellen Sie daher sicher, dass TPE-Stecker an Ihrem Arbeitsplatz eindeutig als Netzwerkstecker gekennzeichnet sind.
- Stellen Sie sicher, dass die Länge eines Kabels, welches an den RJ-45-Stecker angeschlossen ist, 100 Meter nicht überschreitet.
- Stellen Sie sicher, dass der TPE-Stecker ausschliesslich mit einem Safety-Extra-Low-Voltage-Stromkreis (SELV) verbunden ist.
- Wenden Sie sich bei Fragen an ihren Systemadministrator

AMC-Module

Eingeschränkte Betriebstemperaturbereich
Werden AMC-Module auf dem Blade installiert, deren Betriebstemperaturbereiche kleiner sind als der Betriebstemperaturbereich des Blades selber, so führt dies zu einer Einschränkung des Betriebstemperaturbereiches des Blades. Stellen Sie sicher, dass sich die Betriebstemperaturbereiche des Blades sowie installierter AMCModuleinnerhalb erlaubter Bereiche bewegen.

Verletzung von EMV-Grenzwerten und verminderte Kühlung des Shelfs.
Ein leerer AMC-Steckplatz kann zu verminderter Kühlung des Shelfs sowie starker elektromagnetischer Strahlung führen und somit eine Überschreitung von EMV-Grenzwerten zur Folge haben. Installieren Sie daher immer ein Filler-Panel in einen anderweitig nicht verwendeten AMCSteckplatz.

Hot Swap

Datenverlust
Wenn Sie das Produkt ausbauen, obwohl die blaue Hot-Swap LED noch blinkt, kann dies zu Datenverlust führen.
Warten Sie daher, bis die blaue LED durchgehend leuchtet, bevor Sie das Produkt ausbauen.

SFP/SFP+ Modules

Gefahr von Verletzungen sowie von Beschädigung des RTMs und SFP/SFP+-Modulen
Die Installation und der Betrieb von SFP/SFP+-Modulen, welche nicht zertifiziert sind und welche nicht den Sicherheitsstandards entsprechen, kann Verletzungen zur Folge haben sowie zur Beschädigung des RTMs und von SFP/SFP+-Modulen führen.
Verwenden Sie daher nur SFP/SFP+-Module, die zertifiziert sind und die den Sicherheitsstandards entsprechen.

Verletzungsgefahr
Optische SFP/SFP+-Module können als Laserprodukte klassifiziert sein. Wenn Sie solche SFP/SFP+-Module installieren und betreiben, so gelten die entsprechenden Bestimmungen für Laserprodukte für das gesamte RTM. Werden diese Bestimmungen nicht eingehalten, so können Verletzungen die Folge sein.
Wenn Sie SFP/SFP+-Module betreiben, die als Laserprodukte klassifiziert sind, stellen Sie sicher, dass die entsprechenden Bestimmungen für Laserprodukte eingehalten werden.

Verletzungsgefahr der Augen
Optische SFP/SFP+-Module können Laserstrahlen aussenden, wenn kein Kabel angeschlossen ist.
Blicken Sie daher nicht direkt in die Öffnung eines SFP/SFP+-Moduls, um Verletzungen der Augen zu vermeiden.

Beschädigung von SFP/SFP+-Modulen
Die Schutzkappe eines SFP/SFP+-Modules dient dazu, die sensible Optik des SFP/SFP+-Modules gegen Staub und Schmutz zu schützen.
Entfernen Sie die Schutzkappe nur dann, wenn Sie beabsichtigen, ein Kabel anzuschließen. Andernfalls belassen Sie die Schutzkappe auf dem SFP/SFP+-Modul.

Batterie

Datenverlust
Wenn Sie einen anderen Batterietyp installieren als der, der bei Auslieferung des Produktes installiert war, kann Datenverlust die Folge sein, da die neu installierte Batterie für andere Umgebungsbedingungen oder eine andere Lebenszeit ausgelegt sein könnte.
Verwenden Sie daher den gleichen Batterietyp, der bei Auslieferung des Produktes installiert war.

Beschädigung des PCBs und der Batteriehalterung
Wenn Sie die Batterie mit einem Schraubendreher ausbauen, können das PCB und die Batteriehalterung beschädigt werden.
Benutzen Sie keinesfalls einen Schraubendreher, um die Batterie aus der Halterung zu nehmen.

Umweltschutz

Umweltverschmutzung
Falsche Entsorgung der Produkte schadet der Umwelt.
Entsorgen Sie alte Produkte gemäß der in Ihrem Land gültigen Gesetzgebung und den Empfehlungen des Herstellers.