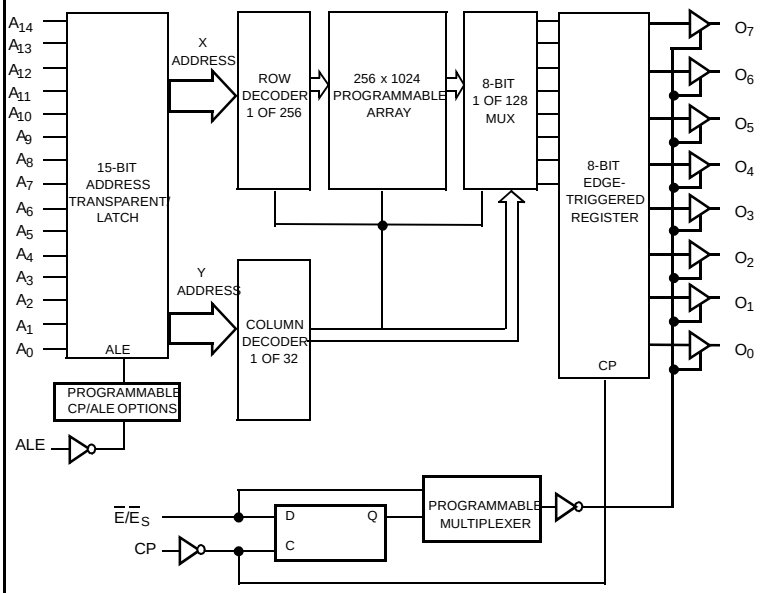
CY7C277

32K x 8 Reprogrammable Registered PROM

Features

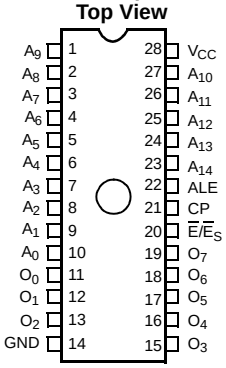
- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
  - 30-ns address set-up
  - 15-ns clock to output
- Low power
  - 60 mW (commercial)
  - 715 mW (military)
- Programmable address latch enable input
- Programmable synchronous or asynchronous output enable
- On-chip edge-triggered output registers
- EPROM technology, 100% programmable
- Slim 300-mil, 28-pin plastic or hermetic DIP
- 5V ±10% V_{CC}, commercial and military
- TTL-compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 2001V static discharge

Logic Block Diagram



Pin Configurations

DIP/Flatpack
Top View



Selection Guide

		7C277-30	7C277-40	Unit
Minimum Address Set-Up Time		30	40	ns
Maximum Clock to Output		15	20	ns
Maximum Operating Current	Com'l	120		mA
	Mil		130	mA

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Functional Description

The CY7C277 is a high-performance 32K word by 8-bit CMOS PROMs. It is packaged in the slim 28-pin 300-mil package. The ceramic package may be equipped with an erasure window; when exposed to UV light, the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide algorithms.

The CY7C277 offers the advantages of low power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

On the CY7C277, the outputs are pipelined through a master-slave register. On the rising edge of CP, data is loaded into the 8-bit edge triggered output register. The $\overline{E}/\overline{E}_S$ input provides a programmable bit to select between asynchronous and synchronous operation. The default condition is asynchronous. When the asynchronous mode is selected, the $\overline{E}/\overline{E}_S$ pin operates as an asynchronous output enable. If the synchronous mode is selected, the $\overline{E}/\overline{E}_S$ pin is sampled on the rising edge of CP to enable and disable the outputs. The 7C277 also provides a programmable bit to enable the Address Latch input. If this bit is not programmed, the device will ignore the ALE pin and the address will enter the device asynchronously. If the ALE function is selected, the address enters the PROM while the ALE pin is active, and is captured when ALE is deasserted. The user may define the polarity of the ALE signal, with the default being active HIGH.

Maximum Ratings[1]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential .....–0.5V to +7.0V (Pin 24 to Pin 12)

DC Voltage Applied to Outputs in High Z State .....–0.5V to +7.0V

DC Input Voltage .....–3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[2]	–55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		7C277-30 Min.	7C277-30 Max.	7C277-40 Min.	7C277-40 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		–10	+10	–10	+10	µA
V_{CD}	Input Clamp Diode Voltage			Note 4				
I_{OZ}	Output Leakage Current	0 ≤ V_{OUT} ≤ V_{CC}, Output Disabled[5]		–40	+40	–40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		–20	–90	–20	–90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, I_{OUT} = 0 mA	Commercial		120			mA
			Military				130	
V_{PP}	Programming Supply Voltage			12	13	12	13	V
I_{PP}	Programming Supply Current				50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4	V

Notes:

1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See "Introduction to CMOS PROMs" in this Book for general information on testing.
5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

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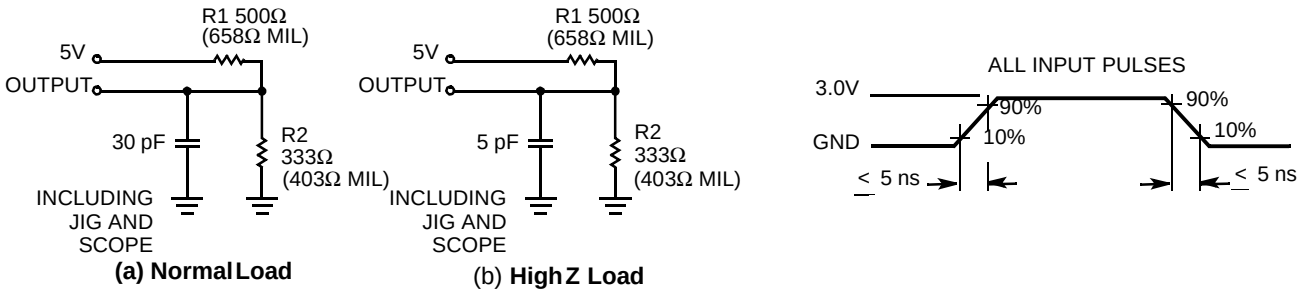
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 5.0V$	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms[4]



Equivalent to: THÉVENIN EQUIVALENT

CY7C277 Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C277-30		7C277-40		Unit
		Min.	Max.	Min.	Max.	
t_{AL}	Address Set-Up to ALE Inactive	5		10		ns
t_{LA}	Address Hold from ALE Inactive	10		10		ns
t_{LL}	ALE Pulse Width	10		10		ns
t_{SA}	Address Set-Up to Clock HIGH	30		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	12		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		10		ns
t_{CO}	Clock HIGH to Output Valid		15		20	ns
t_{PWC}	Clock Pulse Width	15		20		ns
t_{LZC}[7]	Output Valid from Clock HIGH		15		20	ns
t_{HZC}	Output High Z from Clock HIGH		15		20	ns
t_{LZE}[8]	Output Valid from $\overline{E}$ LOW		15		20	ns
t_{HZE}[8]	Output High Z from $\overline{E}$ HIGH		15		20	ns

Notes:
7. Applies only when the synchronous ($\overline{E}_S$) function is used.
8. Applies only when the asynchronous ($\overline{E}$) function is used.

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Architecture Configuration Bits

Architecture Bit	Architecture Verify D_7–D_0		Function
ALE	D_1	0 = DEFAULT	Input Transparent
		1 = PGMED	Input Latched
ALEP	D_2	0 = DEFAULT	ALE = Active HIGH
		1 = PGMED	ALE = Active LOW
$\overline{E}/\overline{E}_S$	D_0	0 = DEFAULT	Asynchronous Output Enable ($\overline{E}$)
		1 = PGMED	Synchronous Output Enable ($\overline{E}_S$)

Bit Map

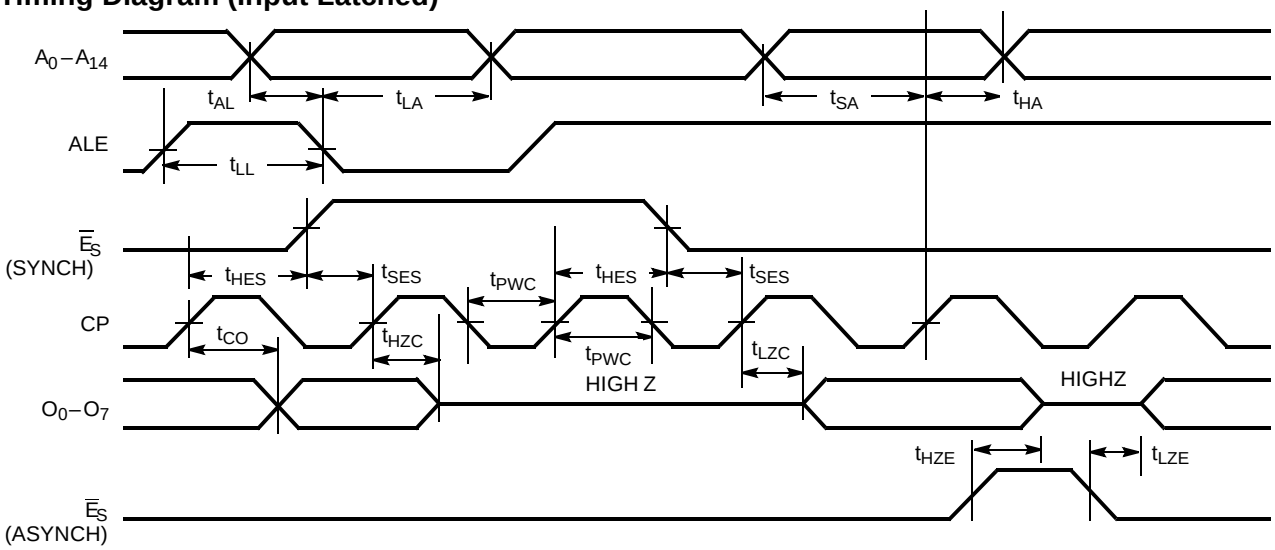
Programmer Address (Hex.)	RAM Data
0000	Data
.	.
.	.
.	.
7FFF	Data
8000	Control Byte

Architecture Byte (8000)

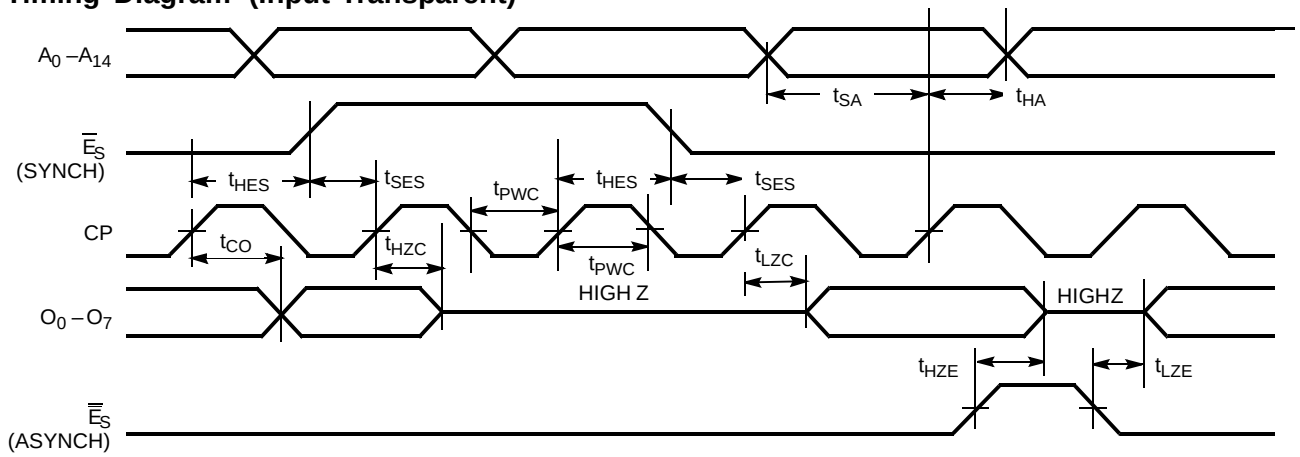
D7 D0

C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0

Timing Diagram (Input Latched)[9]



Timing Diagram (Input Transparent)



Note:

9. ALE is shown with positive polarity.

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Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[10]				
	Read or Output Disable	**A_{14}–A_0**	**$\overline{E}$, $\overline{E}_S$**	**CP**	**ALE**	**O_7–O_0**
	Other	**A_{14}–A_0**	**VFY**	**PGM**	**V_{PP}**	**D_7–D_0**
Read		A_{14}–A_0	V_{IL}	V_{IH}	V_{IL}	O_7–O_0
Output Disable		A_{14}–A_0	V_{IH}	X	X	High Z
Program		A_{14}–A_0	V_{IHP}	V_{ILP}	V_{PP}	D_7–D_0
Program Verify		A_{14}–A_0	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	O_7–O_0
Program Inhibit		A_{14}–A_0	V_{IHP}	V_{IHP}	V_{PP}	High Z
Blank Check		A_{14}–A_0	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	O_7–O_0

Note:
10. X = “don’t care” but not to exceed V_{CC} ±5%.

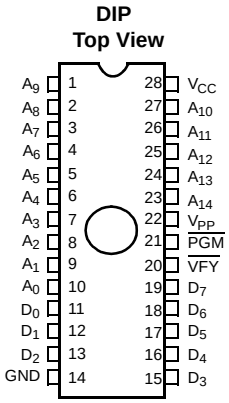

Figure 1. Programming Pinouts

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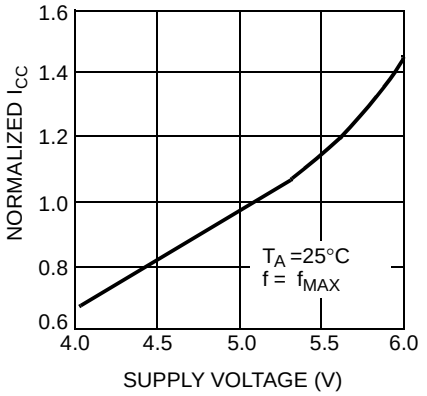
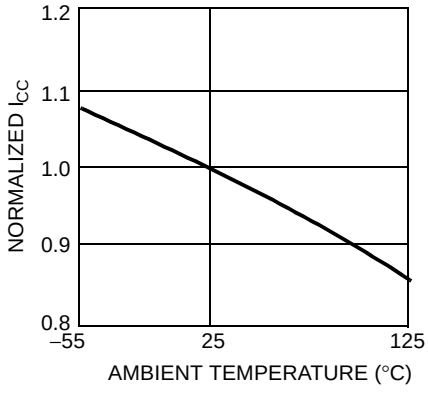
Typical DC and AC Characteristics

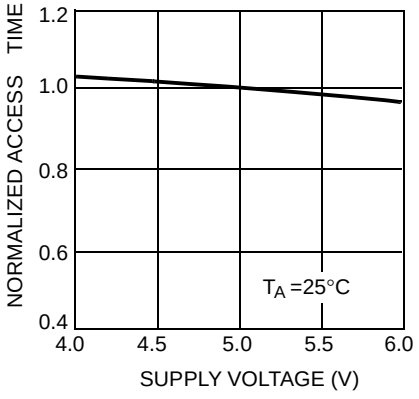
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



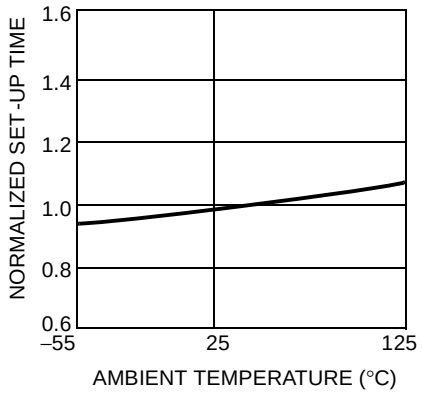
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



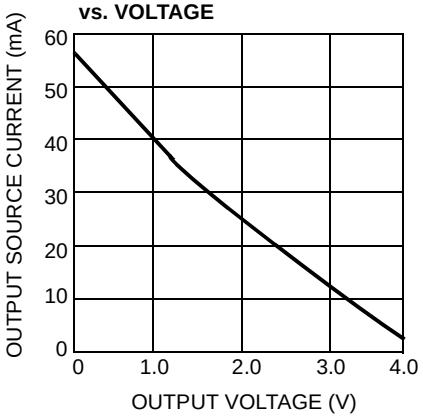
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



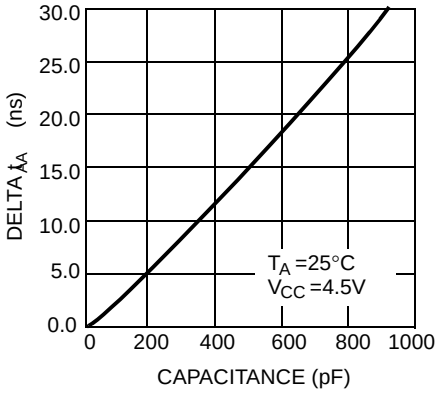
NORMALIZED SET-UP TIME vs. TEMPERATURE



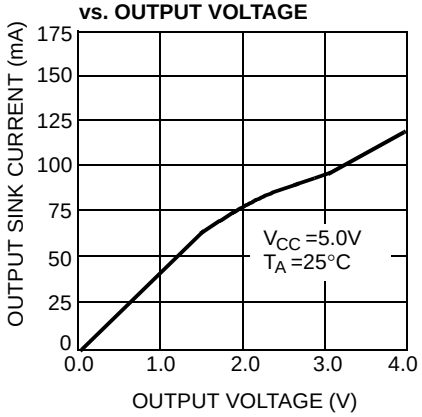
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C277-12

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Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C277-30WC	W22	28-Lead (300-Mil) Windowed CerDIP	Commercial
40	CY7C277-40WMB	W22	28-Lead (300-Mil) Windowed CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

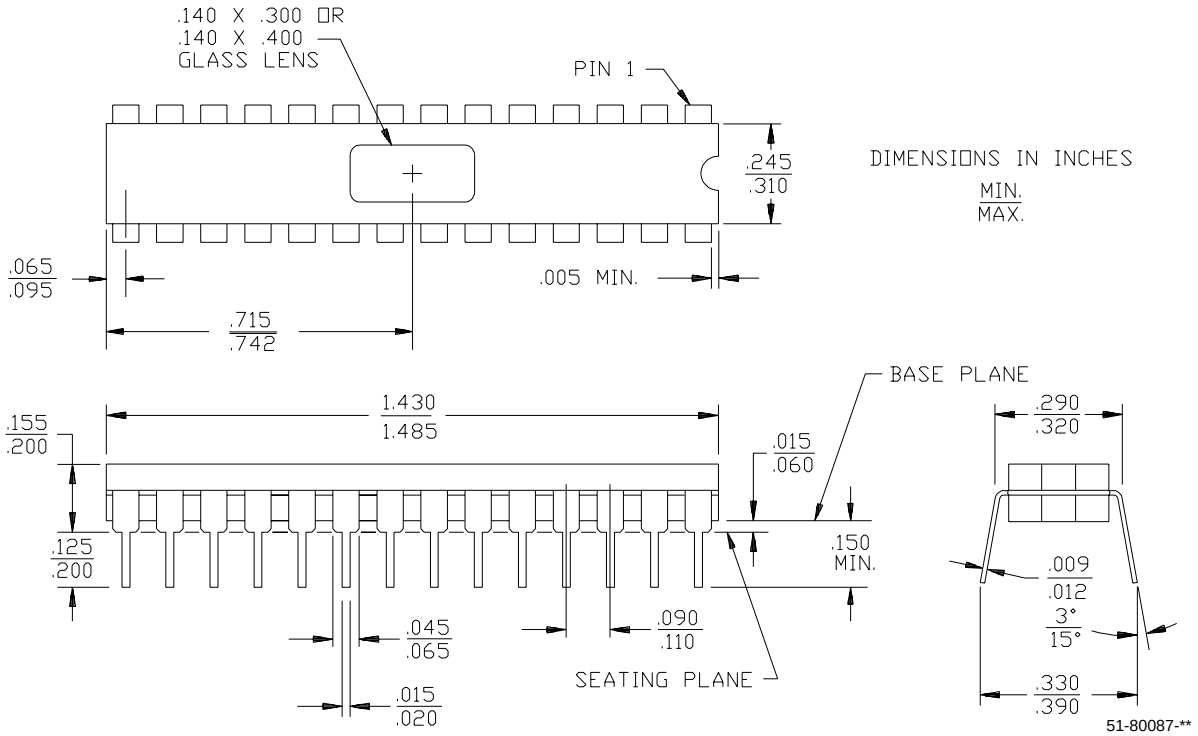
Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11

Package Diagrams

28-Lead (300-Mil) Windowed CerDIP W22
MIL-STD-1835 D-15 Config. A



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Document History Page

Document Title: CY7C277 32K x 8 Programmable Registered PROM Document Number: 38-04006				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	113862	3/8/02	DSG	Change from Spec number: 38-00085 to 38-04006
*A	118901	10/09/02	GBI	Update ordering information
*B	122247	12/27/02	RBI	Add power up requirements to Operating Conditions information

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