

# 4-Mbit (128K × 36) Flow-Through Sync SRAM

## Features

- 128K × 36 common I/O
- 3.3 V core Power Supply ( $V_{DD}$ )
- 2.5 V or 3.3 V I/O Supply ( $V_{DDQ}$ )
- Fast Clock-to-output times
  - 8.0 ns (100 MHz version)
- Provide high performance 2-1-1-1 access rate
- User selectable burst counter supporting Intel Pentium interleaved or Linear Burst Sequences
- Separate Processor and Controller Address Strokes
- Synchronous Self Timed Write
- Asynchronous output enable
- Available in Pb-free 165-ball FBGA Package
- ZZ Sleep Mode option

## Functional Description

The CY7C13451G is a 128K × 36 synchronous cache RAM designed to interface with high speed microprocessors with minimum glue logic. The maximum access delay from clock rise is 8.0 ns (100 MHz version). A 2 bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive edge triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address pipelining Chip Enable ( $\overline{CE}_1$ ), depth expansion Chip Enables ( $\overline{CE}_2$  and  $\overline{CE}_3$ ), Burst Control inputs (ADSC, ADSP, and ADV), Write Enables ( $BW_x$ , and  $BWE$ ), and Global Write (GW). Asynchronous inputs include the Output Enable (OE) and the ZZ pin.

The CY7C13451G enables either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses are initiated with the Processor Address Strobe (ADSP) or the cache Controller Address Strobe (ADSC) inputs.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ( $\overline{ADSP}$ ) or Address Strobe Controller ( $\overline{ADSC}$ ) is active. Subsequent burst addresses are internally generated as controlled by the Advance pin (ADV).

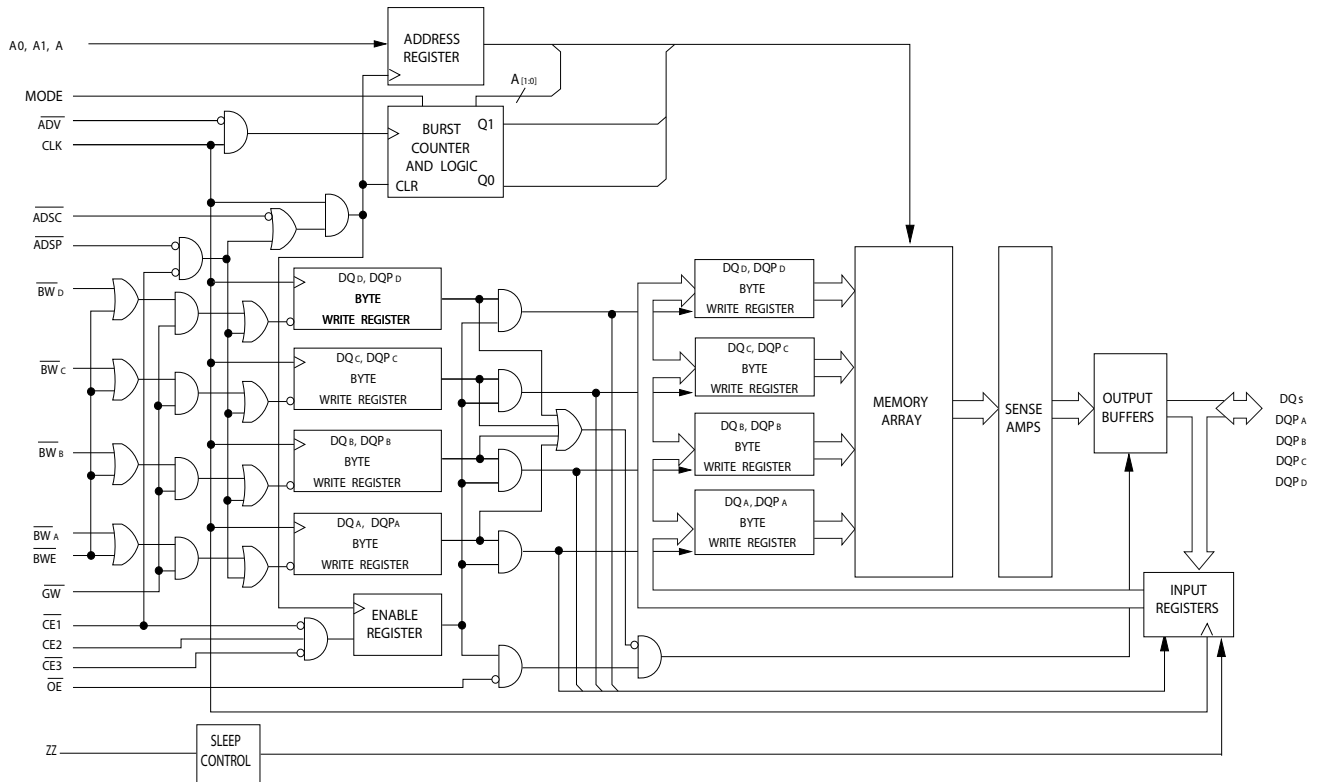
The CY7C13451G operates from a +3.3 V core power supply while all outputs operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC standard JESD8-5 compatible.

For a complete list of related documentation, click [here](#).

## Selection Guide

Description	100 MHz	Unit
Maximum Access Time	8.0	ns
Maximum Operating Current	180	mA
Maximum CMOS Standby Current	60	mA

**Logic Block Diagram**



## Contents

<b>Pin Configurations</b> .....	<b>4</b>	<b>Switching Characteristics</b> .....	<b>13</b>
<b>Pin Definitions</b> .....	<b>5</b>	<b>Timing Diagrams</b> .....	<b>14</b>
<b>Functional Overview</b> .....	<b>6</b>	<b>Ordering Information</b> .....	<b>18</b>
Single Read Accesses .....	6	Ordering Code Definitions .....	18
Single Write Accesses Initiated by $\overline{\text{ADSP}}$ .....	6	<b>Package Diagrams</b> .....	<b>19</b>
Single Write Accesses Initiated by ADSC .....	6	<b>Acronyms</b> .....	<b>20</b>
Burst Sequences .....	7	<b>Document Conventions</b> .....	<b>20</b>
Sleep Mode .....	7	Units of Measure .....	20
Interleaved Burst Address Table .....	7	<b>Errata</b> .....	<b>21</b>
Linear Burst Address Table .....	7	Part Numbers Affected .....	21
ZZ Mode Electrical Characteristics .....	7	Product Status .....	21
<b>Truth Table</b> .....	<b>8</b>	Ram9 Sync ZZ Pin Issues Errata Summary .....	21
<b>Truth Table for Read or Write</b> .....	<b>9</b>	<b>Document History Page</b> .....	<b>22</b>
<b>Maximum Ratings</b> .....	<b>10</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>23</b>
<b>Operating Range</b> .....	<b>10</b>	Worldwide Sales and Design Support .....	23
<b>Neutron Soft Error Immunity</b> .....	<b>10</b>	Products .....	23
<b>Electrical Characteristics</b> .....	<b>10</b>	PSoC@Solutions .....	23
<b>Capacitance</b> .....	<b>11</b>	Cypress Developer Community .....	23
<b>Thermal Resistance</b> .....	<b>11</b>	Technical Support .....	23
<b>AC Test Loads and Waveforms</b> .....	<b>12</b>		

## Pin Configurations

Figure 1. 165-ball FBGA pinout <sup>[1]</sup>

CY7C13451G (128K × 36)

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
<b>B</b>	NC/144M	A	$CE_2$	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
<b>C</b>	DQP <sub>C</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC/1G	DQP <sub>B</sub>
<b>D</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>E</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>F</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>G</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>H</b>	NC	NC	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
<b>J</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>K</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>L</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>M</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>N</b>	DQP <sub>D</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	NC/18M	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>A</sub>
<b>P</b>	NC	NC/72M	A	A	NC	A1	NC	A	A	A	NC/9M
<b>R</b>	MODE	NC/36M	A	A	NC	A0	NC	A	A	A	A

### Note

- Errata:** The ZZ pin (Ball H11) needs to be externally connected to ground. For more information, see "Errata" on page 21.

## Pin Definitions

Name	I/O	Description
$A_0, A_1, A$	Input-Synchronous	<b>Address Inputs Used to Select One of the 128K Address Locations.</b> Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1, CE_2,$ and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the two bit counter.
$\overline{BW}_A, \overline{BW}_B, \overline{BW}_C, \overline{BW}_D$	Input-Synchronous	<b>Byte Write Select Inputs, Active LOW.</b> Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	<b>Global Write Enable Input, Active LOW.</b> When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $BW_{[A:D]}$ and $\overline{BWE}$ ).
$\overline{BWE}$	Input-Synchronous	<b>Byte Write Enable Input, Active LOW.</b> Sampled on the rising edge of CLK. This signal is asserted LOW to conduct a byte write.
CLK	Input Clock	<b>Clock Input.</b> Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-Synchronous	<b>Chip Enable 1 Input, Active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $CE_2$ and $CE_3$ to select or deselect the device. ADSP is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
$CE_2$	Input-Synchronous	<b>Chip Enable 2 Input, Active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $CE_3$ to select or deselect the device. $CE_2$ is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	<b>Chip Enable 3 Input, Active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $CE_2$ to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	<b>Output Enable, Asynchronous Input, Active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins act as outputs. When deasserted HIGH, I/O pins are tristated and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
ADV	Input-Synchronous	<b>Advance Input Signal,</b> Sampled on the Rising Edge of CLK. When asserted, it automatically increments the address in a burst cycle.
ADSP	Input-Synchronous	<b>Address Strobe from Processor, Sampled on the Rising Edge of CLK, Active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ADSP is ignored when $\overline{CE}_1$ is deasserted HIGH.
ADSC	Input-Synchronous	<b>Address Strobe from Controller, Sampled on the Rising Edge of CLK, Active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
ZZ [2]	Input-Asynchronous	<b>ZZ sleep Input, Active HIGH.</b> When asserted HIGH places the device in a non-time critical sleep condition with data integrity preserved. During normal operation, this pin is low or left floating. ZZ pin has an internal pull down.
$DQs, DQP_A, DQP_B, DQP_C, DQP_D$	I/O-Synchronous	<b>Bidirectional Data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ . When $\overline{OE}$ is asserted LOW, the pins act as outputs. When HIGH, DQs and $DQP_{[A:D]}$ are placed in a tristate condition.
$V_{DD}$	Power Supply	<b>Power Supply Inputs to the Core of the Device.</b>
$V_{SS}$	Ground	<b>Ground for the Core of the Device.</b>
$V_{DDQ}$	I/O Power Supply	<b>Power Supply for the I/O Circuitry.</b>

### Note

2. **Errata:** The ZZ pin (Ball H11) needs to be externally connected to ground. For more information, see "Errata" on page 21.

**Pin Definitions** (continued)

Name	I/O	Description
MODE	Input Static	<b>Selects Burst Order.</b> When tied to GND selects linear burst sequence. When tied to $V_{DD}$ or left floating selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode Pin has an internal pull up.
NC	–	<b>No Connects.</b> Not Internally connected to the die.
NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	<b>No Connects.</b> Not internally connected to the die. NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M, and NC/1G are address expansion pins and are not internally connected to the die.

**Functional Overview**

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ( $t_{CO}$ ) is 8.0 ns (100 MHz device).

The CY7C13451G supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable and is determined by sampling the MODE input. Accesses are initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two bit on-chip wrap around burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select ( $BW_{[A:D]}$ ) inputs. A Global Write Enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous Chip Selects ( $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{CE}_3$ ) and an asynchronous Output Enable ( $\overline{OE}$ ) provide for easy bank selection and output tristate control. ADSP is ignored if  $CE_1$  is HIGH.

**Single Read Accesses**

A single read access is initiated when the following conditions are satisfied at clock rise:

- $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{CE}_3$  are all asserted active.
- ADSP or ADSC is asserted LOW (if the access is initiated by ADSC, the write inputs are deasserted during this first cycle).

The address presented to the address inputs is latched into the address register and the burst counter or control logic and presented to the memory core. If the  $\overline{OE}$  input is asserted LOW, the requested data is available at the data outputs a maximum to  $t_{CDV}$  after clock rise. ADSP is ignored if  $\overline{CE}_1$  is HIGH.

**Single Write Accesses Initiated by ADSP**

Single write access is initiated when the following conditions are satisfied at clock rise:

- $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{CE}_3$  are all asserted active
- ADSP is asserted LOW.

The addresses presented are loaded into the address register and the burst inputs ( $\overline{GW}$ ,  $\overline{BWE}$ , and  $\overline{BW}_x$ ) are ignored during this first clock cycle. If the write inputs are asserted active (see **Write Cycle Descriptions table** for appropriate states that indicate a write) on the next clock rise, the appropriate data is latched and written into the device. Byte writes are allowed. During byte writes,  $\overline{BW}_A$  controls  $DQ_A$  and  $\overline{BW}_B$  controls  $DQ_B$ ,  $\overline{BW}_C$  controls  $DQ_C$ , and  $\overline{BW}_D$  controls  $DQ_D$ . All I/Os are tristated during a byte write. Since this is a common I/O device, the asynchronous  $\overline{OE}$  input signal is deasserted and the I/Os are tristated prior to the presentation of data to  $DQ_s$ . As a safety precaution, the data lines are tristated after a write cycle is detected, regardless of the state of  $\overline{OE}$ .

**Single Write Accesses Initiated by ADSC**

This write access is initiated when the following conditions are satisfied at clock rise:

- $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{CE}_3$  are all asserted active.
- ADSC is asserted LOW.
- ADSP is deasserted HIGH
- The write input signals ( $\overline{GW}$ ,  $\overline{BWE}$ , and  $\overline{BW}_x$ ) indicate a write access. ADSC is ignored if ADSP is active LOW.

The addresses presented are loaded into the address register and the burst counter or control logic and delivered to the memory core. The information presented to  $DQ_{[D:A]}$  is written into the specified address location. Byte writes are allowed. During byte writes,  $\overline{BW}_A$  controls  $DQ_A$ ,  $\overline{BW}_B$  controls  $DQ_B$ ,  $\overline{BW}_C$  controls  $DQ_C$ , and  $\overline{BW}_D$  controls  $DQ_D$ . All I/Os and even a byte write are tristated when a write is detected. Since this is a common I/O device, the asynchronous  $\overline{OE}$  input signal is deasserted and the I/Os are tristated prior to the presentation of data to  $DQ_s$ . As a safety precaution, the data lines are tristated after a write cycle is detected, regardless of the state of  $\overline{OE}$ .

### Burst Sequences

The CY7C13451G provides an on-chip two bit wrap around burst counter inside the SRAM. The burst counter is fed by  $A_{[1:0]}$  and follows either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE selects a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles are required to enter into or exit from this sleep mode. In this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device is deselected prior to entering the sleep mode. CEs, ADSP, and ADSC must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

### Interleaved Burst Address Table

(MODE = Floating or  $V_{DD}$ )

First Address A <sub>1</sub> , A <sub>0</sub>	Second Address A <sub>1</sub> , A <sub>0</sub>	Third Address A <sub>1</sub> , A <sub>0</sub>	Fourth Address A <sub>1</sub> , A <sub>0</sub>
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

### Linear Burst Address Table

(MODE = GND)

First Address A <sub>1</sub> , A <sub>0</sub>	Second Address A <sub>1</sub> , A <sub>0</sub>	Third Address A <sub>1</sub> , A <sub>0</sub>	Fourth Address A <sub>1</sub> , A <sub>0</sub>
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

### ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
$I_{DDZZ}$	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2 V$	–	40	mA
$t_{ZZS}$	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2 V$	–	$2t_{CYC}$	ns
$t_{ZZREC}$	ZZ recovery time	$ZZ \leq 0.2 V$	$2t_{CYC}$	–	ns
$t_{ZZI}$	ZZ Active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
$t_{RZZI}$	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

## Truth Table

The Truth Table for part CY7C13451G is as follows. [3, 4, 5, 6, 7]

Cycle Description	Address Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power down	None	H	X	X	L	X	L	X	X	X	L-H	Tristate
Deselected Cycle, Power down	None	L	L	X	L	L	X	X	X	X	L-H	Tristate
Deselected Cycle, Power down	None	L	X	H	L	L	X	X	X	X	L-H	Tristate
Deselected Cycle, Power down	None	L	L	X	L	H	L	X	X	X	L-H	Tristate
Deselected Cycle, Power down	None	X	X	H	L	H	L	X	X	X	L-H	Tristate
Sleep Mode, Power down	None	X	X	X	H	X	X	X	X	X	X	Tristate
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Tristate
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Tristate
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tristate
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tristate
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tristate
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tristate
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

### Notes

- X = "Don't Care," H = Logic HIGH, and L = Logic LOW.
- $\overline{WRITE} = L$  when any one or more Byte Write enable signals ( $\overline{BW}_A$ ,  $\overline{BW}_B$ ,  $\overline{BW}_C$ ,  $\overline{BW}_D$ ) and  $\overline{BWE} = L$  or  $\overline{GW} = L$ .  $\overline{WRITE} = H$  when all Byte write enable signals ( $\overline{BW}_A$ ,  $\overline{BW}_B$ ,  $\overline{BW}_C$ ,  $\overline{BW}_D$ ),  $\overline{BWE}$ ,  $\overline{GW} = H$ .
- The DQ pins are controlled by the current cycle and the  $\overline{OE}$  signal.  $\overline{OE}$  is asynchronous and is not sampled with the clock.
- The SRAM always initiates a read cycle when  $\overline{ADSP}$  is asserted, regardless of the state of  $\overline{GW}$ ,  $\overline{BWE}$ , or  $\overline{BW}_{[A:D]}$ . Writes may occur only on subsequent clocks after the  $\overline{ADSP}$  or with the assertion of  $\overline{ADSC}$ . As a result,  $\overline{OE}$  is driven HIGH prior to the start of the write cycle to enable the outputs to tristate.  $\overline{OE}$  is a "Do Not Care" for the remainder of the write cycle.
- $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tristate when  $\overline{OE}$  is inactive or when the device is deselected, and all data bits behave as output when  $\overline{OE}$  is active (LOW).



## Truth Table for Read or Write

The Truth Table for read or write for part CY7C13451G is as follows. [8, 9]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte (A, DQP <sub>A</sub> )	H	L	H	H	H	L
Write Byte (B, DQP <sub>B</sub> )	H	L	H	H	L	H
Write Bytes (B, A, DQP <sub>A</sub> , DQP <sub>B</sub> )	H	L	H	H	L	L
Write Byte (C, DQP <sub>C</sub> )	H	L	H	L	H	H
Write Bytes (C, A, DQP <sub>C</sub> , DQP <sub>A</sub> )	H	L	H	L	H	L
Write Bytes (C, B, DQP <sub>C</sub> , DQP <sub>B</sub> )	H	L	H	L	L	H
Write Bytes (C, B, A, DQP <sub>C</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	H	L	L	L
Write Byte (D, DQP <sub>D</sub> )	H	L	L	H	H	H
Write Bytes (D, A, DQP <sub>D</sub> , DQP <sub>A</sub> )	H	L	L	H	H	L
Write Bytes (D, B, DQP <sub>D</sub> , DQP <sub>A</sub> )	H	L	L	H	L	H
Write Bytes (D, B, A, DQP <sub>D</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	L	H	L	L
Write Bytes (D, B, DQP <sub>D</sub> , DQP <sub>B</sub> )	H	L	L	L	H	H
Write Bytes (D, B, A, DQP <sub>D</sub> , DQP <sub>C</sub> , DQP <sub>A</sub> )	H	L	L	L	H	L
Write Bytes (D, C, A, DQP <sub>D</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

### Notes

8. X = "Don't Care," H = Logic HIGH, and L = Logic LOW.

9. This table is only a partial listing of the byte write combinations. Any combination of  $\overline{BW}_x$  is valid. Appropriate write is done based on the active byte write.

## Maximum Ratings

Exceeding the maximum ratings may shorten the battery life of the device. These user guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C

Ambient Temperature with  
Power Applied ..... -55 °C to +125 °C

Supply Voltage on  
 $V_{DD}$  Relative to GND ..... -0.5 V to +4.6 V

Supply Voltage on  
 $V_{DDQ}$  Relative to GND ..... -0.5 V to + $V_{DD}$

DC Voltage Applied to Outputs  
in tristate ..... -0.5 V to  $V_{DDQ} + 0.5$  V

DC Input Voltage ..... -0.5 V to  $V_{DD} + 0.5$  V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage  
(MIL-STD-883, Method 3015) ..... >2001 V

Latch up Current ..... >200 mA

## Operating Range

Range	Ambient Temperature	$V_{DD}$	$V_{DDQ}$
Automotive	-40 °C to +125 °C	3.3 V - 5% / + 10%	2.5 V - 5% to $V_{DD}$

## Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical Single-Bit Upsets	25 °C	361	394	FIT/Mb
LMBU	Logical Multi-Bit Upsets	25 °C	0	0.01	FIT/Mb
SEL	Single Event Latch up	85 °C	0	0.1	FIT/Dev

\* No LMBU or SEL events occurred during testing; this column represents a statistical  $\chi^2$ , 95% confidence limit calculation. For more details refer to Application Note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

## Electrical Characteristics

Over the Operating Range

Parameter <sup>[10, 11]</sup>	Description	Test Conditions	Min	Max	Unit
$V_{DD}$	Power Supply Voltage		3.135	3.6	V
$V_{DDQ}$	I/O Supply Voltage		2.375	$V_{DD}$	V
$V_{OH}$	Output HIGH Voltage	for 3.3 V I/O, $I_{OH} = -4.0$ mA	2.4	-	V
		for 2.5 V I/O, $I_{OH} = -1.0$ mA	2.0	-	V
$V_{OL}$	Output LOW Voltage	for 3.3 V I/O, $I_{OL} = 8.0$ mA	-	0.4	V
		for 2.5 V I/O, $I_{OL} = 1.0$ mA	-	0.4	V
$V_{IH}$	Input HIGH Voltage	for 3.3 V I/O	2.0	$V_{DD} + 0.3$	V
		for 2.5 V I/O	1.7	$V_{DD} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>[10]</sup>	for 3.3 V I/O	-0.3	0.8	V
		for 2.5 V I/O	-0.3	0.7	V
$I_X$	Input Leakage Current except ZZ and MODE	$GND \leq V_I \leq V_{DDQ}$	-5	5	$\mu$ A
	Input Current of MODE	Input = $V_{SS}$	-30	-	$\mu$ A
		Input = $V_{DD}$	-	5	$\mu$ A
	Input Current of ZZ	Input = $V_{SS}$	-5	-	$\mu$ A
Input = $V_{DD}$		-	30	$\mu$ A	
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{DDQ}$ , Output Disabled	-5	5	$\mu$ A

### Notes

10. Overshoot:  $V_{IH}(AC) < V_{DD} + 1.5$  V (Pulse width less than  $t_{CYC}/2$ ), undershoot:  $V_{IL}(AC) > -2$  V (Pulse width less than  $t_{CYC}/2$ ).

11.  $T_{Power\ up}$ : Assumes a linear ramp from 0 V to  $V_{DD}(\min)$  within 200 ms. During this time  $V_{IH} < V_{DD}$  and  $V_{DDQ} \leq V_{DD}$ .

**Electrical Characteristics** (continued)

Over the Operating Range

Parameter <sup>[10, 11]</sup>	Description	Test Conditions	Min	Max	Unit	
$I_{DD}$	$V_{DD}$ Operating Supply Current	$V_{DD} = \text{Max.}$ , $I_{OUT} = 0 \text{ mA}$ , $f = f_{MAX} = 1/t_{CYC}$	100 MHz	–	180	mA
$I_{SB1}$	Automatic CE Power-down Current – TTL Inputs	Max. $V_{DD}$ , Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$ , inputs switching	100 MHz (Automotive)	–	150	mA
$I_{SB2}$	Automatic CE Power-down Current – CMOS Inputs	Max. $V_{DD}$ , Device Deselected, $V_{IN} \geq V_{DD} - 0.3 \text{ V}$ or $V_{IN} \leq 0.3 \text{ V}$ , $f = 0$ , inputs static	100 MHz (Automotive)	–	40	mA
$I_{SB3}$	Automatic CE Power-down Current – CMOS Inputs	Max. $V_{DD}$ , Device Deselected, $V_{IN} \geq V_{DDQ} - 0.3 \text{ V}$ or $V_{IN} \leq 0.3 \text{ V}$ , $f = f_{MAX}$ , inputs switching	100 MHz (Automotive)	–	120	mA
$I_{SB4}$	Automatic CE Power-down Current – TTL Inputs	Max. $V_{DD}$ , Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = 0$ , inputs static	100 MHz (Automotive)	–	60	mA

**Capacitance**

Parameter <sup>[12]</sup>	Description	Test Conditions	165-ball FBGA Max.	Unit
$C_{IN}$	Input capacitance	$T_A = 25 \text{ }^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{DD} = 3.3 \text{ V}$ , $V_{DDQ} = 2.5 \text{ V}$	5	pF
$C_{CLK}$	Clock input capacitance		5	pF
$C_{I/O}$	Input/Output capacitance		7	pF

**Thermal Resistance**

Parameter <sup>[12]</sup>	Description	Test Conditions	165-ball FBGA Package	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	16.8	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		3.0	$^\circ\text{C/W}$

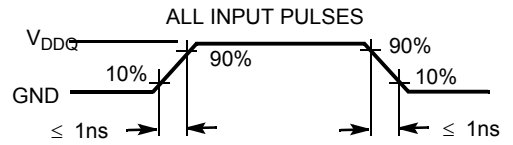
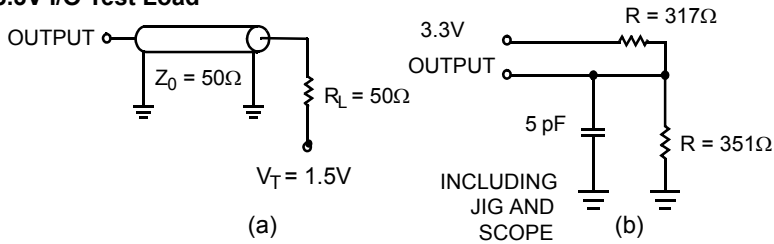
**Note**

12. Tested initially and after any design or process change that may affect these parameters.

**AC Test Loads and Waveforms**

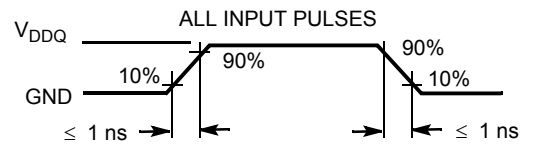
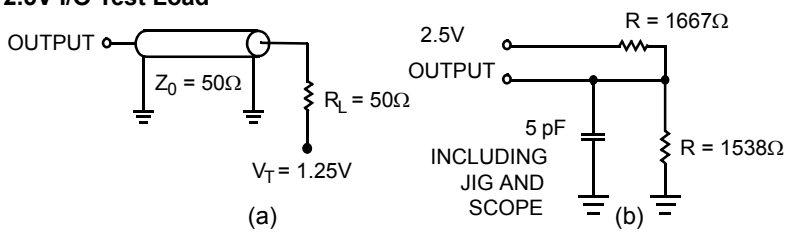
**Figure 2. AC Test Loads and Waveforms**

**3.3V I/O Test Load**



(c)

**2.5V I/O Test Load**



(c)

## Switching Characteristics

Over the Operating Range

Parameter [13, 14]	Description	-100		Unit
		Min	Max	
$t_{POWER}$	$V_{DD}$ (Typical) to the first Access [15]	1	–	ms
<b>Clock</b>				
$t_{CYC}$	Clock Cycle Time	10	–	ns
$t_{CH}$	Clock HIGH	4.0	–	ns
$t_{CL}$	Clock LOW	4.0	–	ns
<b>Output Times</b>				
$t_{CDV}$	Data Output Valid After CLK Rise	–	8.0	ns
$t_{DOH}$	Data Output Hold After CLK Rise	2.0	–	ns
$t_{CLZ}$	Clock to Low Z [16, 17, 18]	0	–	ns
$t_{CHZ}$	Clock to High Z [16, 17, 18]	–	3.5	ns
$t_{OEV}$	$\overline{OE}$ LOW to Output Valid	–	3.5	ns
$t_{OELZ}$	$\overline{OE}$ LOW to Output Low Z [16, 17, 18]	0	–	ns
$t_{OEZH}$	$\overline{OE}$ HIGH to Output High Z [16, 17, 18]	–	3.5	ns
<b>Setup Times</b>				
$t_{AS}$	Address Setup Before CLK Rise	2.0	–	ns
$t_{ADS}$	ADSP, ADSC Setup Before CLK Rise	2.0	–	ns
$t_{ADVS}$	$\overline{ADV}$ Setup Before CLK Rise	2.0	–	ns
$t_{WES}$	$\overline{GW}$ , $\overline{BWE}$ , $\overline{BW}_x$ Setup Before CLK Rise	2.0	–	ns
$t_{DS}$	Data Input Setup Before CLK Rise	2.0	–	ns
$t_{CES}$	Chip Enable Setup	2.0	–	ns
<b>Hold Times</b>				
$t_{AH}$	Address Hold After CLK Rise	0.5	–	ns
$t_{ADH}$	ADSP, ADSC Hold After CLK Rise	0.5	–	ns
$t_{WEH}$	$\overline{GW}$ , $\overline{BWE}$ , $\overline{BW}_x$ Hold After CLK Rise	0.5	–	ns
$t_{ADVH}$	$\overline{ADV}$ Hold After CLK Rise	0.5	–	ns
$t_{DH}$	Data Input Hold After CLK Rise	0.5	–	ns
$t_{CEH}$	Chip Enable Hold After CLK Rise	0.5	–	ns

### Notes

13. Timing reference level is 1.5V when  $V_{DDQ} = 3.3V$  and is 1.25V when  $V_{DDQ} = 2.5V$ .

14. Test conditions shown in (a) of unless otherwise noted.

15. This part has a voltage regulator internally;  $t_{POWER}$  is the time that the power needs to be supplied above  $V_{DD}$ (minimum) initially before a read or write operation is initiated.

16.  $t_{CHLZ}$ ,  $t_{CLZ}$ ,  $t_{OELZ}$ , and  $t_{OEZH}$  are specified with AC test conditions shown in (b) of Figure 2 on page 12. Transition is measured  $\pm 200$  mV from steady state voltage.

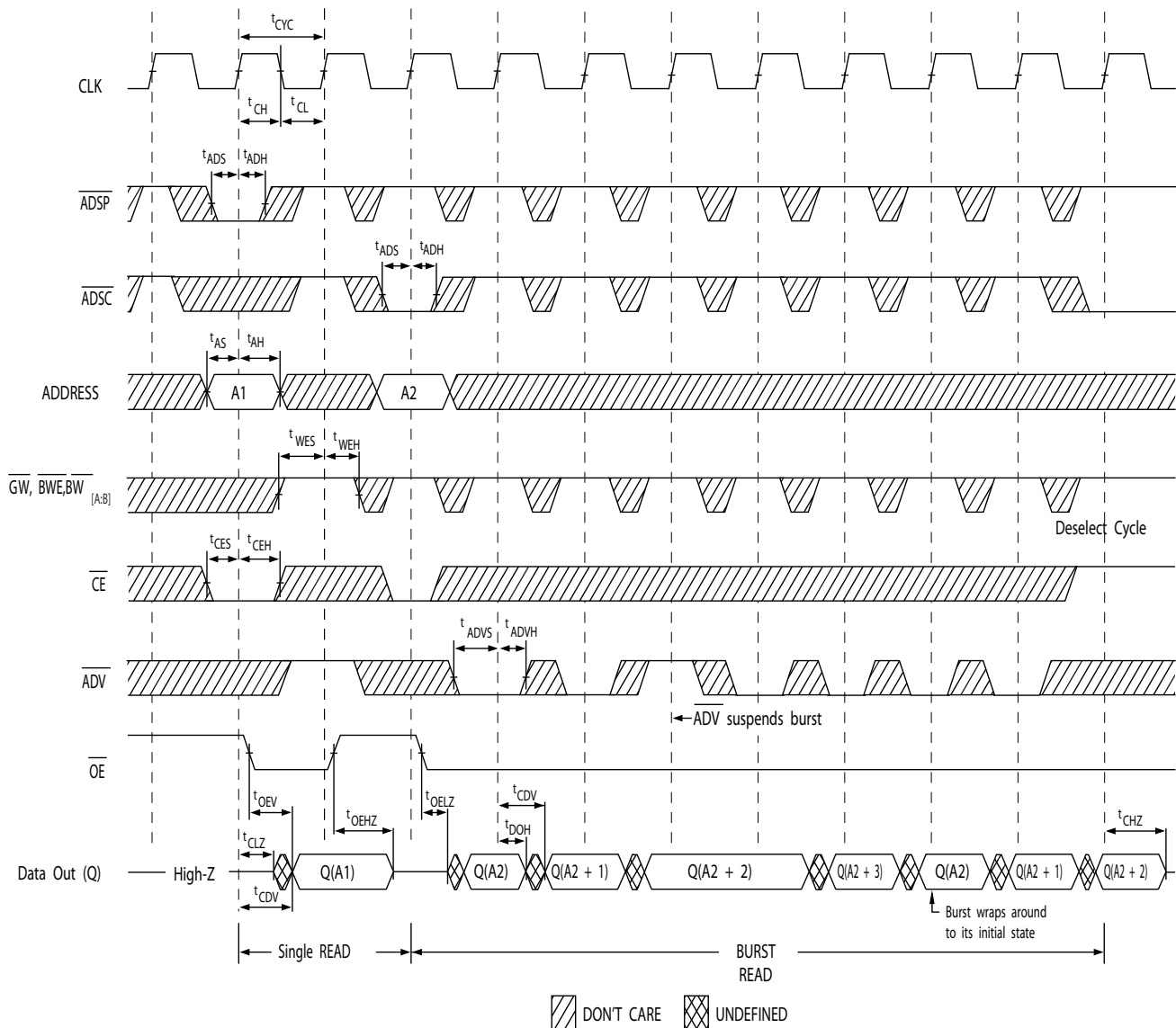
17. At any voltage and temperature,  $t_{OEZH}$  is less than  $t_{OELZ}$  and  $t_{CHZ}$  is less than  $t_{CLZ}$  to eliminate bus contention between SRAMs when sharing the same data bus.

These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.

18. This parameter is sampled and not 100% tested.

**Timing Diagrams**

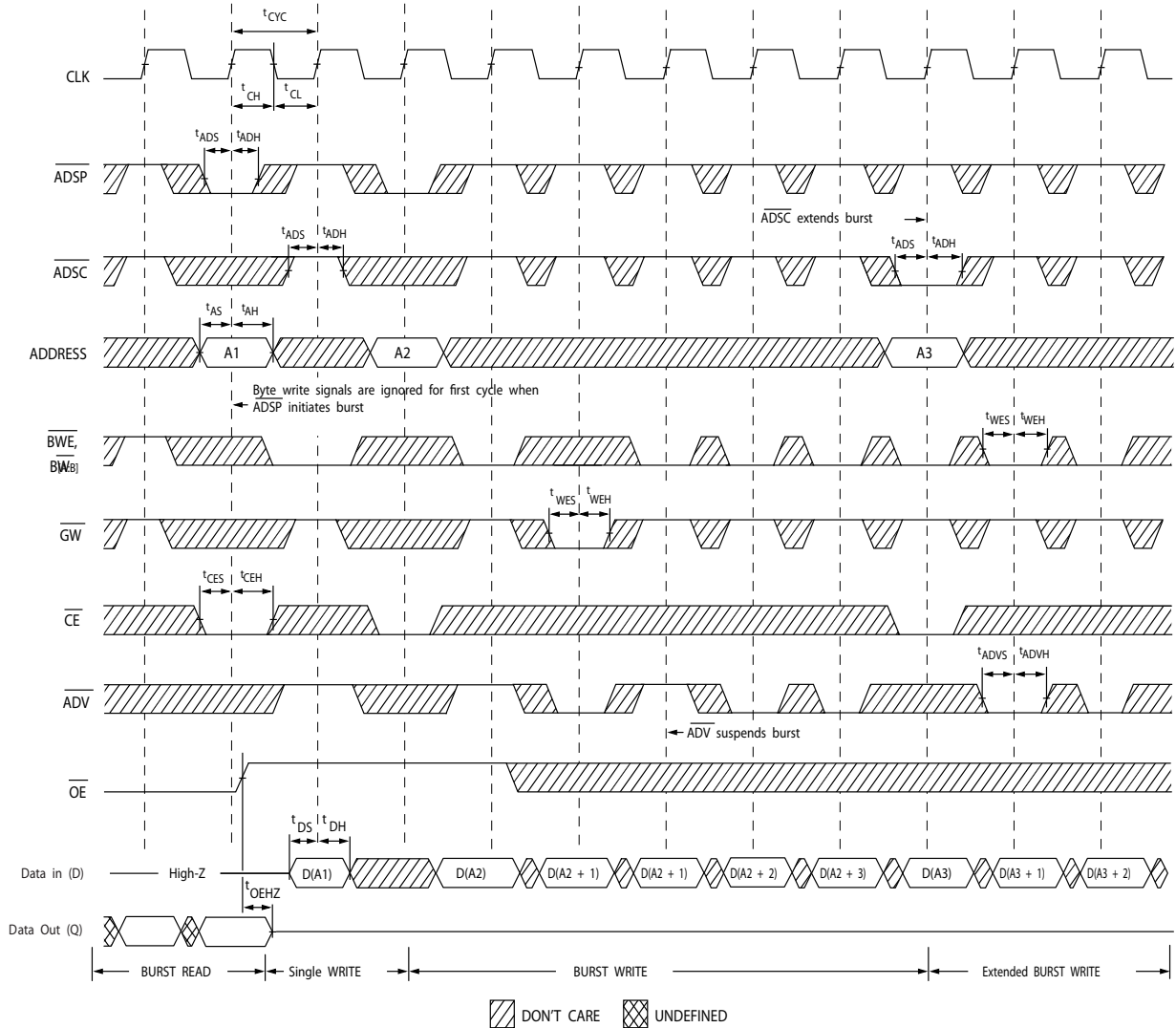
**Figure 3. Read Cycle Timing [19]**



**Note**  
19. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.

Timing Diagrams (continued)

Figure 4. Write Cycle Timing [20, 21]

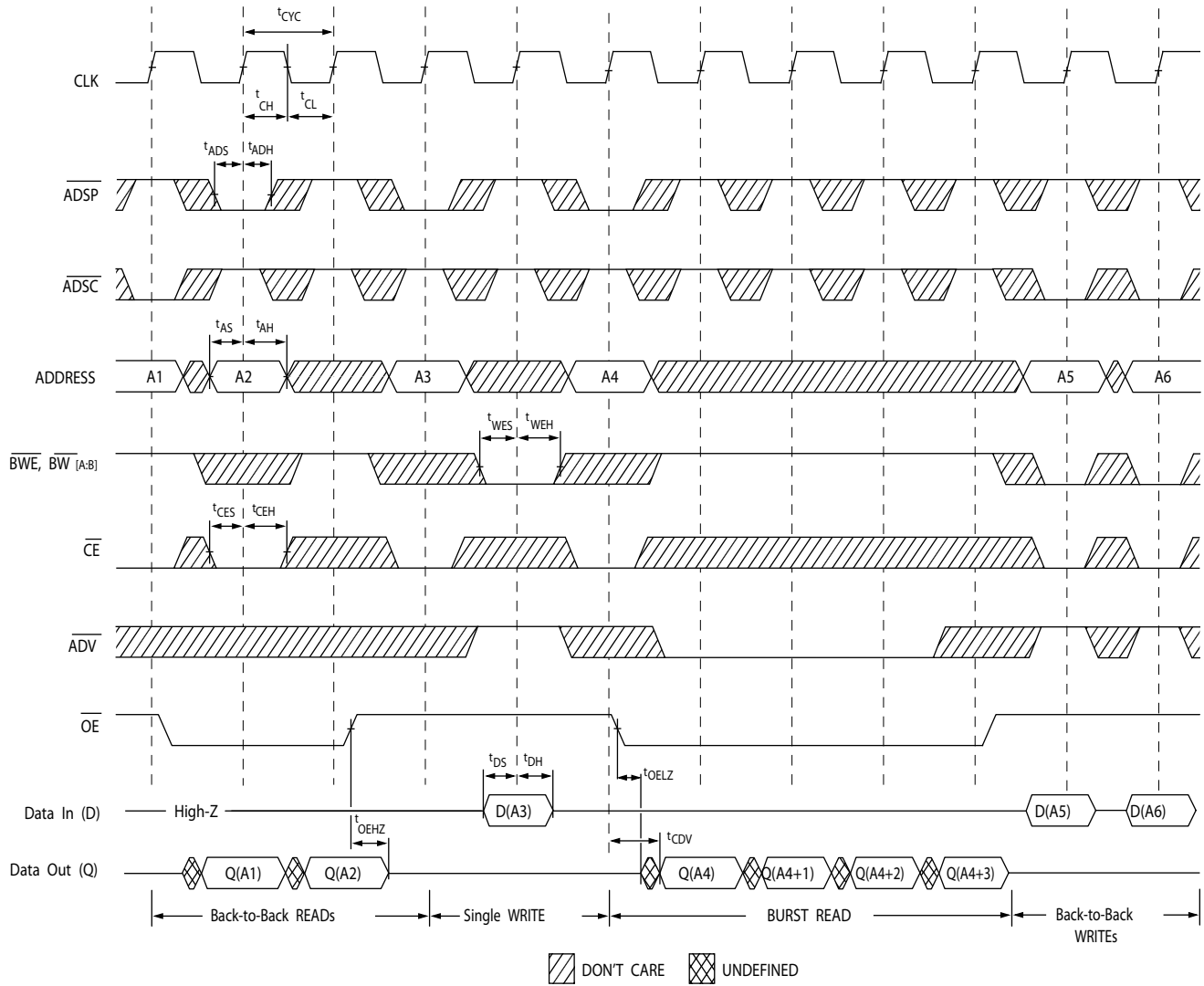


Notes

- 20. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.
- 21. Full width write can be initiated by either  $\overline{GW}$  LOW; or by  $\overline{GW}$  HIGH,  $\overline{BWE}$  LOW and  $\overline{BWX}$  LOW.

Timing Diagrams (continued)

Figure 5. Read/Write Timing [22, 23, 24]



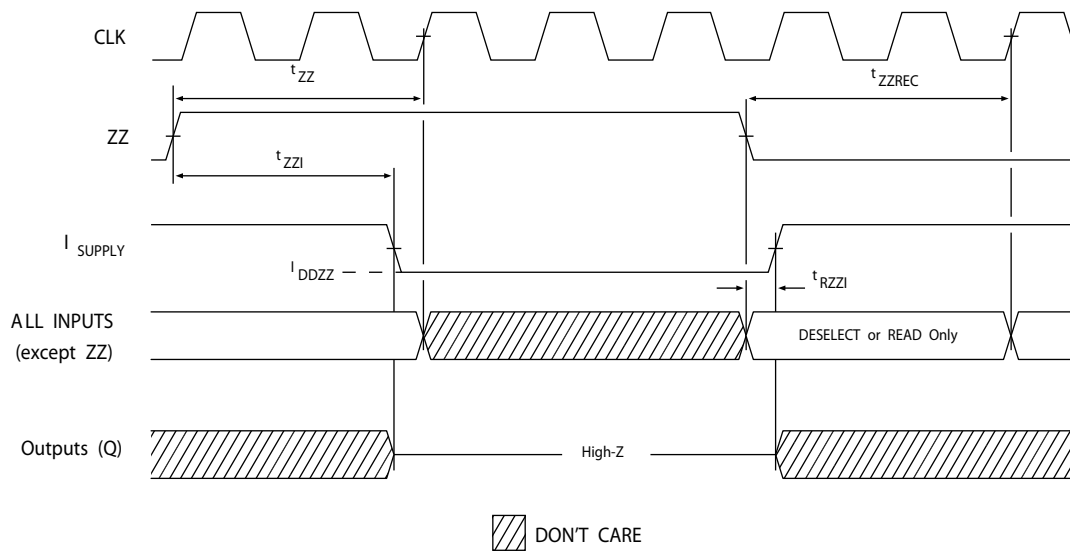
Notes

- 22. Full width write can be initiated by either  $\overline{GW}$  LOW; or by  $\overline{GW}$  HIGH,  $\overline{BWE}$  LOW and  $\overline{BW}_x$  LOW.
- 23. The data bus (Q) remains in High Z following a WRITE cycle, unless a new read access is initiated by  $\overline{ADSP}$  or  $\overline{ADSC}$ .
- 24.  $\overline{GW}$  is HIGH.



**Timing Diagrams** (continued)

**Figure 6. ZZ Mode Timing** [25, 26]



**Notes**

- 25. Device must be deselected when entering ZZ mode. See [Truth Table on page 8](#) for all possible signal conditions to deselect the device.
- 26. DQs are in High Z when exiting ZZ sleep mode.

### Ordering Information

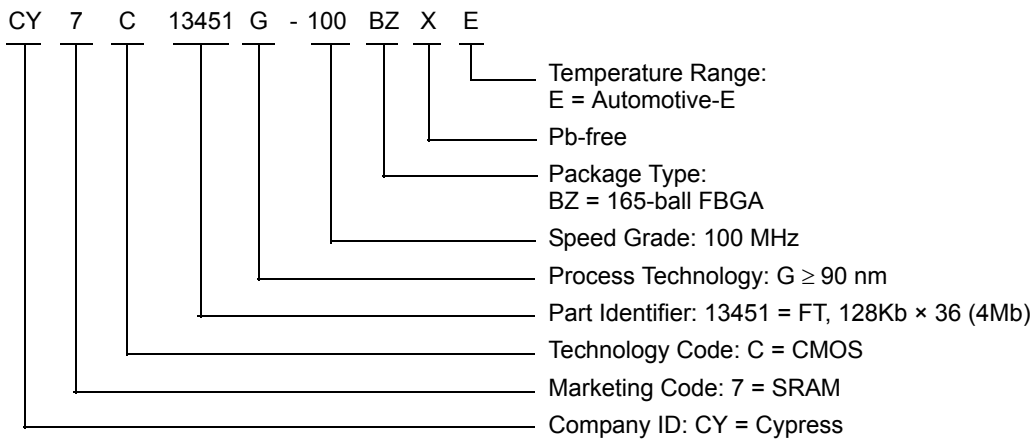
The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products>

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**Table 1. Ordering Information**

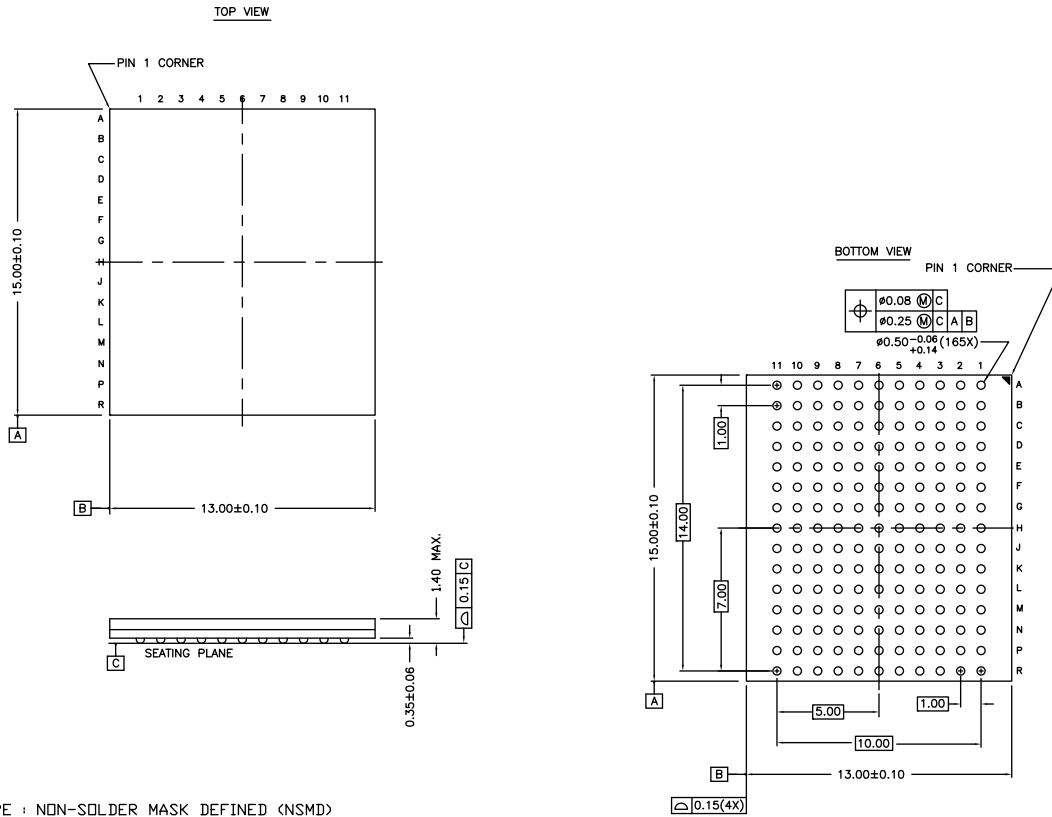
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
100	CY7C13451G-100BZX E	51-85180	165-ball FBGA (13 × 15 × 1.4 mm) Pb-free	Automotive

### Ordering Code Definitions



### Package Diagrams

Figure 7. 165-ball FBGA (13 × 15 × 1.4 mm) BB165D/BW165D (0.5 Ball Diameter) Package Outline, 51-85180



NOTES :  
 SOLDER PAD TYPE : NON-SOLDER MASK DEFINED (NSMD)  
 JEDEC REFERENCE : MO-216 / ISSUE E  
 PACKAGE CODE : BB0AC/BW0AC  
 PACKAGE WEIGHT : SEE CYPRESS PACKAGE MATERIAL DECLARATION DATASHEET (PMDD) POSTED ON THE CYPRESS WEB.

51-85180 \*G

## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
CEN	Clock Enable
GW	Global Write
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
WE	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
MHz	megahertz
ns	nanosecond
pF	picofarad
V	volt
W	watt

## Errata

This section describes the Ram9 Sync SRAM ZZ pin issues. Details include trigger conditions, the devices affected, proposed workaround and silicon revision applicability. Please contact your local Cypress sales representative if you have further questions.

### Part Numbers Affected

Density & Revision	Package Type	Operating Range
4Mb-Ram9 Synchronous SRAMs: CY7C134**G	165-ball FBGA	Automotive

### Product Status

All of the devices in the Ram9 4Mb Sync family are qualified and available in production quantities.

### Ram9 Sync ZZ Pin Issues Errata Summary

The following table defines the errata applicable to available Ram9 4Mb Sync family devices.

Item	Issues	Description	Device	Fix Status
1.	ZZ Pin	When asserted HIGH, the ZZ pin places device in a “sleep” condition with data integrity preserved. The ZZ pin currently does not have an internal pull-down resistor and hence cannot be left floating externally by the user during normal mode of operation.	4M-Ram9 (90nm)	For the 4M Ram9 (90 nm) devices, there is no plan to fix this issue.

#### 1. ZZ Pin Issue

##### ■ PROBLEM DEFINITION

The problem occurs only when the device is operated in the normal mode with ZZ pin left floating. The ZZ pin on the SRAM device does not have an internal pull-down resistor. Switching noise in the system may cause the SRAM to recognize a HIGH on the ZZ input, which may cause the SRAM to enter sleep mode. This could result in incorrect or undesirable operation of the SRAM.

##### ■ TRIGGER CONDITIONS

Device operated with ZZ pin left floating.

##### ■ SCOPE OF IMPACT

When the ZZ pin is left floating, the device delivers incorrect data.

##### ■ WORKAROUND

Tie the ZZ pin externally to ground.

##### ■ FIX STATUS

For the 4M Ram9 (90 nm) devices, there is no plan to fix this issue

## Document History Page

Document Title: CY7C13451G, 4-Mbit (128K × 36) Flow-Through Sync SRAM Document Number: 001-88572				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4077242	PRIT	09/12/2013	New data sheet.
*A	4287129	PRIT	02/20/2014	Updated <a href="#">Electrical Characteristics</a> : Changed maximum value of I <sub>DD</sub> parameter from 205 mA to 180 mA. Changed maximum value of I <sub>SB1</sub> parameter from 80 mA to 150 mA. Changed maximum value of I <sub>SB3</sub> parameter from 65 mA to 120 mA. Changed maximum value of I <sub>SB4</sub> parameter from 45 mA to 60 mA.
*B	4419347	PRIT	06/25/2014	Included 100-pin TQFP package related information in all instances across the document. Updated <a href="#">Pin Configurations</a> : Updated <a href="#">Figure 1</a> . Updated <a href="#">Ordering Information</a> (Updated part numbers). Updated <a href="#">Package Diagrams</a> : Added spec 51-85050 *E.
*C	4430376	PRIT	07/04/2014	Changed status from Preliminary to Final. Removed 100-pin TQFP package related information across the document. Updated <a href="#">Ordering Information</a> (Updated part numbers). Updated <a href="#">Package Diagrams</a> : Removed spec 51-85050 *E.
*D	4598640	PRIT	12/16/2014	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, click <a href="#">here</a> ." at the end. Updated to new template.
*E	5099908	PRIT	01/22/2016	Updated <a href="#">Package Diagrams</a> : spec 51-85180 – Changed revision from *F to *G. Completing Sunset Review.
*F	5329574	PRIT	06/29/2016	Updated <a href="#">Truth Table</a> . Updated to new template.
*G	5974265	AESATMP9	11/22/2017	Updated logo and copyright.

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